REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R233-93	92-09-01	M. L. Poelking
B	Changes in accordance with NOR 5962-R224-94	93-07-05	M. L. Poelking
C	Add device type 03. Editorial changes throughout.	94-10-10	M. L. Poelking
D	Add device type 04. Update boilerplate. Editorial changed throughout.	96-01-15	M. L. Poelking
E	Add case outline Z and U. Changes to boilerplate. Editorial changes throughout.	97-01-29	M. L. Poelking
F	Add Appendix A. Editorial changes throughout. – tmh	97-07-11	Thomas M. Hess
G	Changes in accordance with NOR 5962-R042-99	99-03-04	M. L. Poelking
H	Added junction temperature to document - LTG	99-11-19	M. L. Poelking

REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	H	F	H	H	H	G	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Thomas M. Hess

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
Monica L. Poelking

MICROCIRCUIT, DIGITAL, CMOS DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

DRAWING APPROVAL DATE
93-03-26

AMSC N/A

REVISION LEVEL
H

SIZE	CAGE CODE	
A	**67268**	**5962-92058**

SHEET
1 OF 53

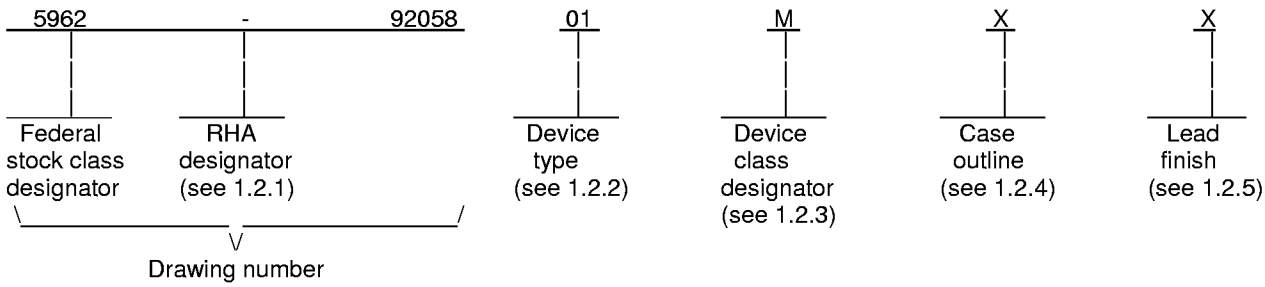
DSCC FORM 2233
APR 97

5962-E056-00

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and Appendix F of MIL-PRF-38535 , "General provisions for TAB microcircuits" and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C31	Digital signal processor, 27 MHz 1/
02	320C31	Digital signal processor, 33 MHz
03	320C31	Digital signal processor, 40 MHz
04	320C31	Digital signal processor, 50 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535
Q or V	Certification and qualification to MIL-PRF-38535 and Appendix F of MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	141	Pin grid array
Y	See figure 1	132	Quad flatpack with non-conductive tie bar
Z	See figure 1	132	Tape automated bond
U	See figure 1	132	Environmentally protected tape automated bond

1/ Not available from an approved source of supply.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 and Appendix F of MIL-PRF-38535, for device classes Q and V or MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535 for device class M.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{DD}) 3/	-0.3 V dc to 7.0 V dc
Input voltage range	-0.3 V dc to 7.0 V dc
Output voltage range	-0.3 V dc to 7.0 V dc
Continuous power dissipation 4/	3.15 W
Storage temperature range	-65°C to +150°C
Junction temperature (T_J):	
Case outlines X and Y	150°C
Case outlines 9, U and Z	125°C
Thermal resistance, junction to case (Θ_{JC}):	
Case X	4.25°C/W
Cases Y	2.13°C/W
Maximum die temperature rise for the die at 100%	
Cases Z and U	0.9°C/W

1.4 Recommended operating conditions.

Supply voltages (V_{DD}):	
Device type 01 and 02	4.5 V dc min to 5.5 V dc max
Device type 03 and 04	4.75 V dc min to 5.25 V dc max
Supply voltages (CVSS, etc.)(V_{SS})	0 V dc nominal
High level input voltage (V_{IH}) 5/	2.1 V dc min to V_{DD} +0.3 V dc max
Low level input voltage (V_{IL}) 5/	-0.3 V dc min to 0.8 V dc max
High level output current (I_{OH})	-300 µA max
Low level output current (I_{OL})	2 mA max
CLKIN high level input voltage (V_{TH}) 5/	3.0 V dc Min to V_{DD} +0.3 V dc max
Operating case temperature (T_C)	-55°C min to +125°C max

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage values are with respect to V_{SS}.
4/ Actual operating power will be less. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible.
5/ V_{IH} max, V_{IL} min, and V_{TH} max are guaranteed from characterization but not tested.
6/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, and Appendix F of MIL-PRF-38535 "Generial provisions for TAB microcircuits" and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, and Appendix F of MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The switching waveform and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535, and Appendix F of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{DD} = Min (see 1.4) I_{OH} = -300 µA		1,2,3	All	2.4		V
Low level output voltage 2/	V_{OL}	V_{DD} = Min (see 1.4) I_{OL} = 2 mA					0.6	
Three-state current	I_Z	V_{DD} = Min (see 1.4)				-20	20	µA
Input current	I_I	$V_I = V_{SS}$ to V_{DD}				-10	10	
Input current with internal pull-ups 3/	I_{IP}					-600	20	
Input current, (X2/CLKIN)	I_{IC}	V_I = 0.0 V to V_{DD} Max				-50	50	
Supply current 4/	I_{CC}	V_{DD} = Max	f_x = 27 MHz	1	01		250	mA
			f_x = 33 MHz		02		325	
			f_x = 40 MHz		03		400	
			f_x = 50 MHz		04		500	
Input capacitance	C_{IN}	See 4.4.1b		4	All		15	pF
Output capacitance	C_{OUT}						20	
X2/CLKIN capacitance	C_X						25	
Functional testing		See 4.4.1d		7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Fall time, CLKIN 5/	t_{F1}	See figure 4 X2/CLKIN timing	9,10,11	All		5	ns
Pulse duration, CLKIN low	t_{W1}	t_{C1} = 37 ns		01	13		
		t_{C1} = 30 ns		02	10.5		
		t_{C1} = 25 ns		03	9		
		t_{C1} = 20 ns		04	7		
Pulse duration, CLKIN high	t_{W2}	t_{C1} = 37 ns		01	13		
		t_{C1} = 30 ns		02	10.5		
		t_{C1} = 25 ns		03	9		
		t_{C1} = 20 ns		04	7		
Rise time, CLKIN 5/	t_{R1}			All		5	
Cycle time, CLKIN	t_{C1}			01	37	303	
				02	30	303	
				03	25	303	
				04	20	303	
Fall time, H1/H3	t_{F2}	See figure 4 H1/H3 timing		01		4	
				02-04		3	
Pulse duration, H1/H3 low	t_{W3}	P = t_{C1}		01-02	P-6		
				03-04	P-5		
Pulse duration, H1/H3 high	t_{W4}			01-02	P-7		
				03-04	P-6		
Rise time, H1/H3	t_{R2}			01-02		4	
				03-04		3	
Delay time, from H1(H3) low to 6/ H3(H1) high	t_{D1}			01-02	0	5	
				03-04	0	4	
Cycle time, H1/H3	t_{C2}			01	74	606	
				02	60	606	
				03	50	606	
				04	40	606	
Delay time, from H1 low to 6/ (M)STRB low	t_{D2}	See figure 4 Memory ((M)STRB = 0)		01-02	0	10	
				03	0	6	
				04	0	4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, from H1 low to 6/ (M)STRB high	t_{D3}	See figure 4 Memory ((M)STRB = 0)	9,10,11	01-02 03 04	0 0 0	10 6 4	
Delay time, from H1 high to R/W low 6/	t_{D4}			01-02 03 04	0 0 0	10 9 7	ns
Delay time, from H1 low to A valid 6/	t_{D6}			01 02 03-04	0 0 0	16 14 10	
Set-up time, D valid before H1 low (read)	t_{SU1}			01 02 03 04	18 16 14 10		
Hold time, (X)D after H1 low (read) 6/	t_{H1}			All	0		
Set-up time, RDY before H1 high	t_{SU3}			01 02-03 04	10 8 6		
Hold time, XRDY after H1 high	t_{H2}			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, from H1 high to (X)R/W high (write)	t_{D8}	See figure 4 Memory ((M)STRB = 0)	9,10,11	01 02 03 04		12 10 9 7	ns
(X)D valid after H1 low (write)	t_{V1}			01-02 03 04		20 17 14	
Hold time, X(D) after H1 high (write)	t_{H3}			All	0		
Delay time, from H1 high to A valid on back-to-back write cycles	t_{D9}			01 02 03 04		22 18 15 14	
Delay time, from (X)RDY to A valid 5/	t_{D11}			01-02 03 04		8 7 7/	
Delay time, from H3 high to XF0 low	t_{D17}	See figure 4 Timing for XF0 and XF1 when executing LDFI or LDII		01 02 03 04		19 15 13 12	
Set-up time, XF1 valid before H1 low	t_{SU7}			01 02 03 04	13 12 9 8		
Hold time, XF1 after H1 low	t_{H7}			All	0		
Delay time, from H3 high to XF0 high	t_{D18}	See figure 4 Timing for XF0 when executing a STFI or STII		01 02 03 04		19 18 13 12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, from H3 high to XFO low	t_{D19}	See figure 4 Timing for XF0 and XF1 when executing a SIGI	9,10,11	01		19	ns
				02		15	
				03		13	
				04		12	
Delay time, from H3 high to XFO high	t_{D20}			01		19	
				02		18	
				03		13	
				04		12	
Set-up time, XF1 valid before H1 low	t_{SU8}			01	13		
				02	12		
				03	9		
				04	8		
Hold time, XF1 after H1 low	t_{H8}			All	0		
XF valid after H3 high	t_{V3}	See figure 4 Timing for loading XF register when conformed as an output pin		01		19	
				02		15	
				03		13	
				04		12	
Hold time, XF after H3 high 5/	t_{H9}	See figure 4 Change of XF from output to input mode		01		20	
				02		15	
				03		13	
				04		12	
Set-up time, XF before H1 low	t_{SU9}			01-02	12		
				03	9		
				04	8		
Hold time, XF after H1 low	t_{H10}			All	0		
Delay time, from H3 high to XF switching from input to output	t_{D21}	See figure 4 Change of XF from input to output mode		01-02		20	
				03		17	
				04		15	
Set-up time, for RESET before CLKIN low	t_{SU10}	See figure 4 RESET timing		All	10		
Delay time, from CLKIN high to H1 high	t_{D22}			01-03	2	14	
				04	2	10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, from CLKIN high to H1 low	t_{D23}	See figure 4 RESET TIMING	9,10,11	01-03	2	14	ns
				04	2	10	
Set-up time, $\overline{RESET}$ high before H1 low and after 10 H1 clock cycles 6/	t_{SU11}			01	13		
				02	10		
				03	9		
				04	7		
Delay time, from CLKIN high to H3 low	t_{D24}			01-03	2	14	
				04	2	10	
Delay time, from CLKIN high to H3 high	t_{D25}			01-03	2	14	
				04	2	10	
Disable time, from H1 high to (X)D three-state 5/	t_{DIS1}			01		19	
				02		18	
				03		15	
				04		12	
Disable time, from H3 high to (X)A three-state 5/	t_{DIS2}			01		12	
				02		10	
				03		9	
				04		8	
Delay time, from H3 high to control signals high 5/	t_{D26}			01-02		10	
				03		9	
				04		8	
Delay time, from H1 high to IACK high 5/	t_{D27}			01		12	
				02		10	
				03		9	
				04		8	
Disable time, from RESET low to asynchronously reset signals 5/	t_{DIS3}			01-02		25	
				03		21	
				04		17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Set-up time, INT(3-0) before H1 low	t_{SU12}	See figure 4 INT(3-0) response timing	9,10,11	01-02 03 04	15 13 11		ns
Pulse duration, to guarantee one interrupt seen 5/ 6/ 8/	t_{W5}			All	P	2P 6/	
Delay time, from H1 high to IACK low	t_{D28}	See figure 4 IACK timing		01 02 03 04		12 10 9 8	
Delay time, from H1 high to IACK high during first cycle of IACK instruction data read	t_{D29}			01 02 03 04		12 10 9 8	
Delay time, from H1 high to internal CLKX/R	t_{D30}	See figure 4 Data rate mode		01 02 03 04		17 15 13 10	
Cycle time, CLKX/R	t_{C3}	CLKX/R ext 6/		All	t_{c2} x 2.6		
		CLKX/R int 5/			t_{c2} x 2	t_{c2} x 2^{32}	
Pulse width, CLKX/R	t_{W6}	CLKX/R ext 6/		01,02, 03 04	$t_{c2}+12$ $t_{c2}+10$		
		CLKX/R int		01-03 04	$(t_{c3}/2)$ -15 $(t_{c3}/2)$ -5	$(t_{c3}/2)$ +5 $(t_{c3}/2)$ +5	
Rise time, CLKX/R 5/	t_{R3}			01,02 03 04		8 7 6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Fall time, CLKX/R 5/	t_{F3}	See figure 4 Fixed data rate mode	9,10,11	01-02		8	ns
				03		7	
				04		6	
Delay time, from CLKX to DX valid	t_{D31}	CLKX ext		01-02		35	
				03		30	
				04		24	
		CLKX int		01-02		20	
				03		17	
				04		16	
Set-up time, DR before CLKR low	t_{SU13}	CLKR ext		01-02	10		
				03-04	9		
		CLKR int		01-02	25		
				03	21		
				04	17		
Hold time, DR from CLKR low	t_{H11}	CLKR ext		01-02	10		
				03-04	9		
		CLKR int 6/		All	0		
Delay time, from CLKX to internal FSX high/low	t_{D32}	CLKX ext		01-02		32	
				03		27	
				04		22	
		CLKX int		01-02		17	
				03-04		15	
Set-up time, FSR before CLKR low	t_{SU14}	CLKR ext		01-02	10		
				03	9		
				04	7		
		CLKR int		01-02	10		
				03	9		
				04	7		
Hold time, FSX/R from CLKX/R low	t_{H12}	CLKX/R ext		01-02	10		
				03	9		
				04	7		
		CLKX/R int 6/		All	0		
Set-up time, external FSX before CLKX	t_{SU15}	CLKX ext 5/			$-(t_{c2}-8)$	$(t_C3/2)-10$	
		CLKX int 5/			$-(t_{c2}-21)$	$t_C3/2$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Delay time, from CLKX to first DX bit, FSX precedes CLKX high	t_{D33}	See figure 4 Variable rate data mode	CLKX ext	9,10,11	01-02		36	ns
					03		30	
					04		24	
			CLKX int		01-02		21	
					03		18	
					04		14	
Delay time, from FSX to first DX bit, CLKX precedes FSX	t_{D34}				01-02		36	
					03		30	
					04		24	
Delay time, from CLKX high to DX high-Z following last data bit 5/	t_{D35}				01-02		20	
					03		17	
					04		15	
Set-up time, HOLD valid before H1 low	t_{SU16}	See figure 4 HOLD/HOLDA timing			01,02	15		
					03	13		
					04	9		
HOLDA valid after H1 low 6/	t_{V4}				01-02	0	10	
					03-04	0	9	
Pulse width, HOLD low	t_{W7}				All	2		H1 cycles
Pulse width, HOLDA low 6/	t_{W8}				01-03	t_{C2}-5		ns
					04	32		
Delay time, from H1 low to STRB high for a HOLD 5/ 6/	t_{D36}				01-02	0	10	
					03	0	9	
					04	0	7	
Disable time, from H1 low to STRB high impedance state 5/ 6/	t_{DIS4}				01-02	0	10	
					03	0	9	
					04	0	7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable time, from H1 low to STRB active 5/ 6/	t_{EN1}	See figure 4 HOLD/HOLDA timing	9,10,11	01-02 03 04	0 0 0	10 9 7	ns
Disable time, from H1 low to R/W high impedance state 5/ 6/	t_{DIS5}			01-02 03 04	0 0 0	10 9 8	
Enable time, from H1 low to R/W active 5/ 6/	t_{EN2}			01-02 03 04	0 0 0	10 9 7	
Disable time, from H1 low to address high impedance state 5/ 6/	t_{DIS6}			01 02 03 04	0 0 0 0	13 10 9 8	
Enable time, from H1 low to address valid 5/ 6/	t_{EN3}			01-02 03 04	0 0 0	15 13 10	
Disable time, from H1 high to data high impedance state 5/ 6/	t_{DIS7}			01-02 03 04	0 0 0	15 12 10	
Set-up time, general purpose input before H1 low	t_{SU17}	See figure 4 Peripheral pin general General purpose I/O timing		01 02 03 04	15 12 10 9		
Hold time, general-purpose input after H1 low	t_{H13}			All	0		
Delay time, general purpose output after H1 high	t_{D37}			01-02 03 04		15 13 10	

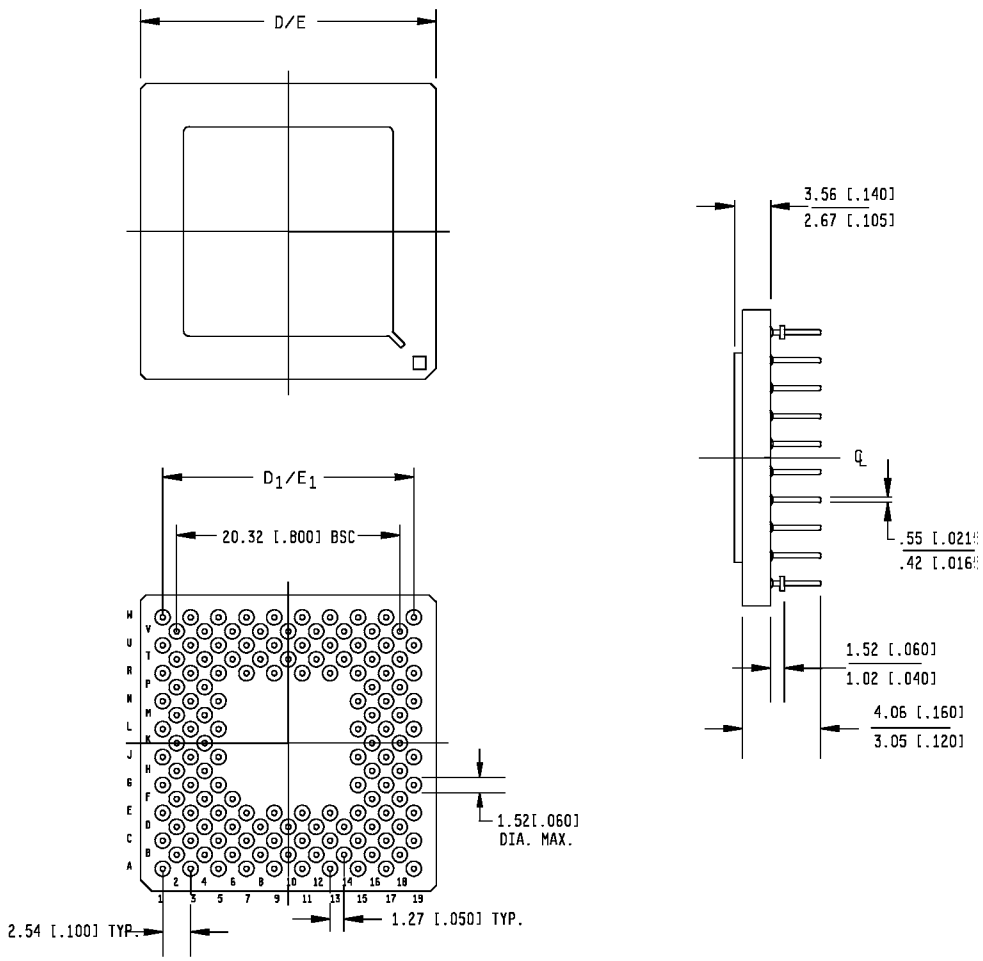
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Set-up time, TCLK ext before H1 low	t_{SU18}	See figure 4 Timer pin timing	9,10,11	01 02 03-04	15 12 10		ns
Hold time, TCLK ext after H1 low	t_{H14}			All	0		
Delay time, TCLK int valid after H1 high	t_{D38}			01 02 03 04		13 12 9 8	
Hold time, after H1 high 5/	t_{H15}	See figure 4 Change of peripheral pin from general purpose output to input mode		01-02 03 04		15 13 10	
Set-up time, peripheral pin before H1 low	t_{SU19}			01 02 03-04	13 12 9		
Hold time, peripheral pin after H1 low	t_{H16}			All	0		
Delay time, from H1 high to peripheral pin switching from input to output	t_{D39}	See figure 4 Change of peripheral pin from general purpose input to output mode		01-02 03 04		15 13 10	

1/ Unless otherwise specified, for devices 01 and 02: $4.5 V \le V_{DD} \le 5.5 V$, for devices 03 and 04: $4.75 V \le V_{DD} \le 5.25 V$. All other test conditions shall be worst case conditions unless otherwise specified.
2/ This parameter is guaranteed but not tested for XA12-XA0.
3/ Pins with internal pull-up devices: INT(0-3), MC/MP, RSV(0-10). Although RSV(0-10) have internal pull-up devices, external pull-ups should be used on each pin.
4/ Actual operating current will be less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the primary bus at the maximum rate possible.
5/ Maximum limit is guaranteed if not tested to the limits specified in table I.
6/ Minimum limit is guaranteed if not tested to the limits specified in table I.
7/ This value is frequency dependent and can be calculated by (delay, H_1 low to H_1 high) - (t_{D6}) - (t_{SU3}).
8/ Interrupt pulse width must be at least 1 P wide to guarantee it will be seen. It must be less than 2 P wide to guarantee it will be responded to only once. The recommended pulse width is 1.5 P. P = one H1 cycle.

Case X

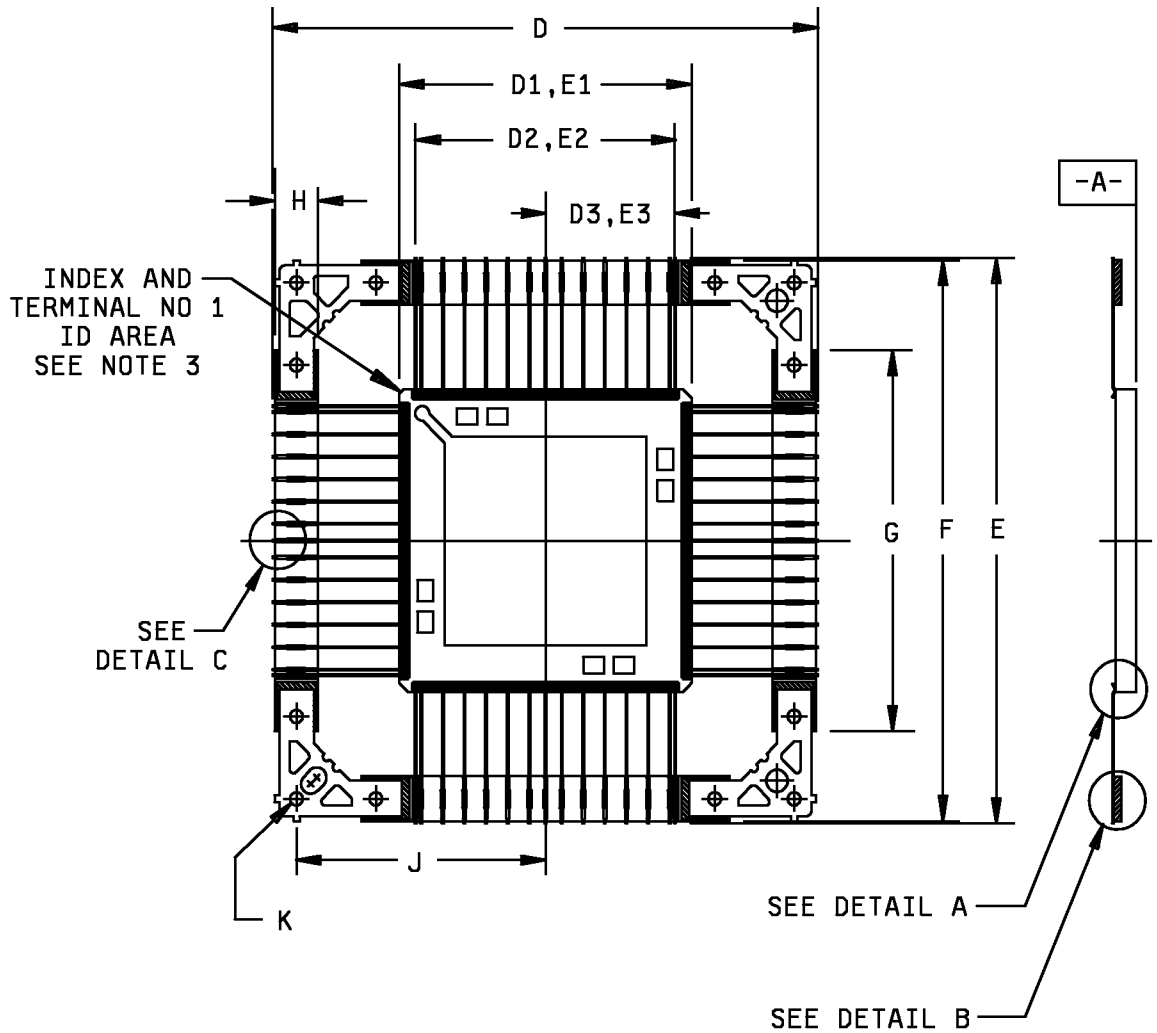


Letter	Millimeters		Inches	
	Min	Max	Min	Max
D/E	26.42	27.43	1.040	1.080
D_1/E_1	22.86 BSC		0.900 BSC	
M	19		19	
N	141		141	
S	.000 BSC		.000 BSC	

NOTES:
1. Dimensions are in millimeters.
2. Inch equivalents are given for information only.

FIGURE 1. Case outlines.

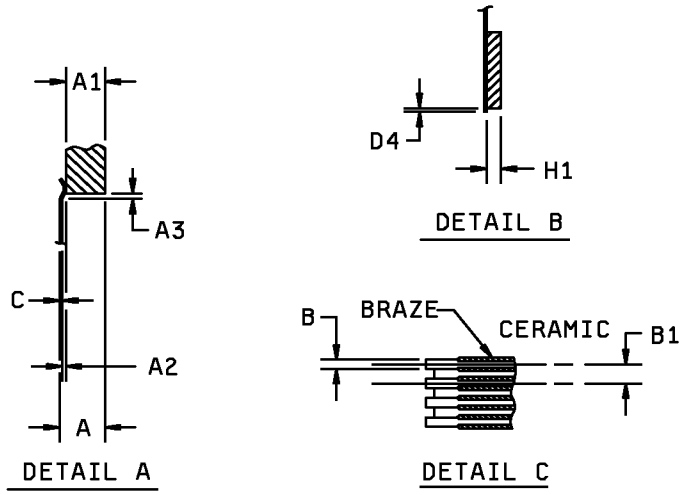
Case Y



NOTES:
1. Actual pin count not represented for clarity purposes.
2. Metric equivalents for information purposes only.
3. A terminal 1 identification mark shall be located at the index corner in the area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown. The index corner shall be clearly unique.

FIGURE 1. Case outline.

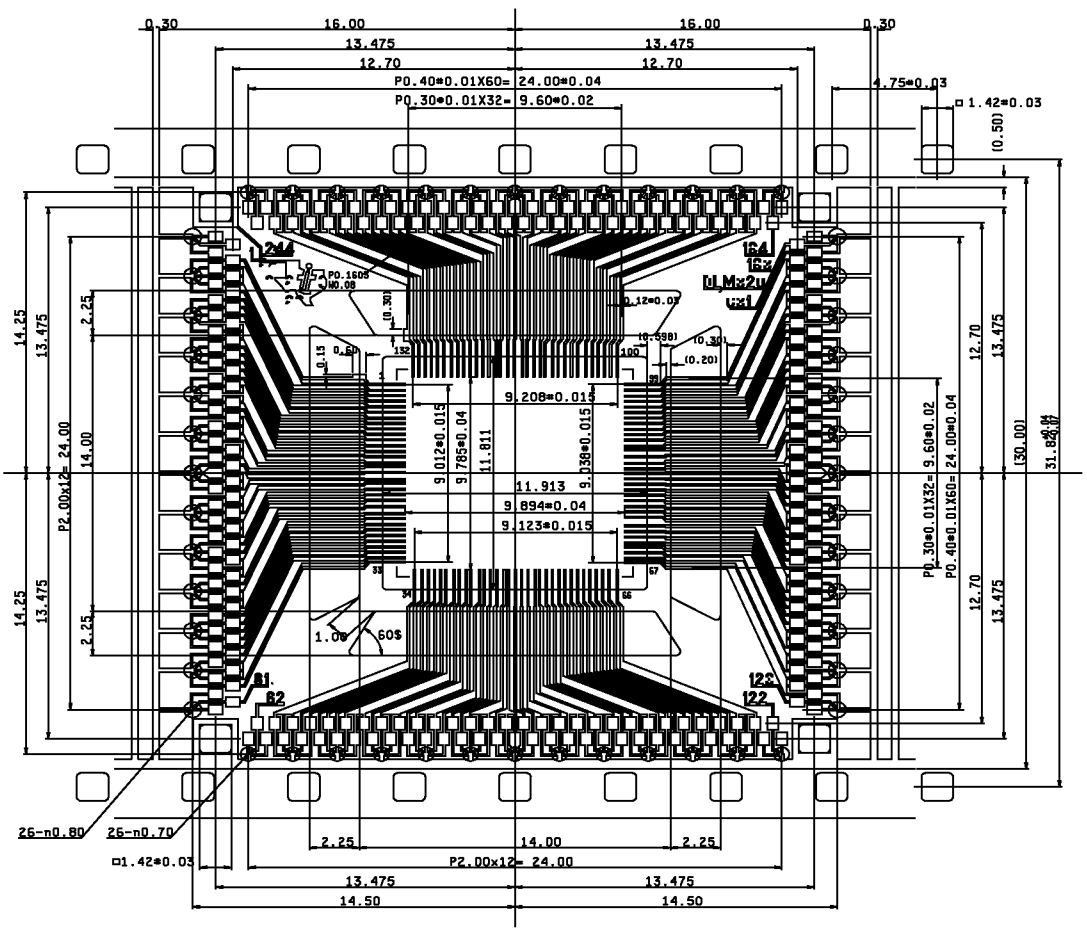
Case Y



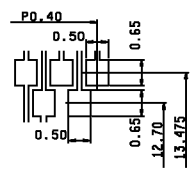
Letter	Inches		Millimeters		NOTES
	Min	Max	Min	Max	
A	---	0.116	---	2.95	
A1	---	0.091	---	2.31	
A2	0.002	0.014	0.05	0.35	At braze pads
B	0.009	0.016	0.22	0.41	
B1	0.025 BSC		0.064		
C	0.005	0.010	0.12	0.26	
D	-----	2.025	-----	51.44	
D1,E1	0.945	0.960	24.00	24.38	
D2,E2	0.800 BSC		20.32 BSC		
D4	0.005 BSC		0.13 BSC		
E	-----	2.025	-----	51.44	
F	1.990	2.015	50.55	51.18	Tie bar dimension
G	1.210 BSC		30.73 BSC		Tie bar dimension
H	0.195	0.205	4.95	5.21	Tie bar dimension
H1	0.030	0.040	0.76	1.02	Tie bar dimension
K	0.058	0.062	1.4	1.57	4 Places

FIGURE 1. Case outlines - continued

Case Z, U



Detail of Test Pads (X20)



Detail of Inner Leads (X50)

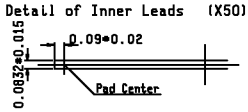


Figure 1. Case Outline - Continued

Device types 01,02,03 and 04

1/ 2/ 3/ 4/ 5/

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
L1	A0	V10	D9	H18	IACK	L5	V_{SSL}
K2	A1	W9	D10	J17	INT0	H2	DV_{SS}
J1	A2	U9	D11	E19	INT1	M4	CV_{SS}
J3	A3	V8	D12	F18	INT2	F4	DV_{SS}
G1	A4	W7	D13	G17	INT3	T6	CV_{SS}
F2	A5	U7	D14	C11	MCBL/MP	P4	V_{SSL}
E1	A6	V6	D15	L19	R/W	T10	V_{SSL}
E3	A7	W5	D16	N17	RDY	K4	DV_{SS}
D2	A8	U5	D17	K18	RESET	T4	IV_{SS}
C1	A9	V4	D18	A17	SHZ	G3	DV_{SS}
C3	A10	W3	D19	M18	STRB	K16	CV_{SS}
B2	A11	U3	D20	B16	TCLK0	Y8	IV_{SS}
A1	A12	V2	D21	C15	TCLK1	J15	V_{SSL}
C5	A13	W1	D22	G5	AV_{DD}	W13	DV_{SS}
B4	A14	R3	D23	E7	AV_{DD}	D10	CV_{SS}
A3	A15	T2	D24	E5	AV_{DD}	D16	IV_{SS}
C7	A16	U1	D25	N5	V_{DDL}	T16	DV_{SS}
B6	A17	N3	D26	R5	V_{DDL}	D12	V_{SSL}
C9	A18	P2	D27	H4	DV_{DD}	F16	CV_{SS}
B8	A19	R1	D28	J5	DV_{DD}	H16	IV_{SS}
A7	A20	L3	D29	T14	DV_{DD}	D14	V_{SUBS}
A9	A21	M2	D30	R7	V_{DDL}	U15	DV_{SS}
B10	A22	N1	D31	R9	V_{DDL}	C13	CV_{SS}
A11	A23	C19	DR0	R13	DV_{DD}	T18	X1
E17	CLKR0	C17	DX0	R15	DV_{DD}	U19	X2/CLKIN
A19	CLKX0	B14	EMU0	P16	CV_{DD}	J19	XF0
W19	D0	A13	EMU1	N15	CV_{DD}	G19	XF1
V16	D1	B12	EMU2	G15	V_{DDL}	F6	N. C.
W17	D2	A15	EMU3	E15	V_{DDL}	D4	DV_{SS}
U13	D3	D18	FSR0	L15	PV_{DD}	N19	DV_{SS}
V14	D4	B18	FSX0	E9	PV_{DD}	R17	DV_{SS}
W15	D5	P18	HOLD	E13	V_{DDL}	L17	DV_{SS}
U11	D6	R19	HOLDA	E11	V_{DDL}	M16	DV_{SS}
V12	D7	V18	H1	T12	DV_{SS}	D6	DV_{SS}
W11	D8	U17	H3	R11	V_{SSL}	A5	DV_{SS}
						D8	DV_{SS}

FIGURE 2. Terminal connections.

Device types 01,02,03 and 04

1/ 2/ 3/ 4/ 5/

Case outline Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A9	34	DV_{SS}	67	DV_{SS}	100	V_{SUBS}
2	DV_{SS}	35	D19	68	CV_{SS}	101	SHZ
3	A8	36	D18	69	IV_{SS}	102	DV_{SS}
4	A7	37	D17	70	X2/CLKIN	103	TCLK0
5	A6	38	D16	71	X1	104	PV_{DD}
6	A5	39	D15	72	HOLDA	105	TCLK1
7	AV_{DD}	40	CV_{SS}	73	HOLD	106	EMU3
8	A4	41	D14	74	CV_{DD}	107	EMU0
9	A3	42	DV_{DD}	75	RDY	108	EMU1
10	A2	43	D13	76	STROBE	109	EMU2
11	A1	44	IV_{SS}	77	R/W	110	MCBL/MP
12	A0	45	D12	78	RESET	111	CV_{SS}
13	CV_{SS}	46	D11	79	XF0	112	A23
14	D31	47	D10	80	CV_{DD}	113	A22
15	V_{DDL}	48	V_{DDL}	81	XF1	114	V_{DDL}
16	V_{DDL}	49	V_{DDL}	82	IACK	115	V_{DDL}
17	D30	50	D9	83	INT0	116	A21
18	V_{SSL}	51	D8	84	DV_{SS}	117	A20
19	V_{SSL}	52	DV_{SS}	85	V_{SSL}	118	V_{SSL}
20	DV_{SS}	53	V_{SSL}	86	INT1	119	DV_{SS}
21	D29	54	V_{SSL}	87	V_{DDL}	120	A19
22	D28	55	D7	88	V_{DDL}	121	AV_{DD}
23	DV_{DD}	56	D6	89	INT2	122	A18
24	D27	57	DV_{DD}	90	INT3	123	A17
25	IV_{SS}	58	D5	91	DR0	124	A16
26	D26	59	D4	92	CV_{SS}	125	A15
27	D25	60	D3	93	FSR0	126	A14
28	D24	61	D2	94	CLKR0	127	A13
29	D23	62	D1	95	CLKX0	128	A12
30	D22	63	D0	96	IV_{SS}	129	A11
31	D21	64	H1	97	FSX0	130	AV_{DD}
32	DV_{DD}	65	H3	98	PV_{DD}	131	A10
33	D20	66	DV_{DD}	99	DX0	132	CV_{SS}

1/ ADV_{DD}, DV_{DD}, CV_{DD}, and PV_{DD} pins are on a common plane internal to the device.

2/ V_{DD} pins are on a common plane internal to the device.

3/ V_{SS}, CV_{SS}, and IV_{SS} pins (B2, B14, C8, H3, H13, N8, and P14) are on a common plane internal to the device.

4/ DV_{SS} pins (C3, C13, N3, and N13) are on a common plane internal to the device.

5/ These V_{subs} are connected to die metalization. Tie these pins to a clean ground.

FIGURE 2. Terminal connections - Continued.

Case Z, U

Die Side #1

C31 Die Bond Pad Locations	Die/Tab Bond Pad Identity	Tab C31 Test Pads Locations	X Coordinate of Center of Bond Pad	Y Coordinate of Center of Bond Pad	Pitch of Lead (#,#) Ref Which Die Bonds
	N/C	1,2,3			
1	A9	4	0	0	300.00 (1,2)
2	DV_{SS}	5,6,7	0	-300	269.20 (2,3)
3	A8	8	0	-569.2	274.60 (3,4)
4	A7	9	0	-843.8	293.20 (4,5)
5	A6	10	0	-1137	278.60 (5,6)
6	A5	11	0	-1415.6	295.20 (6,7)
7	AV_{DD}	12,13,14	0	-1710.8	263.20 (7,8)
8	A4	15	0	-1974	277.40 (8,9)
9	A3	16	0	-2251.4	285.00 (9,10)
10	A2	17	0	-2536.4	273.40 (10,11)
11	A1	18	0	-2809.8	298.40 (11,12)
12	A0	19	0	-3108.2	297.80 (12,13)
13	CV_{SS}	20,21,22	0	-3406	256.80 (13,14)
14	D31	23	0	-3662.8	320.80 (14,15)
15	V_{DDL}	24,25,26	0	-3983.6	180.40 (15,16)
16	V_{DDL}	27,28,29	0	-4164	293.80 (16,17)
17	D30	30	0	-4457.8	363.60 (17,18)
18	V_{SSL}	31,32,33	0	-4821.4	180.00 (18,19)
19	V_{SSL}	34,35,36	0	-5001.4	315.40 (19,20)
20	DV_{SS}	37,38,39	0	-5316.8	278.00 (20,21)
21	D29	40	0	-5594.8	278.40 (21,22)
22	D28	41	0	-5873.2	320.20 (22,23)
23	DV_{DD}	42,43,44	0	-6193.4	349.80 (23,24)
24	D27	45	0	-6543.2	253.20 (24,25)
25	IV_{SS}	46,47,48	0	-6796.4	305.80 (25,26)
26	D26	49	0	-7102.2	272.20 (26,27)
27	D25	50	0	-7374.4	285.20 (27,28)
28	D24	51	0	-7659.6	287.80 (28,29)
29	D23	52	0	-7947.4	290.40 (29,30)
30	D22	53	0	-8237.8	258.80 (30,31)
31	D21	54	0	-8496.6	291.60 (31,32)
32	DV_{DD}	55,56,57	0	-8788.2	224.20 (32,33)
33	D20	58	0	-9012.4	
	N/C	59,60,61			

Figure 2. Terminal connections.

Die Side #2

C31 Die Bond Pad Locations	Die/Tab Bond Pad Identity	Tab C31 Test Pads Locations	X Coordinate of Center of Bond Pad	Y Coordinate of Center of Bond Pad	Pitch of Lead (#,#) Ref Which Die Bonds
	N/C	62,63,64			
34	DV_{SS}	65,66,67	508.6	-9480.4	352.60 (34,35)
35	D19	68	861.2	-9480.4	280.80 (35,36)
36	D18	69	1142	-9480.4	272.00 (36,37)
37	D17	70	1414	-9480.4	268.80 (37,38)
38	D16	71	1682.8	-9480.4	243.20 (38,39)
39	D15	72	1926	-9480.4	375.60 (39,40)
40	CV_{SS}	73,74,75	2301.6	-9480.4	212.40 (40,41)
41	D14	76	2514	-9480.4	314.00 (41,42)
42	DV_{DD}	77,78,79	2828	-9480.4	207.60 (42,43)
43	D13	80	3035.6	-9480.4	400.60 (43,44)
44	IV_{SS}	81,82,83	3436.2	-9480.4	214.60 (44,45)
45	D12	84	3650.8	-9480.4	268.80 (45,46)
46	D11	85	3919.6	-9480.4	293.60 (46,47)
47	D10	86	4213.2	-9480.4	343.40 (47,48)
48	V_{DDL}	87,88,89	4556.6	-9480.4	179.60 (48,49)
49	V_{DDL}	90,91,92	4736.2	-9480.4	315.40 (49,50)
50	D9	93	5051.6	-9480.4	281.60 (50,51)
51	D8	94	5333.2	-9480.4	285.20 (51,52)
52	DV_{SS}	95,96,97	5618.4	-9480.4	340.00 (52,53)
53	V_{SSL}	98,99,100	5958.4	-9480.4	180.40 (53,54)
54	V_{SSL}	101,102,103	6138.8	-9480.4	289.60 (54,55)
55	D7	104	6428.4	-9480.4	286.40 (55,56)
56	D6	105	6714.8	-9480.4	297.80 (56,57)
57	DV_{DD}	106,107,108	7012.6	-9480.4	267.00 (57,58)
58	D5	109	7279.6	-9480.4	280.80 (58,59)
59	D4	110	7560.4	-9480.4	282.40 (59,60)
60	D3	111	7842.8	-9480.4	284.80 (60,61)
61	D2	112	8127.6	-9480.4	276.00 (61,62)
62	D1	113	8403.6	-9480.4	285.60 (62,63)
63	D0	114	8689.2	-9480.4	290.40 (63,64)
64	H1	115	8979.6	-9480.4	274.40 (64,65)
65	H3	116	9254	-9480.4	377.20 (65,66)
66	DV_{DD}	117,118,119	9631.2	-9480.4	
	N/C	120,121,122			

Figure 2. Terminal connections - Continued

Case Z, U

Die Side #3

C31 Die Bond Pad Locations	Die/Tab Bond Pad Identity	Tab C31 Test Pads Locations	X Coordinate of Center of Bond Pad	Y Coordinate of Center of Bond Pad	Pitch of Lead (#,#) Ref Which Die Bonds
	N/C	123,124			
67	DV_{SS}	125,126,127	10074	-9032.6	210.40 (67,68)
68	CV_{SS}	128,129,130	10074	-8822.2	280.00 (68,69)
69	IV_{SS}	131,132,133	10074	-8542.2	301.80 (69,70)
70	X2/CLKIN	134	10074	-8240.4	186.20 (70,71)
71	X1	135	10074	-8054.2	311.40 (71,72)
72	HOLDA^	136	10074	-7742.8	282.80 (72,73)
73	HOLD^	137	10074	-7460	293.00 (73,74)
74	CV_{DD}	138,139,140	10074	-7167	431.00 (74,75)
75	RDY^	141	10074	-6736	276.80 (75,76)
76	STRB^	142	10074	-6459.2	268.00 (76,77)
77	R/W^	143	10074	-6191.2	295.20 (77,78)
78	RESET^	144	10074	-5896	278.40 (78,79)
79	XF0	145	10074	-5617.6	266.60 (79,80)
80	CV_{DD}	146,147,148	10074	-5351	291.00 (80,81)
81	XF1	149	10074	-5060	275.20 (81,82)
82	IACK	150	10074	-4784.8	280.80 (82,83)
83	INT0^	151	10074	-4504	224.80 (83,84)
84	DV_{SS}	152,153,154	10074	-4279.2	280.40 (84,85)
85	V_{SSL}	155,156,157	10074	-3998.8	326.80 (85,86)
86	INT1^	158	10074	-3672	341.40 (86,87)
87	V_{DDL}	159,160,161	10074	-3330.6	180.40 (87,88)
88	V_{DDL}	162,163,164	10074	-3150.2	323.80 (88,89)
89	INT2^	165	10074	-2826.4	279.80 (89,90)
90	INT3^	166	10074	-2546.6	266.40 (90,91)
91	DR0	167	10074	-2280.2	310.00 (91,92)
92	CV_{SS}	168,169,170	10074	-1970.2	270.80 (92,93)
93	FSR0	171	10074	-1699.4	275.60 (93,94)
94	CLKR0	172	10074	-1423.8	280.60 (94,95)
95	CLKX0	173	10074	-1143.2	280.40 (95,96)
96	IV_{SS}	174,175,176	10074	-862.8	261.40 (96,97)
97	FSX0	177	10074	-601.4	312.80 (97,98)
98	PV_{DD}	178,179,180	10074	-288.6	294.20 (98,99)
99	DX0	181	10074	5.6	
	N/C	182,183			

Figure 2. Terminal connections - Continued

Case Z, U

Die Side #4

C31 Die Bond Pad Locations	Die/Tab Bond Pad Identity	Tab C31 Test Pads Locations	X Coordinate of Center of Bond Pad	Y Coordinate of Center of Bond Pad	Pitch of Lead (#,#) Ref Which Die Bonds
	N/C	184,185,186			
100	V_{SUBS}	187,188,189	9649.4	484.8	314.20 (100,101)
101	SHZ^	190	9335.2	484.8	279.60 (101,102)
102	DV_{SS}	191,192,193	9055.6	484.8	278.80 (102,103)
103	TCLK0	194	8776.8	484.8	270.00 (103,104)
104	PV_{DD}	195,196,197	8506.8	484.8	283.60 (104,105)
105	TCLK1	198	8223.2	484.8	372.20 (105,106)
106	EMU3	199	7851	484.8	270.40 (106,107)
107	EMU0	200	7580.6	484.8	303.20 (107,108)
108	EMU1	201	7277.4	484.8	300.80 (108,109)
109	EMU2	202	6976.6	484.8	240.00 (109,110)
110	MCBL/MP^	203	6736.6	484.8	342.60 (110,111)
111	CV_{SS}	204,205,206	6394	484.8	203.00 (111,112)
112	A23	207	6191	484.8	295.60 (112,113)
113	A22	208	5895.4	484.8	330.80 (113,114)
114	V_{DDL}	209,210,211	5564.6	484.8	180.40 (114,115)
115	V_{DDL}	212,213,214	5384.2	484.8	397.40 (115,116)
116	A21	215	4986.8	484.8	282.00 (116,117)
117	A20	216	4704.8	484.8	338.00 (117,118)
118	V_{SSL}	217,218,219	4366.8	484.8	180.40 (118,119)
119	DV_{SS}	220,221,222	4186.4	484.8	322.60 (119,120)
120	A19	223	3863.8	484.8	277.40 (120,121)
121	AV_{DD}	224,225,226	3586.4	484.8	295.60 (121,122)
122	A18	227	3290.8	484.8	276.20 (122,123)
123	A17	228	3014.6	484.8	290.20 (123,124)
124	A16	229	2724.4	484.8	267.00 (124,125)
125	A15	230	2457.4	484.8	284.80 (125,126)
126	A14	231	2172.6	484.8	346.60 (126,127)
127	A13	232	1826	484.8	276.00 (127,128)
128	A12	233	1550	484.8	278.20 (128,129)
129	A11	234	1271.8	484.8	282.80 (129,130)
130	AV_{DD}	235, 236, 237	989	484.8	273.80 (130,131)
131	A10	238	715.2	484.8	274.20 (131,132)
132	CV_{SS}	239, 240, 241	441	484.8	
	N/C	242 ,243 ,244			

Note: ^ denotes Active Low

FIGURE 2. Terminal connections - continued

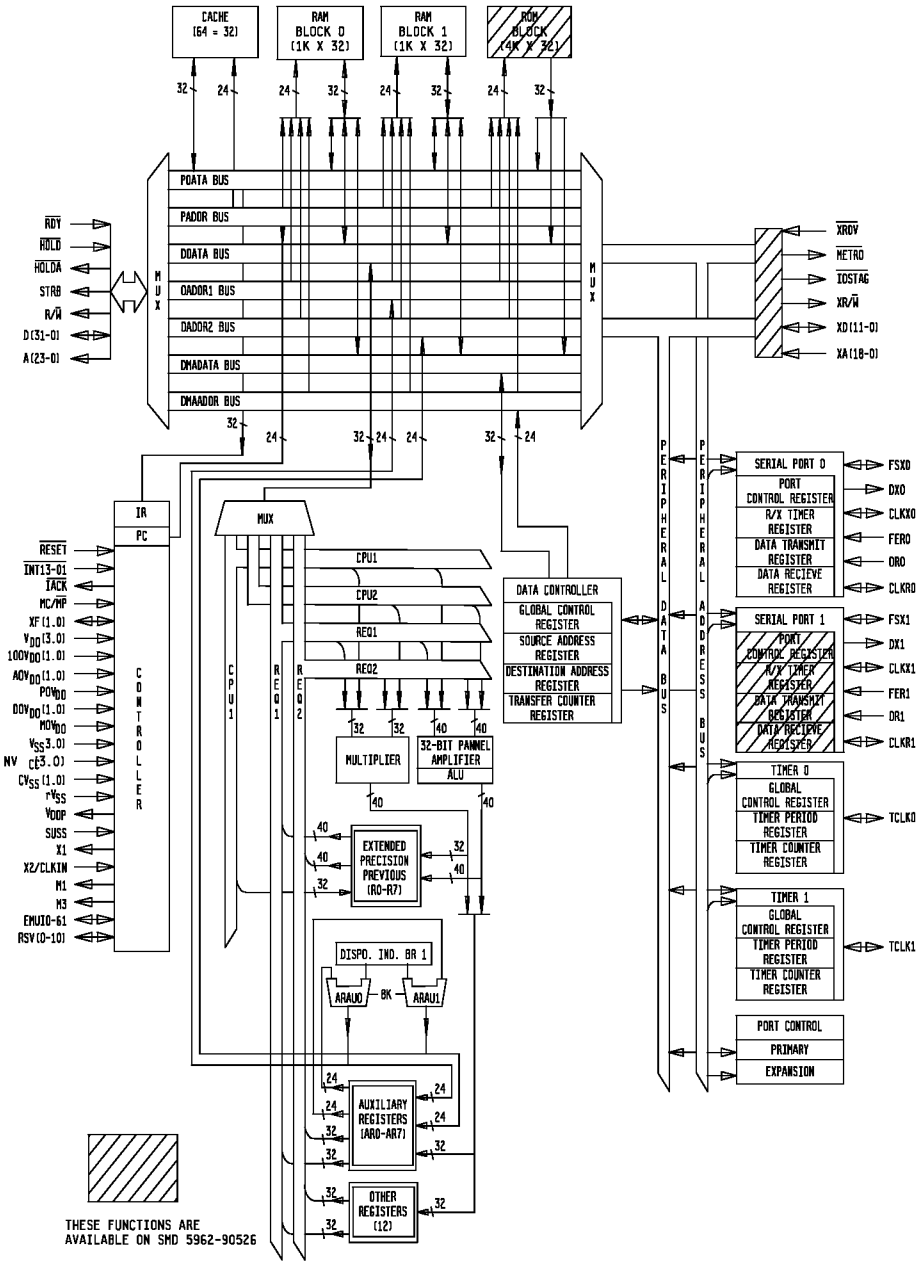
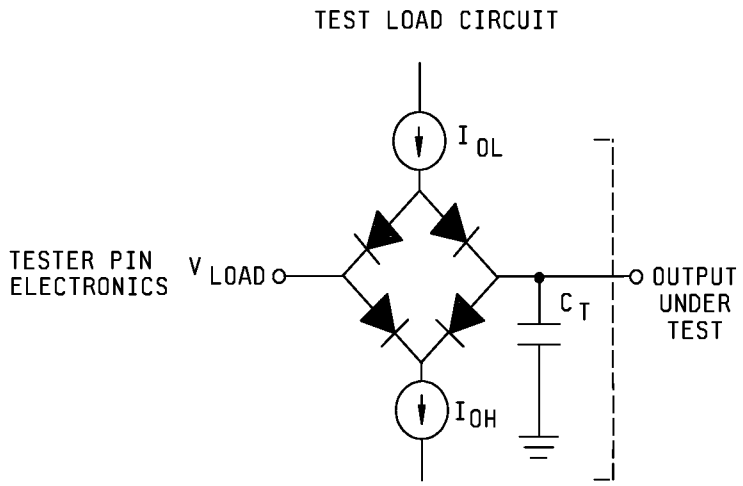
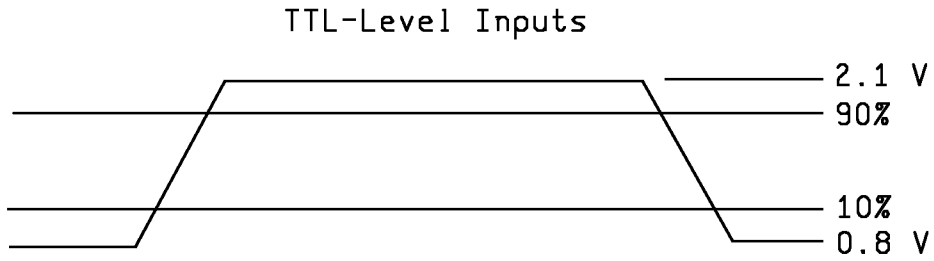


FIGURE 3. Functional block diagram

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-92058
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL F	SHEET 27



Where: I_{OL} = 2.0 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{Load} = 1.54 V to emulate 50Ω
C_T = 80 pF typical load circuit capacitance.



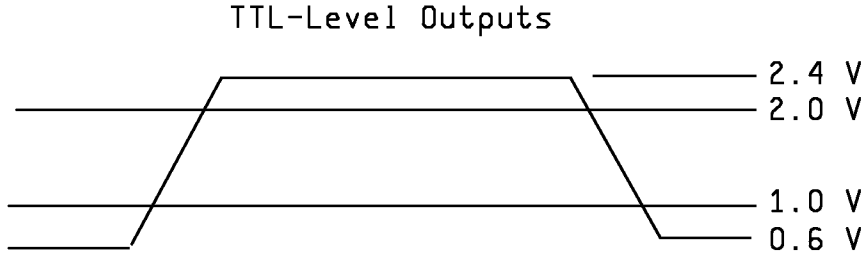
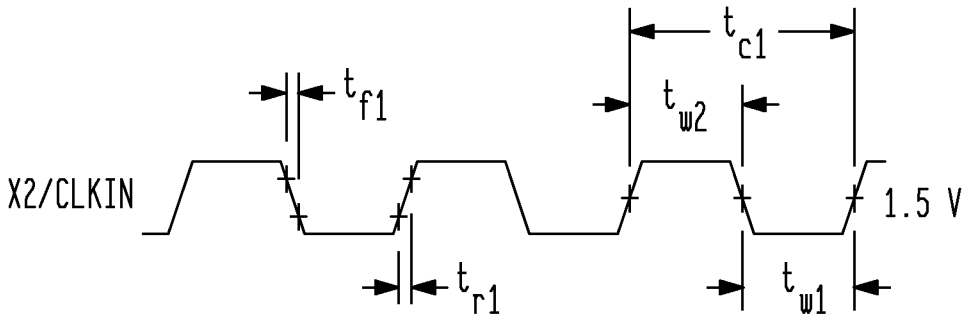


FIGURE 4. Switching waveforms and test circuit.

X2/CLKIN timing



H1/H3 timing

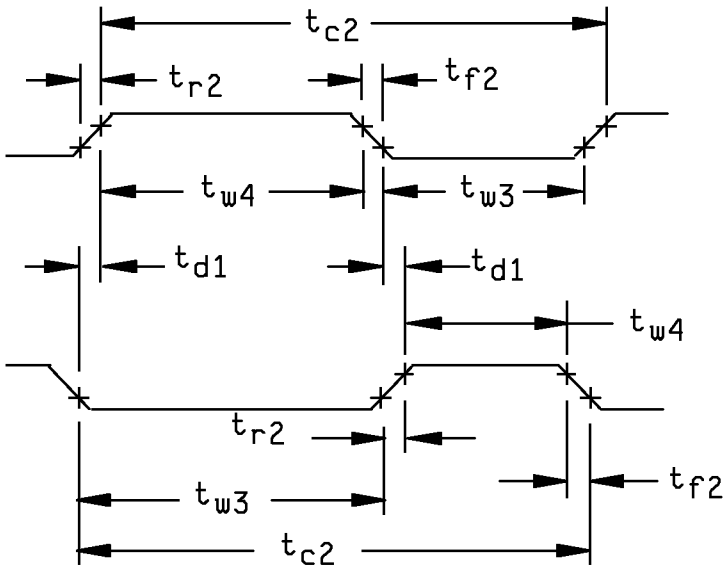


FIGURE 4. Switching waveforms and test circuit - continued.

Memory ((M)$\overline{\text{STRB}}$ = 0) Read

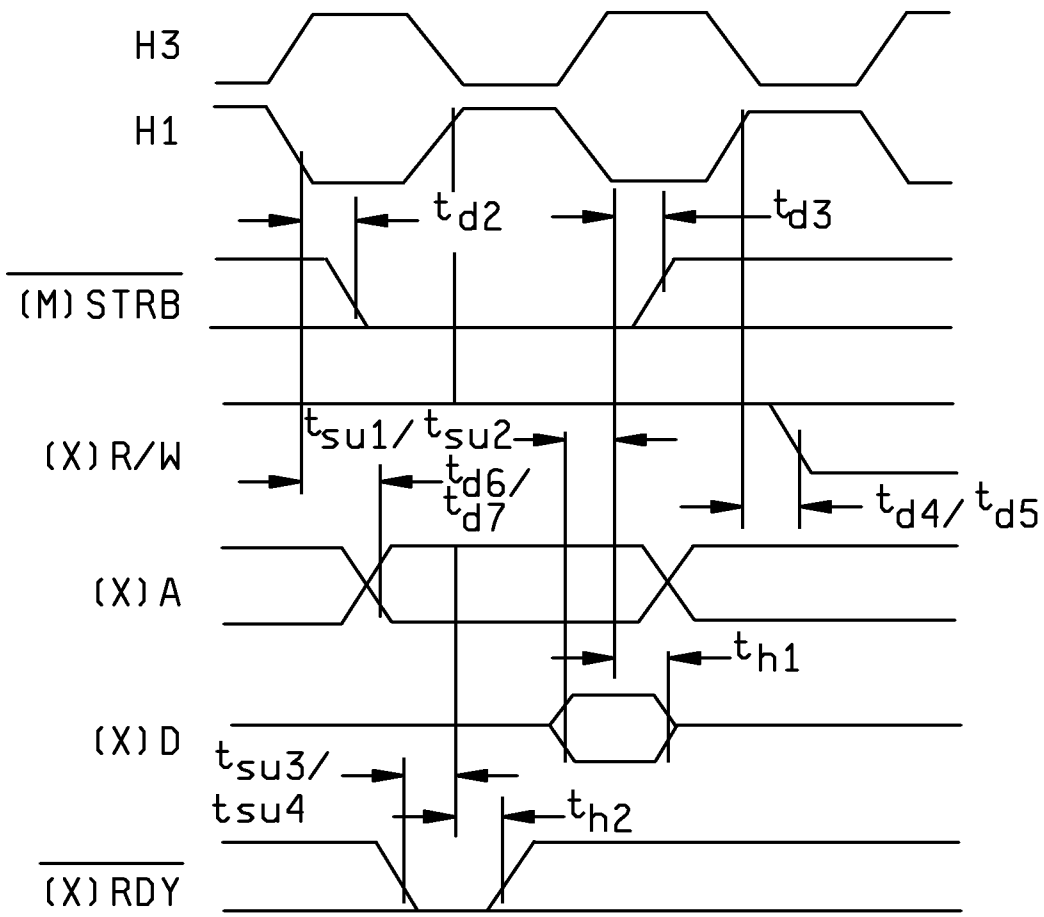


FIGURE 4. Switching waveforms and test circuit - continued.

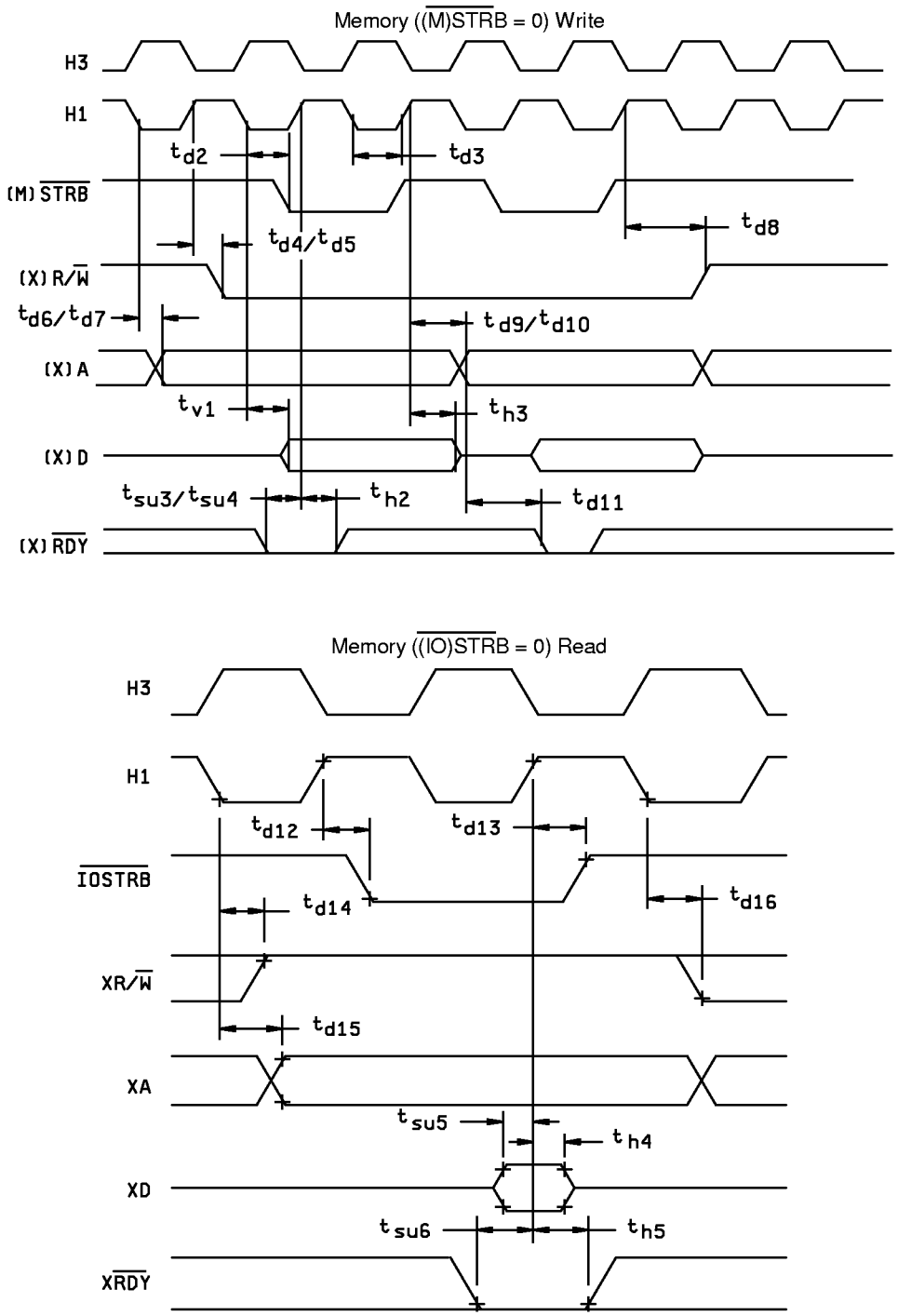
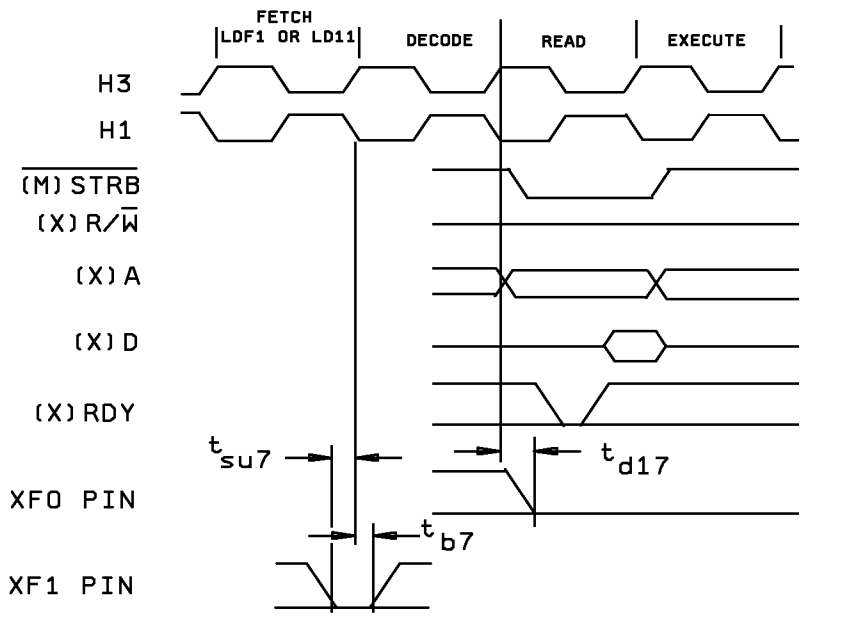
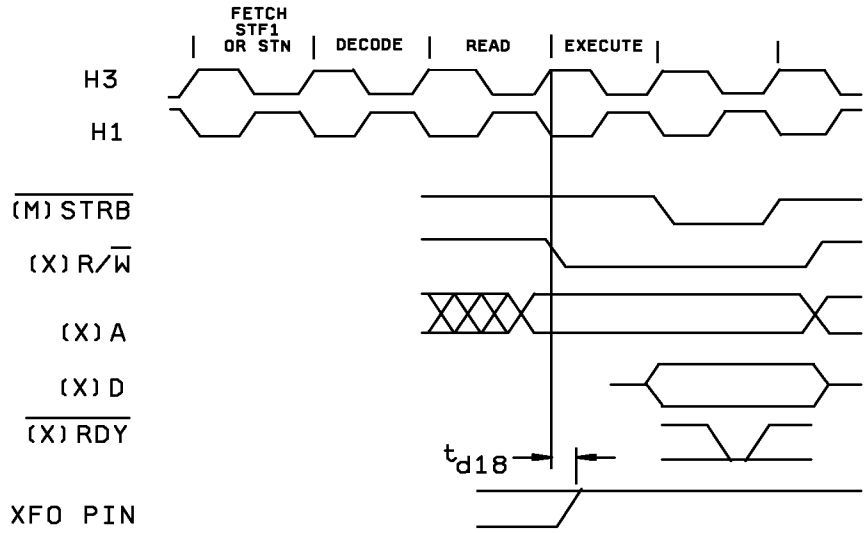


FIGURE 4. Switching waveforms and test circuit - continued.

Timing XF0 and XF1 when executing LDF1 or LDII

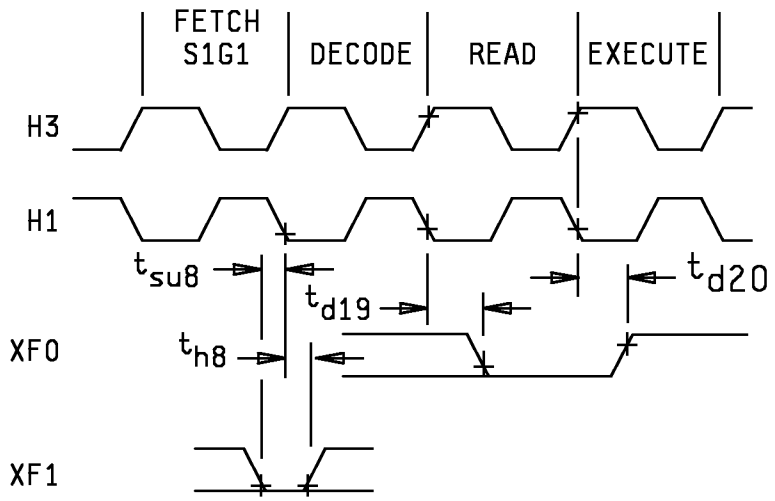




Timing for XF0 when executing a STF1 or STII

FIGURE 4. Switching waveforms and test circuit - continued.

Timing for XF0 and XF1 when executing SIGI



Timing for loading XF register when configured as an output pin

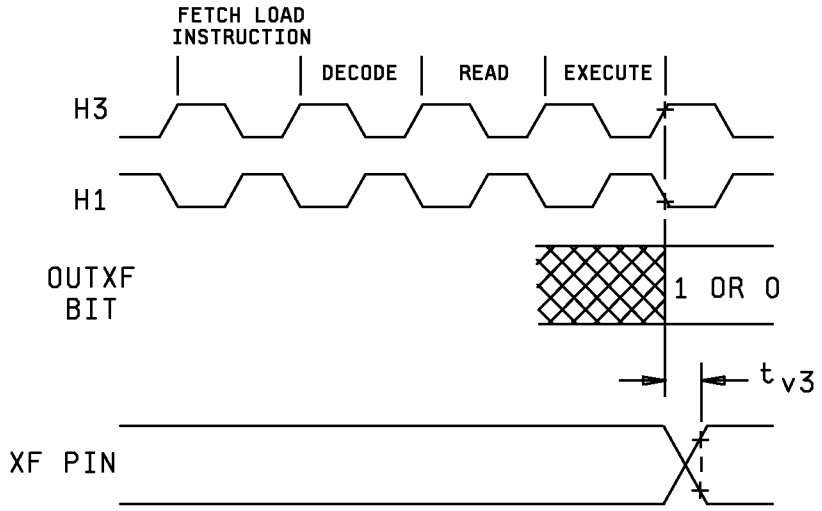
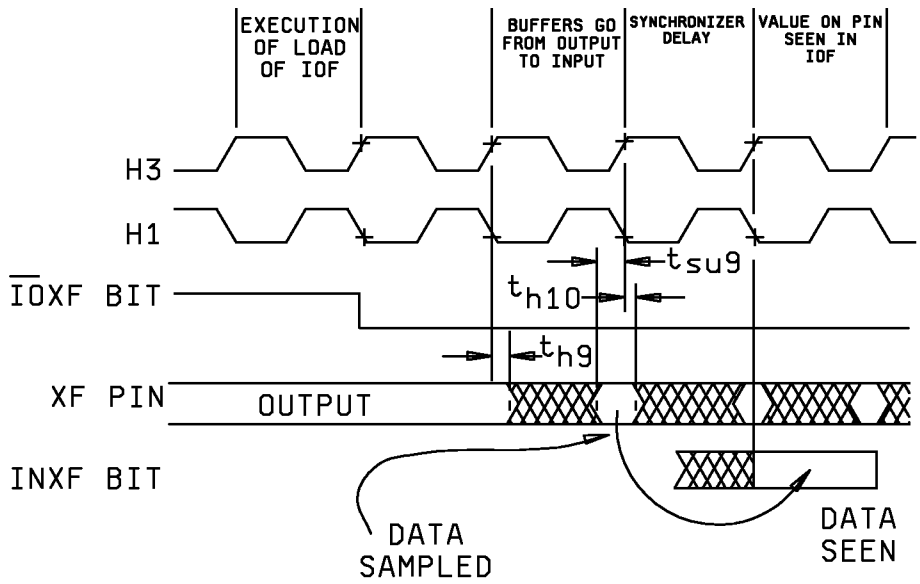


FIGURE 4. Switching waveforms and test circuit - continued.

Change of XF from output to input mode



Change of XF from input to output mode

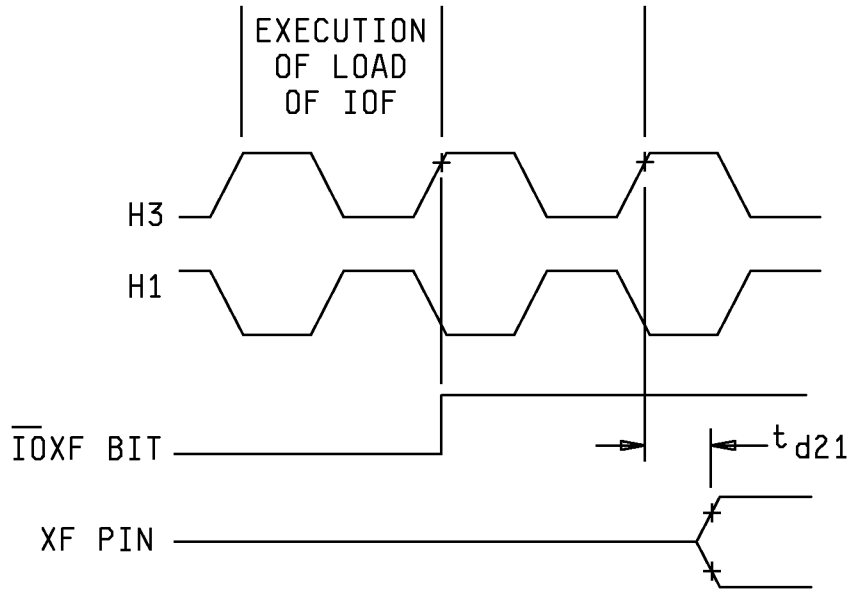
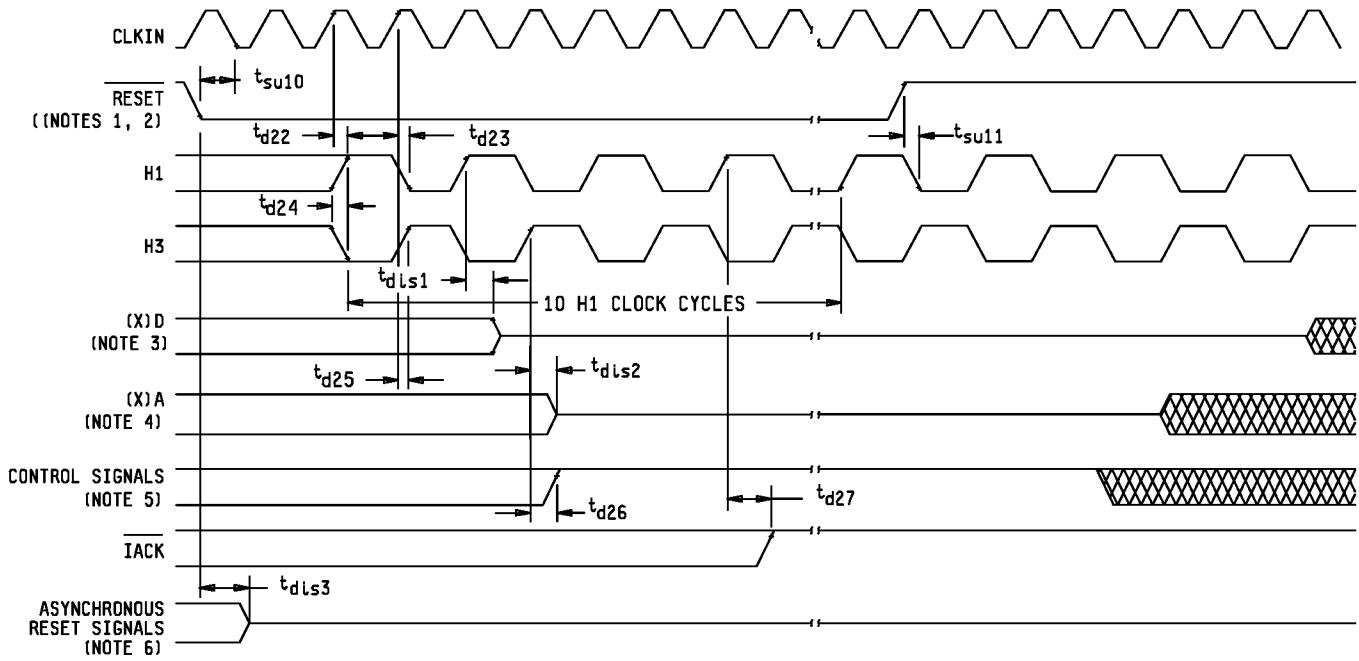


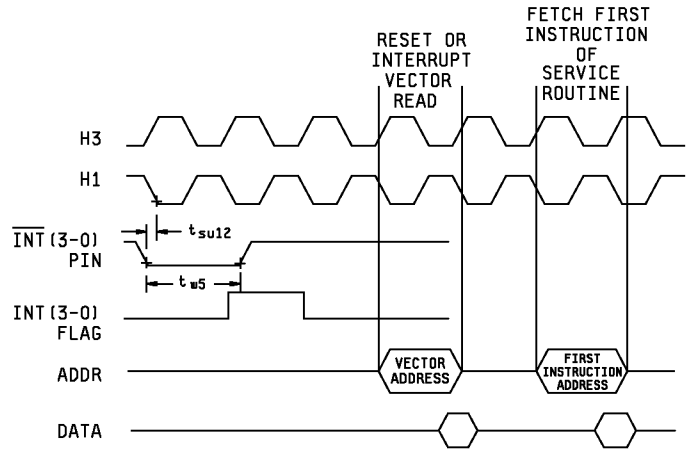
FIGURE 4. Switching waveforms and test circuit - continued.



NOTES:
1. RESET is asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.
2. Note that the R/W outputs are placed in a high impedance state during reset and can be provided with a resistive pull-up, nominally 20 KΩ, if desirable spurious writes could be caused when these outputs go low.
3. (X)D includes D(31-0) and XD(31-0).
4. (X)A includes A(23-0), XA(12-0).
5. Control signals include STRB, MSTRB, and IOSTRB.
6. Asynchronously reset signals include XF1, XF0, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, and TCLK1.

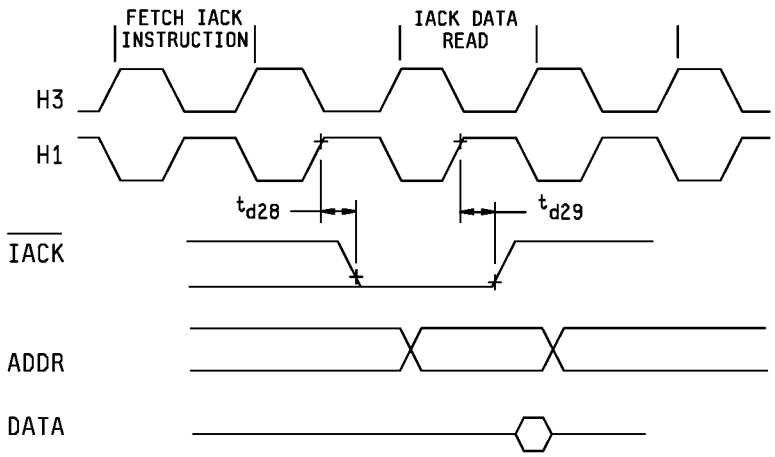
FIGURE 4. Switching waveforms and test circuit - continued.

$\overline{\text{INT}}$(3-0) response timing



NOTES:
7. Interrupt pulse width must be at least 1 P wide to guarantee it will be seen. It must be less than 2 P wide to guarantee it will be responded to only once. The recommended pulse width is 1.5 P.
8. INT is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

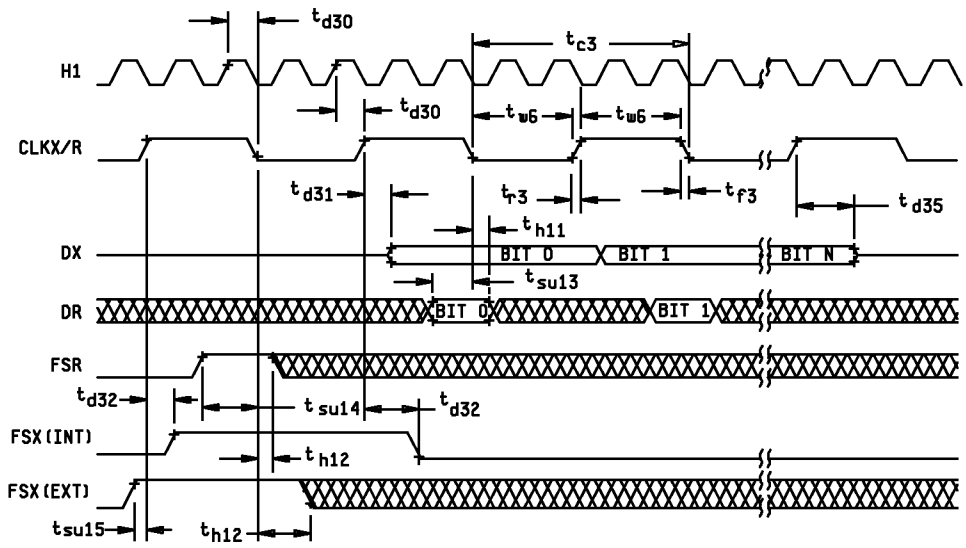
$\overline{\text{IACK}}$ timing



NOTE:
9. The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is therefore extended if the bus cycle utilizes wait states.

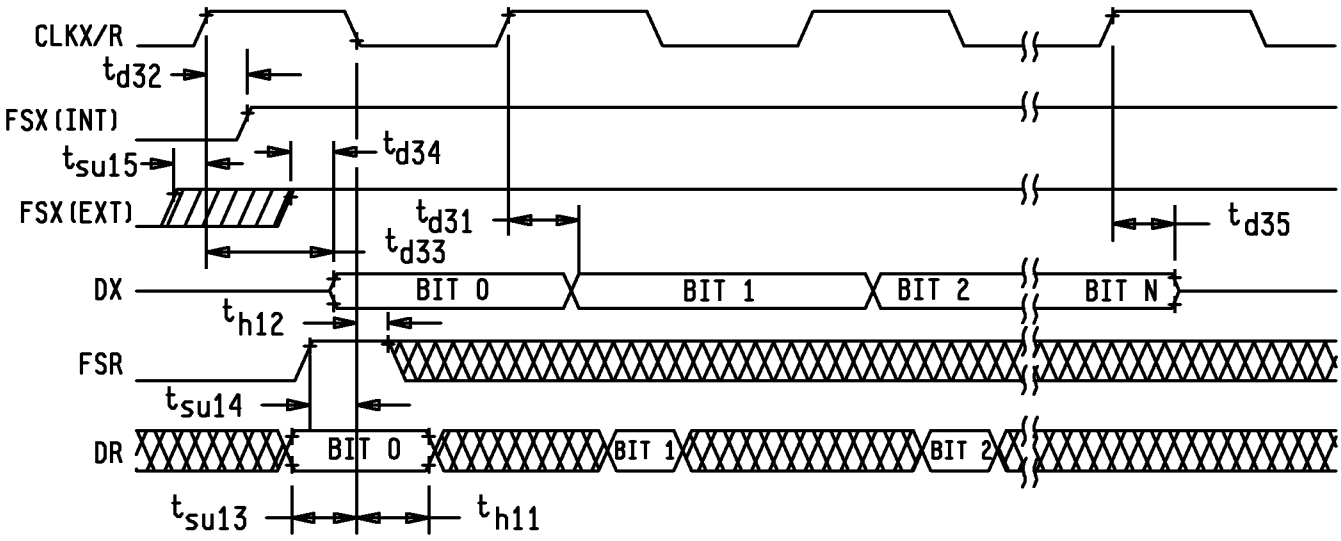
FIGURE 4. Switching waveforms and test circuit - Continued.

Fixed data rate mode



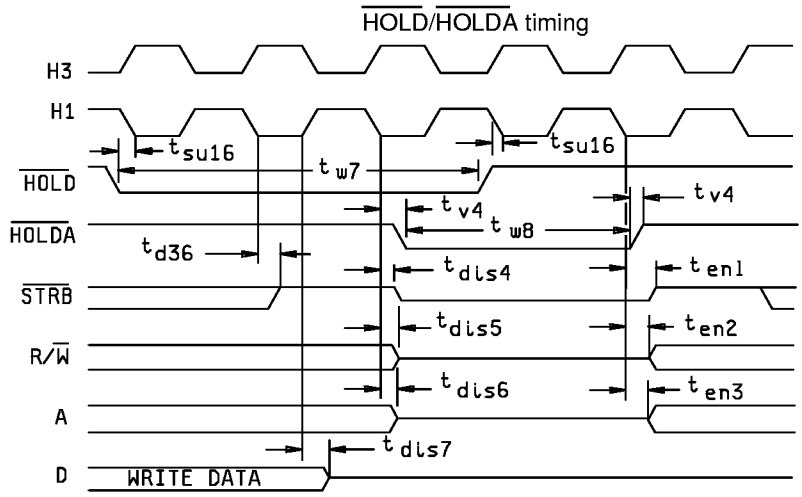
NOTES:
10. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
11. These timings are valid for all serial port modes, including handshake, except where otherwise indicated.

Variable data rate mode



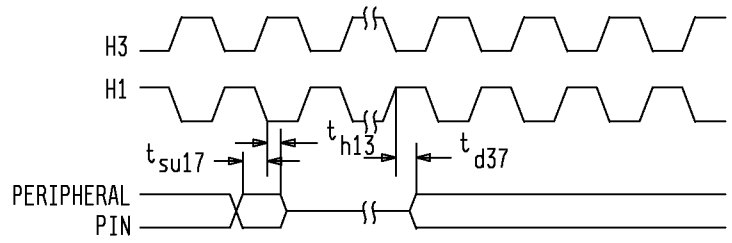
NOTES:
12. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
13. Timings not expressly specified for variable data rate mode are the same as those for fixed data rate mode.
14. Timings are valid for all serial port modes, including handshake mode, except where otherwise indicated.

FIGURE 4. Switching waveforms and test circuit - Continued.



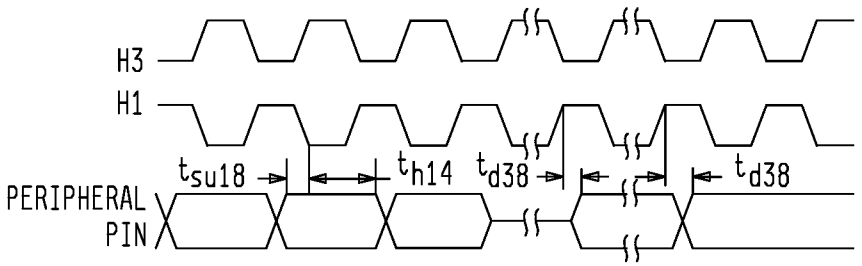
NOTE 15: HOLD is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

Peripheral pin general-purpose I/O timing



NOTE 16: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

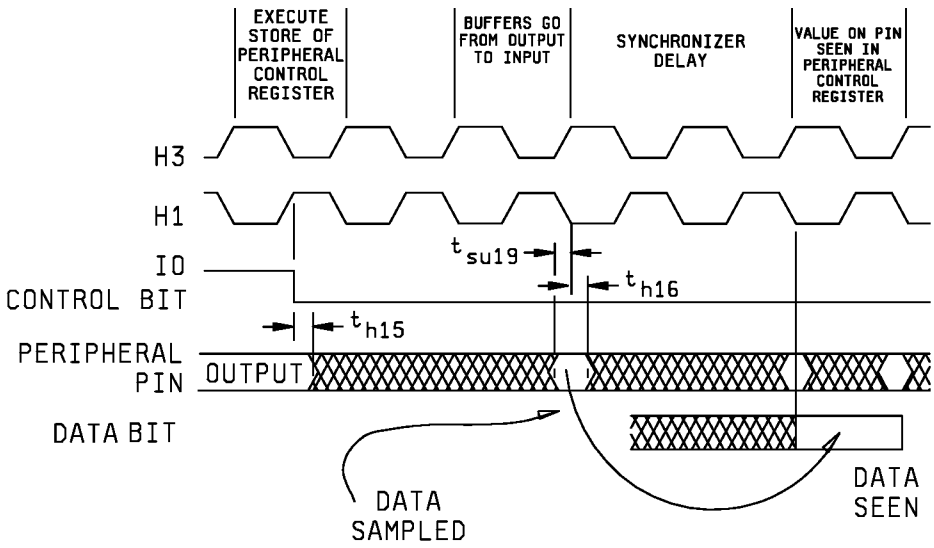
Timer pin timings



NOTE 17: Period and polarity of valid logic level are specified by contents of internal control registers.

FIGURE 4. Switching waveforms and test circuit - continued.

Change of peripheral pin from general purpose output to input mode



Change of peripheral pin from general-purpose input to output mode

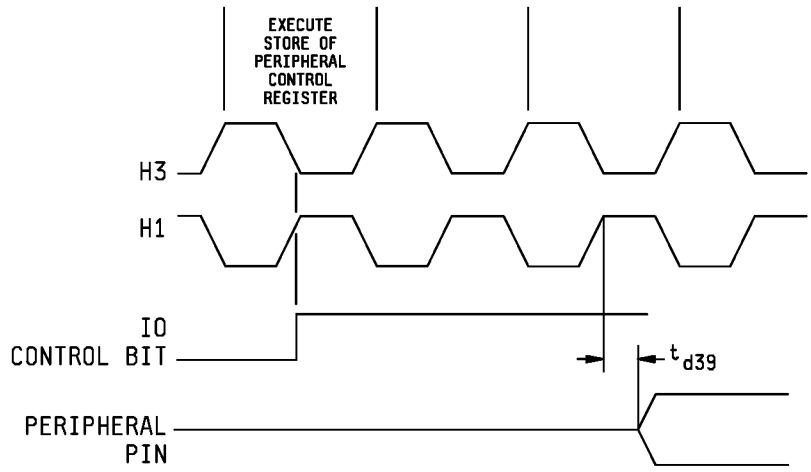


FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and Appendix F of MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and Appendix F of MIL-PRF-38535 and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535 and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN}, C_{OUT} and C_X measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

c. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B Inspection.

a. Attachability is not a requirement of Case outlines Z and U .

b. For Case outlines Z and U bond strength (method 2011) shall not be less than 30 g.

c. For Case outlines Z and U constant acceleration in accordance with Method 2001 test condition E, Y1 direction, is required. 4 devices are to be tested with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - - -	- - - -	- - - -
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group D end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group E end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25° C ±5° C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

PIN Name	PIN Numbers	I/O/Z 1/	Description
			Primary bus interface
D31-D0	32	I/O/Z	32-bit data port of the primary bus interface.
A23-A0	24	O/Z	24-bit address port of the primary bus interface.
R/$\overline{W}$	1	O/Z	Read/write signal for primary bus interface. This pin is high when a read is performed and low when a write is performed over the parallel interface.
$\overline{STRB}$	1	O/Z	External access strobe for the primary bus interface.
$\overline{RDY}$	1	I	Ready signal. This pin indicates that the external device is prepared for a primary bus interface transaction to complete. As long as RDY is a logic high, the data and address buses of the primary bus interface remain valid.
$\overline{HOLD}$	1	I	Hold signal for primary bus interface. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. The A23-A0, D31-D0, $\overline{STRB}$, and R/W signals are placed in a high-impedance state, and all transactions over the primary bus interface are held until $\overline{HOLD}$ becomes a logic high.
$\overline{HOLDA}$	1	O	Hold acknowledge signal for primary bus interface. This signal is generated in response to a logic low on $\overline{HOLD}$. It signals that A23-A0, D31-D0, $\overline{STRB}$, and R/W are placed in a high impedance state and that all transactions over the bus will be held. $\overline{HOLDA}$ will be high in response to a logic high of $\overline{HOLD}$.

6.5 Symbols, definitions, and functional descriptions - Continued.

PIN Name	PIN Numbers	I/O/Z 1/	Description
			Expansion bus interface
			Expansion bus interface
XD31-XD0	32	I/O/Z	32-bit data port of the expansion bus interface.
XA12-XA0	13	O/Z	13-bit address port of the expansion bus interface.
XR/$\overline{W}$	1	O/Z	Read/write signal for expansion bus interface. When a read is performed, this pin is held high; when a write is performed, this pin is low.
$\overline{MSTRB}$	1	O	External memory access strobe for the expansion bus interface.
$\overline{IOSTRB}$	1	O	External I/O access strobe for the expansion bus interface.
$\overline{XRDY}$	1	I	Ready signal. This pin indicates that the external device is prepared for an expansion bus interface transaction to complete. As long as XRDY is high, the data and address buses of the expansion bus interface remain valid.
			Control signals
$\overline{RESET}$	1	I	Reset. When this pin is a logic low, the device is placed in the reset condition. When RESET becomes a logic high, execution begins from the location specified by the reset vector.
$\overline{INT3}$-$\overline{INT0}$	4	I	External interrupts.
$\overline{IACK}$	1	O	Interrupt acknowledge signal. $\overline{IACK}$ is set to 1 by the $\overline{IACK}$ instruction. This can be used to indicate the beginning or end of an interrupt service routine.
$\overline{MC}$/MP	1	I	Microcomputer/microprocessor mode pin.
XF1, XF0	2	I/O	External flag pins. They are used as general-purpose I/O pins or to support interlocked processor instructions.
			Serial port 0 signals
CLKX0	1	I/O	Serial port 0 transmit clock. This pin serves as the serial shift clock for the serial port 0 transmitter.
DX0	1	O/Z	Data transmit output. Serial port 0 transmits serial data on this pin.
FSX0	1	I/O	Frame synchronization pulse for transmit. The FSX0 pulse initiates the transmit data process over pin DX0.
CLKR0	1	I/O	Serial port 0 receive clock. This pin serves as the serial shift clock for the serial port 0 transmitter.
DR0	1	I	Data receive. Serial port 0 receives serial data via the DR0 pin.
FSR0	1	I	Frame synchronization pulse for receive. The FSR0 pulse initiates the receive data process over DR0.

See footnotes at end of table.

6.5 Symbols, definitions, and functional descriptions - Continued.

PIN Name	Numbers	I/O/Z 1/	Description
			Serial port 1 signals
CLKX1	1	I/O	Serial port 1 transmit clock. This pin serves as the serial shift clock for the serial port 1 transmitter.
DX1	1	O/Z	Data transmit output. Serial port 1 transmits serial data on this pin.
FSX1	1	I/O	Frame synchronization pulse for transmit. The FSX1 pulse initiates the transmit data process over pin DX1.
CLKR1	1	I/O	Serial port 1 receive clock. This pin serves as the serial shift clock for the serial port 1 receiver.
DR1	1	I	Data receive. Serial port 1 receives serial data via the DR1 pin.
FSR1	1	I	Frame synchronization pulse for receive. The FSR1 pulse initiates the receive data process over DR1.
			Timer 0 signals
TCLKO	1	I/O	Timer clock. As an input, TCLK0 is used by timer 0 to count external pulses. As an output pin, TCLK0 outputs pulses generated by timer 0.
			Timer 1 signals
TCLK1	1	I/O	Timer clock. As an input, TCLK1 is used by timer 1 to count external pulses. As an output pin, TCLK1 outputs pulses generated by timer 1.
			Supply and oscillator signals 2/
V_{DD}	4/8	I	+5 V supply pin.
$IODV_{DD}$	2/3	I	+5 V supply pin.
ADV_{DD}	2/3	I	+5 V supply pin.
PDV_{DD}	1/2	I	+5 V supply pin.
DDV_{DD}	2/2	I	+5 V supply pin.
MDV_{DD}	1/2	I	+5 V supply pin.
V_{SS}	4/8	I	Ground pin.
DV_{SS}	4/4	I	Ground pin.
CV_{SS}	2/4	I	Ground pin.
IV_{SS}	1/2	I	Ground pin.
V_{BBP}	1/1	NC	V_{BB} pump oscillator output.

See footnotes at end of table.

6.5 Symbols, definitions, and functional descriptions - Continued.

PIN Name	I/O/Z Numbers	1/	Description Supply and oscillator signals 2/
V_{SUBS}	1/2	I	Substrate pin. Tie to ground.
X1	1	O	Output pin from the internal oscillator for the crystal. If a crystal is not used, this pin should be left unconnected.
X2/CLKIN	1	I	Input pin to the internal oscillator from the crystal or a clock.
H1	1	O	External H1 clock. This clock has a period equal to twice CLKIN.
H3	1	O	External H3 clock. This clock has a period equal to twice CLKIN.
	Reserved		
EMU0-EMU2	3	I	Reserved. Use pullups to +5 volts.
EMU3	1	O	Reserved.
EMU4	1	I	Reserved. Use pullups to +5 volts.
EMU5,EMU6	2	NC	Reserved.
RSV0-RSV10	11	I	Reserved. Use pullups to +5 volts.

1/ I = input, O = output, Z = high impedance state.
2/ Case X and Y power pins.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

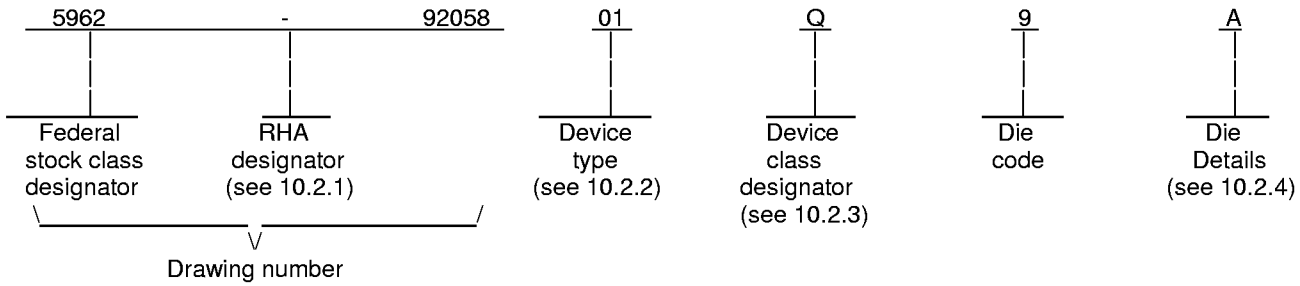
APPENDIX A

APPENDIX A FORMS A PART OF SMD 5962-92058

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	320C31-27	Digital signal processor, 27 MHz
02 1/	320C31-33	Digital signal processor, 33 MHz
03	320C31-40	Digital signal processor, 40 MHz
04 1/	320C31-50	Digital signal processor, 50 MHz

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

1/ Device types 01, 02, and 04 are not available as QML die only. These devices shall be procured as packaged devices per the main body of this document.

APPENDIX A

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10.2.4. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die physical dimensions.

Die type	Figure number
03	A-1

10.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
03	A-1

10.2.4.3. Interface materials.

Die type	Figure number
03	A-1

10.2.4.4. Assembly related information.

Die type	Figure number
03	A-1

10.3. Absolute maximum ratings.

See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.

See paragraph 1.4 within the body of this drawing for details.

APPENDIX A

APPENDIX A FORMS A PART OF SMD 5962-92058

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physlcal dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figures A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figures A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figures A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figures A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein.

50. Die carrier

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

6.0 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 296 mils x 317 mils.
Die thickness: 19 mils.

Interface materials.
Top metallization: Ti/TiW/AlSiCu.5 500A/3KA/4.5KA
Backside metallization: Silicon

Glassivation.
Type: Ox/N
Thickness: 3kA/ kA

Substrate: Silicon

Assembly related information.
Substrate potential: Biased to Ground
Special assembly instructions: None

APPENDIX A

PAD	X CENTER	Y CENTER	PAD NAME	PAD	X CENTER	Y CENTER	PAD NAME
1	0.00	0.00	A9	41	1786.32	-7219.80	D14
2	0.00	-224.46	DVSS	42	1974.78	-7219.80	DVDD
3	0.00	-426.24	A8	43	2162.16	-7219.80	D13
4	0.00	-650.70	A7	44	2350.62	-7219.80	IVSS
5	0.00	-875.16	A6	45	2538.00	-7219.80	D12
6	0.00	-1099.62	A5	46	2748.06	-7219.80	D11
7	0.00	-1302.48	AVDD	47	2958.12	-7219.80	D10
8	0.00	-1504.26	A4	48	3150.90	-7219.80	VDDL
9	0.00	-1728.72	A3	49	3313.26	-7219.80	VDDL
10	0.00	-1953.18	A2	50	3499.38	-7219.80	D9
11	0.00	-2177.64	A1	51	3709.44	-7219.80	D8
12	0.00	-2402.10	A0	52	3897.90	-7219.80	DVSS
13	0.00	-2604.96	CVSS	53	4068.00	-7219.80	VSSL
14	0.00	-2828.34	D31	54	4230.36	-7219.80	VSSL
15	0.00	-3100.32	VDDL	55	4416.48	-7219.80	D7
16	0.00	-3262.68	VDDL	56	4626.54	-7219.80	D6
17	0.00	-3463.20	D30	57	4815.00	-7219.80	DVDD
18	0.00	-3670.38	VSSL	58	5002.38	-7219.80	D5
19	0.00	-3832.74	VSSL	59	5212.44	-7219.80	D4
20	0.00	-4011.66	DVSS	60	5422.50	-7219.80	D3
21	0.00	-4256.64	D29	61	5632.56	-7219.80	D2
22	0.00	-4481.10	D28	62	5842.62	-7219.80	D1
23	0.00	-4669.56	DVDD	63	6052.68	-7219.80	D0
24	0.00	-4950.54	D27	64	6262.74	-7219.80	H1
25	0.00	-5153.40	IVSS	65	6472.80	-7219.80	H3
26	0.00	-5333.58	D26	66	6646.86	-7219.80	DVDD
27	0.00	-5536.44	D25	67	7136.64	-6714.54	DVSS
28	0.00	-5739.30	D24	68	7136.64	-6555.96	CVSS
29	0.00	-5942.16	D23	69	7136.64	-6402.42	IVSS
30	0.00	-6145.02	D22	70	7136.64	-6241.86	X2
31	0.00	-6347.88	D21	71	7136.64	-6072.30	X1
32	0.00	-6522.48	DVDD	72	7136.64	-5780.16	HOLDA
33	0.00	-6699.46	D20	73	7136.64	-5574.60	HOLD
34	396.72	-7219.80	DVSS	74	7136.64	-5392.62	CVDD
35	577.44	-7219.80	D19	75	7136.64	-5116.14	RDY
36	780.30	-7219.80	D18	76	7136.64	-4898.16	STRB
37	990.36	-7219.80	D17	77	7136.64	-4673.70	RW
38	1200.42	-7219.80	D16	78	7136.64	-4453.74	RESET
39	1410.48	-7219.80	D15	79	7136.64	-4235.76	XF0
40	1598.94	-7219.80	CVSS	80	7136.64	-4032.90	CVDD

FIGURE A-1. Die bonding pad locations and electrical functions

PAD	X CENTER	Y CENTER	PAD NAME	PAD	X CENTER	Y CENTER	PAD NAME
81	7136.64	-3809.52	XF1	107	5248.08	452.52	C0
82	7136.64	-3585.06	IACK	108	5063.40	452.52	C1
83	7136.64	-3365.10	INT0	109	4878.72	452.52	SCANIN
84	7136.64	-3168.72	DVSS	110	4694.04	452.52	INT2
85	7136.64	-2988.54	VSSL	111	4526.46	452.52	CVSS
86	7136.64	-2791.26	INT1	112	4324.68	452.52	A23
87	7136.64	-2590.56	VDDL	113	4129.02	452.52	A22
88	7136.64	-2428.20	VDDL	114	3862.62	452.52	VDDL
89	7136.64	-2232.18	INT2	115	3700.26	452.52	VDDL
90	7136.64	-2018.70	INT3	116	3421.98	452.52	A21
91	7136.64	-1750.32	DR0	117	3226.50	452.52	A20
92	7136.64	-1547.46	CVSS	118	3052.44	452.52	VSSL
93	7136.64	-1345.68	FSR0	119	2901.06	452.52	DVSS
94	7136.64	-1121.22	CLKR0	120	2728.08	452.52	A19
95	7136.64	-896.76	CLKX0	121	2554.02	452.52	AVDD
96	7136.64	-693.90	IVSS	122	2381.04	452.52	A18
97	7136.64	-492.12	FSX0	123	2185.38	452.52	A17
98	7136.64	-289.26	PVDD	124	1989.72	452.52	A16
99	7136.64	-15.48	DX0	125	1794.06	452.52	A15
100	6705.00	452.52	SUBSTRATE	126	1598.40	452.52	A14
101	6480.90	452.52	MCS	127	1316.34	452.52	A13
102	6298.92	452.52	DVSS	128	1120.68	452.52	A12
103	6125.94	452.52	TCLK0	129	925.02	452.52	A11
104	5951.88	452.52	PVDD	130	750.96	452.52	AVDD
105	5721.30	452.52	TCLK1	131	577.98	452.52	A10
106	5439.24	452.52	SCANOUT	132	403.92	452.52	CVSS

Note:

HOLDA, HOLD, RDY, STRB, RW, RESET, IACK, INT0, INT1, INT2, and INT3 are active low.

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-11-19

Approved sources of supply for SMD 5962-92058 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9205801MXA 5962-9205801MYA	3/	SMJ320C31GFAM27 SMJ320C31HFGM27
5962-9205802MXA 5962-9205802MYA 5962-9205802QZC 5962-9205802QUC	3/	SMJ320C31GFAM33 SMJ320C31HFGM33 SMJ320C31TBM33 SMJ320C31TAM33
5962-9205803MXA 5962-9205803MYA 5962-9205803QZC 5962-9205803Q9A	01295	SMJ320C31GFAM40 SMJ320C31HFGM40 SMJ320C31TBM40 SMJ320C31KGDM40B
5962-9205804MXA 5962-9205804MYA	01295	SMJ320C31GFAM50 SMJ320C31HFGM50

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448