FEMTOCLOCK™ CRYSTAL-TO-LVDS/ LVCMOS FREQUENCY SYNTHESIZER

ICS844020-45

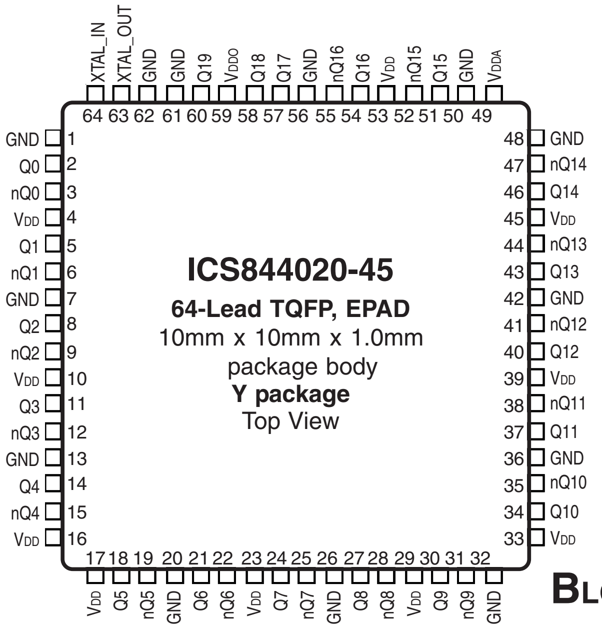
General Description

The ICS844020-45 is a 20 output synthesizer optimized to generate Gigabit and 10 Gigabit Ethernet clocks and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. Using a 25MHz 18pF parallel resonant crystal, the device will generate 156.25, 125MHz, 25MHz and 3.90625MHz clocks with mixed LVDS and LVTTL output logic. The ICS844020-45 uses ICS' 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS844020-45 is packaged in a 64-pin TQFP package with exposed pad for optimum thermal performance.

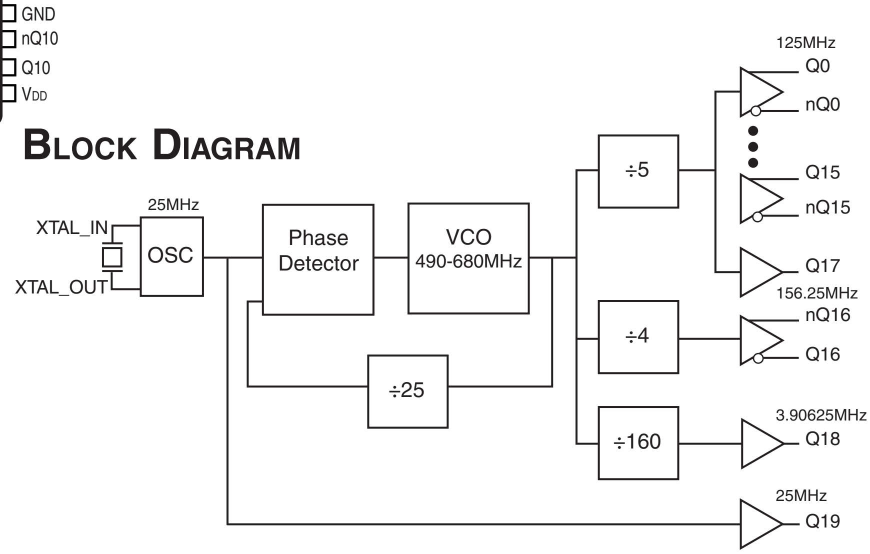
Features

- Sixteen differential LVDS outputs at 125MHz
  One differential LVDS output at 156.25MHz
  One LVCMOS/LVTTL single-ended output at 125MHz
  One LVCMOS/LVTTL single-ended output at 25MHz
  One LVCMOS/LVTTL single-ended output at 3.90625MHz
- Crystal oscillator interface
- VCO range: 490MHz - 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.4ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.37ps (typical)
- Full 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

Pin Assignment



Block Diagram



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7, 13, 20, 26, 32, 36, 42, 48, 50, 56, 61, 62	GND	Power		Power supply ground.
2, 3 5, 6 8, 9 11, 12 14, 15 18, 19 21, 22 24, 25 27, 28 30, 31 34, 35 37, 38 40, 41 43, 44 46, 47 51, 52 54, 55	Q0, nQ0 Q1, nQ1 Q2, nQ2 Q3, nQ3 Q4, nQ4 Q5, nQ5 Q6, nQ6 Q7, nQ7 Q8, nQ8 Q9, nQ9 Q10, nQ10 Q11, nQ11 Q12, nQ12 Q13, nQ13 Q14, nQ14 Q15, nQ15 Q16, nQ16	Output		Differential clock output pair. LVPECL interface levels.
4, 10, 16, 17, 23, 29, 33, 39, 45, 53	V_{DD}	Power		Core power supply pins.
49	V_{DDA}	Power		Analog supply pin.
57, 58, 60	Q17, Q18, Q19	Output		Single-Ended clock outputs. LVCMOS/LVTTL interface levels.
59	V_{DDO}	Power		Output power supply pin for LVCMOS outputs.
63, 64	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance			TBD		pF
R_{OUT}	Output Impedance		5	7	12	Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	22.3°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V ± 5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - I_{DDA}$*10Ω	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V ± 5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1	Q17:Q19	V_{DDO} = 2.625V±5%	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	Q17:Q19	V_{DDO} = 2.625V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, Output Load Test Circuit diagram.

TABLE 3C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%, T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			TBD		mV
ΔV_{OD}	V_{OD} Magnitude Change			TBD		mV
V_{OS}	Offset Voltage			TBD		V
ΔV_{OS}	V_{OS} Magnitude Change			TBD		mV

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

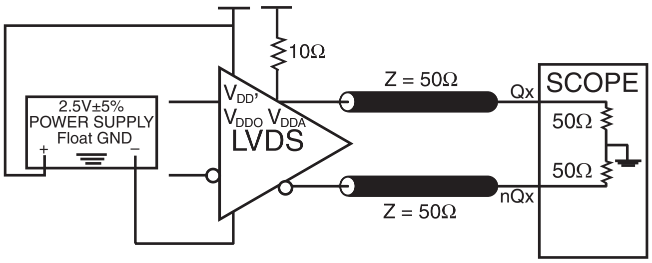
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%, T_A = 0°C$ TO $70°C$

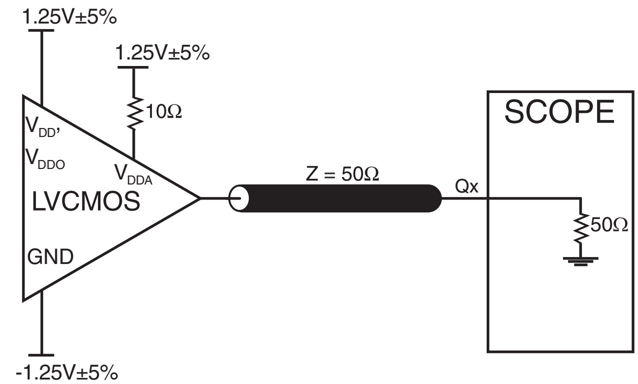
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q0:15/nQ0:15			125		MHz
		Q17			125		MHz
		Q16/nQ16			156.25		MHz
		Q18			3.90625		MHz
		Q19			25		MHz
*t*sk(o)	Output Skew; NOTE 1, 2				TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	Q0:15/nQ0:15	125MHz, (1.875MHz - 20MHz)		0.40		ps
		Q16/nQ16	156.25MHz, (1.875MHz - 20MHz)		0.37		ps
t_R / t_F	Output Rise/Fall Time	Q0:15/nQ0:15	125MHz, 20% to 80%		0.55		ns
		Q16:nQ16	156.25MHz, 20% to 80%		200		ps
odc	Output Duty Cycle	Q0:15/nQ0:15	125MHz	45		55	%
		Q16/nQ16	156.25MHz	40		60	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plots.

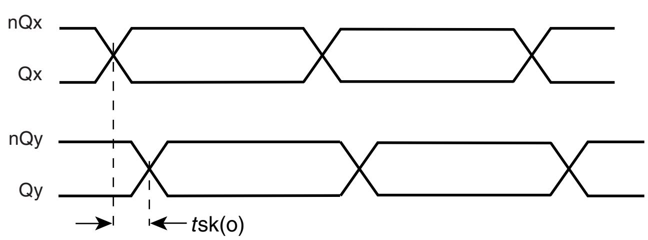
Parameter Measurement Information



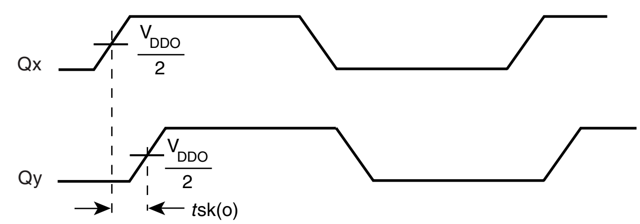
2.5V LVDS Output Load AC Test Circuit



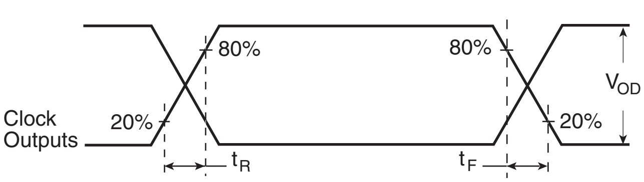
2.5V LVCMOS Output Load AC Test Circuit



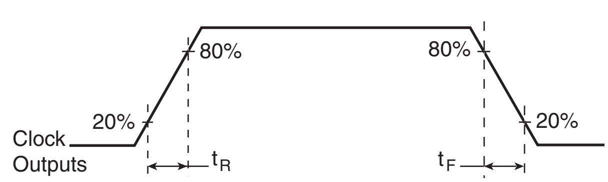
LVDS Output Skew



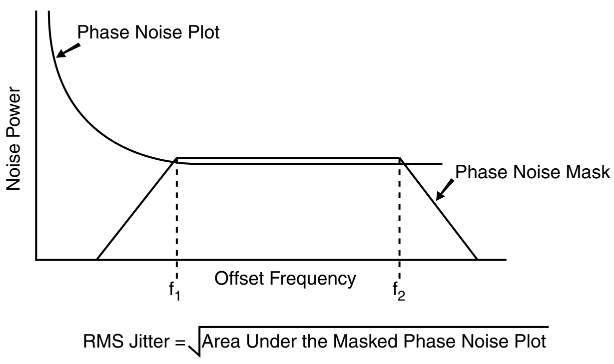
LVCMOS Output Skew



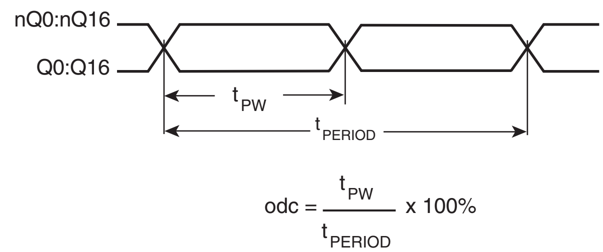
LVDS Output Rise/Fall Time



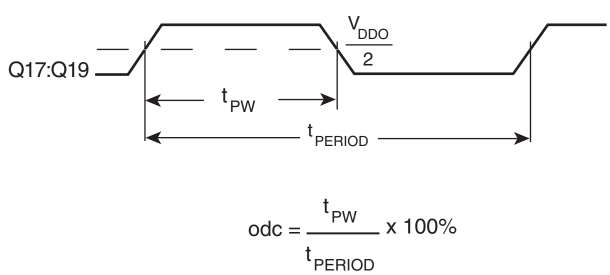
LVCMOS Output Rise/Fall Time



RMS PHASE JITTER

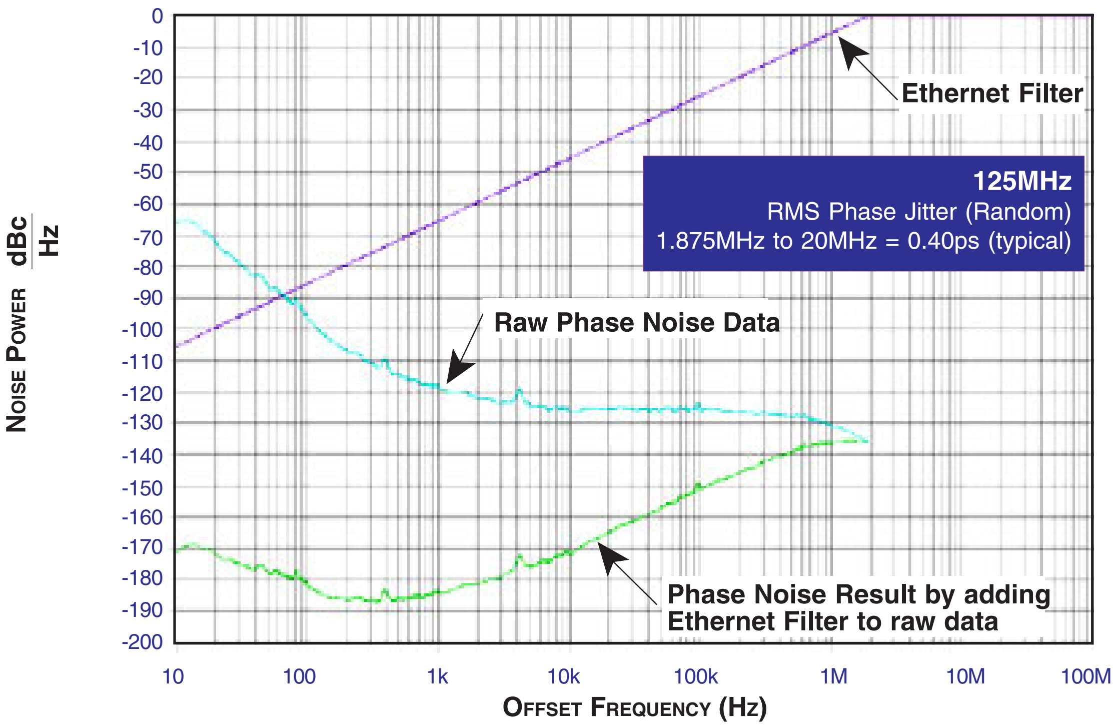


LVDS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

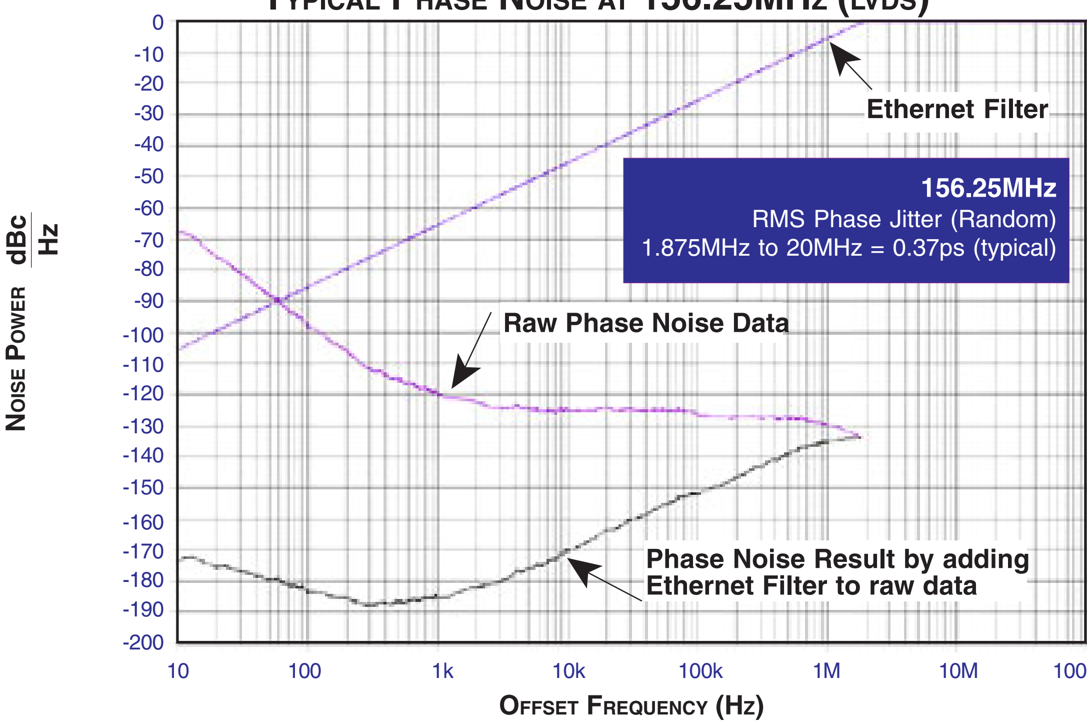


LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

TYPICAL PHASE NOISE AT 125MHZ (LVDS)



TYPICAL PHASE NOISE AT 156.25MHZ (LVDS)



Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844020-45 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

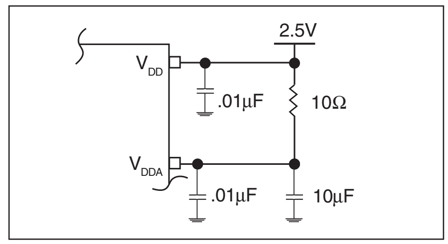


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844020-45 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

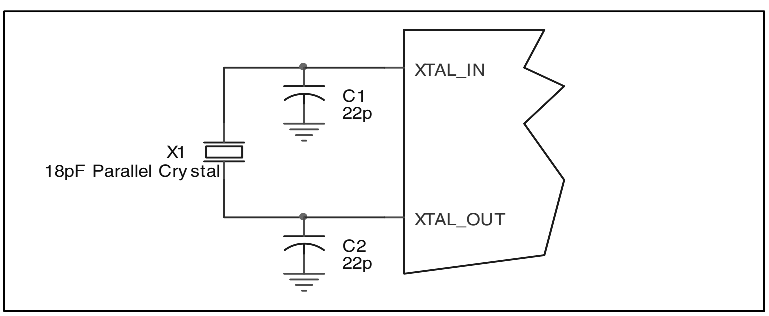


Figure 2. Crystal Input Interface

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

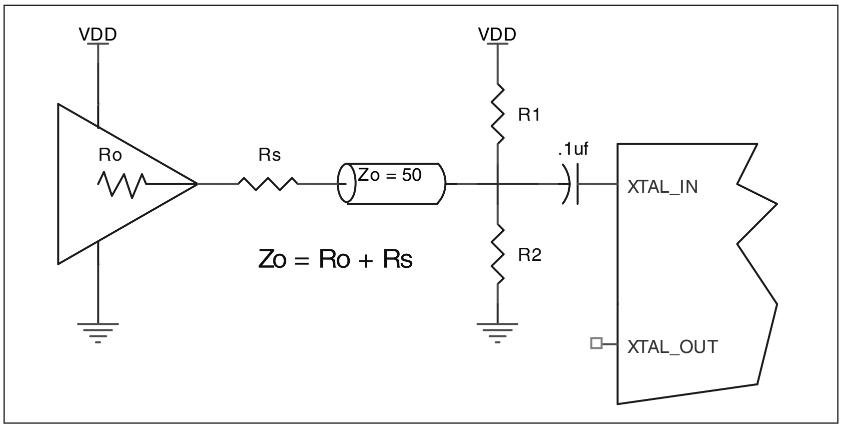


Figure 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. There should be no trace attached.

LVDS OUTPUT
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

2.5V LVDS Driver Termination

Figure 4 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.

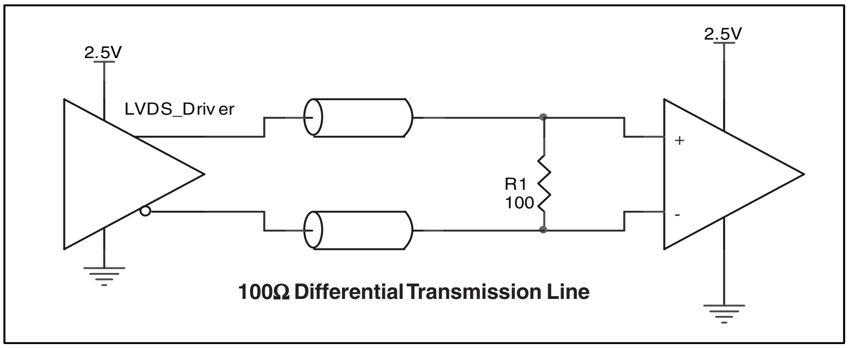


Figure 4. Typical LVDS Driver Termination

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 5.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

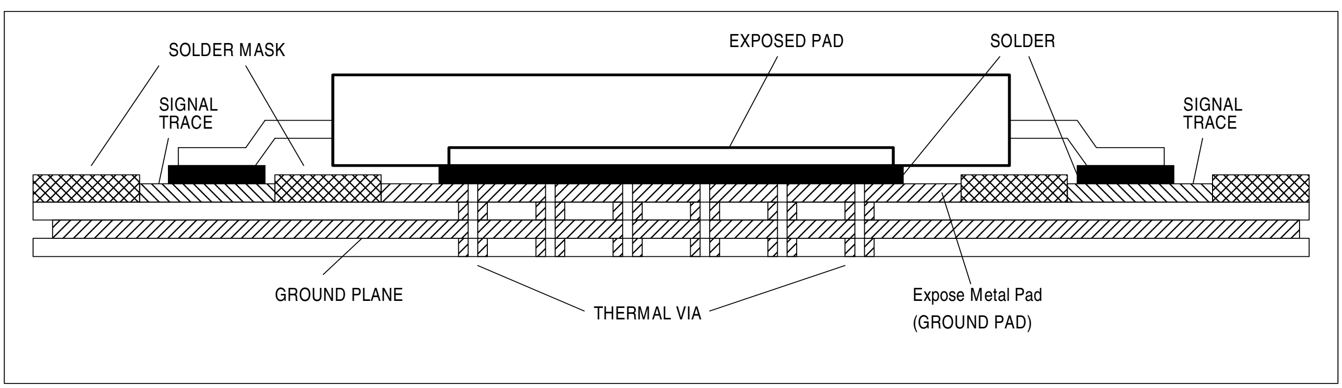


Figure 5. P.C. Board for Exposed Pad Thermal Release Path Example

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 64 Lead TQFP, E-Pad

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	22.3°C/W	17.2°C/W	15.1°C/W

Transistor Count

The transistor count for ICS844020-45 is: 1782

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844020AY-45	ICS844020AY-45	64 Lead TQFP, E-Pad	Tray	0°C to 70°C
ICS844020AY-45T	ICS844020AY-45	64 Lead TQFP, E-Pad	500 Tape & Reel	0°C to 70°C
ICS844020AY-45LF	TBD	64 Lead "Lead-Free" TQFP, E-Pad	Tray	0°C to 70°C
ICS844020AY-45LFT	TBD	64 Lead "Lead-Free" TQFP, E-Pad	500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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