

FEATURES

- Operating frequency from 100 MHz to 4000 MHz
- Digitally controlled VGA with serial and parallel interfaces
- 6-bit, 0.5 dB digital step attenuator
- 31.5 dB gain control range with ± 0.25 dB step accuracy
- Gain block amplifier specifications
 - Gain: 19.7 dB at 2.14 GHz
 - OIP3: 41.0 dBm at 2.14 GHz
 - P1dB: 19.5 dBm at 2.14 GHz
 - Noise figure: 2.9 dB at 2.14 GHz
- Gain block or digital step attenuator can be first
- Single supply operation from 4.75 V to 5.25 V
- Low quiescent current of 93 mA
- Thermally efficient, 5 mm \times 5 mm, 32-lead LFCSP
- The companion [ADL5243](#) integrates a $\frac{1}{4}$ W driver amplifier to the output of the gain block and DSA

APPLICATIONS

- Wireless infrastructure
- Automated test equipment
- RF/IF gain control

GENERAL DESCRIPTION

The [ADL5240](#) is a high performance, digitally controlled variable gain amplifier (VGA) operating from 100 MHz to 4000 MHz. The VGA integrates a high performance, 20 dB gain, internally matched amplifier (AMP) with a 6-bit digital step attenuator (DSA) that has a gain control range of 31.5 dB in 0.5 dB steps with ± 0.25 dB step accuracy. The attenuation of the DSA can be controlled using a serial or parallel interface.

Both the gain block and DSA are internally matched to 50 Ω at their inputs and outputs and are separately biased. The separate bias allows all or part of the [ADL5240](#) to be used, which facilitates easy reuse throughout a design. The pinout of the [ADL5240](#) also enables either the gain block or DSA to be first, giving the VGA maximum flexibility in a signal chain.

The [ADL5240](#) consumes just 93 mA and operates from a single supply ranging from 4.75 V to 5.25 V. The VGA is packaged in a thermally efficient, 5 mm \times 5 mm, 32-lead LFCSP and is fully specified for operation from -40°C to $+85^{\circ}\text{C}$. A fully populated evaluation board is available.

FUNCTIONAL BLOCK DIAGRAM

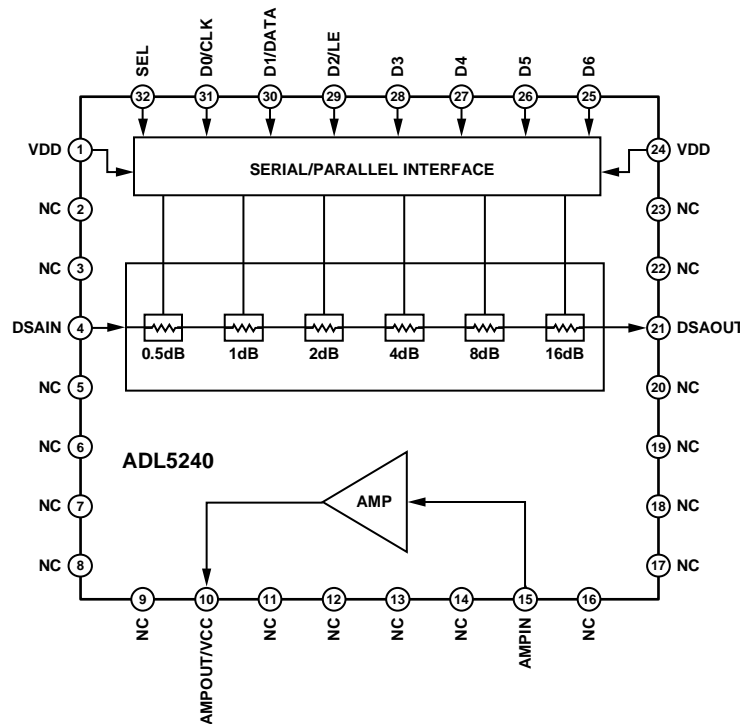


Figure 1.

Rev. 0

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REVISION HISTORY

7/11—Revision 0: Initial Version

SPECIFICATIONS

VDD = 5 V, VCC = 5 V, T_A = 25°C

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		100		4000	MHz
AMPLIFIER FREQUENCY = 150 MHz	Using the AMPIN and AMPOUT pins				
Gain			17.6		dB
vs. Frequency	±50 MHz		±1.0		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.04		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Input Return Loss	S11		−10.4		dB
Output Return Loss	S22		−7.7		dB
Output 1 dB Compression Point			18.3		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		30.0		dBm
Noise Figure			2.8		dB
AMPLIFIER FREQUENCY = 450 MHz	Using the AMPIN and AMPOUT pins				
Gain			20.3		dB
vs. Frequency	±50 MHz		±0.11		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.36		dB
vs. Supply	4.75 V to 5.25 V		±0.01		dB
Input Return Loss	S11		−18.3		dB
Output Return Loss	S22		−15.7		dB
Output 1 dB Compression Point			20.2		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		39.0		dBm
Noise Figure			2.9		dB
AMPLIFIER FREQUENCY = 748 MHz	Using the AMPIN and AMPOUT pins				
Gain			20.6		dB
vs. Frequency	±50 MHz		±0.01		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.31		dB
vs. Supply	4.75 V to 5.25 V		±0.01		dB
Input Return Loss	S11		−25.7		dB
Output Return Loss	S22		−23.7		dB
Output 1 dB Compression Point			20.2		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		40.0		dBm
Noise Figure			2.7		dB
AMPLIFIER FREQUENCY = 943 MHz	Using the AMPIN and AMPOUT pins				
Gain		19.0	20.5	22.0	dB
vs. Frequency	±18 MHz		±0.01		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.27		dB
vs. Supply	4.75 V to 5.25 V		±0.01		dB
Input Return Loss	S11		−30.3		dB
Output Return Loss	S22		−24.8		dB
Output 1 dB Compression Point		18.5	20.1		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		40.0		dBm
Noise Figure			2.7		dB

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AMPLIFIER FREQUENCY = 1960 MHz					
Gain	Using the AMPIN and AMPOUT pins		19.8		dB
vs. Frequency	±30 MHz		±0.03		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.26		dB
vs. Supply	4.75 V to 5.25 V		±0.03		dB
Input Return Loss	S11		−11.9		dB
Output Return Loss	S22		−12.6		dB
Output 1 dB Compression Point			19.8		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		40.0		dBm
Noise Figure			2.9		dB
AMPLIFIER FREQUENCY = 2140 MHz					
Gain	Using the AMPIN and AMPOUT pins	18.0	19.7	22.0	dB
vs. Frequency	±30 MHz		±0.02		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.25		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Input Return Loss	S11		−11.0		dB
Output Return Loss	S22		−12.0		dB
Output 1 dB Compression Point		17.5	19.5		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		41.0		dBm
Noise Figure			2.9		dB
AMPLIFIER FREQUENCY = 2630 MHz					
Gain	Using the AMPIN and AMPOUT pins	18.0	19.6	22.0	dB
vs. Frequency	±60 MHz		±0.01		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.22		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Input Return Loss	S11		−11.0		dB
Output Return Loss	S22		−13.3		dB
Output 1 dB Compression Point		18.0	19.9		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		41.0		dBm
Noise Figure			2.9		dB
AMPLIFIER FREQUENCY = 3600 MHz					
Gain	Using the AMPIN and AMPOUT pins		19.6		dB
vs. Frequency	±100 MHz		±0.03		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.05		dB
vs. Supply	4.75 V to 5.25 V		±0.10		dB
Input Return Loss	S11		−15.1		dB
Output Return Loss	S22		−12.2		dB
Output 1 dB Compression Point			18.8		dBm
Output Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone		37.0		dBm
Noise Figure			3.1		dB
DSA FREQUENCY = 150 MHz					
Insertion Loss	Using the DSAIN and DSAOUT pins		−1.5		dB
vs. Frequency	Minimum attenuation		±0.12		dB
vs. Temperature	±50 MHz		±0.09		dB
Attenuation Range	−40°C ≤ T _A ≤ +85°C		28.8		dB
Attenuation Step Error	All attenuation states		±0.18		dB
Attenuation Absolute Error	All attenuation states		±1.35		dB
Input Return Loss	Minimum attenuation		−13.3		dB
Output Return Loss	Minimum attenuation		−13.4		dB
Input Third-Order Intercept	Δf = 1 MHz, P _{OUT} = 4 dBm/tone, minimum attenuation		45.5		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DSA FREQUENCY = 450 MHz	Using the DSAIN and DSAOUT pins				
Insertion Loss	Minimum attenuation		-1.5		dB
vs. Frequency	± 50 MHz		± 0.02		dB
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 0.10		dB
Attenuation Range			30.7		dB
Attenuation Step Error	All attenuation states		± 0.14		dB
Attenuation Absolute Error	All attenuation states		± 0.42		dB
Input Return Loss	Minimum attenuation		-17.6		dB
Output Return Loss	Minimum attenuation		-17.6		dB
Input Third-Order Intercept	$\Delta f = 1$ MHz, $P_{\text{OUT}} = 4$ dBm/tone, minimum attenuation		41.0		dBm
DSA FREQUENCY = 748 MHz	Using the DSAIN and DSAOUT pins				
Insertion Loss	Minimum attenuation		-1.6		dB
vs. Frequency	± 50 MHz		± 0.02		dB
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 0.11		dB
Attenuation Range			30.9		dB
Attenuation Step Error	All attenuation states		± 0.15		dB
Attenuation Absolute Error	All attenuation states		± 0.32		dB
Input Return Loss	Minimum attenuation		-17.4		dB
Output Return Loss	Minimum attenuation		-17.4		dB
Input Third-Order Intercept	$\Delta f = 1$ MHz, $P_{\text{OUT}} = 4$ dBm/tone, minimum attenuation		40		dBm
DSA FREQUENCY = 943 MHz	Using the DSAIN and DSAOUT pins				
Insertion Loss	Minimum attenuation		-1.6		dB
vs. Frequency	± 18 MHz		± 0.01		dB
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 0.12		dB
Attenuation Range			30.9		dB
Attenuation Step Error	All attenuation states		± 0.13		dB
Attenuation Absolute Error	All attenuation states		± 0.30		dB
Input Return Loss	Minimum attenuation		-16.6		dB
Output Return Loss	Minimum attenuation		-16.5		dB
Input 1 dB Compression Point	Minimum attenuation		30.5		dBm
Input Third-Order Intercept	$\Delta f = 1$ MHz, $P_{\text{OUT}} = 4$ dBm/tone, minimum attenuation		48.5		dBm
DSA FREQUENCY = 1960 MHz	Using the DSAIN and DSAOUT pins				
Insertion Loss	Minimum attenuation		-2.4		dB
vs. Frequency	± 30 MHz		± 0.02		dB
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 0.16		dB
Attenuation Range			31.0		dB
Attenuation Step Error	All attenuation states		± 0.15		dB
Attenuation Absolute Error	All attenuation states		± 0.29		dB
Input Return Loss	Minimum attenuation		-12.0		dB
Output Return Loss	Minimum attenuation		-11.5		dB
Input 1 dB Compression Point	Minimum attenuation		31.5		dBm
Input Third-Order Intercept	$\Delta f = 1$ MHz, $P_{\text{OUT}} = 4$ dBm/tone, minimum attenuation		45.0		dBm
DSA FREQUENCY = 2140 MHz	Using the DSAIN and DSAOUT pins				
Insertion Loss	Minimum attenuation		-2.5		dB
vs. Frequency	± 30 MHz		± 0.02		dB
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 0.17		dB
Attenuation Range			31.0		dB
Attenuation Step Error	All attenuation states		± 0.12		dB
Attenuation Absolute Error	All attenuation states		± 0.26		dB
Input Return Loss	Minimum attenuation		-11.9		dB
Output Return Loss	Minimum attenuation		-11.2		dB
Input 1 dB Compression Point	Minimum attenuation		31.5		dBm
Input Third-Order Intercept	$\Delta f = 1$ MHz, $P_{\text{OUT}} = 4$ dBm/tone, minimum attenuation		44.5		dBm

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DSA FREQUENCY = 2630 MHz					
Insertion Loss	Using the DSAIN and DSAOUT pins				
vs. Frequency	Minimum attenuation ±60 MHz		-2.6		dB
vs. Temperature	-40°C ≤ T _A ≤ +85°C		±0.04		dB
Attenuation Range			±0.19		dB
Attenuation Step Error	All attenuation states		31.2		dB
Attenuation Absolute Error	All attenuation states		±0.16		dB
Input Return Loss	Minimum attenuation		±0.19		dB
Output Return Loss	Minimum attenuation		-13.1		dB
Input 1 dB Compression Point	Minimum attenuation		-12.0		dB
Input Third-Order Intercept	Minimum attenuation		31.5		dBm
	Δf = 1 MHz, P _{OUT} = 4 dBm/tone, minimum attenuation		43.0		dBm
DSA FREQUENCY = 3600 MHz					
Insertion Loss	Using the DSAIN and DSAOUT pins				
vs. Frequency	Minimum attenuation ±100 MHz		-2.8		dB
vs. Temperature	-40°C ≤ T _A ≤ +85°C		±0.03		dB
Attenuation Range			±0.21		dB
Attenuation Step Error	All attenuation states		32.1		dB
Attenuation Absolute Error	All attenuation states		±0.37		dB
Input Return Loss	Minimum attenuation		±0.31		dB
Output Return Loss	Minimum attenuation		-20.2		dB
Input 1 dB Compression Point	Minimum attenuation		-18.2		dB
Input Third-Order Intercept	Minimum attenuation		31.0		dBm
	Δf = 1 MHz, P _{OUT} = 4 dBm/tone, minimum attenuation		43.0		dBm
DIGITAL STEP ATTENUATOR GAIN SETTling					
Minimum Attenuation to Maximum Attenuation			36		ns
Maximum Attenuation to Minimum Attenuation			36		ns
AMP-DSA LOOP FREQUENCY = 943 MHz					
Gain	Using the AMPIN and DSAOUT pins, DSA at minimum attenuation				
vs. Frequency	±18 MHz		18.9		dB
Gain Range	Between maximum and minimum attenuation states		±0.01		dB
Input Return Loss	S11		30.8		dB
Output Return Loss	S22		-20.5		dB
Output 1 dB Compression Point			-19.7		dB
Output Third-Order Intercept			18.6		dBm
Noise Figure	Δf = 1 MHz, P _{OUT} = 1 dBm/tone		36.0		dBm
			2.7		dB
AMP-DSA LOOP FREQUENCY = 2140 MHz					
Gain	Using the AMPIN and DSAOUT pins, DSA at minimum attenuation				
vs. Frequency	±30 MHz		18.2		dB
Gain Range	Between maximum and minimum attenuation states		±0.01		dB
Input Return Loss	S11		31.3		dB
Output Return Loss	S22		-14.9		dB
Output 1 dB Compression Point			-16.4		dB
Output Third-Order Intercept			17.9		dBm
Noise Figure	Δf = 1 MHz, P _{OUT} = 1 dBm/tone		37.5		dBm
			3.0		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AMP-DSA LOOP FREQUENCY = 2630 MHz	Using the AMPIN and DSAOUT pins, DSA at minimum attenuation				
Gain			17.7		dB
vs. Frequency	±60 MHz		±0.11		dB
Gain Range			31.5		dB
Input Return Loss	S11		-15.2		dB
Output Return Loss	S22		-9.6		dB
Output 1 dB Compression Point			16.9		dBm
Output Third-Order Intercept	$\Delta f = 1 \text{ MHz}, P_{\text{OUT}} = 1 \text{ dBm/tone}$		33.7		dBm
Noise Figure			3.0		dB
DSA-AMP LOOP FREQUENCY = 943 MHz	Using the DSAIN and AMPOUT pins, DSA at minimum attenuation				
Gain			18.9		dB
vs. Frequency	±18 MHz		±0.01		dB
Gain Range	Between maximum and minimum attenuation states		30.8		dB
Input Return Loss	S11		-17.2		dB
Output Return Loss	S22		-23.7		dB
Output 1 dB Compression Point			20.2		dBm
Output Third-Order Intercept	$\Delta f = 1 \text{ MHz}, P_{\text{OUT}} = 4 \text{ dBm/tone}$		40.0		dBm
Noise Figure			4.4		dB
DSA-AMP LOOP Frequency = 2140 MHz	Using the DSAIN and AMPOUT pins, DSA at minimum attenuation				
Gain			18.0		dB
vs. Frequency	±30 MHz		±0.01		dB
Gain Range	Between maximum and minimum attenuation states		31.1		dB
Input Return Loss	S11		-13.7		dB
Output Return Loss	S22		-10.0		dB
Output 1 dB Compression Point			19.7		dBm
Output Third-Order Intercept	$\Delta f = 1 \text{ MHz}, P_{\text{OUT}} = 4 \text{ dBm/tone}$		37.5		dBm
Noise Figure			4.9		dB
DSA-AMP LOOP Frequency = 2630 MHz	Using the DSAIN and AMPOUT pins, DSA at minimum attenuation				
Gain			18.2		dB
vs. Frequency	±60 MHz		±0.01		dB
Gain Range	Between maximum and minimum attenuation states		31.7		dB
Input Return Loss	S11		-15.7		dB
Output Return Loss	S22		-16.9		dB
Output 1 dB Compression Point			19.8		dBm
Output Third-Order Intercept	$\Delta f = 1 \text{ MHz}, P_{\text{OUT}} = 4 \text{ dBm/tone}$		40.8		dBm
Noise Figure			5.2		dB
POWER SUPPLIES	Using the VDD and VCC pins				
Voltage		4.75	5.0	5.25	V
Supply Current					
Amplifier			93	120	mA
Digital Step Attenuator			0.5		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VDD, VCC)	6.5 V
Input Power	
AMPIN	16 dBm
DSAIN	30 dBm
Internal Power Dissipation	0.5 W
θ_{JA} (Exposed Pad Soldered Down)	36.8°C/W
θ_{JC} (Exposed Pad is the Contact)	6.9°C/W
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 60 sec)	240°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

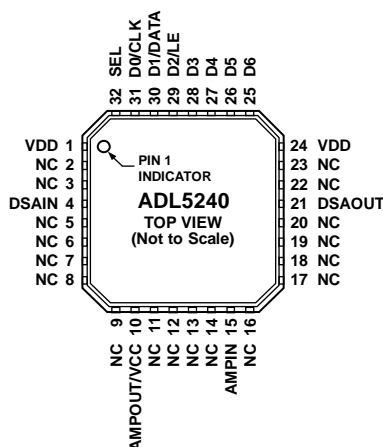
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
 2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

09H30-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 24	VDD	Supply Voltage for DSA. Connect this pin to a 5 V supply.
2, 3, 5, 6, 7, 8, 9, 11, 12, 13, 14, 16, 17, 18, 19, 20, 22, 23	NC	No Connect. Do not connect to this pin.
4	DSAIN	RF Input to DSA.
10	AMPOUT/VCC	RF Output from Amplifier/Supply Voltage for Amplifier. A bias to the amplifier is provided through a choke inductor connected to this pin.
15	AMPIN	RF Input to Amplifier.
21	DSAOUT	RF Output from DSA.
25	D6	Data Bit in Parallel Mode (LSB). Connect this pin to the supply in serial mode.
26	D5	Data Bit in Parallel Mode. Connect this pin to ground in serial mode.
27	D4	Data Bit in Parallel Mode. Connect this pin to ground in serial mode.
28	D3	Data Bit in Parallel Mode. Connect this pin to ground in serial mode.
29	D2/LE	Data Bit in Parallel Mode/Latch Enable in Serial Mode.
30	D1/DATA	Data Bit in Parallel Mode (MSB)/Data in Serial Mode.
31	D0/CLK	Connect this pin to ground in parallel mode. This pin functions as a clock in serial mode.
32	SEL	Select Pin. Connect this pin to the supply to select parallel mode operation; connect this pin to ground to select serial mode operation.
	EPAD	Exposed Pad. The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

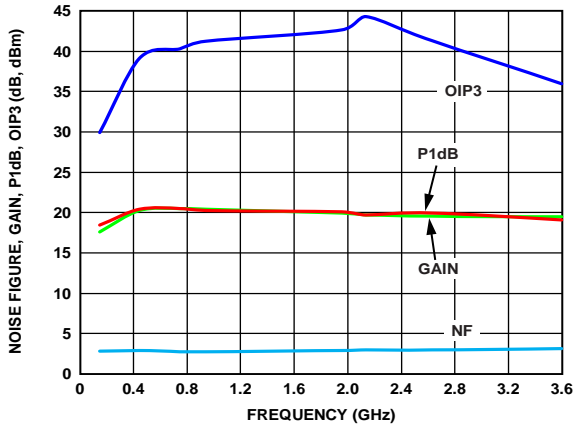


Figure 3. AMP: Gain, P1dB, OIP3 at $P_{OUT} = 4$ dBm/Tone and Noise Figure vs. Frequency

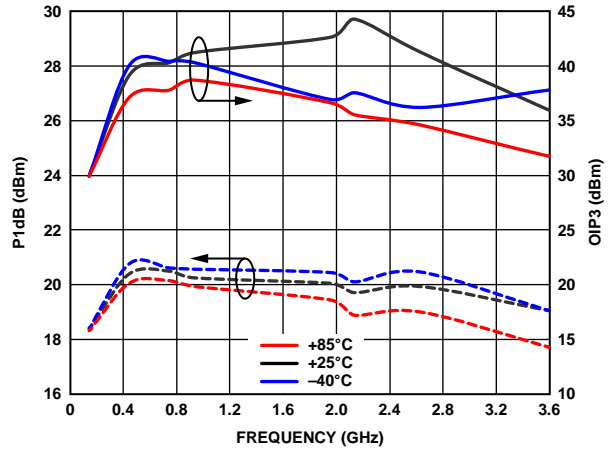


Figure 6. AMP: OIP3 at $P_{OUT} = 4$ dBm/Tone and P1dB vs. Frequency and Temperature

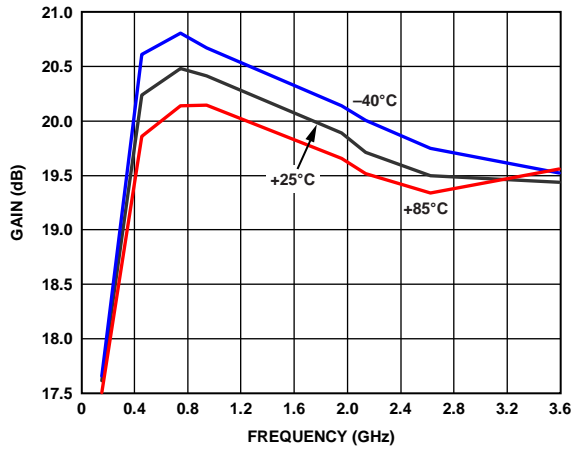


Figure 4. AMP: Gain vs. Frequency and Temperature

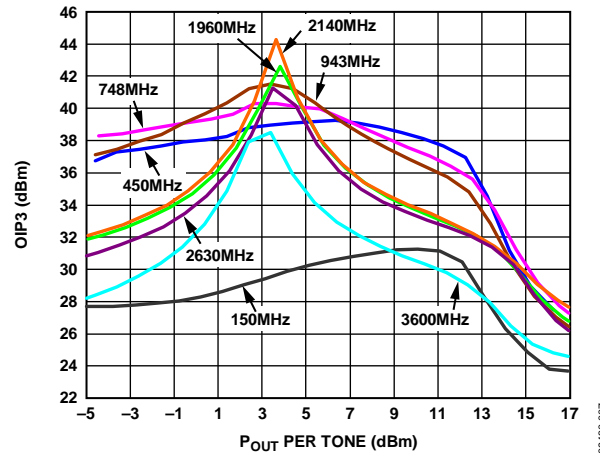


Figure 7. AMP: OIP3 vs. P_{OUT} and Frequency

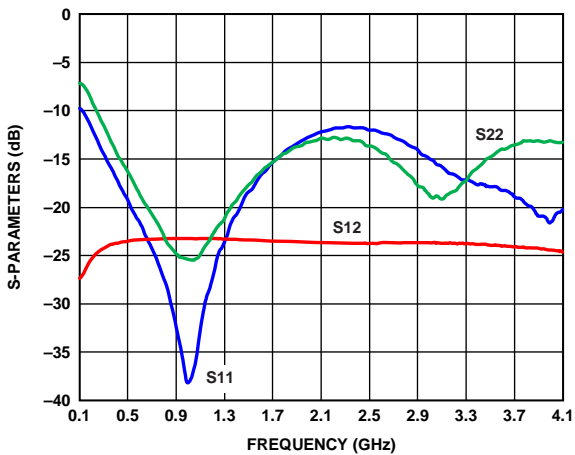


Figure 5. AMP: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

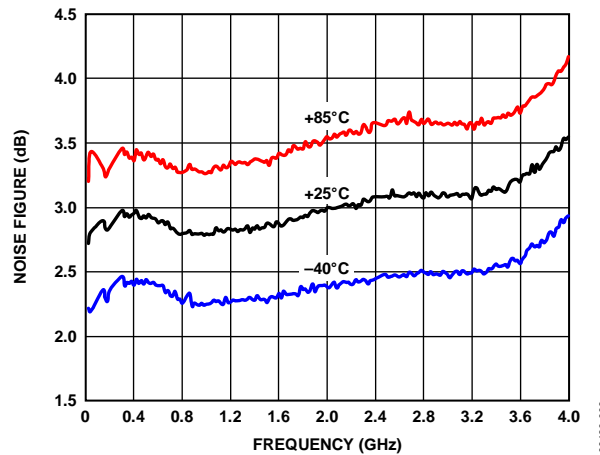


Figure 8. AMP: Noise Figure vs. Frequency and Temperature

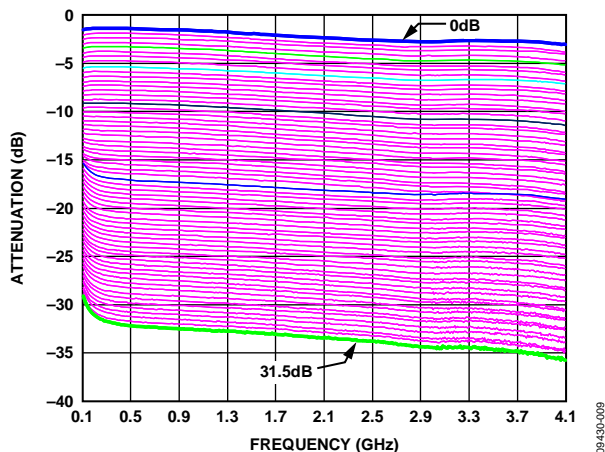


Figure 9. DSA: Attenuation vs. Frequency

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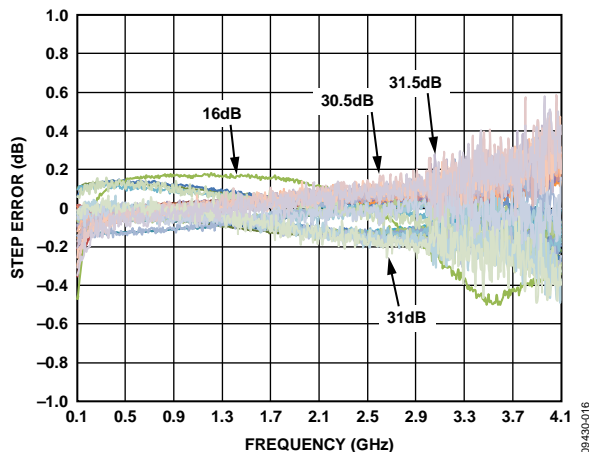


Figure 12. DSA: Step Error vs. Frequency, All Attenuation States

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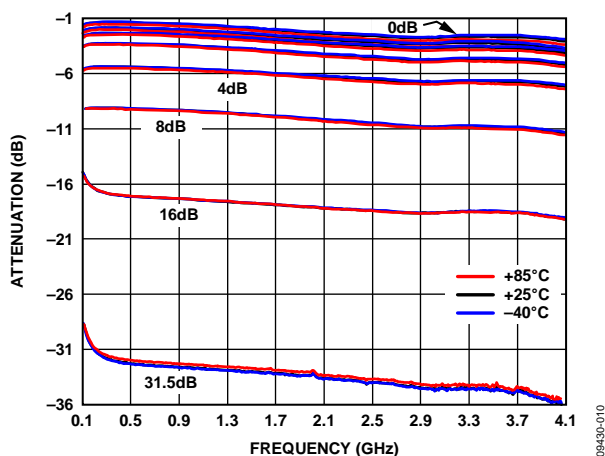


Figure 10. DSA: Attenuation vs. Frequency and Temperature

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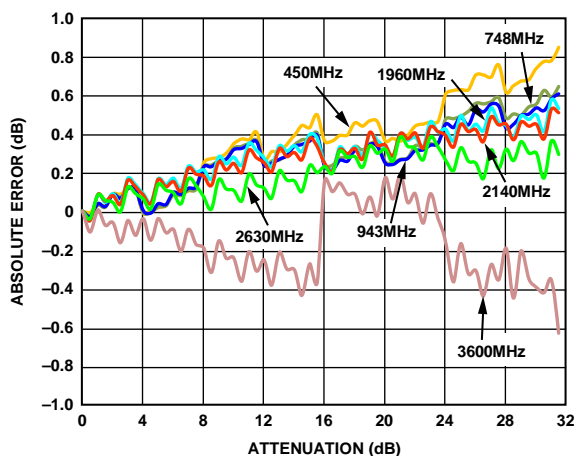


Figure 13. DSA: Absolute Error vs. Attenuation

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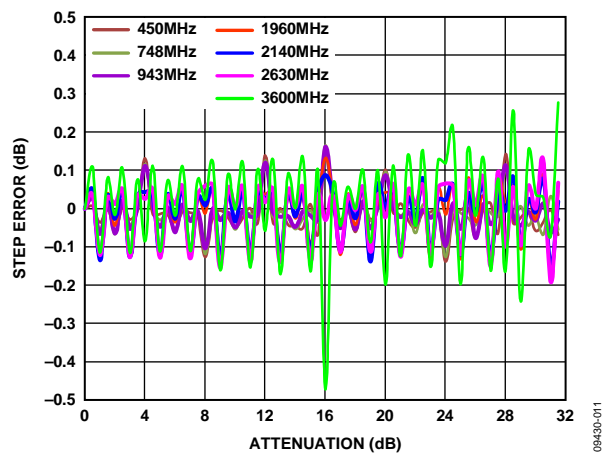


Figure 11. DSA: Step Error vs. Attenuation

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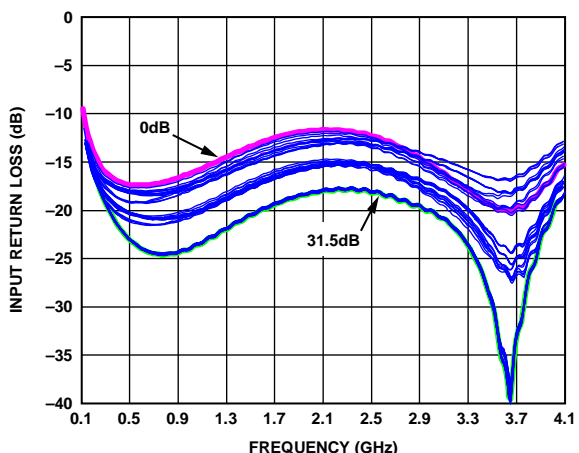


Figure 14. DSA: Input Return Loss vs. Frequency, All States

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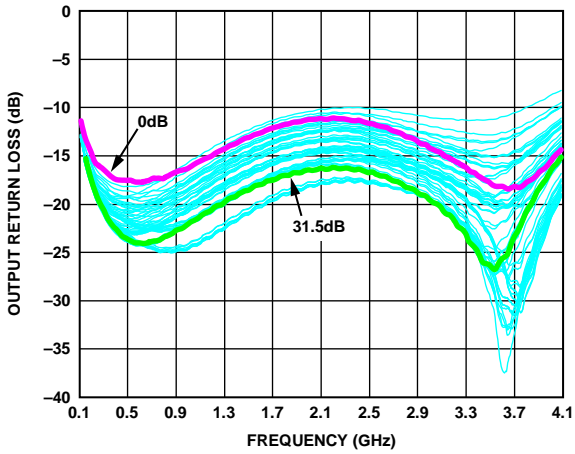


Figure 15. DSA: Output Return Loss vs. Frequency, All States

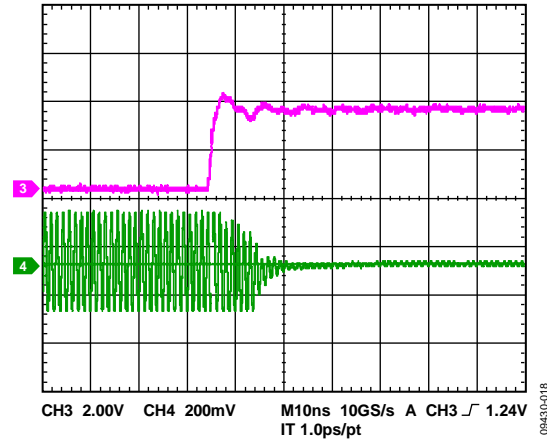


Figure 18. DSA: Gain Settling Time, 0 dB to 31.5 dB

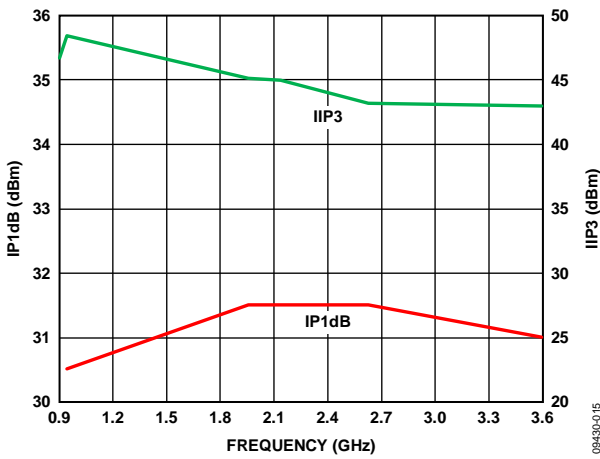


Figure 16. DSA: Input P1dB and Input IP3 vs. Frequency, Minimum Attenuation State

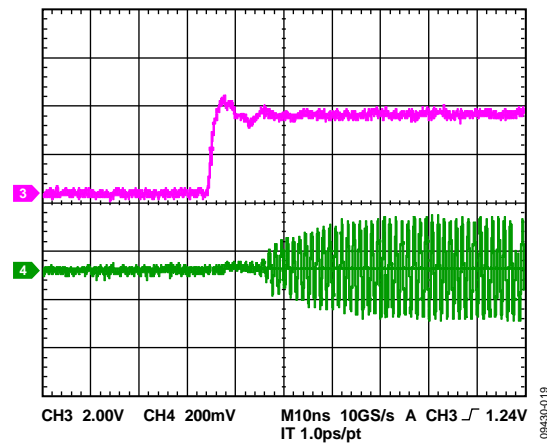


Figure 19. DSA: Gain Settling Time, 31.5 dB to 0 dB

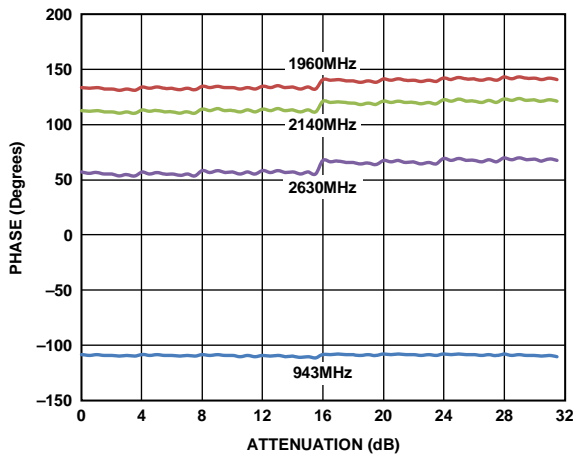


Figure 17. DSA: Phase vs. Attenuation

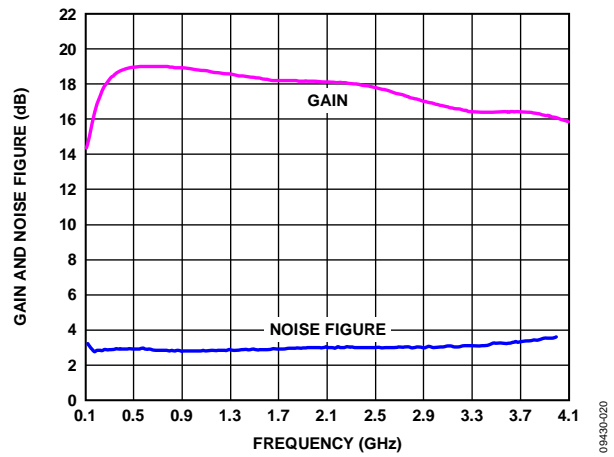


Figure 20. AMP-DSA Loop: Gain and Noise Figure vs. Frequency, Minimum Attenuation State

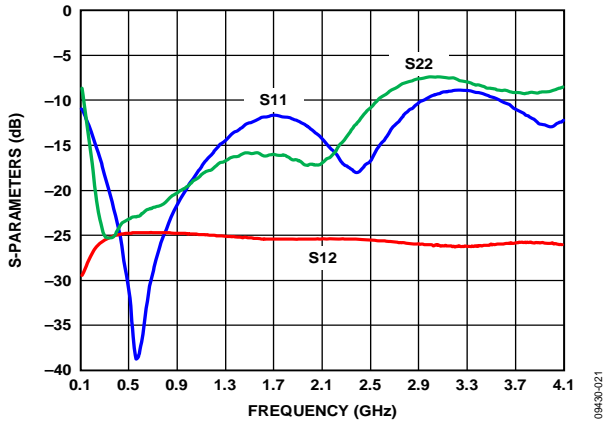


Figure 21. AMP-DSA Loop: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, Minimum Attenuation State

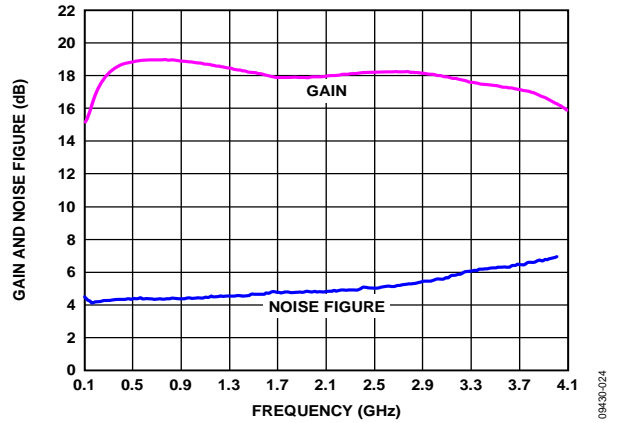


Figure 24. DSA-AMP Loop: Gain and Noise Figure vs. Frequency, Minimum Attenuation State

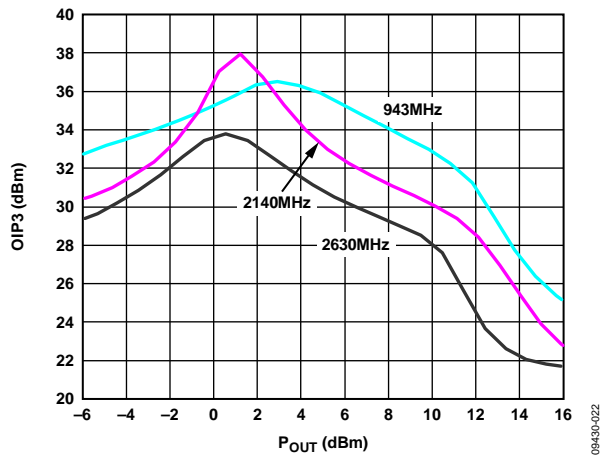


Figure 22. AMP-DSA Loop: OIP3 vs. P_{OUT} and Frequency, Minimum Attenuation State

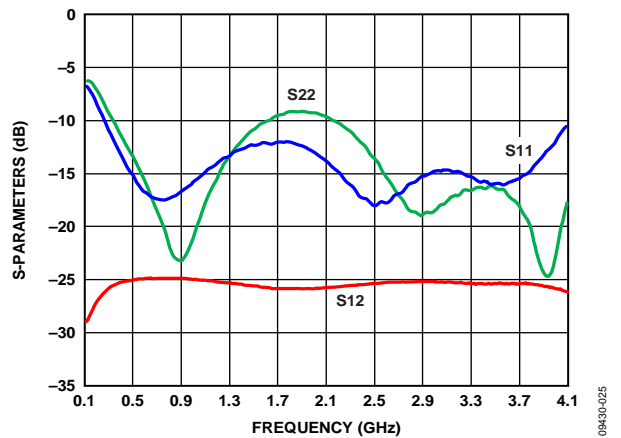


Figure 25. DSA-AMP Loop: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, Minimum Attenuation State

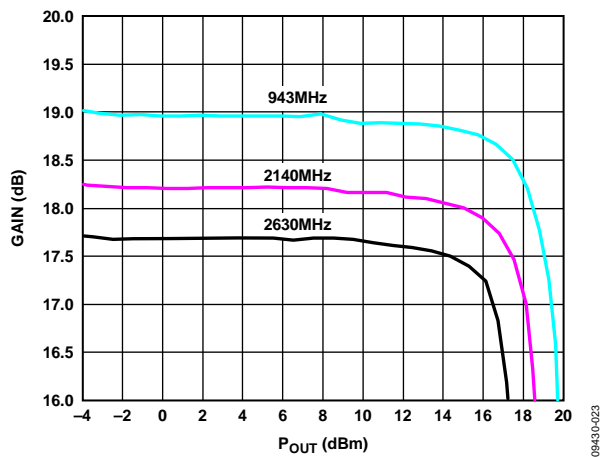


Figure 23. AMP-DSA Loop: Gain vs. P_{OUT} and Frequency, Minimum Attenuation State

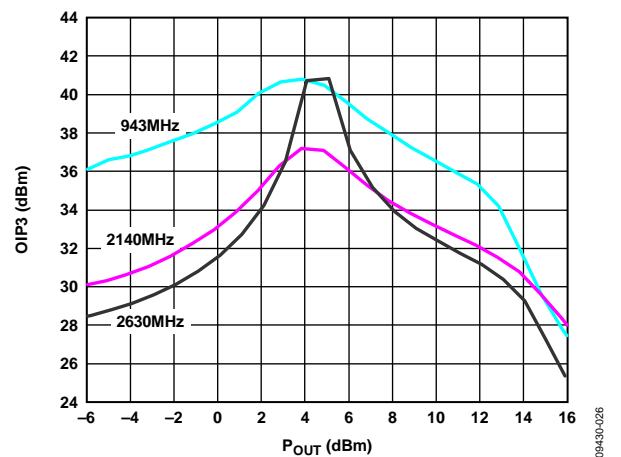


Figure 26. DSA-AMP Loop: OIP3 vs. P_{OUT} and Frequency, Minimum Attenuation State

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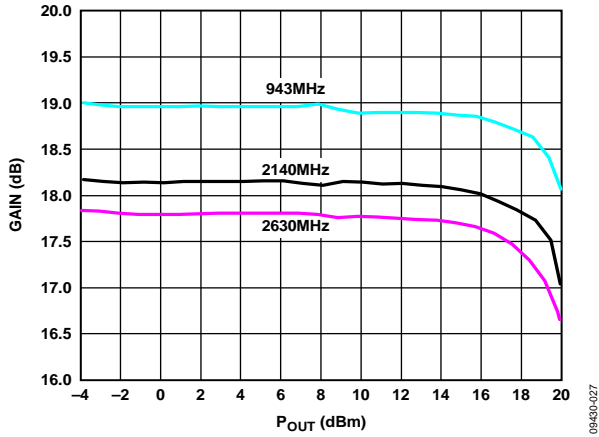


Figure 27. DSA-AMP Loop: Gain vs. P_{OUT} and Frequency, Minimum Attenuation State

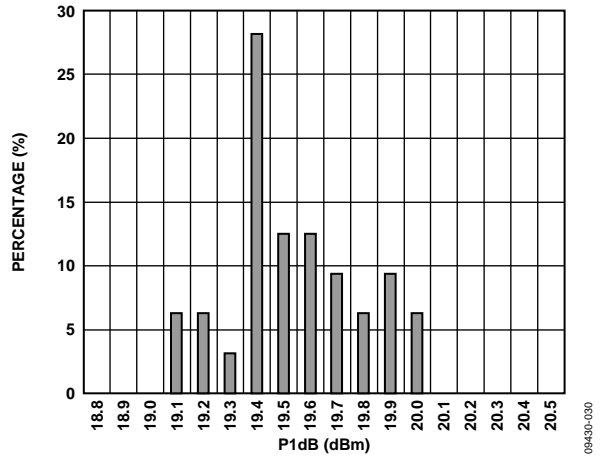


Figure 30. AMP: P1dB Distribution at 2140 MHz

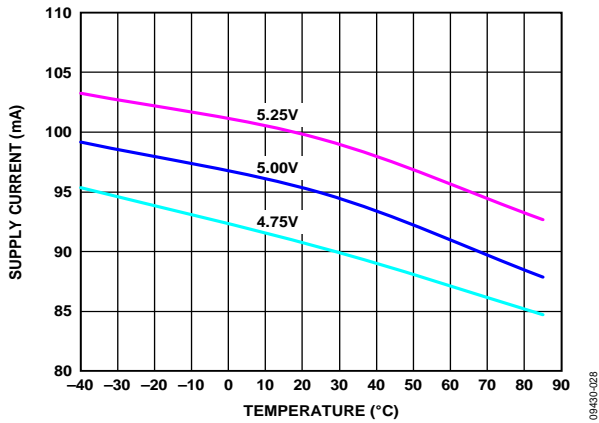


Figure 28. AMP: Supply Current vs. Voltage and Temperature

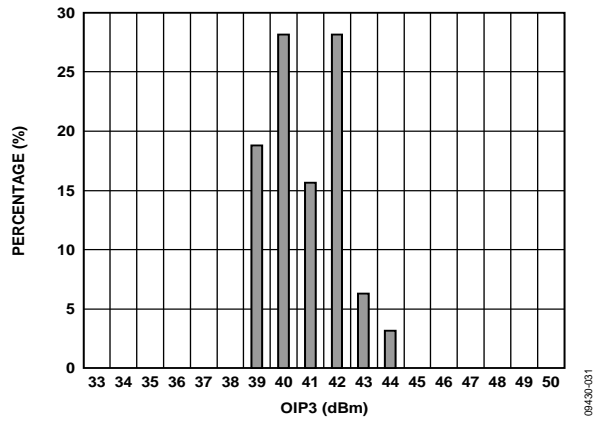


Figure 31. AMP: OIP3 Distribution at 2140 MHz

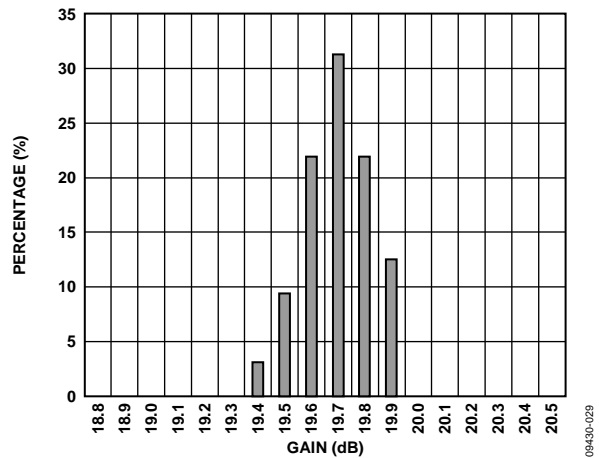


Figure 29. AMP: Gain Distribution at 2140 MHz

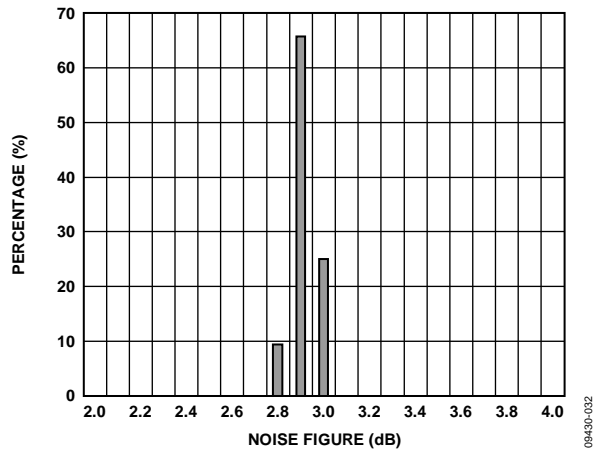


Figure 32. AMP: Noise Figure Distribution at 2140 MHz

APPLICATIONS INFORMATION

BASIC LAYOUT CONNECTIONS

The basic connections for operating the [ADL5240](#) are shown in Figure 33.

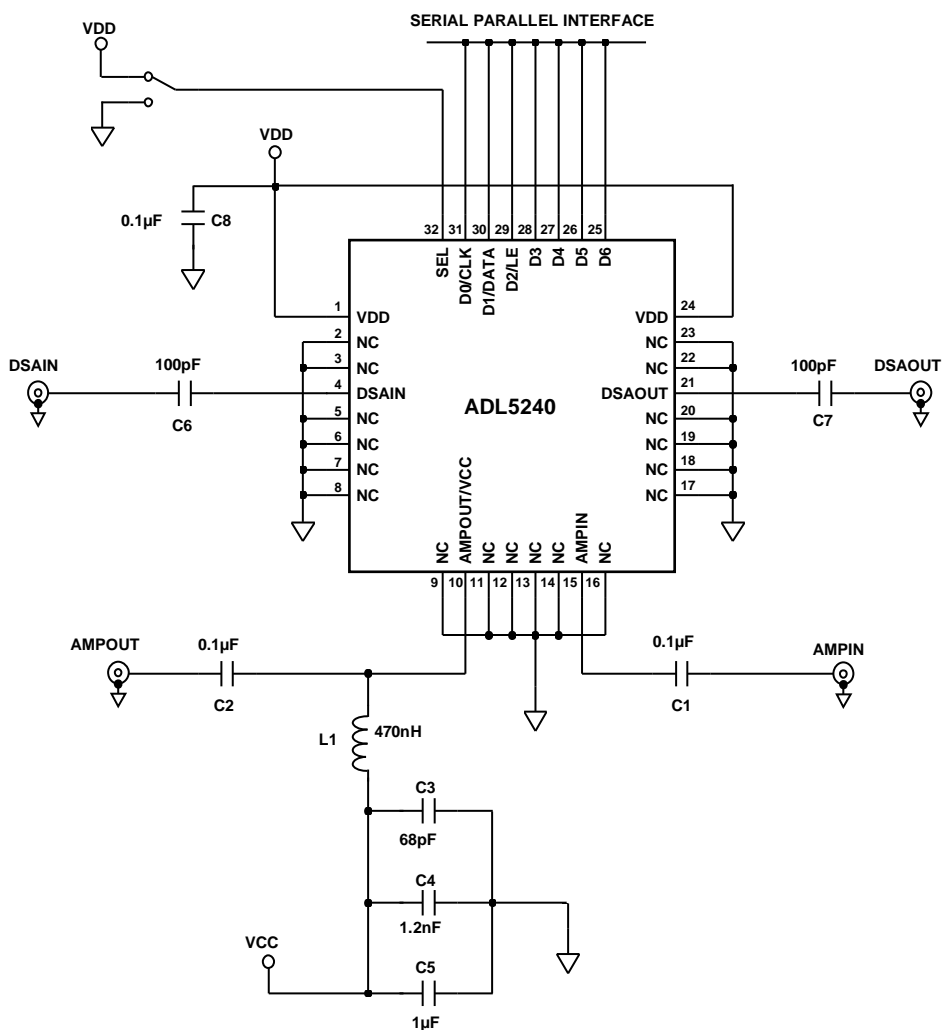


Figure 33. Basic Connections

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Amplifier Bias

The dc bias for the amplifier in [ADL5240](#) is supplied through Inductor L1 and is connected to the AMPOUT pin. Three decoupling capacitors (C3, C4, and C5) are used to prevent RF signals from propagating onto the dc lines. The dc supply ranges from 4.75 V to 5.25 V and should be connected to the VCC test point on the evaluation board.

Digital Step Attenuator Bias

The bias for the DSA is provided through the VDD pin. At least one decoupling capacitor (C8) is recommended on the VDD trace. The voltage ranges from 4.75 V to 5.25 V and should be connected to the VDD test point on the evaluation board. The DSA is shown to work for dc voltages as low as 2.5 V.

Amplifier RF Input Interface

Pin 15 is the RF input for the amplifier of [ADL5240](#). The amplifier is internally matched to 50 Ω at the input; therefore, no external components are required. Only a dc blocking capacitor (C1) is required.

Amplifier RF Output Interface

Pin 10 is the RF output for the amplifier of [ADL5240](#). The amplifier is internally matched to 50 Ω at the output; therefore, no external components are required. Only a dc blocking capacitor (C2) is required. The bias is provided through this pin via a choke inductor.

DSA RF Input Interface

Pin 4 is the RF input for the DSA of [ADL5240](#). The input impedance of the DSA is close to 50 Ω over the entire frequency range; therefore, no external components are required. Only a dc blocking capacitor (C6) is required.

DSA RF Output Interface

Pin 21 is the RF output for the DSA of [ADL5240](#). The output impedance of the DSA is close to 50 Ω over the entire frequency range; therefore, no external components are required. Only a dc blocking capacitor (C7) is required.

DSA SPI Interface

The DSA of the [ADL5240](#) can operate in either serial or parallel mode. Pin 32 (SEL) controls the mode of operation. To select serial mode, connect SEL to ground; to select parallel mode, connect SEL to VDD. In parallel mode, Pin 25 to Pin 30 (D6 to D1) are the data bits, with D6 being the LSB. Connect Pin 31 (D0) to ground during the parallel mode of operation. In serial mode, Pin 29 is the latch enable (LE), Pin 30 is the data (DATA), and Pin 31 is the clock (CLK). Pin 26, Pin 27, and Pin 28 are not used in serial mode and should be connected to ground. Pin 25 (D6) should be connected to VDD during the serial mode of operation. To prevent noise from coupling onto the digital signals, an RC filter can be used on each data line.

SPI TIMING

Table 5 provides details about the timing characteristics for the SPI signals—namely, the clock (CLK), latch enable (LE), and data (DATA) signals—and Figure 34 shows the corresponding SPI timing diagram.

SPI Timing Sequence

Figure 35 is the timing sequence for the SPI function using a 6-bit operation. The clock can be as fast as 20 MHz. In serial mode, Register B5 (MSB) is first and Register B0 (LSB) is last.

Table 4. Mode Selection Table

Pin 32 (SEL)	Functionality
Connect to Ground	Serial mode
Connect to Supply	Parallel mode

Table 5. SPI Timing Setup

Parameter	Limit	Unit	Test Conditions/Comments
f_{CLK}	10	MHz	Data clock frequency
t_1	30	ns min	Clock high time
t_2	30	ns min	Clock low time
t_3	10	ns min	Data to clock setup time
t_4	10	ns min	Clock to data hold time
t_5	10	ns min	Clock low to LE setup time
t_6	30	ns min	LE pulse width

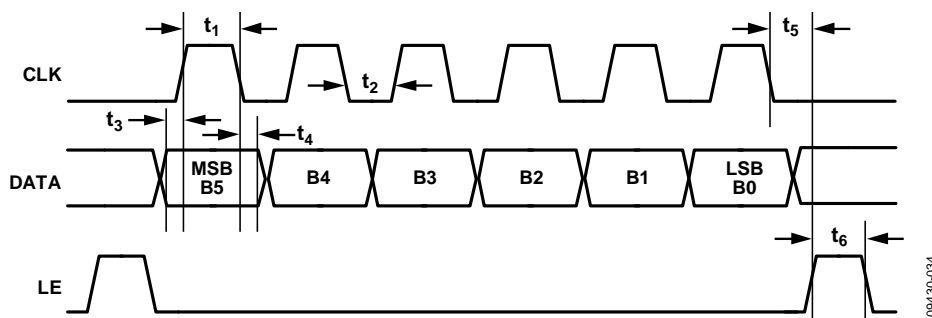


Figure 34. SPI Timing Diagram (Data Is Loaded MSB First), Serial Mode

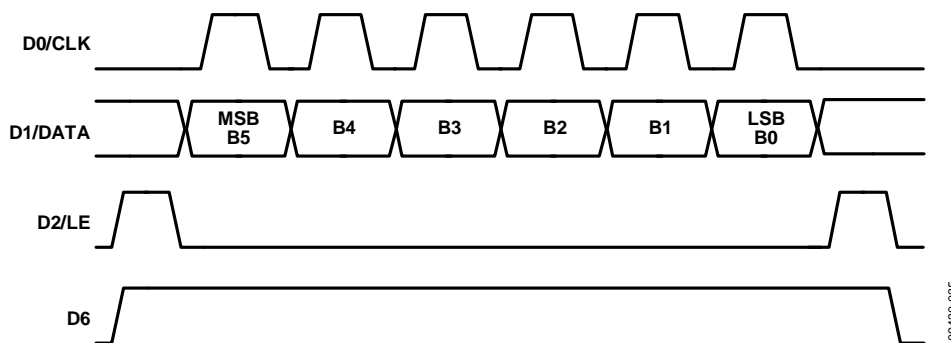


Figure 35. SPI Timing Sequence, Serial Mode

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Table 6. DSA Attenuation Truth Table—Serial Mode

Attenuation State (dB)	B5 (MSB)	B4	B3	B2	B1	B0 (LSB)
0 (Reference)	1	1	1	1	1	1
0.5	1	1	1	1	1	0
1.0	1	1	1	1	0	1
2.0	1	1	1	0	1	1
4.0	1	1	0	1	1	1
8.0	1	0	1	1	1	1
16.0	0	1	1	1	1	1
31.5	0	0	0	0	0	0

Table 7. DSA Attenuation Truth Table—Parallel Mode

Attenuation State (dB)	D1 (MSB)	D2	D3	D4	D5	D6 (LSB)
0 (Reference)	1	1	1	1	1	1
0.5	1	1	1	1	1	0
1.0	1	1	1	1	0	1
2.0	1	1	1	0	1	1
4.0	1	1	0	1	1	1
8.0	1	0	1	1	1	1
16.0	0	1	1	1	1	1
31.5	0	0	0	0	0	0

LOOP PERFORMANCE

The ADL5240 can be configured so that either the DSA precedes the amplifier (see Figure 36) or the amplifier precedes the DSA (see Figure 37). The performance of the loop configurations is presented in Figure 20 to Figure 27. To improve the overall return loss, a shunt capacitor can be placed between the amplifier and DSA. This helps to align the phases of the two blocks.

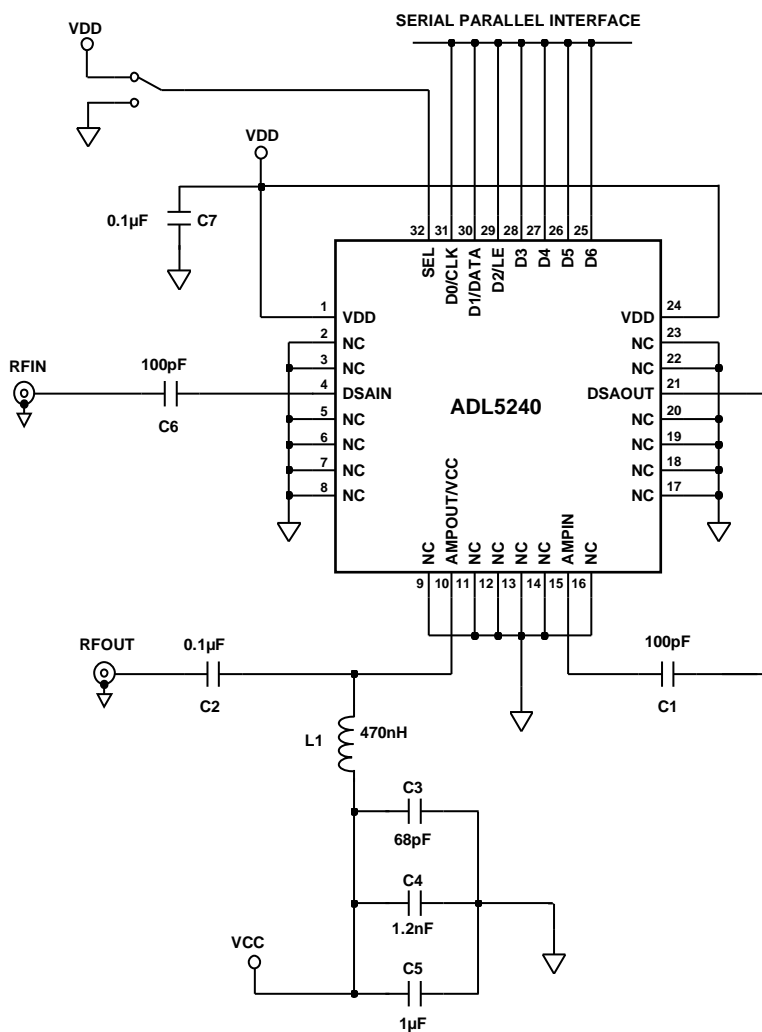


Figure 36. DSA-AMP Loop Configuration

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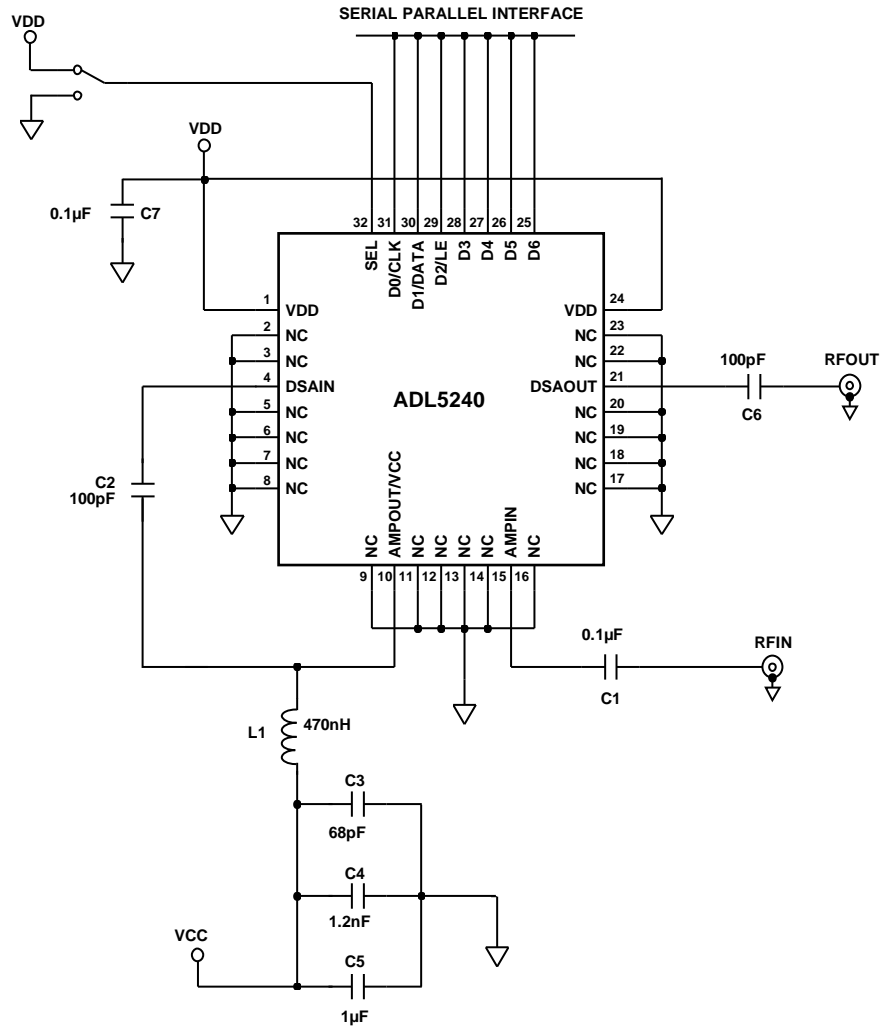


Figure 37. AMP-DSA Loop Configuration

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THERMAL CONSIDERATIONS

The ADL5240 is packaged in a thermally efficient, 5 mm × 5 mm, 32-lead LFCSP. The thermal resistance from junction to air (θ_{JA}) is 36.8°C/W. The thermal resistance for the product was extracted assuming a standard 4-layer JEDEC board with 25 conductive, epoxy filled thermal vias. The thermal resistance from junction to case (θ_{JC}) is 6.9°C/W, where case is the exposed pad of the lead frame package.

The ADL5240 consumes approximately 93 mA with a 5 V supply voltage. Even though the part dissipates less than 0.5 W, for the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LFCSP. The thermal resistance values given in this section assume a minimum of 25 thermal vias arranged in a 5 × 5 array with a diameter of 13 mils and a pitch of 25 mils. Figure 38 shows a close-up of the thermal via distribution under the exposed pad.

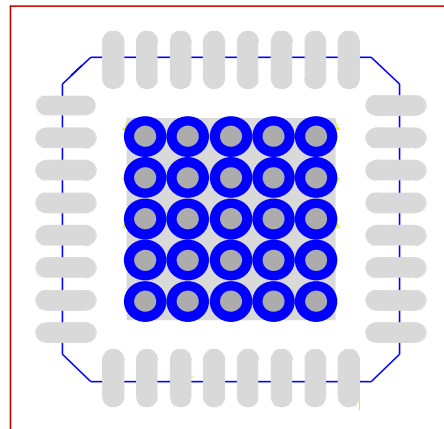


Figure 38. Exposed Pad with Thermal Via Distribution

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EVALUATION BOARD

The schematic of the [ADL5240](#) evaluation board is shown in Figure 39, the evaluation board configuration options are detailed in Table 8, and the layout of the [ADL5240](#) evaluation board is shown in Figure 40 and Figure 41. Each RF trace on the evaluation board has a characteristic impedance of $50\ \Omega$ and is fabricated on Rogers3003 material. In addition, each trace is a coplanar waveguide (CPWG) with a width of 25 mils, a spacing of 20 mils, and a dielectric thickness of 10 mils. The input to and output from the DSA and amplifier should be ac-coupled with capacitors of appropriate values to ensure the broadband performance.

The bias to the amplifier is provided by connecting a choke to the AMPOUT pin. Bypassing capacitors are recommended on all supply lines to minimize the RF coupling. The DSA and the amplifier can be individually biased or connected to the VDD plane using Resistors R2 and R1.

The [ADL5240](#) can be operated in two ways: the amplifier can precede the DSA (AMP-DSA loop configuration) or the DSA can precede the amplifier (DSA-AMP loop configuration). The evaluation board can be configured to handle either option. In normal operation, R12 and R13 are open, and R10 and R11 are $0\ \Omega$ and are used to terminate any RF coupling onto the bypass trace. To configure the [ADL5240](#) in AMP-DSA loop configuration, R12 should be replaced with a capacitor, R13 should be replaced with a $0\ \Omega$ resistor, and R10 and R11 should be left open. Similarly, to configure the [ADL5240](#) in the DSA-AMP loop configuration, R16 should be replaced with a capacitor, R17 should be replaced with a $0\ \Omega$ resistor, and R14 and R15 should be left open.

The digital signal traces incorporate a footprint for an RC filter to prevent potential noise from coupling onto the signal. In normal operation, Resistors R3 to R9 are $0\ \Omega$ and Capacitors C9 to C15 are open.

ADL5240

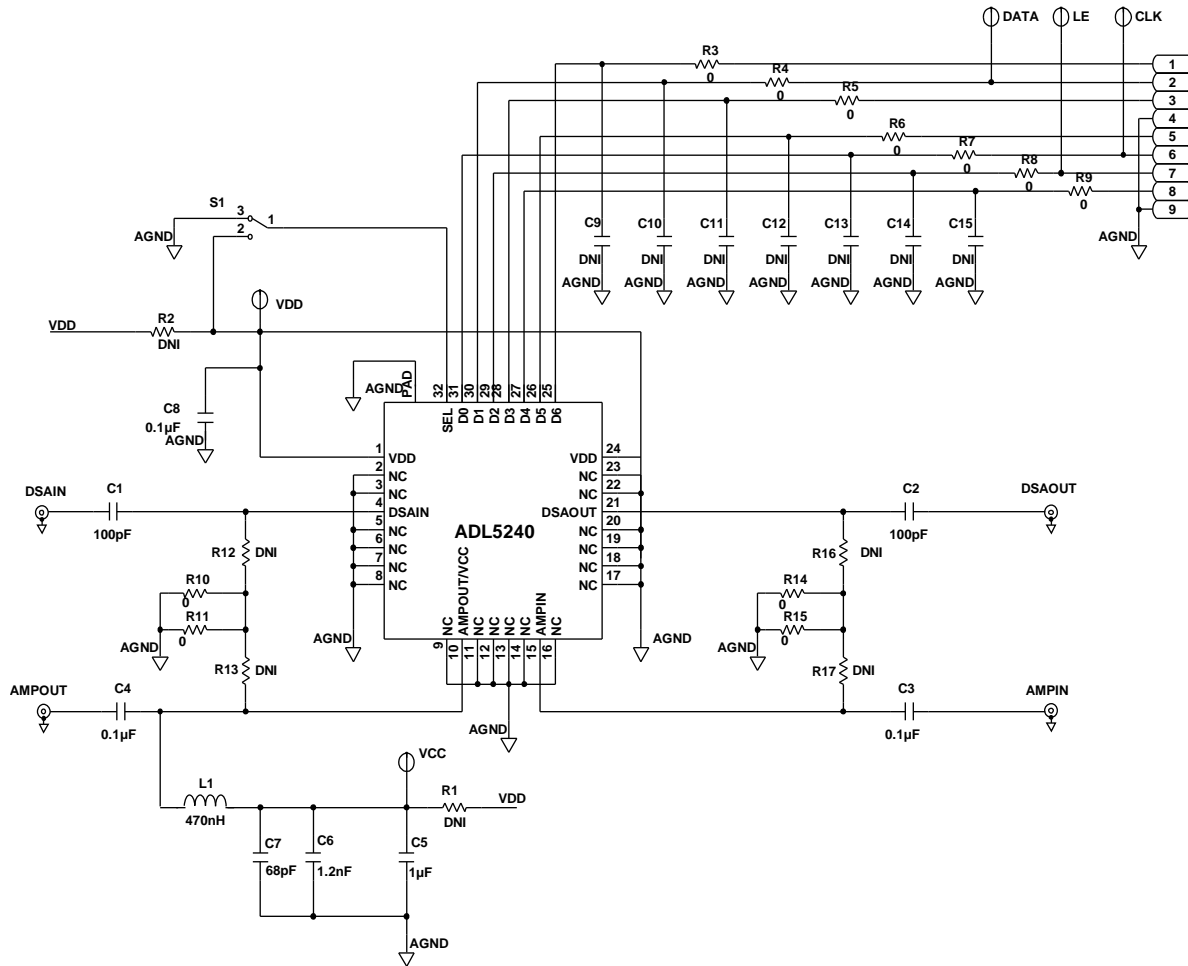


Figure 39. ADL5240 Evaluation Board

Table 8. Evaluation Board Configuration Options

Component	Function/Notes	Default Value
C1, C2	Input/output dc blocking capacitors for DSA.	C1, C2 = 100 pF
C3, C4	Input/output dc blocking capacitors for AMP.	C3, C4 = 0.1 µF
C5, C6, C7	Power supply decoupling for amplifier. The bias associated with the AMPOUT pin is the most sensitive to noise because the bias is connected directly to the output. The smallest capacitor (C7) should be the closest to the AMPOUT pin.	C5 = 1 µF C6 = 1.2 nF C7 = 68 pF
C8	Power supply decoupling for the DSA.	C8 = 0.1 µF
C9, C10, C11, C12, C13, C14, C15	Capacitors of the RC filter on the digital signals leading to the SPI chip.	C9, C10, C11, C12, C13, C14, C15 = open
L1	The bias for the amplifier comes through L1 when VCC is connected to a 5 V supply. L1 should be high impedance for the frequency of operation while providing low resistance for the dc current.	L1 = 470 nH
R1, R2	Resistors to connect the supply for the amplifier and the DSA to the same VDD plane.	R1, R2 = open
R3, R4, R5, R6, R7, R8, R9	Resistors of the RC filter on the digital signals leading to the SPI chip.	R3, R4, R5, R6, R7, R8, R9 = 0 Ω
R10, R11, R14, R15	These resistors are used to terminate RF coupling onto the traces and to close the loop.	R10, R11, R14, R15 = 0 Ω
R12, R13, R16, R17	R12 and R16 are replaced with capacitors, and R13 and R17 are replaced with 0 Ω to close the loop.	R12, R13, R16, R17 = open
S1	Switch to change between the serial mode and parallel mode of operation. Connect to supply for parallel mode and to ground for serial mode operation.	S1 connected to ground

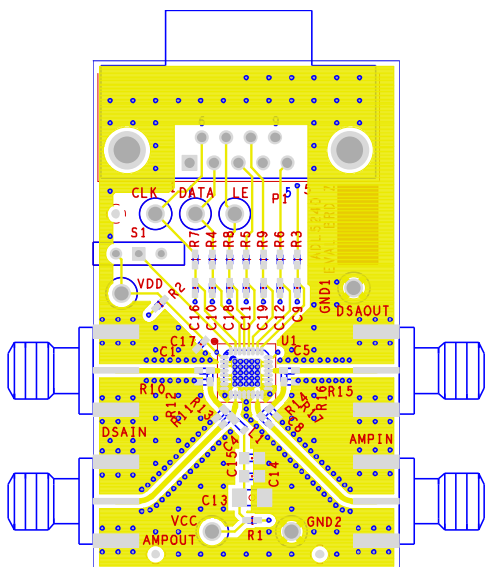


Figure 40. Evaluation Board Layout—Top

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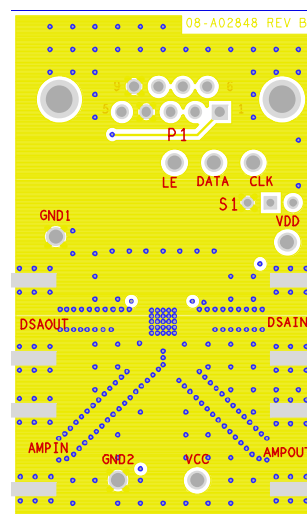
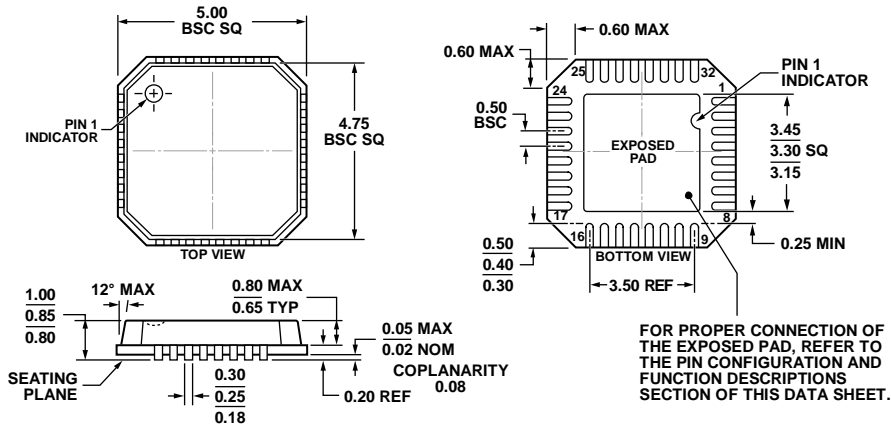


Figure 41. Evaluation Board Layout—Bottom

08430-041

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 42. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]

5 mm × 5 mm Body, Very Thin Quad

(CP-32-3)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADL5240ACPZ-R7	-40°C to +85°C	32 Lead LFCSP_VQ, 7" Tape and Reel	CP-32-3
ADL5240-EVALZ		Evaluation Board	

¹ Z = RoHS Compliant Part.