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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage	V_D		2.7	—	5.5	V
Analog Supply Voltage	V_A		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Digital Power Supply Power-Up Rise Time	V_{DRISE}		10	—	—	μ s
Analog Power Supply Power-Up Rise Time	V_{ARISE}		10	—	—	μ s
Interface Power Supply Power-Up Rise Time	V_{IORISE}		10	—	—	μ s
Ambient Temperature	T_A		-20	25	85	$^{\circ}$ C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_D = V_A = 3.3$ V and 25 $^{\circ}$ C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings^{1,2}

Parameter	Symbol	Value	Unit
Digital Supply Voltage	V_D	-0.5 to 5.8	V
Analog Supply Voltage	V_A	-0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	-0.5 to 3.9	V
Input Current ³	I_{IN}	± 10	mA
Input Voltage ³	V_{IN}	-0.3 to ($V_{IO} + 0.3$)	V
Operating Temperature	T_{OP}	-40 to 95	$^{\circ}$ C
Storage Temperature	T_{STG}	-55 to 150	$^{\circ}$ C
RF Input Level ⁴		0.4	V_{pk}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4702 device is a high-performance RF integrated circuit with an ESD rating of < 2 kV HBM. Handling and assembly of this device should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, GPIO1, GPIO2, and GPIO3.
4. At RF input pins.

Table 3. DC Characteristics $(V_D = V_A = 2.7$ to 3.6 V, $V_{IO} = 1.5$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Operating Supply Current ¹	I_A	ENABLE = 1	—	13.2	—	mA
Digital Operating Supply Current ¹	I_D	ENABLE = 1	—	4.2	—	mA
Interface Operating Supply Current ¹	I_{IO}	ENABLE = 1	—	0.4	—	mA
Total Operating Supply Current ^{1,2,3,4}	I_{OP}	ENABLE = 1, Low SNR Signal	—	18.8	24.5	mA
Total Operating Supply Current ^{1,2,3}	I_{OP}	ENABLE = 1	—	17.8	23.6	mA
Analog Powerdown Supply Current ^{1,6}	I_{APD}	ENABLE = 0	—	1.9	—	uA
Digital Powerdown Supply Current ^{1,6}	I_{DPD}	ENABLE = 0	—	1.9	—	uA
Interface Powerdown Supply Current ^{1,6,7}	I_{IOPD}	ENABLE = 0 SCLK, RCLK inactive	—	2.0	—	uA
Total Powerdown Supply Current ^{1,6}	I_{PD}	ENABLE = 0	—	5.8	14.1	uA
High Level Input Voltage ⁸	V_{IH}		$0.7 \times V_{IO}$	—	$V_{IO} + 0.3$	V
Low Level Input Voltage ⁸	V_{IL}		-0.3	—	$0.3 \times V_{IO}$	V
High Level Input Current ⁸	I_{IH}	$V_{IN} = V_{IO} = 3.6$ V	-10	—	10	μA
Low Level Input Current ⁸	I_{IL}	$V_{IN} = 0$ V, $V_{IO} = 3.6$ V	-10	—	10	μA
High Level Output Voltage ⁹	V_{OH}	$I_{OUT} = 500$ μA	$0.8 \times V_{IO}$	—	—	V
Low Level Output Voltage ⁹	V_{OL}	$I_{OUT} = -500$ μA	—	—	$0.2 \times V_{IO}$	V

Notes:

1. Refer to Register 02h, "Power Configuration" on page 22 for ENABLE bit description.
2. The LNA is automatically switched to higher current mode for optimum sensitivity in low SNR conditions.
3. Analog and digital supply currents are simultaneously adjusted based on SNR level.
4. Stereo and RDS functionality are disabled at low SNR levels.
5. RDS functionality only available for Si4703.
6. Refer to Section 4.8. "Reset, Powerup, and Powerdown" on page 17.
7. All GPIO pins are grounded.
8. For input pins SCLK, SEN, SDIO, RST, RCLK, GPIO1, GPIO2, and GPIO3.
9. For output pins SDIO, GPIO1, GPIO2, and GPIO3.

Table 4. Reset Timing Characteristics (Busmode Select Method 1)^{1,2,3}

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
$\overline{\text{RST}}$ pulse width and GPIO3 Setup to $\overline{\text{RST}}\uparrow$	t_{GSRST1}^4	GPIO3 = 0	100	—	—	μs
$\overline{\text{SEN}}$ and SDIO Setup to $\overline{\text{RST}}\uparrow$	t_{SRST1}		30	—	—	ns
$\overline{\text{SEN}}$, SDIO, and GPIO3 Hold from $\overline{\text{RST}}\uparrow$	t_{HRST1}		30	—	—	ns

Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
2. When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$ and that it stays high until after the first start condition.
4. If GPIO3 is driven low by the user, minimum t_{GSRST1} is only 30 ns. If GPIO3 is hi-Z, minimum t_{GSRST1} is 100 μs to provide time for an on-chip 1 M Ω pulldown device (active while $\overline{\text{RST}}$ is low) to discharge the pin.

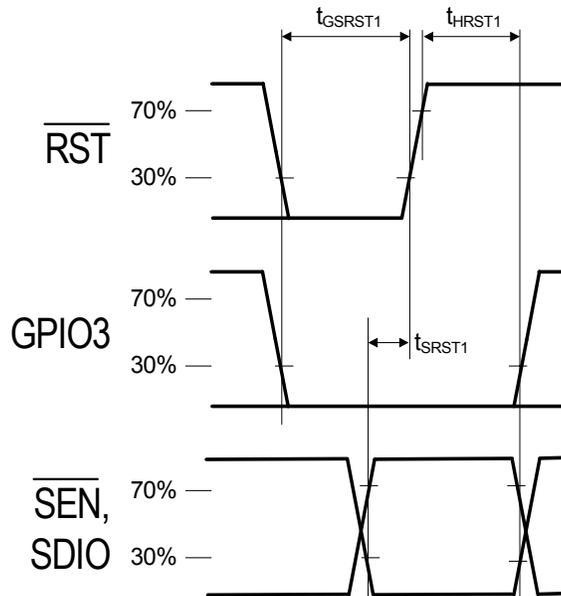


Figure 1. Reset Timing Parameters for Busmode Select Method 1 (GPIO3 = 0)

Table 5. Reset Timing Characteristics (Busmode Select Method 2)^{1,2,3}

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GPIO1 and GPIO3 setup to $\overline{\text{RST}}\uparrow$	t_{SRST2}	GPIO3 = 1	30	—	—	ns
GPIO1 and GPIO3 hold from $\overline{\text{RST}}\uparrow$	t_{HRST2}		30	—	—	ns

Notes:

- When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
- When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
- When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$ and stays high until after the first start condition.

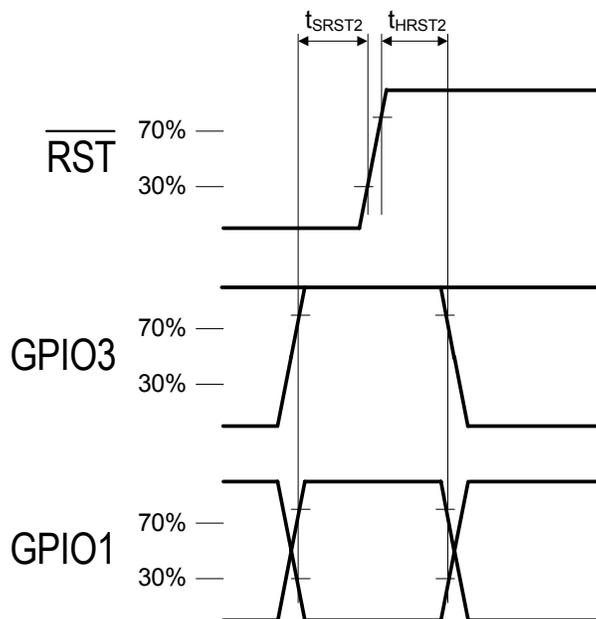


Figure 2. Reset Timing Parameters for Busmode Select Method 2 (GPIO3 = 1)

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Table 6. 3-Wire Control Interface Characteristics

($V_D = V_A = 2.7$ to 5.5 V, $V_{IO} = 1.5$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, \overline{SEN} to SCLK \uparrow Setup	t_s		20	—	—	ns
SDIO Input to SCLK \uparrow Hold	t_{HSDIO}		10	—	—	ns
\overline{SEN} Input to SCLK \downarrow Hold	t_{HSEN1}		10	—	—	ns
\overline{SEN} Input to SCLK \uparrow Hold	t_{HSEN2}		10	—	—	ns
SCLK \uparrow to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK \uparrow to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

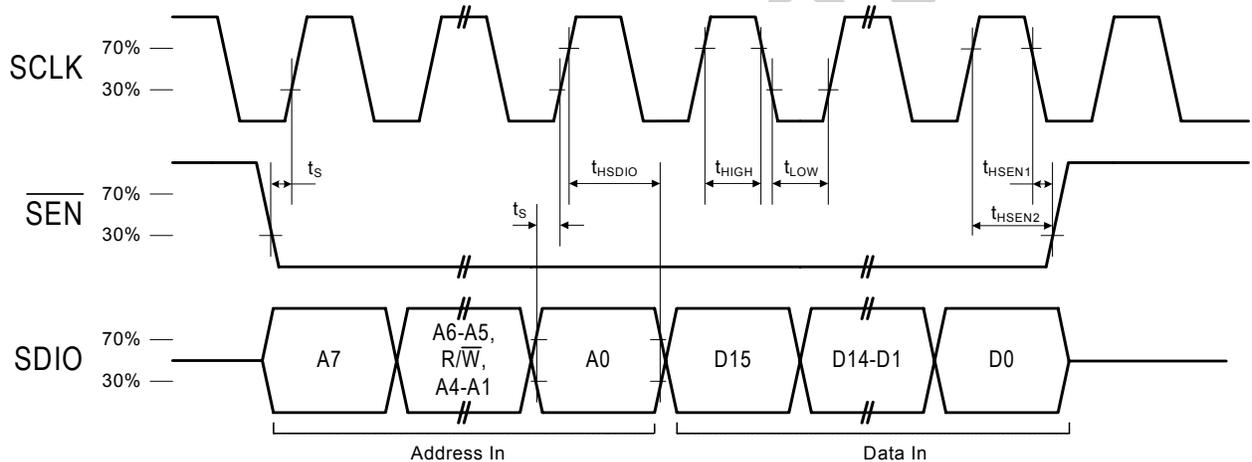


Figure 3. 3-Wire Control Interface Write Timing Parameters

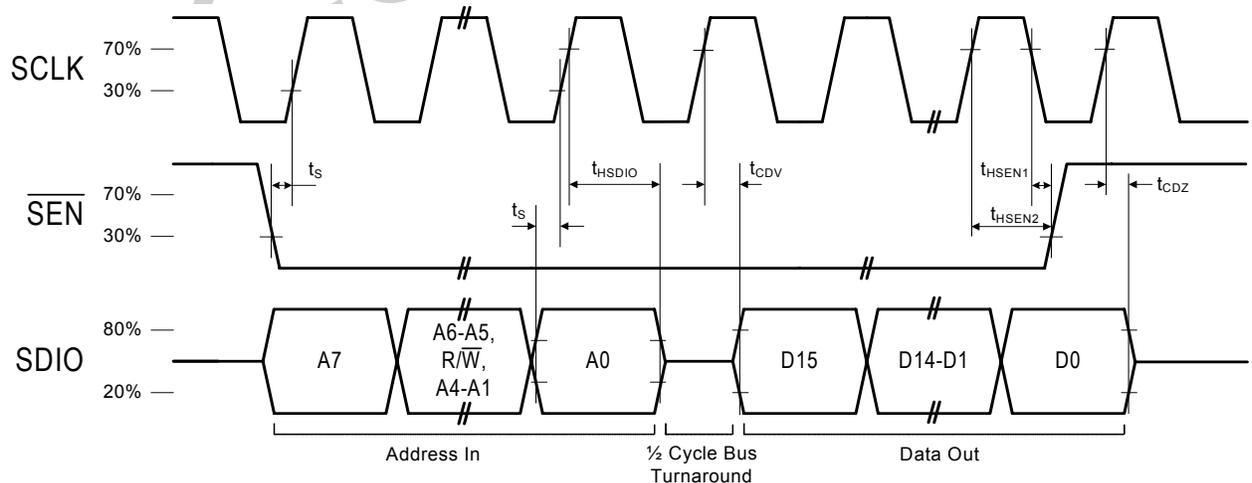


Figure 4. 3-Wire Control Interface Read Timing Parameters

Table 7. 2-Wire Control Interface Characteristics^{1,2,3}(V_D = V_A = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f _{SCL}		0	—	400	kHz
SCLK Low Time	t _{LOW}		1.3	—	—	μs
SCLK High Time	t _{HIGH}		0.6	—	—	μs
SCLK Input to SDIO↓ Setup (START)	t _{SU:STA}		0.6	—	—	μs
SCLK Input to SDIO↓ Hold (START)	t _{HD:STA}		0.6	—	—	μs
SDIO Input to SCLK↑ Setup	t _{SU:DAT}		100	—	—	ns
SDIO Input to SCLK↓ Hold ^{4, 5}	t _{HD:DAT}		0	—	900	ns
SCLK input to SDIO↑ Setup (STOP)	t _{SU:STO}		0.6	—	—	μs
STOP to START Time	t _{BUF}		1.3	—	—	μs
SDIO Output Fall Time	t _{f:OUT}		20 + 0.1 C _b	—	250	ns
SDIO Input, SCLK Rise/Fall Time	t _{f:IN} t _{r:IN}		20 + 0.1 C _b	—	300	ns
SCLK, SDIO Capacitive Loading	C _b		—	—	50	pF
Input Filter Pulse Suppression	t _{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low-impedance.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$ and that it stays high until after the first start condition.
3. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
4. As a transmitter, the Si4703 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the 0 ns t_{HD:DAT} specification.
5. The maximum t_{HD:DAT} has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 kHz, t_{HD:DAT} may be violated so long as all other timing parameters are met.

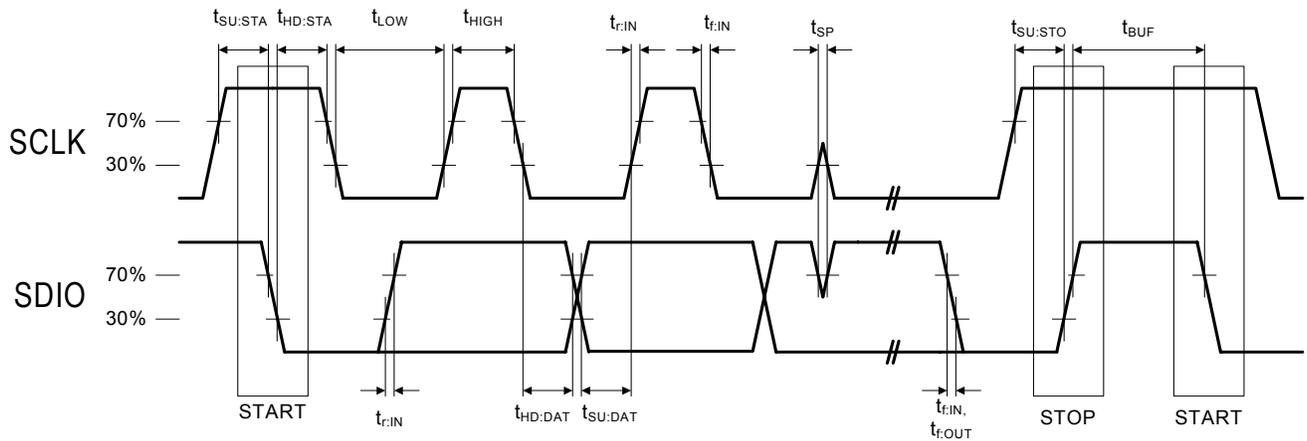


Figure 5. 2-Wire Control Interface Read and Write Timing Parameters

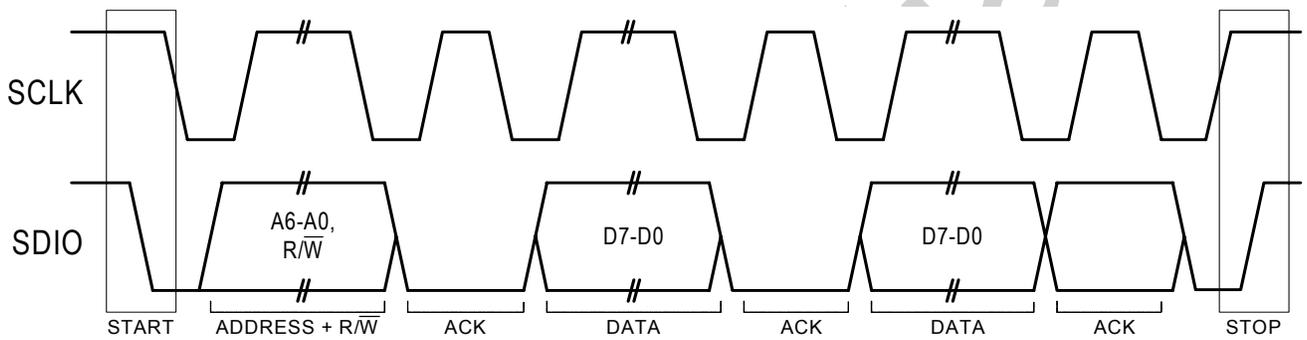


Figure 6. 2-Wire Control Interface Read and Write Timing Diagram

Table 8. FM Receiver Characteristics^{1,2}(V_D = V_A = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f _{RF}		76	—	108	MHz
Sensitivity ^{3,4,5,6,7,8}		(S+N)/N = 26 dB	—	2.2	3.5	μVEMF
Sensitivity (50 Ω matching network) ^{3,4,5,6}		(S+N)/N = 26 dB	—	1.1	—	μVEMF
LNA Input Resistance ^{8,9}			3	4	5	kΩ
LNA Input Capacitance ^{8,9}			4	5	6	pF
Input IP3 ^{8,10}			104	108	—	dBμVEMF
AM Suppression ^{3,4,5,8,9}		m = 0.3	40	55	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection ⁸		In-band	35	—	—	dB
RCLK Frequency			—	32.768	—	kHz
RCLK Frequency Tolerance ¹¹		SPACE[1:0] = 00 or 01	-200	—	200	ppm
		SPACE[1:0] = 10	-50	—	50	
Audio Output Voltage ^{3,4,5,9}			72	80	90	mV _{RMS}
Audio Output L/R Imbalance ^{3,4,9,12}			—	—	1	dB
Audio Band Limits ^{3,4,8,9}		±1.5 dB	30	—	15 k	Hz
Audio Stereo Separation ^{3,9,12}			25	—	—	dB
Mono/Stereo Switching Level ^{3,8,12}		BLNDADJ = 10 10 dB stereo separation	—	34	—	dBμVEMF

Notes:

- Additional testing information is available in Application Note AN234. Volume = maximum for all tests.
- To ensure proper operation and FM receiver performance, follow the guidelines in "AN231: Si4700/01/02/03 Headphone and Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
- F_{MOD} = 1 kHz, 75 μs de-emphasis.
- MONO = 1, and L = R unless noted otherwise.
- Δf = 22.5 kHz.
- B_{AF} = 300 Hz to 15 kHz, A-weighted.
- Typical sensitivity with headphone matching network.
- Guaranteed by characterization.
- Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz.
- |f₂ - f₁| > 1 MHz, f₀ = 2 x f₁ - f₂. AGC is disabled by setting AGCD = 1. Refer to Section "6. Register Descriptions" on page 21.
- The channel spacing is selected with the SPACE[1:0] bits. Refer to Section "6. Register Descriptions". Seek/Tune timing is guaranteed for 100 and 200 kHz channel spacing.
- Δf = 75 kHz.
- The de-emphasis time constant is selected with the DE bit. Refer to Section "6. Register Descriptions".
- At LOUT and ROUT pins.
- Do not enable STC interrupts before the powerup time is complete. If STC interrupts are enabled before the powerup time is complete, an interrupt will be generated within the powerup interval when the initial default tune operation is complete. See "AN230: Si4700/01/02/03 Programmer's Guide" for more information.
- Min and Max at room temperature (25 °C).

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Table 8. FM Receiver Characteristics^{1,2} (Continued)

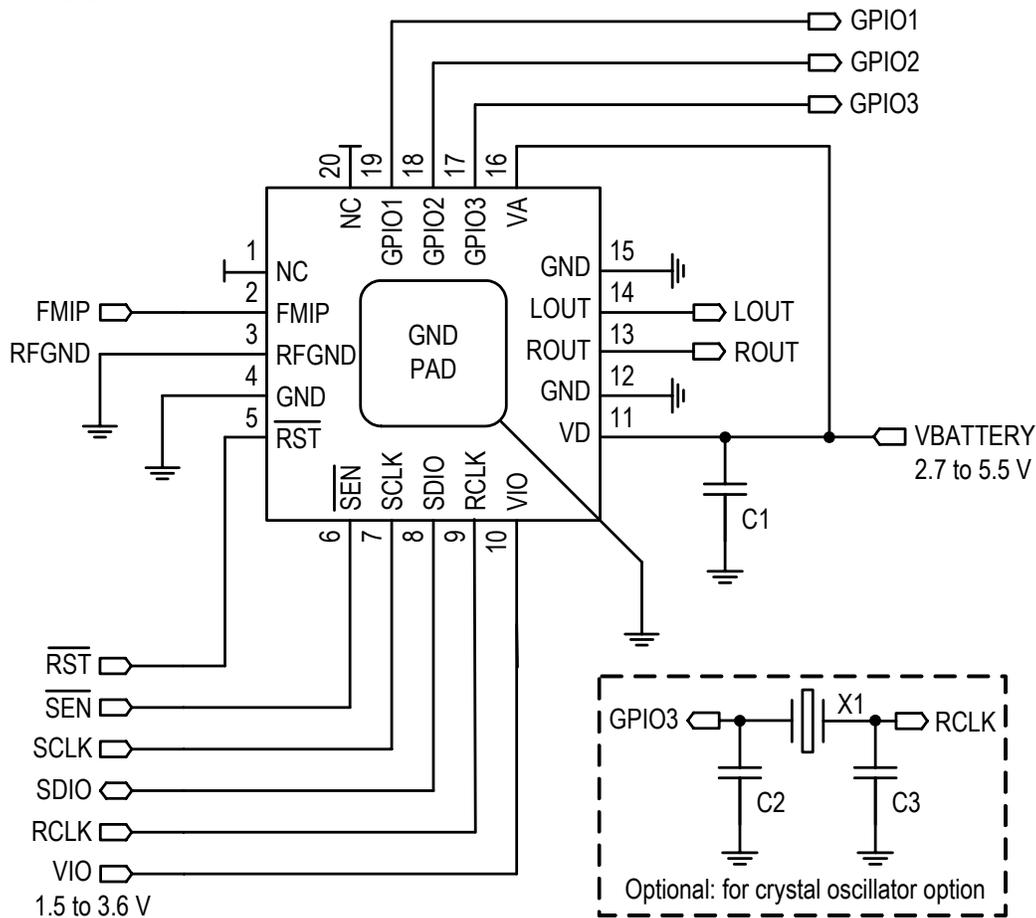
($V_D = V_A = 2.7$ to 5.5 V, $V_{IO} = 1.5$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Mono S/N ^{3,4,5,6,9}			55	59	—	dB
Audio Stereo S/N ^{5,8}		BLNDADJ = 10	—	58	—	dB
Audio THD ^{3,4,9,12}			—	0.1	0.5	%
De-emphasis Time Constant ¹³		DE = 0	70	75	80	μs
		DE = 1	45	50	54	μs
Audio Common Mode Voltage ¹⁴		ENABLE = 1	0.7	0.8	0.9	V
Audio Common Mode Voltage ¹⁴		ENABLE = 0 AHIZEN = 1	—	$0.5 \times V_{IO}$	—	V
Audio Output Load Resistance ^{8,14}	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance ^{8,14}	C_L	Single-ended	—	—	50	pF
Seek/Tune Time ^{8,11}		SPACE[1:0] = 0x, RCLK tolerance = 200 ppm, (x = 0 or 1)	—	—	60	ms/ channel
Powerup Time ¹⁵		From powerdown (Write ENABLE bit to 1)	—	—	110	ms
RSSI Offset ¹⁶		Input levels of 8 and 60 dBμV at RF input	-3	—	3	dB

Notes:

- Additional testing information is available in Application Note AN234. Volume = maximum for all tests.
- To ensure proper operation and FM receiver performance, follow the guidelines in “AN231: Si4700/01/02/03 Headphone and Antenna Interface.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
- $F_{MOD} = 1$ kHz, 75 μs de-emphasis.
- MONO = 1, and L = R unless noted otherwise.
- $\Delta f = 22.5$ kHz.
- $B_{AF} = 300$ Hz to 15 kHz, A-weighted.
- Typical sensitivity with headphone matching network.
- Guaranteed by characterization.
- Measured at $V_{EMF} = 1$ mV, $f_{RF} = 76$ to 108 MHz.
- $|f_2 - f_1| > 1$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled by setting AGCD = 1. Refer to Section “6. Register Descriptions” on page 21.
- The channel spacing is selected with the SPACE[1:0] bits. Refer to Section “6. Register Descriptions”. Seek/Tune timing is guaranteed for 100 and 200 kHz channel spacing.
- $\Delta f = 75$ kHz.
- The de-emphasis time constant is selected with the DE bit. Refer to Section “6. Register Descriptions”.
- At LOUT and ROUT pins.
- Do not enable STC interrupts before the powerup time is complete. If STC interrupts are enabled before the powerup time is complete, an interrupt will be generated within the powerup interval when the initial default tune operation is complete. See “AN230: Si4700/01/02/03 Programmer’s Guide” for more information.
- Min and Max at room temperature (25 °C).

2. Typical Application Schematic



Notes:

- Place C1 close to V_D pin.
- All grounds connect directly to GND plane on PCB.
- Pins 1 and 20 are no connects; leave floating.
- FM Receiver performance is subject to adherence to antenna design guidelines in "AN231: Si4700/01/02/03 Headphone and Antenna Interface." Failure to use these guidelines will negatively affect the performance of the Si4702, particularly in weak-signal and noisy environments. Silicon Laboratories will evaluate schematics and layouts for qualified customers.**
- Pin 2 connects to the antenna interface, refer to "AN231: Si4700/01/02/03 Headphone and Antenna Interface."
- Place Si4702 as close as possible to the antenna jack, and keep the FMIP trace as short as possible.
- Refer to Si4702 Internal Crystal Oscillator Errata.
- Refer to "AN299: External 32.768 kHz Crystal Oscillator."

3. Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, $\pm 20\%$, Z5U/X7R	Murata
U1	Si4702 FM Radio Tuner	Silicon Laboratories
C2, C3	Crystal load capacitors, 22 pF, $\pm 5\%$, COG (optional for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (optional for crystal oscillator option)	Epson

4. Functional Description

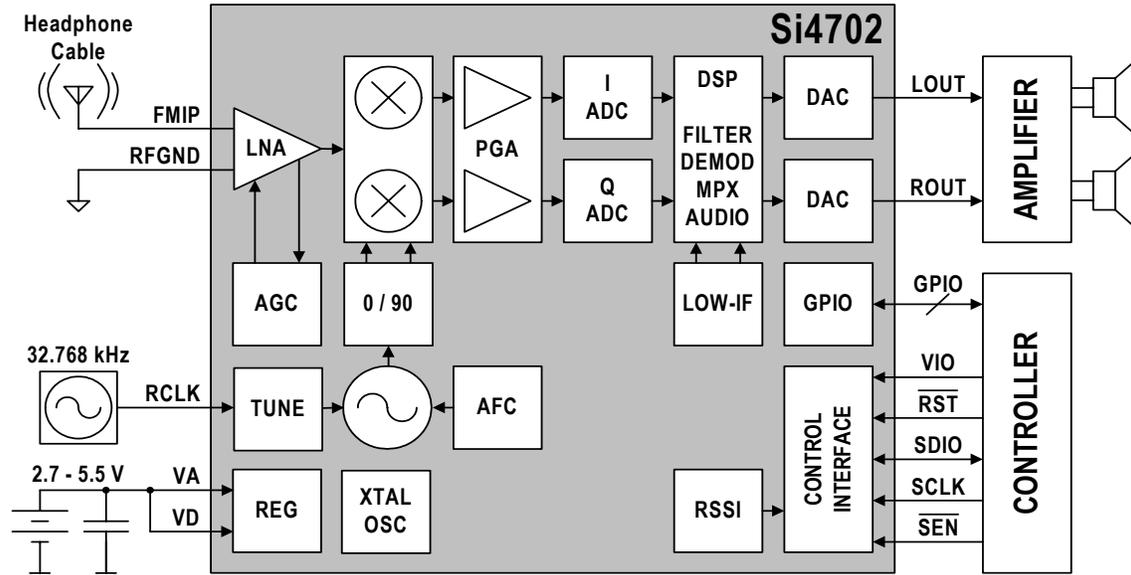


Figure 7. Si4702 FM Receiver Block Diagram

4.1. Overview

The Si4702 extends Silicon Laboratories' Si4700 FM tuner family and further increases the ease and attractiveness of adding FM radio reception to mobile devices through small size and board area, minimum component count, flexible programmability, and superior, proven performance. Si4702 software is backwards-compatible to existing Si4700 FM Tuner designs and leverages Silicon Laboratories' highly-successful and patented Si4700 FM tuner. The Si4702 benefits from proven digital integration and 100% CMOS process technology, resulting in a completely integrated solution. It is the industry's smallest footprint FM tuner IC requiring only 10 mm² of board space and one external bypass capacitor.

The device offers significant programmability and caters to the subjective nature of FM listeners and variable FM broadcast environments world-wide through a simplified programming interface and mature functionality.

The Si4702 is based on the superior, proven performance of Silicon Laboratories' Si4700 architecture offering unmatched interference rejection and leading sensitivity. The device uses the same programming interface as the Si4700 and supports multiple bus modes. Power management is also simplified with an integrated regulator allowing direct connection to a 2.7 to 5.5 V battery.

The Si4702 device's high level of integration and complete FM system production testing increases quality to manufacturers, improves device yields, and simplifies device manufacturing and final testing.

The Si4703, a pin-compatible device that supports RDS/RBDS, is also available. The Si4703 incorporates a digital processor for the European Radio Data System (RDS) and the U.S. Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions.

4.2. FM Receiver

The Si4702's patented, digital, low-IF architecture reduces the number of external components and eliminates the need for factory adjustments. The receive (RX) section integrates a low-noise amplifier (LNA) supporting the worldwide FM broadcast band (76 to 108 MHz). An automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. For testing purposes, the AGC can be disabled with the AGCD bit. Refer to Section 6. "Register Descriptions" on page 21 for additional programming and configuration information.

The Si4702 architecture and antenna design increases system performance. To ensure proper performance and operation, designers should refer to the guidelines in "AN231: Si4700/01/02/03 Headphone and Antenna Interface". Conformance to these guidelines will help ensure excellent performance even in weak-signal or noisy environments.

An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high-resolution analog-to-digital converters (ADCs). This advanced architecture achieves superior performance by using digital signal processing (DSP) to perform channel selection, FM demodulation, and stereo audio processing compared to traditional analog architectures.

4.3. General Purpose I/O Pins

Pins GPIO1–3 can serve multiple functions. GPIO1 and GPIO3 can be used to select between 2-wire and 3-wire modes for the control interface as the device is brought out of reset. See Section “4.8. Reset, Powerup, and Powerdown”. After powerup of the device, pins GPIO1–3 can be used as general-purpose inputs/outputs, and pins GPIO2–3 can be used as interrupt request pins for seek/tune and as a stereo/mono indicator. See register 04h, bits [5:0], in Section 6. “Register Descriptions” on page 21 for information on controlling these pins. It is recommended that the GPIO2–3 pins not be used as interrupt request outputs until the powerup time has completed (see Section “4.8. Reset, Powerup, and Powerdown”). The GPIO3 pin has an internal, $1\text{ M}\Omega$, $\pm 15\%$ pull-down resistor that is only active while $\overline{\text{RST}}$ is low. General-purpose input/output functionality is available regardless of the state of the V_A and V_D supplies, or the ENABLE and DISABLE bits.

4.4. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961 and is used worldwide. Today’s MPX signal format consists of left+right (L+R) audio, left–right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 8.

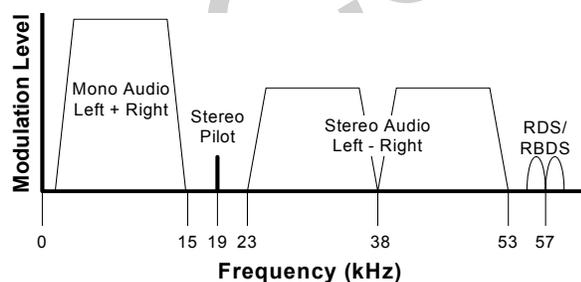


Figure 8. MPX Signal Spectrum

The Si4702’s integrated stereo decoder automatically decodes the MPX signal. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal.

Separate left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals, respectively.

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. The signal level range over which the stereo to mono blending occurs can be adjusted by setting the BLNDADJ[1:0] register. Stereo/mono status can be monitored with the ST register bit and mono operation can be forced with the MONO register bit.

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants, 50 or 75 μs , are used in various regions. The de-emphasis time constant is programmable with the DE bit.

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted with the DMUTE bit. Volume can be adjusted digitally with the VOLUME[3:0] bits. The volume dynamic range can be set to either -28 dBFS (default) or -58 dBFS by setting VOLEXT=1.

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in weak-signal conditions. The soft mute attack and decay rate can be adjusted with the SMUTER[1:0] bits where 00 is the fastest setting. The soft mute attenuation level can be adjusted with the SMUTEA[1:0] bits where 00 is the most attenuated. The soft mute disable (DSMUTE) bit may be set high to disable this feature.

4.5. Tuning

The Si4702 uses Silicon Laboratories’ patented and proven frequency synthesizer technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception. The tuning frequency is defined as:

$$\text{Freq (MHz)} = \text{Spacing (kHz)} \times \text{Channel} + \text{Bottom of Band (MHz)}$$

Channel spacing of 50, 100 or 200 kHz is selected with bits SPACE[1:0]. The channel is selected with bits CHAN[9:0]. Band selection for Japan, Japan wideband, or Europe/U.S./Asia is set with BAND[1:0]. The tuning operation begins by setting the TUNE bit. After tuning completes, the seek/tune complete (STC) bit will be set and the RSSI level is available by reading bits RSSI[7:0]. The TUNE bit must be set low after the STC bit is set high in order to complete the tune operation and clear the STC bit.

Seek tuning searches up or down for a channel with an RSSI greater than or equal to the seek threshold set with the SEEKTH[7:0] bits. In addition, optional SNR and/or impulse noise detector criteria may be used to qualify valid stations. The SKSNR[3:0] bits set the required SNR threshold. The SKCNT[3:0] bits set the impulse noise threshold. Using the extra seek qualifiers can reduce false stops and, in combination with lowering the RSSI seek threshold, increase the number of found stations. The SNR and impulse noise detectors are disabled by default for backwards-compatibility.

Two seek modes are available. When the seek mode (SKMODE) bit is low and a seek is initiated, the device seeks through the band, wraps from one band edge to the other, and continues seeking. If the seek operation is unable to find a valid channel, the seek failure/band limit (SF/BL) bit is set high and the device returns to the channel selected before the seek operation began. When the SKMODE bit is high and a seek is initiated, the device seeks through the band until the band limit is reached and the SF/BL bit is set high. A seek operation is initiated by setting the SEEK and SEEKUP bits. After the seek operation completes, the STC bit is set, and the RSSI level and tuned channel are available by reading bits RSSI[7:0] and bits READCHAN[9:0]. During a seek operation, READCHAN[9:0] is also updated and may be read to determine and report seek progress. The STC bit is set after the seek operation completes. The channel is valid if the seek operation completes and the SF/BL bit is set low. At other times, such as before a seek operation or after a seek completes and the SF/BL bit is set high, the channel is valid if the AFC Rail (AFCRL) bit is set low and the value of RSSI[7:0] is greater than or equal to SEEKTH[7:0]. Note that if a valid channel is found but the AFCRL bit is set, the audio output is muted as in the softmute case discussed in Section "4.4. Stereo Audio Processing". The SEEK bit must be set low after the STC bit is set high in order to complete the seek operation. Setting the STC bit low clears STC status and SF/BL bits. The seek operation may be aborted by setting the SEEK bit low at any time.

The device can be configured to generate an interrupt on GPIO2 when a tune or seek operation completes. Setting the seek/tune complete (STCIEN) bit and GPIO2[1:0] = 01 will configure GPIO2 for a 5 ms low interrupt when the STC bit is set by the device.

For additional recommendations on optimizing the seek function, consult "AN284: Si4700/01/02/03 Seek Adjustability and Settings."

4.6. Reference Clock

The Si4702 accepts a 32.768 kHz reference clock to the RCLK pin. The reference clock is required whenever the ENABLE bit is set high. Refer to Table 3, "DC Characteristics," on page 5 for input switching voltage levels and Table 8, "FM Receiver Characteristics," on page 11 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to 2. "Typical Application Schematic" on page 13. The oscillator must be enabled or disabled while in powerdown (ENABLE = 0) as shown in Figure 9 on page 19. Register 07h, bits [13:0], must be preserved as 0x0100 while in powerdown. Note that the RCLK voltage levels are not specified. When the crystal oscillator is used, the typical RCLK voltage level is $0.3 V_{pk-pk}$.

4.6.1. Si4702 Internal Crystal Oscillator Errata

The Si4702-B16 seek/tune performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4702-B16 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes and/or false stops. SDIO activity during all other operational states does not affect performance.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4702-B16 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus and delaying tuner polling until the tune or seek operation is complete. The STC (seek/tune complete) interrupt should be used instead of polling to determine when a seek/tune operation is complete. Refer to the Si4702-B16 data sheet for specified seek/tune times and register use guidelines.

The layout guidelines in Si4700/01/02/03 Evaluation Board User's Guide, Section 8.3. "Si4702 Daughter Card", should be followed to help ensure robust FM performance. Refer to the posted Si4702 Internal Crystal Oscillator Errata for more information.

4.7. Control Interface

Two-wire, slave-transceiver, and three-wire interfaces are provided for the controller IC to read and write the control registers. Refer to “4.8. Reset, Powerup, and Powerdown” for a description of bus mode selection. Registers may be written and read when the V_{IO} supply is applied regardless of the state of the V_D or V_A supplies. RCLK is not required for proper register operation.

4.7.1. 3-Wire Control Interface

For three-wire operation, a transfer begins when the \overline{SEN} pin is sampled low by the device on a rising SCLK edge. The control word is latched internally on rising SCLK edges and is nine bits in length, comprised of a four-bit chip address, $A7:A4 = 0110b$, a read/write bit (write = 0 and read = 1), and a four-bit register address, $A3:A0$. The ordering of the control word is $A7:A5$, R/W, $A4:A0$. Refer to Section 5. “Register Summary” on page 20 for a list of all registers and their addresses.

For write operations, the serial control word is followed by a 16-bit data word and is latched internally on rising SCLK edges.

For read operations, a bus turnaround of half a cycle is followed by a 16-bit data word shifted out on rising SCLK edges and is clocked into the system controller on falling SCLK edges. The transfer ends on the rising SCLK edge after \overline{SEN} is set high. Note that 26 SCLK cycles are required for a transfer; however, SCLK may run continuously.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 8, Figure 3, “3-Wire Control Interface Write Timing Parameters,” on page 8, and Figure 4, “3-Wire Control Interface Read Timing Parameters,” on page 8.

4.7.2. 2-wire Control Interface

For two-wire operation, the SCLK and SDIO pins function in open-drain mode (pull-down only) and must be pulled up by an external device. A transfer begins with the START condition (falling edge of SDIO while SCLK is high). The control word is latched internally on rising SCLK edges and is eight bits in length, comprised of a seven-bit device address equal to $0010000b$, and a read/write bit (write = 0 and read = 1).

The device acknowledges the address by driving SDIO low after the next falling SCLK edge, for one cycle. For write operations, the device acknowledge is followed by an eight bit data word latched internally on rising edges of SCLK. The device acknowledges each byte of data written by driving SDIO low after the next falling SCLK edge, for one cycle. An internal address counter automatically increments to allow continuous data byte

writes, starting with the upper byte of register 02h, followed by the lower byte of register 02h, and onward until the lower byte of the last register is reached. The internal address counter then automatically wraps around to the upper byte of register 00h and proceeds from there until continuous writes end. Data transfer ends with the STOP condition (rising edge of SDIO while SCLK is high). After every STOP condition, the internal address counter is reset.

For read operations, the device acknowledge is followed by an eight-bit data word shifted out on falling SCLK edges. An internal address counter automatically increments to allow continuous data byte reads, starting with the upper byte of register 0Ah, followed by the lower byte of register 0Ah, and onward until the lower byte of the last register is reached. The internal address counter then automatically wraps around to the upper byte of register 00h and proceeds from there until continuous reads cease. After each byte of data is read, the controller IC must drive an acknowledge ($SDIO = 0$) if an additional byte of data will be requested. Data transfer ends with the STOP condition. After every STOP condition, the internal address counter is reset.

For details on timing specifications and diagrams, refer to Table 7, “2-Wire Control Interface Characteristics^{1,2,3},” on page 9, Figure 5, “2-Wire Control Interface Read and Write Timing Parameters,” on page 10 and Figure 6, “2-Wire Control Interface Read and Write Timing Diagram,” on page 10.

4.8. Reset, Powerup, and Powerdown

Driving the \overline{RST} pin low will disable the Si4702-B16 and its control bus interface and reset the registers to their default settings. Driving the \overline{RST} pin high will bring the device out of reset. As the device is brought out of reset, it will sample the state of several pins to select between 2-wire and 3-wire control interface operation using one of two busmode selection methods.

Busmode selection method 1 requires the use of the GPIO3, \overline{SEN} , and SDIO pins. To use this busmode selection method, the GPIO3 and SDIO pins must be sampled low by the device on the rising edge of \overline{RST} .

The user may either drive the GPIO3 pin low externally, or leave the pin floating. If the pin is not driven by the user, it will be pulled low by an internal 1 M Ω resistor that is active only while \overline{RST} is low. The user must drive the \overline{SEN} and SDIO pins externally to the proper state.

To select 2-wire operation, the \overline{SEN} pin must be sampled high by the device on the rising edge of \overline{RST} .

To select 3-wire operation, the \overline{SEN} pin must be sampled low by the device on the rising edge of \overline{RST} .

Refer to Table 4, “Reset Timing Characteristics (Busmode Select Method 1)^{1,2,3},” on page 6 and Figure 1, “Reset Timing Parameters for Busmode Select Method 1 (GPIO3 = 0),” on page 6.

Busmode selection method 2 requires only the use of the GPIO3 and GPIO1 pins. This is the recommended busmode selection method when not using the internal crystal oscillator. To use this busmode selection method, the GPIO3 pin must be sampled high on the rising edge of \overline{RST} . The user must drive the GPIO3 pin high externally or pull it up with a resistor of 100 k Ω or less. The user must also drive the GPIO1 pin externally to the proper state.

To select 2-wire operation, the GPIO1 pin must be sampled high by the device on the rising edge of \overline{RST} .

To select 3-wire operation, the GPIO1 pin must be sampled low by the device on the rising edge of \overline{RST} .

Refer to Table 5, “Reset Timing Characteristics (Busmode Select Method 2)^{1,2,3},” on page 7 and Figure 2, “Reset Timing Parameters for Busmode Select Method 2 (GPIO3 = 1),” on page 7.

Table 9 summarizes the two bus selection methods.

Table 9. Selecting 2-Wire or 3-Wire Control Interface Busmode Operation^{1,2,3}

Busmode Select Method	\overline{SEN}	SDIO	GPIO1	GPIO3 ²	Bus mode
1	0	0	X	0 ⁴	3-wire
1	1	0	X	0 ⁴	2-wire
1 Xtal Oscillator	0	0	X	0 ⁵	3-wire
1 Xtal Oscillator	1	0	X	0 ⁵	2-wire
2	X	X	0	1 ⁶	3-wire
2	X	X	1	1 ⁶	2-wire
2 Xtal Oscillator	NA	NA	NA	NA	NA
2 Xtal Oscillator	NA	NA	NA	NA	NA

Notes:

- All parameters are applied on the rising edge of \overline{RST} .
- When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of \overline{RST} and that it stays high until the first start condition.
- GPIO3 is internally pulled down with a 1 M Ω resistor.
- GPIO3 should be externally driven low, set to high-Z (10 M Ω or greater pull-up) or float.
- GPIO3 should be left floating.
- GPIO3 should be externally driven high (100 k Ω or smaller pull-up).

When proper voltages are applied to the Si4702-B16, the ENABLE and DISABLE bits in Register 02h can be used to select between powerup and powerdown modes. When voltage is first applied to the device, ENABLE = 0 and DISABLE = 0. Setting ENABLE = 1 and DISABLE = 0 puts the device in powerup mode. To power down the device, the ENABLE and DISABLE bits must both be written to 1.

After being written to 1, both bits will be cleared as part of the internal device powerdown sequence. To put the device back into powerup mode, set ENABLE = 1 and DISABLE = 0 as described above. The ENABLE bit should never be written to a 0.

4.9. Audio Output Summation

The audio outputs, LOUT and ROUT, may be capacitively summed with another device. Setting the audio high-Z enable (AHIZEN) bit maintains a dc bias of $0.5 \times V_{IO}$ on the LOUT and ROUT pins to prevent the ESD diodes from clamping to the V_{IO} or GND rail in response to the output swing of the other device. The bias point is set with a 370 k Ω resistor to V_{IO} and GND. Register 07h containing the AHIZEN bit must not be written during the powerup sequence and only takes effect when in powerdown and V_{IO} is supplied. In powerup, the LOUT and ROUT pins are set to the common-mode voltage specified in Table 8, “FM Receiver Characteristics^{1,2},” on page 11, regardless of the state of AHIZEN. Bits 13:0 of register 07h must be preserved as 0x0100 while in powerdown and as 0x3C04 while in powerup.

4.10. Initialization Sequence

Refer to Figure 9, “Initialization Sequence,” on page 19.

To initialize the device:

- Supply V_A and V_D .
- Supply V_{IO} while keeping the \overline{RST} pin low. Note that steps 1 and 2 may be reversed. Power supplies may be sequenced in any order.
- Select 2-wire or 3-wire control interface bus mode operation as described in Section 4.8. “Reset, Powerup, and Powerdown” on page 17.
- Provide RCLK. Steps 3 and 4 may be reversed when using an external oscillator. Wait 500 ms for oscillator startup when using internal oscillator.
- Set the ENABLE bit high and the DISABLE bit low to power up the device. Software should wait for the powerup time (as specified by Table 8, “FM Receiver Characteristics^{1,2},” on page 11) before continuing with normal part operation.

To power down the device:

1. (Optional) Set the AHIZEN bit high to maintain a dc bias of $0.5 \times V_{IO}$ volts at the LOUT and ROUT pins while in powerdown mode but preserve the states of the other bits in Register 07h. Note that in powerup mode, the LOUT and ROUT pins are set to the common-mode voltage specified in Table 8 on page 11, regardless of the state of AHIZEN.
2. Set the ENABLE bit high and the DISABLE bit high to place the device in powerdown mode. Note that all register states are maintained so long as V_{IO} is supplied and the \overline{RST} pin is high.
3. (Optional) Remove RCLK.
4. Remove V_A and V_D supplies as needed.

To power up the device (after power down):

1. Note that V_{IO} is still supplied in this scenario. If V_{IO} is not supplied, refer to the device initialization procedure above.
2. (Optional) Set the AHIZEN bit low to disable the dc bias of $0.5 \times V_{IO}$ volts at the LOUT and ROUT pins, but preserve the states of the other bits in Register 07h. Note that in powerup, the LOUT and ROUT pins are set to the common mode voltage specified in Table 8 on page 11, regardless of the state of AHIZEN.
3. Supply V_A and V_D .
4. Provide RCLK. Wait 500 ms for oscillator startup when using internal oscillator.
5. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

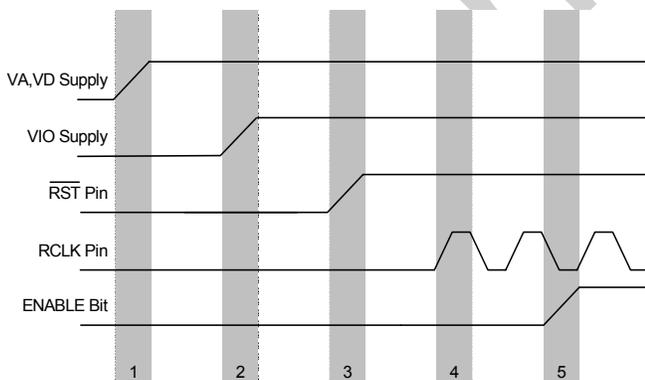


Figure 9. Initialization Sequence

4.11. Programming Guide

Refer to "AN230: Si4700/01 Programming Guide" for control interface programming information.

5. Register Summary

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	DEVICEID	MFGID[11:0]															
01h	CHIPID	PN[3:0]															
02h	POWERCFG	REV[5:0]															
03h	CHANNEL	DEV[3:0]															
04h	SYSCONFIG1	CHAN[9:0]															
05h	SYSCONFIG2	SEEKTH[7:0]															
06h	SYSCONFIG3	SKMNT[3:0]															
07h	TEST1	SKCNTT[3:0]															
08h	TEST2	SKCNTT[3:0]															
09h	BOOTCONFIG	SKCNTT[3:0]															
0Ah	STATUSRSSI	RSSI[7:0]															
0Bh	READCHAN	READCHAN[9:0]															
0Ch	Reserved																
0Dh	Reserved																
0Eh	Reserved																
0Fh	Reserved																

Note: Any register not listed is reserved and should not be written. Writing to reserved registers may result in unpredictable behavior.

6. Register Descriptions

Register 00h. Device ID

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PN[3:0]						MFGID[11:0]									
Type	R						R									

Reset value = 0x1242

Bit	Name	Function
15:12	PN[3:0]	Part Number. 0x01 = Si4702/03
11:0	MFGID[11:0]	Manufacturer ID. 0x242

Register 01h. Chip ID

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REV[5:0]						DEV[3:0]			FIRMWARE[5:0]						
Type	R						R			R						

Reset value = 0x0850 if ENABLE = 1

Reset value = 0x0800 if ENABLE = 0

Bit	Name	Function
15:10	REV[5:0]	Chip Version. 0x02 = Rev B
9:6	DEV[3:0]	Device. 0 before powerup. 0001 after powerup = Si4702. 1001 after powerup = Si4703.
5:0	FIRMWARE[5:0]	Firmware Version. 0 before powerup. Firmware version after powerup = 10.

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Register 02h. Power Configuration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DSMUTE	DMUTE	MONO	0	0	SKMODE	SEEKUP	SEEK	0	DISABLE	0	0	0	0	0	ENABLE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0x0000

Bit	Name	Function
15	DSMUTE	Softmute Disable. 0 = Softmute enable (default). 1 = Softmute disable.
14	DMUTE	Mute Disable. 0 = Mute enable (default). 1 = Mute disable.
13	MONO	Mono Select. 0 = Stereo (default). 1 = Force mono.
12:11	Reserved	Reserved. Always write to 0.
10	SKMODE	Seek Mode. 0 = Wrap at the upper or lower band limit and continue seeking (default). 1 = Stop seeking at the upper or lower band limit.
9	SEEKUP	Seek Direction. 0 = Seek down (default). 1 = Seek up.
8	SEEK	Seek. 0 = Disable (default). 1 = Enable. Notes: <ol style="list-style-type: none"> 1. Seek begins at the current channel and goes in the direction specified with the SEEKUP bit. Seek operation stops when a channel is qualified as valid according to the seek parameters, the entire band has been searched (SKMODE = 0), or the upper or lower band limit has been reached (SKMODE = 1). 2. The STC bit is set high when the seek operation completes and/or the SF/BL bit is set high if the seek operation was unable to find a channel qualified as valid according to the seek parameters. The STC and SF/BL bits must be set low by setting the SEEK bit low before the next seek or tune may begin. 3. Seek performance for 50 kHz channel spacing varies according to RCLK tolerance. Silicon Laboratories recommends ± 50 ppm RCLK crystal tolerance for 50 kHz seek performance. 4. A seek operation may be aborted by setting SEEK = 0.
7	Reserved	Reserved. Always write to 0.

Bit	Name	Function
6	DISABLE	Powerup Disable. Refer to Section 4.8. "Reset, Powerup, and Powerdown" on page 17. Default = 0.
5:1	Reserved	Reserved. Always write to 0.
0	ENABLE	Powerup Enable. Refer to Section "4.8. Reset, Powerup, and Powerdown". Default = 0.

Register 03h. Channel

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TUNE	0	0	0	0	0	CHANNEL[9:0]									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

Reset value = 0x0000

Bit	Name	Function
15	TUNE	Tune. 0 = Disable (default). 1 = Enable. The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The STC bit must be set low by setting the TUNE bit low before the next tune or seek may begin.
14:10	Reserved	Reserved. Always write to 0.
9:0	CHAN[9:0]	Channel Select. Channel value for tune operation. If BAND 05h[7:6] = 00, then Freq (MHz) = Spacing (MHz) x Channel + 87.5 MHz. If BAND 05h[7:6] = 01, BAND 05h[7:6] = 10, then Freq (MHz) = Spacing (MHz) x Channel + 76 MHz. CHAN[9:0] is not updated during a seek operation. READCHAN[9:0] provides the current tuned channel and is updated during a seek operation and after a seek or tune operation completes. Channel spacing is set with the bits SPACE 05h[5:4].

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Register 04h. System Configuration 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	STCIEN	0	0	DE	AGCD	0	0	BLNDADJ[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0x0000

Bit	Name	Function
15	Reserved	Reserved. Always write to 0.
14	STCIEN	Seek/Tune Complete Interrupt Enable. 0 = Disable Interrupt (default). 1 = Enable Interrupt. Setting STCIEN = 1 and GPIO2[1:0] = 01 will generate a 5 ms low pulse on GPIO2 when the STC 0Ah[14] bit is set.
13:12	Reserved	Reserved. Always write to 0.
11	DE	De-emphasis. 0 = 75 μ s. Used in USA (default). 1 = 50 μ s. Used in Europe, Australia, and Japan.
10	AGCD	AGC Disable. 0 = AGC enable (default). 1 = AGC disable.
9:8	Reserved	Reserved. Always write to 0.
6:7	BLNDADJ[1:0]	Stereo/Mono Blend Level Adjustment. Sets the RSSI range for stereo/mono blend. 00 = 31–49 RSSI dB μ V (default). 01 = 37–55 RSSI dB μ V (+6 dB). 10 = 19–37 RSSI dB μ V (–12 dB). 11 = 25–43 RSSI dB μ V (–6 dB). ST bit set for RSSI values greater than low end of range.
5:4	GPIO3[1:0]	General Purpose I/O 3. 00 = High impedance (default). 01 = Mono/Stereo indicator (ST). The GPIO3 will output a logic high when the device is in stereo, otherwise the device will output a logic low for mono. 10 = Low. 11 = High.

Bit	Name	Function
3:2	GPIO2[1:0]	General Purpose I/O 2. 00 = High impedance (default). 01 = STC interrupt. A logic high will be output unless an interrupt occurs as described below. 10 = Low. 11 = High. Setting STCIEN = 1 will generate a 5 ms low pulse on GPIO2 when the STC 0Ah[14] bit is set.
1:0	GPIO1[1:0]	General Purpose I/O 1. 00 = High impedance (default). 01 = Reserved. 10 = Low. 11 = High.

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Register 05h. System Configuration 2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SEEKTH[7:0]							BAND[1:0]		SPACE[1:0]		VOLUME[3:0]				
Type	R/W							R/W		R/W		R/W				

Reset value = 0x0000

Bit	Name	Function
15:8	SEEKTH[7:0]	<p>RSSI Seek Threshold. 0x00 = min RSSI (default). 0x7F = max RSSI. SEEKTH presents the logarithmic RSSI threshold for the seek operation. The Si4702 will not validate channels with RSSI below the SEEKTH value. SEEKTH is one of multiple parameters that can be used to validate channels. For more information, see "AN284: Si4700/01 Firmware 15 Seek Adjustability and Settings."</p>
7:6	BAND[1:0]	<p>Band Select. 00 = 87.5–108 MHz (USA, Europe) (Default). 01 = 76–108 MHz (Japan wide band). 10 = 76–90 MHz (Japan). 11 = Reserved.</p>
5:4	SPACE[1:0]	<p>Channel Spacing. 00 = 200 kHz (USA, Australia) (default). 01 = 100 kHz (Europe, Japan). 10 = 50 kHz.</p>
3:0	VOLUME[3:0]	<p>Volume. Relative value of volume is shifted –30 dBFS with the VOLEXT 06h[8] bit. VOLEXT = 0 (default). 0000 = mute (default). 0001 = –28 dBFS. : : 1110 = –2 dBFS. 1111 = 0 dBFS.</p> <p>VOLEXT = 1. 0000 = mute. 0001 = –58 dBFS. : : 1110 = –32 dBFS. 1111 = –30 dBFS. FS = full scale. Volume scale is logarithmic.</p>

Register 06h. System Configuration 3

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SMUTER[1:0]		SMUTEA[1:0]		0	0	0	VOLEXT	SKSNR[3:0]			SKCNT[3:0]				
Type	R/W		R/W		R/W	R/W	R/W	R/W	R/W			R/W				

Reset value = 0x0000

Bit	Name	Function
15:14	SMUTER[1:0]	Softmute Attack/Recover Rate. 00 = fastest (default) 01 = fast 10 = slow 11 = slowest
13:12	SMUTEA[1:0]	Softmute Attenuation. 00 = 16 dB (default) 01 = 14 dB. 10 = 12 dB. 11 = 10 dB.
11:9	Reserved	Reserved. Always write to zero.
8	VOLEXT	Extended Volume Range. 0 = disabled (default). 1 = enabled. This bit attenuates the output by 30 dB. With the bit set to 0, the 15 volume settings adjust the volume between 0 and –28 dBFS. With the bit set to 1, the 15 volume settings adjust the volume between –30 and –58 dBFS. Refer to 4.4. "Stereo Audio Processing" on page 15. Refer to "AN281: Si4700/01/02/03 Firmware Change List."
7:4	SKSNR[3:0]	Seek SNR Threshold. 0000 = disabled (default). 0001 = min (most stops). 1111 = max (fewest stops). Required channel SNR for a valid seek channel.
3:0	SKCNT[3:0]	Seek FM Impulse Detection Threshold. 0000 = disabled (default). 0001 = max (most stops). 1111 = min (fewest stops). Allowable number of FM impulses for a valid seek channel.

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Register 07h. Test 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	XOSCEN	AHIZEN	Reserved													
Type	R/W	R/W	R/W													

Reset value = 0x0100

Bit	Name	Function
15	XOSCEN	<p>Crystal Oscillator Enable. 0 = Disable (default). 1 = Enable.</p> <p>The internal crystal oscillator requires an external 32.768 kHz crystal as shown in 2. "Typical Application Schematic" on page 13. The oscillator must be enabled before powerup (ENABLE = 1) as shown in Figure 9, "Initialization Sequence," on page 19. It should only be disabled after powerdown (ENABLE = 0). Bits 13:0 of register 07h must be preserved as 0x0100 while in powerdown and as 0x3C04 while in powerup. Refer to Si4702 Internal Crystal Oscillator Errata.</p>
14	AHIZEN	<p>Audio High-Z Enable. 0 = Disable (default). 1 = Enable.</p> <p>Setting AHIZEN maintains a dc bias of $0.5 \times V_{IO}$ on the LOUT and ROUT pins to prevent the ESD diodes from clamping to the V_{IO} or GND rail in response to the output swing of another device. Register 07h containing the AHIZEN bit must not be written during the powerup sequence, and high-Z only takes effect when in powerdown and V_{IO} is supplied. Bits 13:0 of register 07h must be preserved as 0x0100 while in powerdown and as 0x3C04 while in powerup.</p>
13:0	Reserved	<p>Reserved. If written, these bits should be read first and then written with their pre-existing values. Do not write during powerup.</p>

Register 08h. Test 2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved															
Type	R/W															

Reset value = 0x0000

Bit	Name	Function
15:0	Reserved	Reserved. If written, these bits should be read first and then written with their pre-existing values. Do not write during powerup.

Register 09h. Boot Configuration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved															
Type	R/W															

Reset value = 0x0000

Bit	Name	Function
15:0	Reserved	Reserved. If written, these bits should be read first and then written with their pre-existing values. Do not write during powerup.

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Register 0Ah. Status RSSI

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	STC	SF/BL	AFCRL	0			ST	RSSI[7:0]							
Type	R	R	R	R	R	R	R	R	R							

Reset value = 0x0000

Bit	Name	Function
15	Reserved	Reserved. Always write to zero.
14	STC	Seek/Tune Complete. 0 = Not complete (default). 1 = Complete. The seek/tune complete flag is set when the seek or tune operation completes. Setting the SEEK 02h[8] or TUNE 03h[15] bit low will clear STC.
13	SF/BL	Seek Fail/Band Limit. 0 = Seek successful. 1 = Seek failure/Band limit reached. The SF/BL flag is set high when SKMODE 02h[10] = 0 and the seek operation fails to find a channel qualified as valid according to the seek parameters. The SF/BL flag is set high when SKMODE 02h[10] = 1 and the upper or lower band limit has been reached. The SEEK 02h[8] bit must be set low to clear SF/BL.
12	AFCRL	AFC Rail. 0 = AFC not railed. 1 = AFC railed, indicating an invalid channel. Audio output is softmuted when set. AFCRL is updated after a tune or seek operation completes and indicates a valid or invalid channel. During normal operation, AFCRL is updated to reflect changing RF environments.
11	Reserved	Reserved. Always write to zero.
10:9	Reserved	Reserved. If written, these bits should be read first and then written with their pre-existing values. Do not write during powerup.
8	ST	Stereo Indicator. 0 = Mono. 1 = Stereo. Stereo indication is also available on GPIO3 by setting GPIO3 04h[5:4] = 01.
7:0	RSSI[7:0]	RSSI (Received Signal Strength Indicator). RSSI is measured units of dBμV in 1 dB increments with a maximum of approximately 75 dBμV. Si4702-B16 does not report RSSI levels greater than 75 dBuV.

Register 0Bh. Read Channel

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name							READCHAN[9:0]									
Type	R	R	R	R	R	R	R									

Reset value = 0x0000

Bit	Name	Function
15:10	Reserved	Reserved. If written, these bits should be read first and then written with their pre-existing values. Do not write during powerup.
9:0	READCHAN[9:0]	Read Channel. If BAND 05h[7:6] = 00, then Freq (MHz) = Spacing (MHz) x Channel + 87.5 MHz. If BAND 05h[7:6] = 01, BAND 05h[7:6] = 10, then Freq (MHz) = Spacing (MHz) x Channel + 76 MHz. READCHAN[9:0] provides the current tuned channel and is updated during a seek operation and after a seek or tune operation completes. Spacing and channel are set with the bits, SPACE 05h[5:4] and CHAN 03h[9:0].

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Register 0Ch. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset value = 0x0000

Bit	Name	Function
15:0	Reserved	

Register 0Dh. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset value = 0x0000

Bit	Name	Function
15:0	Reserved	

Register 0Eh. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset value = 0x0000

Bit	Name	Function
15:0	Reserved	

Register 0Fh. Reserved

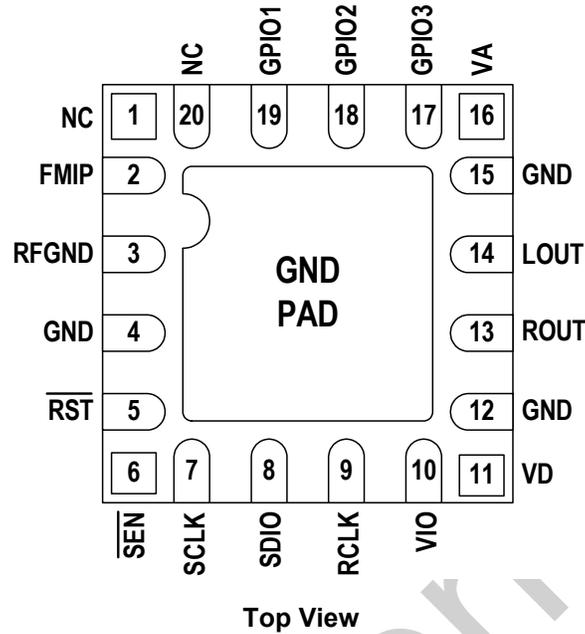
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset value = 0x0000

Bit	Name	Function
15:0	Reserved	

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7. Pin Descriptions: Si4702-GM



Pin Number(s)	Name	Description
1, 20	NC	No Connect. Leave floating.
2	FMIP	FM RF inputs.
3	RFGND	RF ground. Connect to ground plane on PCB.
4, 12, 15, PAD	GND	Ground. Connect to ground plane on PCB.
5	$\overline{\text{RST}}$	Device reset (active low) input.
6	$\overline{\text{SEN}}$	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	V_{IO}	I/O supply voltage.
11	V_{D}	Digital supply voltage. May be connected directly to battery.
13	ROUT	Right audio output.
14	LOUT	Left audio output.
16	V_{A}	Analog supply voltage. May be connected directly to battery.
17, 18, 19	GPIO3, GPIO2, GPIO1	General purpose input/output.

8. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4702-B16-GM	Portable Broadcast Radio Tuner FM Stereo Firmware Revision 16	QFN Pb-free	-20 to 85 °C

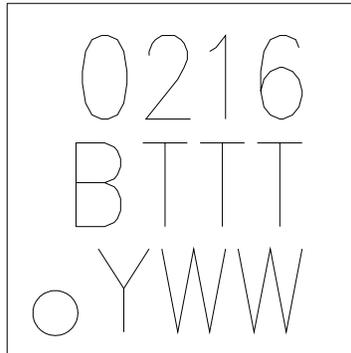
***Note:** Add an "(R)" at the end of the device part number to denote tape and reel option; 2500 quantity per reel.

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9. Package Markings (Top Marks)

9.1. Si4702 Top Mark



9.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	02 = Si4702
	Firmware Revision	16 = Firmware Revision 16
Line 2 Marking:	R = Die Revision	B = Revision B Die
	TTT = Internal Code	Internal tracking code.
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

10. Package Outline: Si4702-GM

Figure 10 illustrates the package details for the Si4702-GM. Table 10 lists the values for the dimensions shown in the illustration.

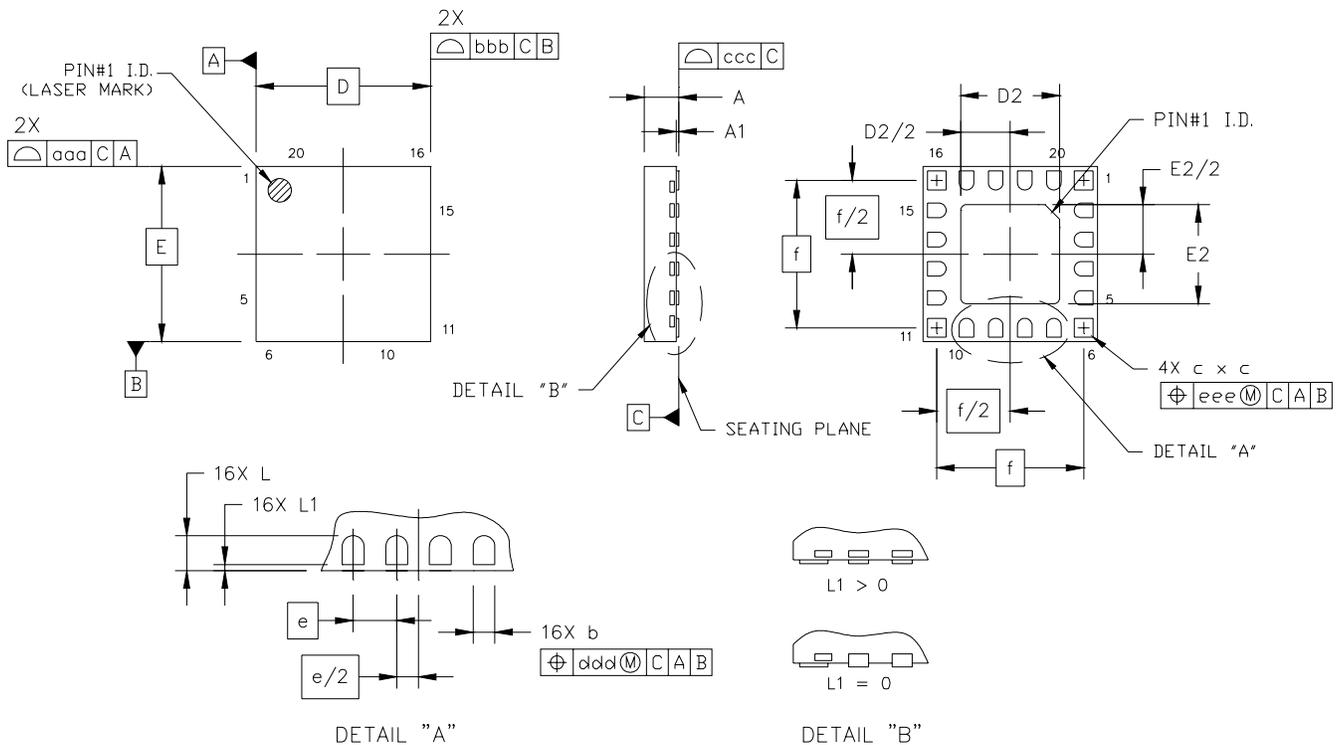


Figure 10. 20-Pin Quad Flat No-Lead (QFN)

Table 10. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.27	0.32	0.37
D	3.00 BSC		
D2	1.65	1.70	1.75
e	0.50 BSC		
E	3.00 BSC		
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f	2.53 BSC		
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

11. PCB Land Pattern: Si4702-GM

Figure 11 illustrates the PCB land pattern details for the Si4702-GM. Table 11 lists the values for the dimensions shown in the illustration.

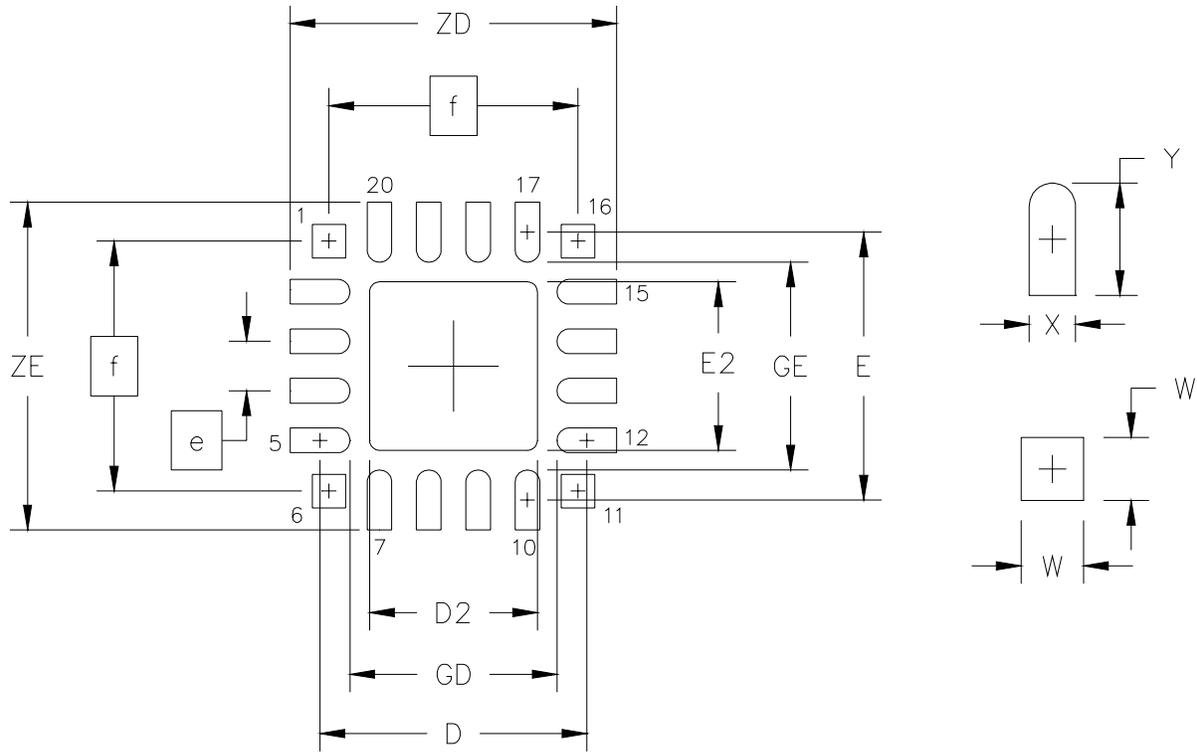


Figure 11. PCB Land Pattern

Table 11. PCB Land Pattern Dimensions

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
D	2.71 REF		GE	2.10	—
D2	1.60	1.80	W	—	0.34
e	0.50 BSC		X	—	0.28
E	2.71 REF		Y	0.61 REF	
E2	1.60	1.80	ZE	—	3.31
f	2.53 BSC		ZD	—	3.31
GD	2.10	—			

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component standoff.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

12. Additional Reference Resources

- AN230: Si4700/01/02/03 Programming Guide
- AN231: Si4700/01/02/03 Headphone and Antenna Interface
- Si4700/01/02/03 EVB User's Guide
- AN234: Si4700/01/02/03 EVB Test Procedure
- AN235: Si4700/01/02/03 EVB Quick Start Guide
- AN281: Si4700/01/02/03 Firmware Change List
- AN284: Si4700/01/02/03 Seek Adjustability and Settings
- AN299: External 32.768 kHz Crystal Oscillator
- Si4702/03 Internal Crystal Oscillator Errata
- Si4700/01/02/03 Customer Support Site: <http://www.mysilabs.com>

This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, register at <http://www.mysilabs.com> and send user's first and last name, company, NDA reference number, and mysilabs user name to fminfo@silabs.com. Silicon Labs recommends an all-lowercase user name.

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DOCUMENT CHANGE LIST

Revision 0.5 to Revision 0.6

- This data sheet is for revision B silicon, firmware revision 15.
- Added PCB land pattern.

Revision 0.6 to Revision 0.61

- Updated to reflect Firmware 15 changes in all text and tables.
- Updated Table 6, "3-Wire Control Interface Characteristics," on page 8 with additional timing parameter for t_{HSEN2} .
- Updated Table 8. "FM Receiver Characteristics" on page 11.
- Updated various texts in "4. Functional Description".
- Updated Table 9, "Selecting 2-Wire or 3-Wire Control Interface Busmode Operation^{1,2,3}," on page 18 to show conditional on rising edge of \overline{RST} .
- Updated "6. Register Descriptions" for clarity.
- Added Blend level adjustments.
- Added Volume scale steps.

Revision 0.61 to Revision 0.7

- Updated to reflect Firmware 16 changes in all text and tables.
- Updated Table 8, "FM Receiver Characteristics^{1,2}," on page 11.
- Updated 2. "Typical Application Schematic" on page 13.
- Updated 4. "Functional Description" on page 14.
- Updated 5. "Register Summary" on page 20.
- Updated 6. "Register Descriptions" on page 21.
- Updated 9. "Package Markings (Top Marks)" on page 36.
- Updated 10. "Package Outline: Si4702-GM" on page 37.
- Updated 11. "PCB Land Pattern: Si4702-GM" on page 38.
- Added additional reference resources to Section 12.

Revision 0.7 to Revision 0.71

- Updated "Table 8. FM Receiver Characteristics^{1,2}" on page 11.

Revision 0.71 to Revision 0.8

- Updated Table 3 on page 5.
- Updated Register 7, "Test 1," on page 28.
- Updated Table 8 on page 11.

- Updated 4.5. "Tuning" on page 15.
- Updated 4.8. "Reset, Powerup, and Powerdown" on page 17.

Revision 0.8 to Revision 1.0

- Updated data sheet with Si4702-specific information.
- Updated Table 3 on page 5.
- Updated Table 8 on page 11.
- Updated Sections 4, 5, 8, 9, 10, and 11.
 - Removed references to Si4703.

Revision 1.0 to Revision 1.1

- Updated Table 1, "Recommended Operating Conditions," on page 4.
- Updated Table 3, "DC Characteristics," on page 5.
- Changed table 4 into two separate tables: Table 4, "Reset Timing Characteristics (Busmode Select Method 1)^{1,2,3}," on page 6 and Table 5, "Reset Timing Characteristics (Busmode Select Method 2)^{1,2,3}," on page 7, along with Figure 1 and Figure 2.
- Updated Figure 1, "Reset Timing Parameters for Busmode Select Method 1 (GPIO3 = 0)," on page 6.
 - Corrected diagram of t_{SRST1} .
- Updated Table 7, "2-Wire Control Interface Characteristics^{1,2,3}," on page 9.
 - Corrected typographical error on $t_{f:out}$ and $t_{f:in}$, $t_{r:in}$.
 - Updated table note.
- Updated Table 8, "FM Receiver Characteristics^{1,2}," on page 11.
- Corrected typographical error in 4.5. "Tuning" on page 15.
- Updated 4.6. "Reference Clock" on page 16.
- Updated 4.7. "Control Interface" on page 17.
- Updated 4.8. "Reset, Powerup, and Powerdown" on page 17.
- Updated notes in Table 9, "Selecting 2-Wire or 3-Wire Control Interface Busmode Operation^{1,2,3}," on page 18.
- Updated Register 1, "Chip ID," on page 21.
 - Corrected typographical error.
 - Corrected reset value information.
- Updated Register 5, "System Configuration 2," on page 26.
 - Corrected typographical error.
 - Corrected max RSSI seek threshold value for $SEEKTH[7:0]$.

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