



Integrated Device Technology, Inc.

3.3V CMOS STATIC RAM 1 MEG (64K x 16-BIT)

IDT71V016SA

FEATURES:

- 64K x 16 advanced high-speed CMOS Static RAM
- Equal access and cycle times
— 10/12/15/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Upper and Lower Byte Enable Pins
- Single 3.3V power supply
- Available in 44-pin Plastic SOJ and 44-pin TSOP package and 48-BALL Plastic FBGA

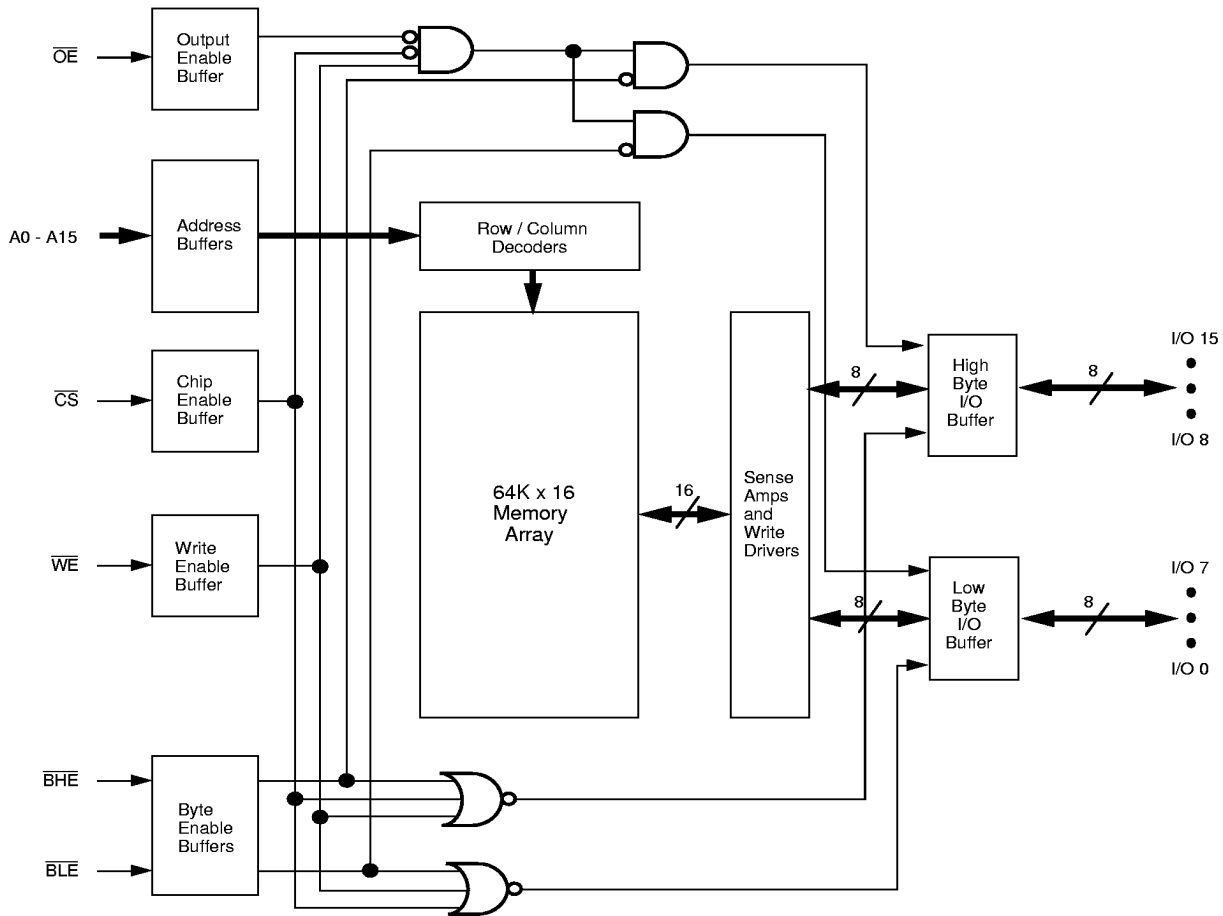
The IDT71V016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V016 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V016 are TTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V016 is packaged in a JEDEC standard 44-pin Plastic SOJ, a 44-pin TSOP Type II and a 48-BALL 7 x 7 mm Plastic FBGA .

DESCRIPTION:

FUNCTIONAL BLOCK DIAGRAM



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3834 drw 01

COMMERCIAL TEMPERATURE RANGE

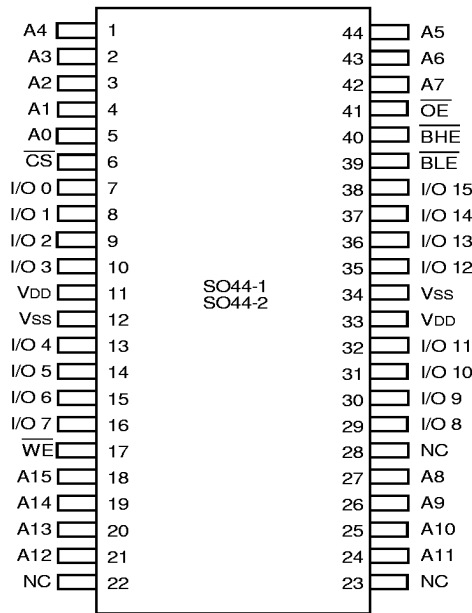
MAY 1999

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DSC-3834/02

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PIN CONFIGURATIONS



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**SOJ/TSOP
TOP VIEW**

	1	2	3	4	5	6
A	$\overline{\text{BLE}}$	$\overline{\text{OE}}$	A	A	A	NC
B	I/OH	$\overline{\text{BHE}}$	A	A	$\overline{\text{CS}}$	I/OL
C	I/OH	I/OH	A	A	I/OL	I/OL
D	VSS	I/OH	NC	A	I/OL	VDD
E	VDD	I/OH	NC	NC	I/OL	VSS
F	I/OH	I/OH	A	A	I/OL	I/OL
G	I/OH	NC	A	A	$\overline{\text{WE}}$	I/OL
H	NC	A	A	A	A	NC

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**FBGA
TOP VIEW**

PIN DESCRIPTIONS

A ₀ – A ₁₅	Address Inputs	Input
$\overline{\text{CS}}$	Chip Select	Input
$\overline{\text{WE}}$	Write Enable	Input
$\overline{\text{OE}}$	Output Enable	Input
$\overline{\text{BHE}}$	High Byte Enable	Input
$\overline{\text{BLE}}$	Low Byte Enable	Input
I/O ₀ - I/O ₁₅	Data Input/Output	I/O
VDD	3.3V Power	Pwr
Vss	Ground	Gnd

3834 tbl 01

TRUTH TABLE⁽¹⁾

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Function
H	X	X	X	X	High-Z	High-Z	Deselected - Standby
L	L	H	L	H	DATAOUT	High-Z	Low Byte Read
L	L	H	H	L	High-Z	DATAOUT	High Byte Read
L	L	H	L	L	DATAOUT	DATAOUT	Word Read
L	X	L	L	L	DATAIN	DATAIN	Word Write
L	X	L	L	H	DATAIN	High-Z	Low Byte Write
L	X	L	H	L	High-Z	DATAIN	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

NOTE:

1.H = V_{IH}, L = V_{IL}, X = Don't care.

3834 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VDD	Supply Voltage Relative to VSS	-0.5 to +4.6	V
VIN, VOUT	Terminal Voltage Relative to VSS	-0.5 to VDD+0.5	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.25	W
IOUT	DC Output Current	50	mA

NOTES:

3834 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	VSS	VDD
Commercial	0°C to +70°C	0V	See Below

3834 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD ⁽¹⁾	Supply Voltage	3.15	3.3	3.6	V
VDD ⁽²⁾	Supply Voltage	3.0	3.3	3.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.0	—	VDD+0.3 ⁽³⁾	V
VIL	Input Low Voltage	-0.3 ⁽⁴⁾	—	0.8	V

NOTE:

3834 tbl 05

- For 71V016SA10 only.
- For all speed grades except 71V016SA10.
- VIH (max.) = VDD+2V for pulse width less than 5ns, once per cycle.
- VIL (min.) = -2V for pulse width less than 5ns, once per cycle.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
CIO	I/O Capacitance	VOUT = 3dV	7	pF

NOTE:

3834 tbl 06

- This parameter is guaranteed by device characterization, but not production tested.

DC ELECTRICAL CHARACTERISTICS

VDD = Min. to Max., Commercial Temperature Range

Symbol	Parameter	Test Condition	IDT71V016SA		Unit
			Min.	Max.	
ILI	Input Leakage Current	VDD = Max., VIN = VSS to VDD	—	5	μA
ILO	Output Leakage Current	VDD = Max., CS = VIH, VOUT = VSS to VDD	—	5	μA
VOL	Output Low Voltage	IOL = 8mA, VDD = Min.	—	0.4	V
VOH	Output High Voltage	I OH = -4mA, VDD = Min.	2.4	—	V

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DC ELECTRICAL CHARACTERISTICS^(1, 2)

(VDD = Min. to Max., VLC = 0.2V, VHC = VDD - 0.2V)

Symbol	Parameter	71V016SA10	71V016SA12	71V016SA15	71V016SA20	Unit
Icc	Dynamic Operating Current CS ≤ VLC, Outputs Open, VDD = Max., f = fMAX ⁽³⁾	170	160	150	140	mA
ISB	Dynamic Standby Power Supply Current CS ≥ VHC, Outputs Open, VDD = Max., f = fMAX ⁽³⁾	45	40	40	40	mA
ISB1	Full Standby Power Supply Current (static) CS ≥ VHC, Outputs Open, VDD = Max., f = 0 ⁽³⁾	10	10	10	10	mA

NOTES:

3834 tbl 08

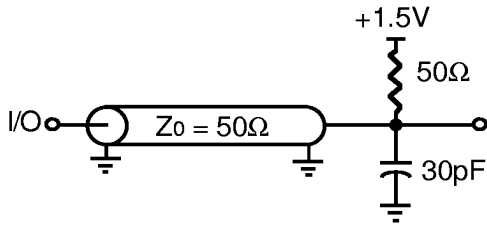
- All values are maximum guaranteed values.
- All inputs switch between 0.2V (Low) and VDD - 0.2V (High).
- fMAX = 1/TRC (all address inputs are cycling at fMAX); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

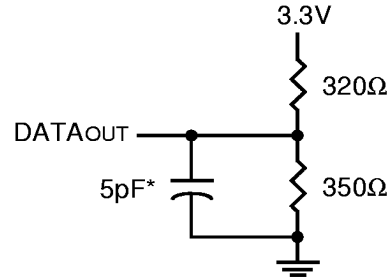
3834 tbl 09

AC TEST LOADS



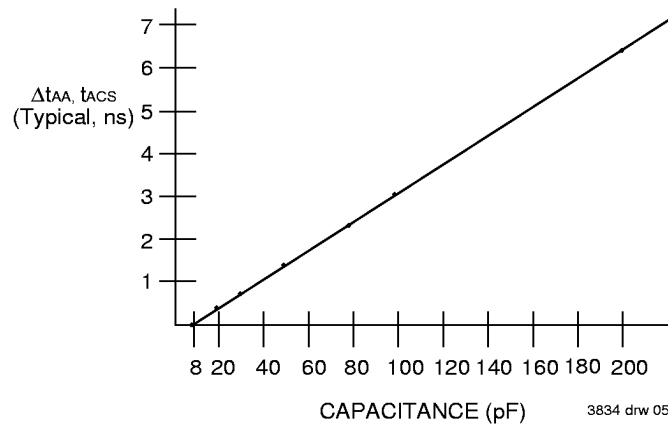
3834 drw 03

Figure 1. AC Test Load



3834 drw 04

Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)
*Including jig and scope capacitance.



3834 drw 05

Figure 3. Output Capacitive Derating

AC ELECTRICAL CHARACTERISTICS (V_{DD} = Min. to Max., Commercial Temperature Range)

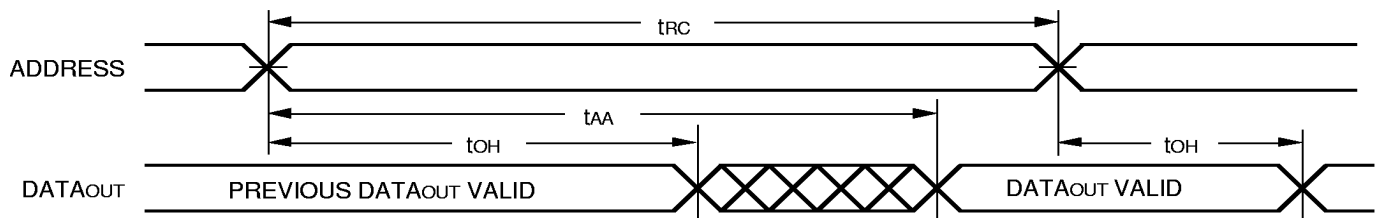
Symbol	Parameter	71V016SA10		71V016SA12		71V016SA15		71V016SA20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t _{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t _{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t _{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
t _{CLZ} ⁽¹⁾	Chip Select Low to Output in Low-Z	4	—	4	—	4	—	4	—	ns
t _{CHZ} ⁽¹⁾	Chip Select High to Output in High-Z	—	5	—	6	—	7	—	8	ns
t _{OE}	Output Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t _{OLZ} ⁽¹⁾	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t _{OHZ} ⁽¹⁾	Output Enable High to Output in High-Z	—	5	—	6	—	7	—	8	ns
t _{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t _{BE}	Byte Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t _{BLZ} ⁽¹⁾	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t _{BHZ} ⁽¹⁾	Byte Enable High to Output in High-Z	—	5	—	6	—	7	—	8	ns
Write C										
t _{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t _{AW}	Address Valid to End of Write	7	—	8	—	10	—	12	—	ns
t _{CW}	Chip Select Low to End of Write	7	—	8	—	10	—	12	—	ns
t _{BW}	Byte Enable Low to End of Write	7	—	8	—	10	—	12	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t _{WR}	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	7	—	8	—	10	—	12	—	ns
t _{DW}	Data Valid to End of Write	5	—	6	—	7	—	9	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t _{OW} ⁽¹⁾	Write Enable High to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t _{WHZ} ⁽¹⁾	Write Enable Low to Output in High-Z	—	5	—	6	—	7	—	8	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3834 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1^(1,2,3)

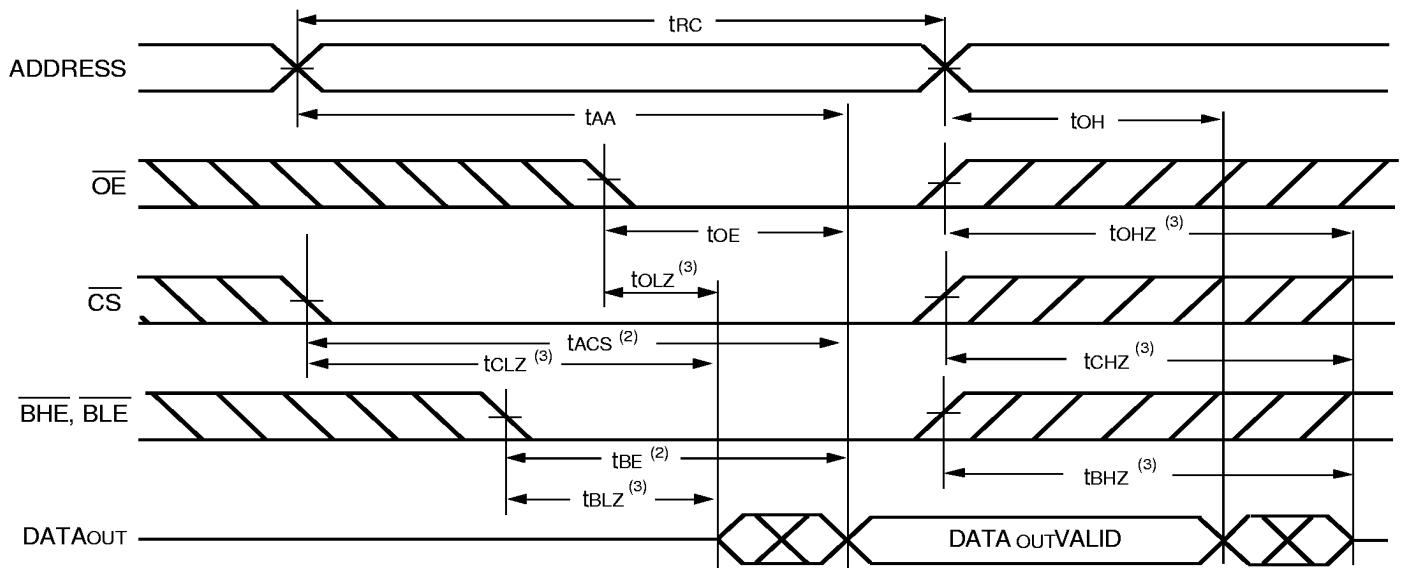


3834 drw 06

NOTES:

1. WE is HIGH for Read Cycle.
2. Device is continuously selected, CS is LOW.
3. OE, BHE, and BLE are LOW.

TIMING WAVEFORM OF READ CYCLE NO. 2⁽¹⁾

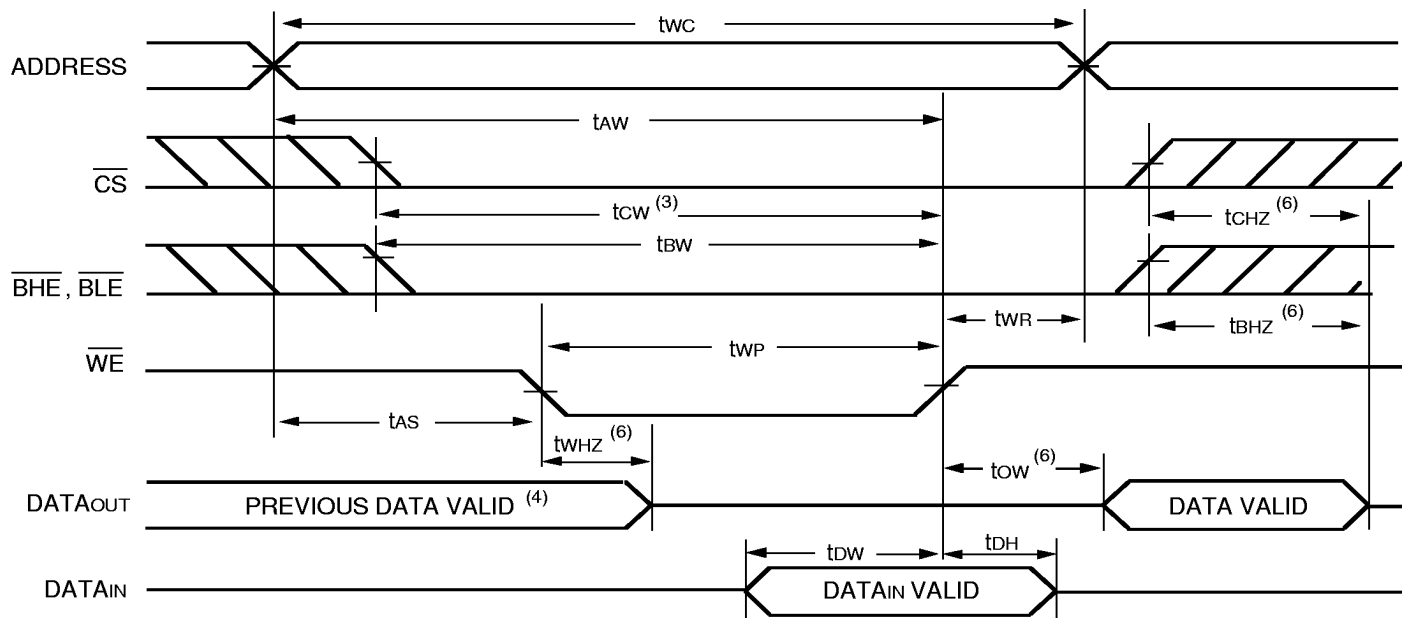


3834 drw 07

NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of \overline{CS} , \overline{BHE} , or \overline{BLE} transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1,2,4)

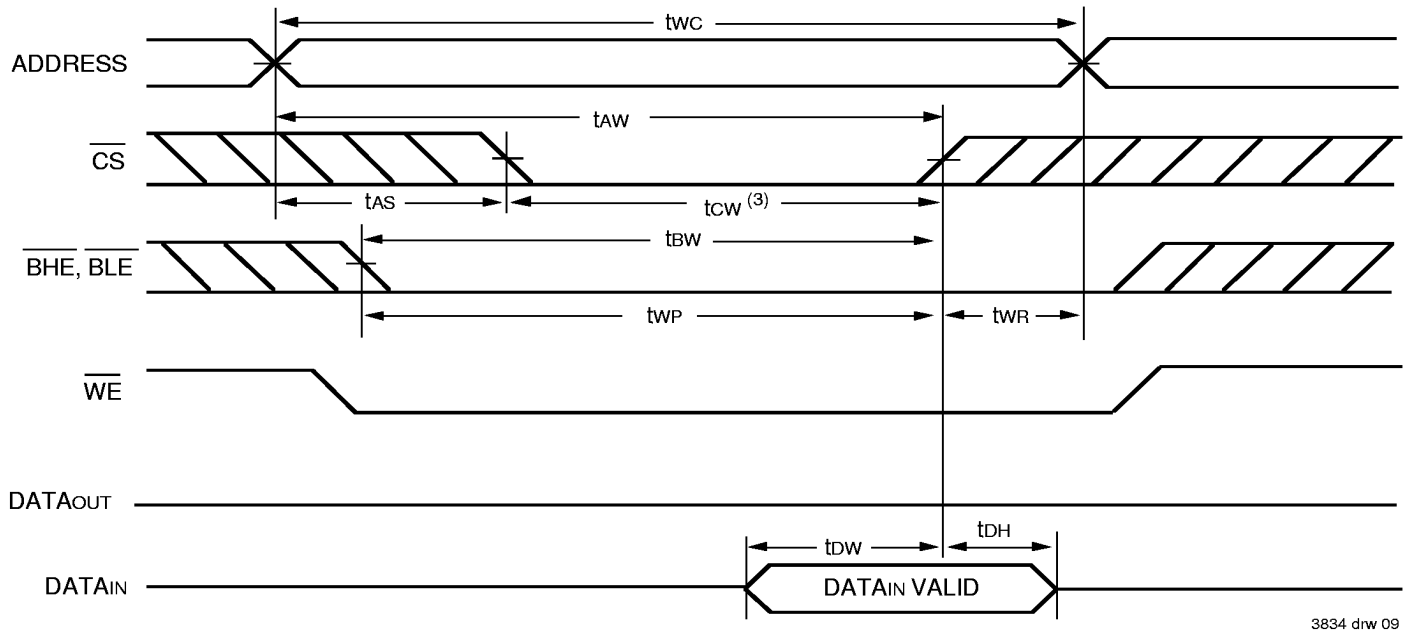


3834 drw 08

NOTES:

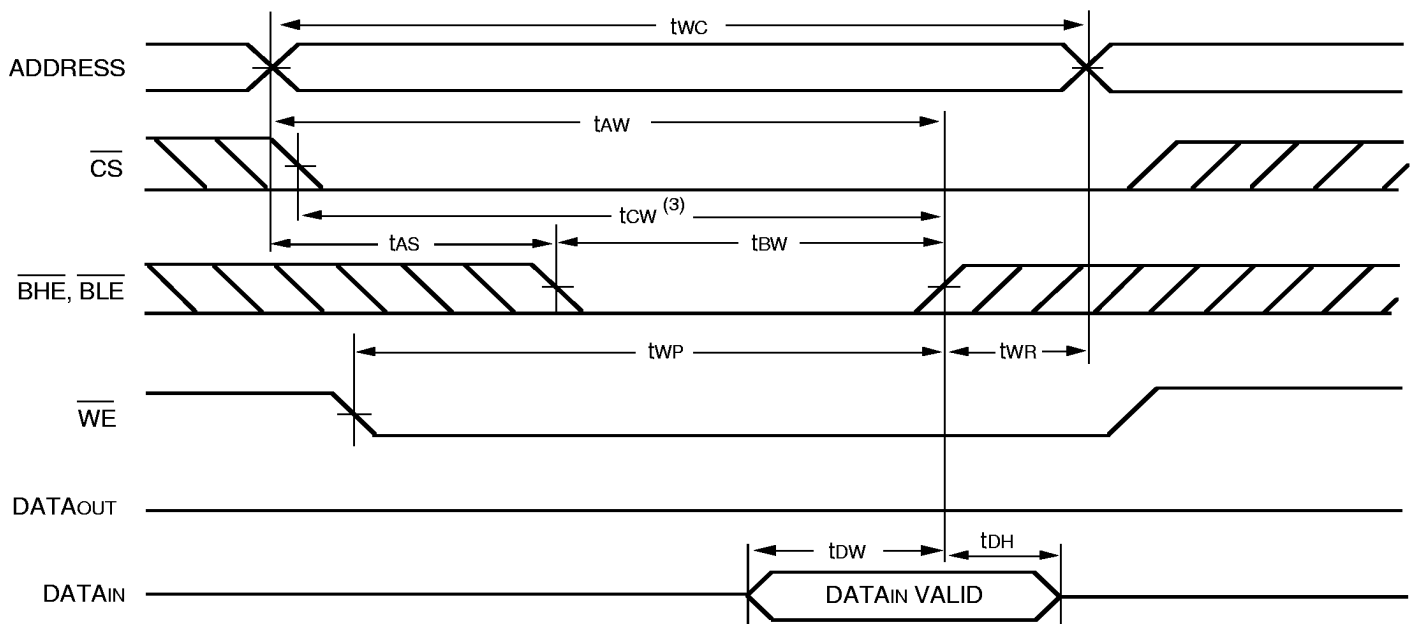
1. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the \overline{CS} LOW or \overline{BHE} and \overline{BLE} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1,4)



3834 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 3 (\overline{BHE} , \overline{BLE} CONTROLLED TIMING)^(1,4)

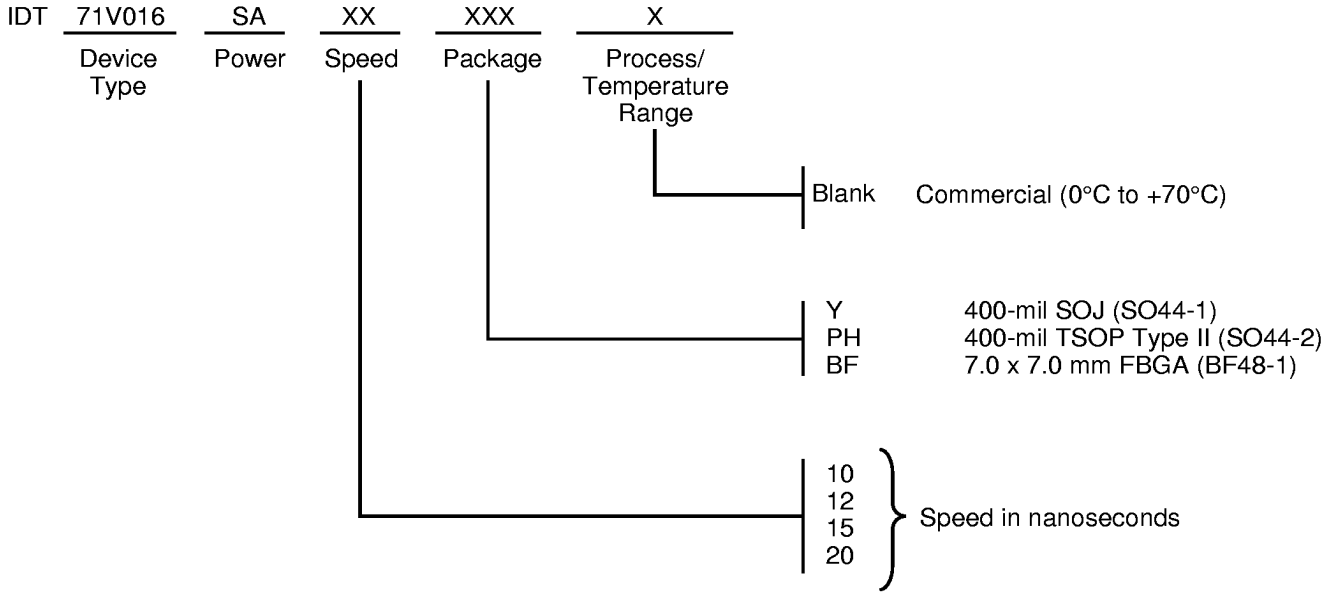


3834 drw 10

NOTES:

1. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the \overline{CS} LOW or \overline{BHE} and \overline{BLE} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

ORDERING INFORMATION



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