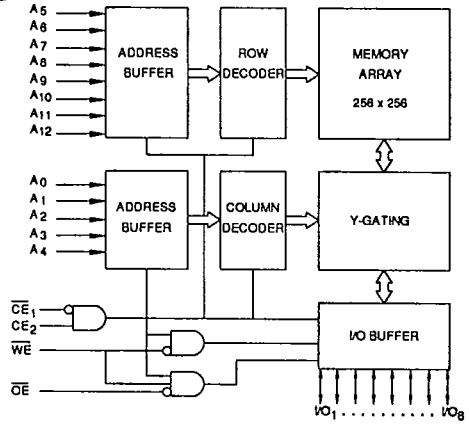
AT38LV64

T-46-23-12

Features

- Fast Read Access Time - 200ns
- Low Power
  - 110mW Maximum (Active) at Vcc = 3.0V
  - 100µW Maximum (Standby)
- 2V Data Retention
- Fully Static: No Clock Required
- Three Control Inputs ($\overline{CE_1}$, CE_2, and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 3.0V to 5.5V Supply
- 28 Lead Dual In-line and Surface Mount Packages
- JEDEC Pinout
- Commercial Temperature Range

Block Diagram



Description

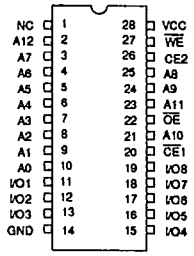
The AT38LV64 is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT38LV64 offers an access time of 200ns with power dissipation of under 110mW at 3 volts. When the AT38LV64 is deselected, the standby current is just 100µA. In addition, the AT38LV64 offers a data retention capability of only 100µW power dissipation when operated on a 2V power supply.

The AT38LV64 powers down to the standby mode when deselected ($\overline{CE_1}$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE_1}$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT38LV64 is completely TTL compatible and requires a single 3V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

Pin Name	Function
A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE_1}$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc, GND	Power, Ground
NC	No Connect



64K (8K x 8) Low Voltage CMOS SRAM

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Absolute Maximum Ratings*

Temperature Under Bias	0° C to 70° C
Storage Temperature	-55° C to 125° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3V to V_{CC}+0.3V
All Output Voltages with Respect to Ground	-0.3V to V_{CC}+0.3V
Maximum Supply Voltage	+7.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the 8 bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the 8 bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as 2 volts without impacting data integrity. Power dissipation will be reduced to 100 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X(1)	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT38LV64-20
Operating Temperature (Case)	Commercial	0°C - 70°C
Vcc Power Supply		3.0V to 5.5V

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D.C. and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN}=0 to Vcc	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2V to Vcc + 0.3V or CE_2 = -0.3V to 0.8V or $\overline{OE}$ = 2.2V to Vcc + 0.3V or $\overline{WE}$ = -0.3V to 0.8V $V_{I/O}$ = 0 to Vcc	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2V$ or $\overline{CE_1} \ge V_{CC}$ - 0.2V, $CE_2 \ge V_{CC}$ - 0.2V or $CE_2 \le 0.2V$ V_{IN} = 0 to Vcc		2	100	µA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3V to 0.8V or $\overline{CE_1}$ = 2.2V to Vcc +0.3V, V_{IN} = 0 to Vcc			3	mA
I_{CC}	Vcc Active Current (TTL)	$\overline{CE_1}$ = -0.3V to 0.8V, CE_2 = 2.2V to Vcc + 0.3V, I_{OUT} = 0mA, min cycle		20	35	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2V		Vcc+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	2.4			V

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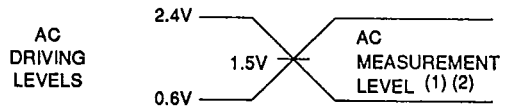
Pin Capacitance (f=1MHz T=25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5ns.
2. Output load: 1TTL gate + 100pF.

A.C. Characteristics for Read

Symbol	Parameter	AT38LV64-20 Min	AT38LV64-20 Max	Units
t_{RC}	Read Cycle Time	200		ns
t_{ACC}	Address Access Time		200	ns
$t_{\overline{CE}1}$,t_{CE2}	$\overline{CE}_1$,CE_2 Access Time		200	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		80	ns
t_{OH}	Output Hold Time	15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		80	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		80	ns

A.C. Characteristics for Write

Symbol	Parameter	AT38LV64-20 Min	AT38LV64-20 Max	Units
t_{WC}	Write Cycle Time	200		ns
t_{AS}	Address Setup Time			ns
t_{WP}	Write Pulse Width	100		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	100		ns
t_{WR}	Write Recovery Time	25		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	25		ns
t_{DS}	Data Setup Time	90		ns
t_{DH}	Data Hold Time			ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		80	ns

A.C. Waveforms for Read Cycle [1]

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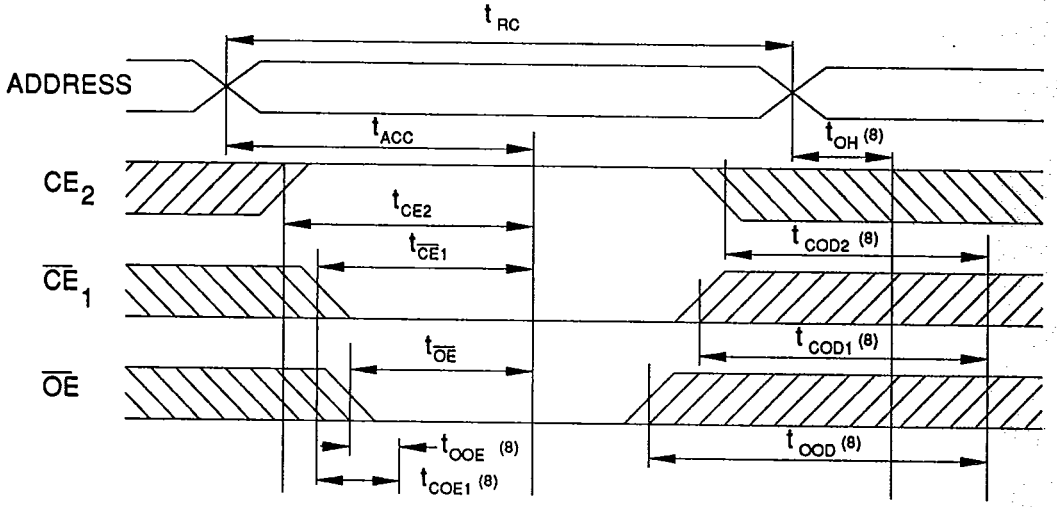
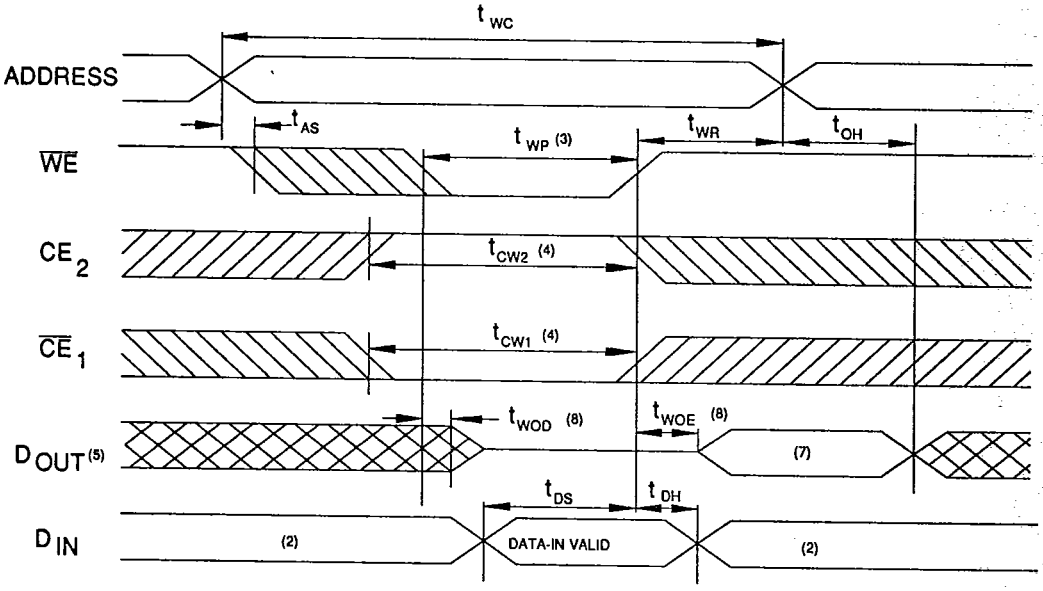


A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



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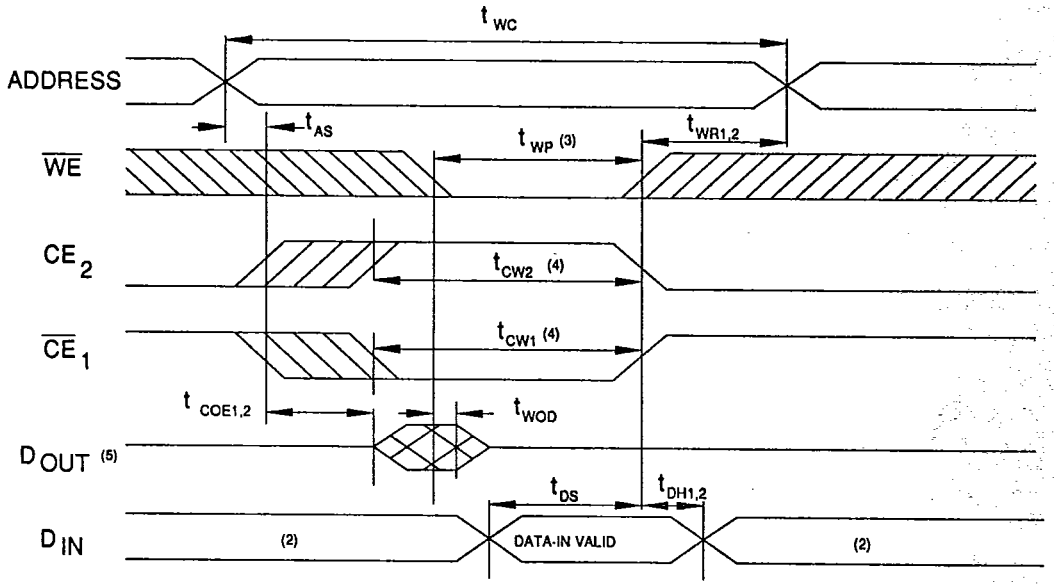
A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) (6)



Notes:

1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE}_1$, CE_2 and $\overline{WE}$ are all active at the same time.
   A Write begins at the latest transition among $\overline{CE}_1$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE}_1$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE}_1$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE}_1$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}=V_{IH}$ or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

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Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Power Supply Voltage	VDR1	$\overline{CE_1} \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$ - 0.2V or $CE_2 \leq 0.2V$	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2V$	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V $\overline{CE_1} \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$-0.2V or $CE_2 \leq 0.2V$		1	50	µA
	I_{CCDR2}	V_{CC} = 3.0V, $CE_2 \leq 0.2V$		1	50	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

Note: 1. t_{RC}=Read Cycle Time

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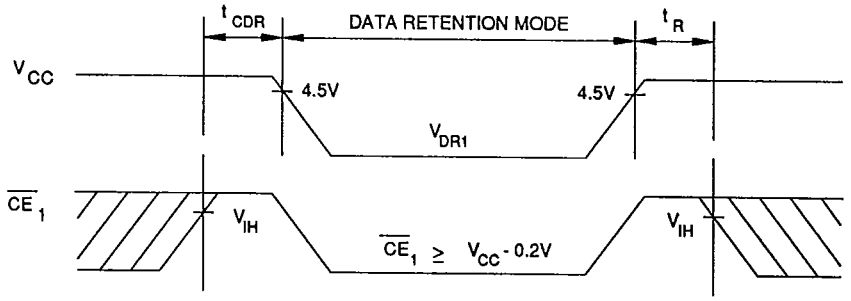
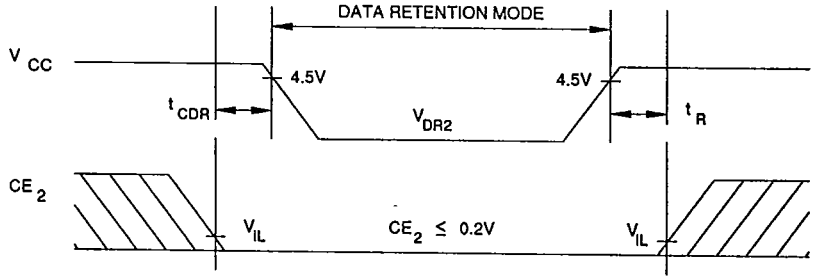
Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE_2 Control)



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Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	35	0.1	AT38LV64L-20PC AT38LV64L-20RC	28P6 28R	Commercial (0° to 70°C)

Package Type	
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28 Lead, 0.330" Wide Plastic Gull Wing Small Outline (SOIC)