AN1488
APPLICATION NOTE

STLC1 LED CLUSTER LAMP DRIVER

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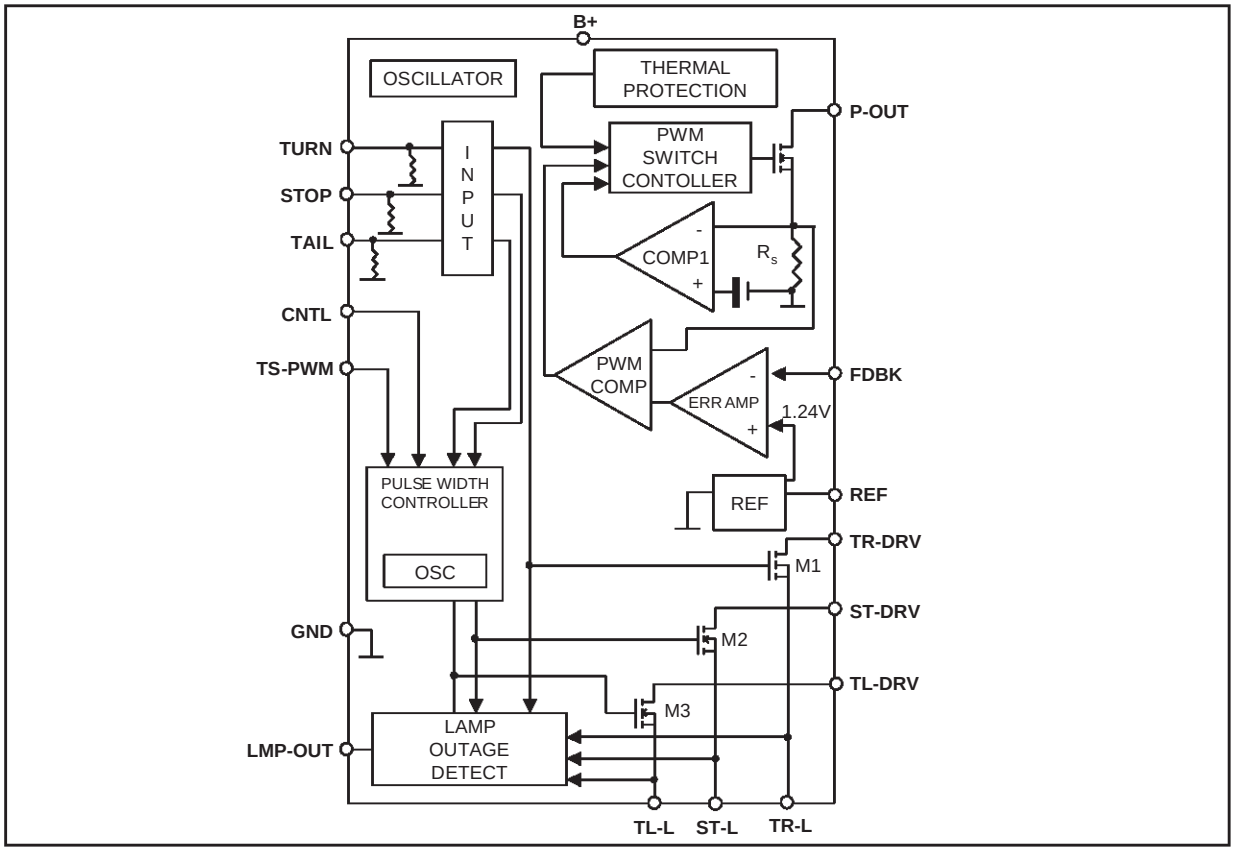
1. ABSTRACT

Nowadays, many applications, such as automotive exterior and interior lights, display and signage lighting and incandescent bulbs, are going to be replaced more and more by LED lamps. This is due to a number of advantages that make the use of this kind of lighting very attractive. Above all, LEDs have an almost unlimited working life, as well as a smaller size and better efficiency, when compared to their incandescent counterparts. Moreover, LEDs have an extremely fast response. They do not require a warm up phase like conventional bulbs do (about 200ms). This ensures added safety especially when used for stoplights. The objective of this application note is to provide a complete explaination of how the STLC1, a monolithic device, is able to drive up to three LED lamps clusters at the same time.

2. GENERAL DEVICE DESCRIPTION.

Figure 1: STLC1 Internal Block Diagram



STLC1 is basically a fixed frequency fully monolithic switching regulator primarily intended for buck-boost and SEPIC (Single Ended Primary Inductor Current) configurations, with three independent smart low side drivers (LSDs), control logic for monitoring lamp fault conditions. It also has a thermal shutdown protection with hysteresis to prevent device overheating. Figure 1 shows the internal block diagram. The STLC1 operates at an internally fixed switching frequency of about 180kHz allowing the user to minimize the number of external components and also allowing smaller sized filter components than what would be needed with a lower frequency switching regulator. The PWM controller has an internal current mode control scheme and the converter's output voltage regulation can be achieved with a simple resistive divider network. The cycle-by-cycle current limitation, the programmable output over-current protection and the device input over-voltage protections give easy and robust design solutions.

3. PIN CONNECTIONS AND DESCRIPTIONS.

STLC1 is housed in a PowerSO-20™ package for SMD assembly. Device pin out is reported in figure 2 and table 1 briefly summarizes the device pin functionality.

Figure 2: STLC1 Device Pinout

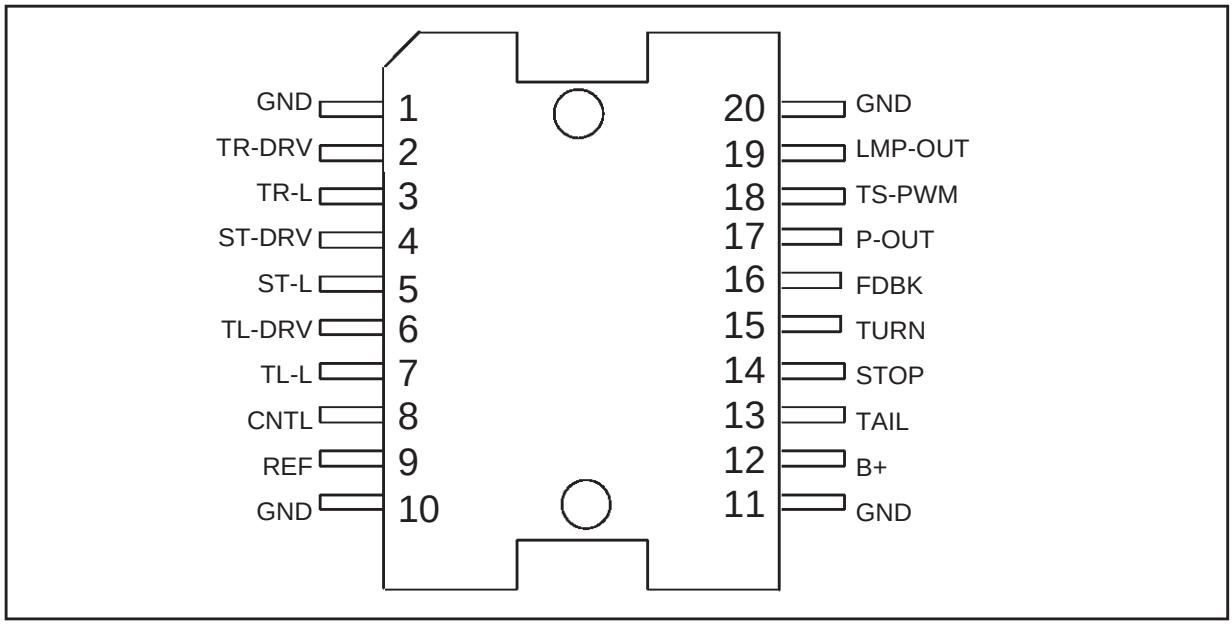


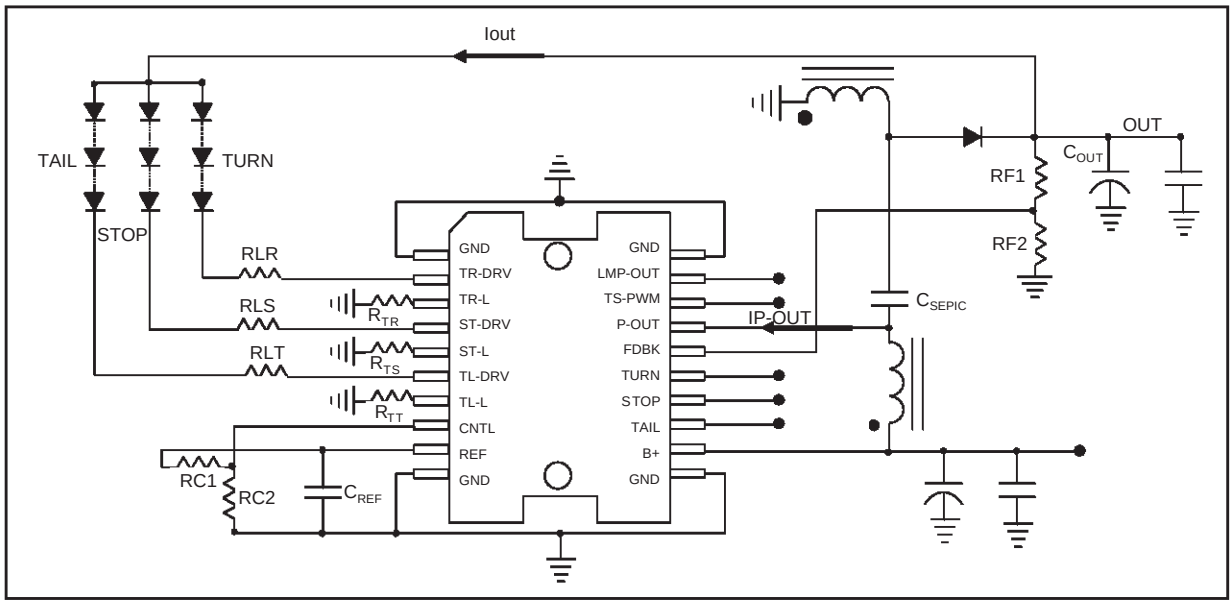
Table 1: STLC1 Pin Functions

PIN #	NAME	FUNCTION
1	GND	Ground
2	TR-DRV	The Low Side Driver drain pin for the TURN LED array
3	TR-L	The Low Side Driver source pin, used to detect either a lamp outage or an over-current condition for the TURN LED array
4	ST-DRV	The Low Side Driver drain pin for the STOP LED array
5	ST-L	The Low Side Driver source pin, used to detect either a lamp outage or an over-current condition for the STOP LED array
6	TL-DRV	The Low Side Driver drain pin for the TAIL LED array
7	TL-L	The Low Side Driver source pin, used to detect either a lamp outage or an over-current condition for the TAIL LED array
8	CNTL	Determines, according to a percentage of the V_{REF}, the Pulse Width Controller internal oscillator duty cycle
9	REF	Stable Reference Voltage
10	GND	Ground
11	GND	Ground
12	B+	STLC1 Power Supply
13	TAIL	TAIL input pin. When brought high, TAIL activates the IC and drives the TAIL LED array
14	STOP	STOP Input pin. When brought high, STOP activates the IC and drives the STOP LED array
15	TURN	TURN Input pin. When brought high, TURN activates the IC and drives the TURN LED array
16	FDBK	Internal Error Amplifier Inverting pin
17	P-OUT	Power MOSFET drain pin
18	TS-PWM	A Three state input. It determines the control logic for TAIL and STOP Low Side Drivers.
19	LMP-OUT	A weak pulled up signal during lamps NO FAULT condition and an active pull down when a FAULT condition is detected
20	GND	Ground

4. DETAILED INTERNAL BLOCK DIAGRAM DESCRIPTION.

In the following sections a detailed description of each block composing the device will be given.

Figure 3: STLC1 Typical Application Diagram



4.1 SMPS Power and Control Section.

The N-channel Power MOSFET, the PWM switch controller, the voltage comparators COMP1 and PWM COMP, the error amplifier and the internal stable voltage reference REF compose this section. The SMPS switch is source-grounded via a sensing resistor R_S whose purpose is both to perform a cycle-by-cycle power switch current limitation and to provide a ramp voltage for a current mode control. Cycle-by-cycle limitation controls the maximum allowable current into the power switch: if the voltage drop on R_S, due to the current flowing through it, exceeds an internal fixed value the Power MOSFET is shut-off until the next switching cycle occurs.

The output voltage regulation is performed using a current mode control scheme without the need of any compensation network. This allows the user to drastically reduce the number of external components. The output voltage is feedback to the FDBK pin device by means of an external resistor divider. The difference between the sampled output voltage and an internal stable bipolar band-gap voltage (error signal) is amplified and then compared with a sawtooth voltage, provided by the sensing resistor R_S times the inductor current whose typical frequency is 180kHz. When the amplified error signal, which varies very slowly with time relative to the switching frequency, is greater than the sawtooth waveform, the power switch is kept on. Otherwise, the switch is off.

4.2 Supply Section.

STLC1 is powered from the B+ pin. Input supply voltages greater than 29V (typical) cause the over voltage protection to act, shutting down the device.

4.3 Input Buffer Section.

Figure 4: Start-up Phase And Input Signal Timing Diagram (With TS-PWM Floating)

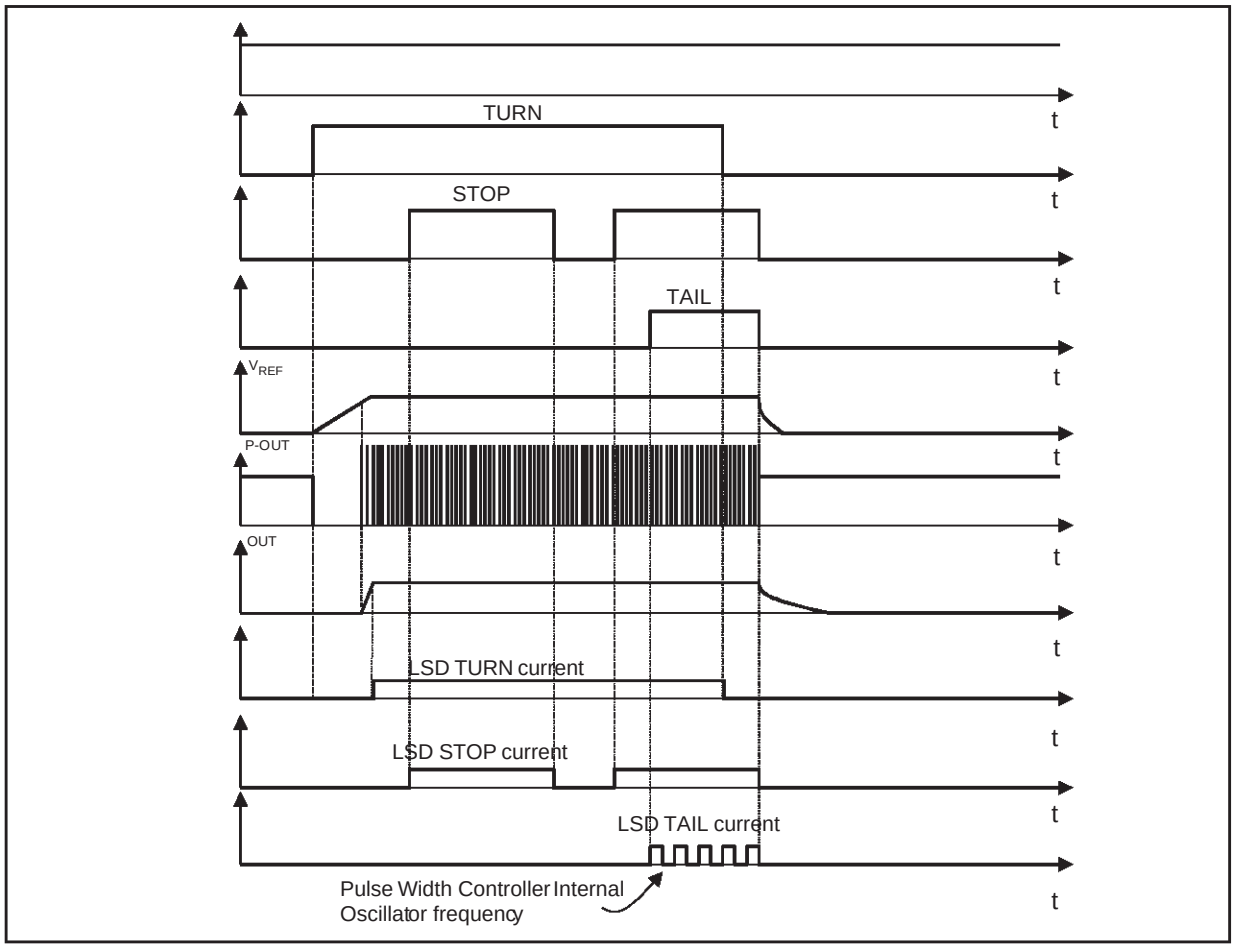
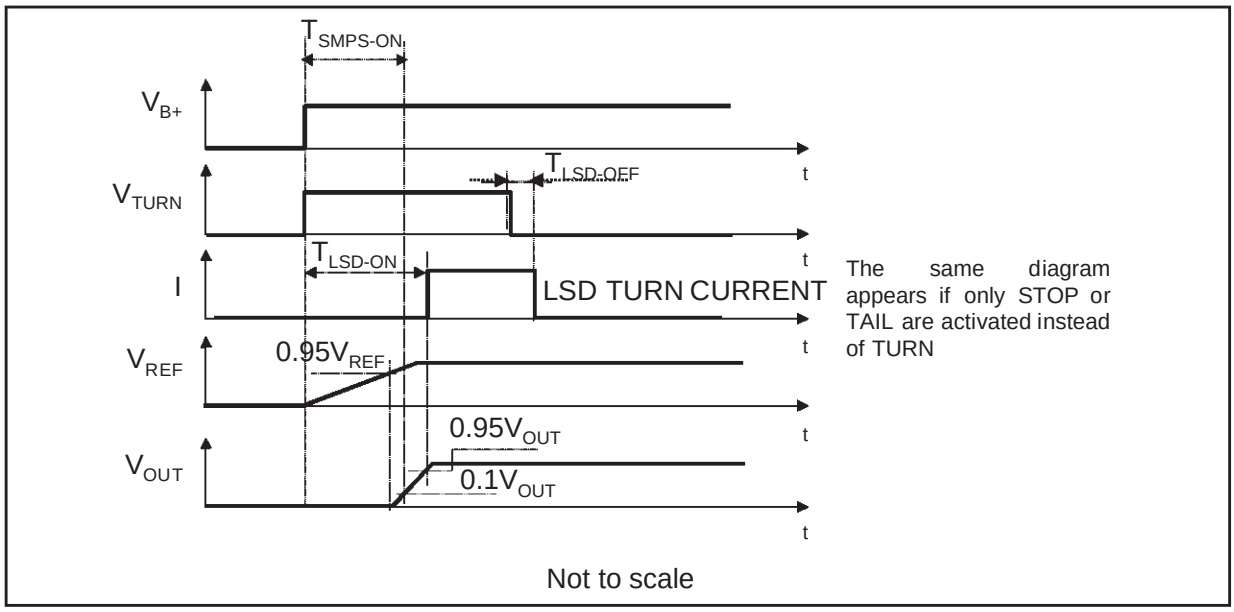


Figure 5: Magnified Start-up Phase (TS-PWM Floating)



TURN, STOP and TAIL are the IC's inputs. These inputs are internally connected to a pull-down and they are active when held high (e.g. connected to B+). If all inputs are disabled, SMPS and most of the internal control and diagnostic circuitry are in idle state. This is done in order to maintain the stand-by quiescent current below very low values, strengthening the battery life in case STLC1 is powered from such a power source.

When only one of these inputs is activated, a device start-up phase begins.

First the C_{REF} capacitor is charged and, as soon as the voltage on it has reached about 95% of its steady state value (V_{REF}), the SMPS starts switching. In order to allow the output to reach the regulated voltage value faster, the LSD corresponding to the input just enabled will only conduct when the OUT voltage is about 95% of its final value. If more than one input is active at the same time, this start-up phase does not take place. Figure 4 shows this start-up phase.

4.4 Low Side Driver Control Section.

The Pulse Width Controller internally drives the STOP and TAIL LSDs, while the external TURN input pin directly drives the corresponding LSD.

The Pulse Width Controller has two inputs: TS-PWM and CNTL.

Table 2: TS-PWM Control Pin Truth Table

		DRIVE TYPE	
TS-PWM PIN VOLTAGE	**INPUT ACTIVATED**	**TAIL ARRAY**	**STOP ARRAY**
LOW ($V_{TS-PWM}<0.1V_{REF}$)	TAIL	PWM	PWM
	STOP	OFF	ON
	TAIL AND STOP	PWM	ON
MID ($V_{TS-PWM}=V_{REF}/2$ or floating)	TAIL	PWM	OFF
	STOP	OFF	ON
	TAIL AND STOP	PWM	ON
HIGH ($V_{TS-PWM}>0.98V_{REF}$)	TAIL	PWM	PWM
	STOP	ON	ON
	TAIL AND STOP	ON	ON

TS-PWM input sets, according to the truth table shown in table 2, the control logic for STOP and TAIL LSD drivers.

CNTL can be used instead to change the duty cycle of the Pulse Width Controller's internal oscillator, performing an LED's dimming. Forcing the CNTL pin voltage to be a fraction of V_{REF} varies the duty cycle of the internal oscillator. This is simply feasible by using a resistor divider.

The duty cycle percentage can be approximately calculated as follows.

Duty Cycle % =

$$\begin{cases} 3.8\% \; if \quad \dfrac{RC1}{RC2 + RC2} \leq \dfrac{0.2}{V_{REF}} \\ \dfrac{RC1}{RC1 + RC2} \cdot 100 \qquad Elsewhere \end{cases}$$

Due to the fact that the TURN LSD is not controlled by the Pulse Width Controller, internal dimming can only be performed on the TAIL and STOP LED arrays. The TURN array can be externally dimmed (as well as TAIL and STOP) driving the corresponding input with a square pulse signal whose maximum frequency must be 200Hz.

If only one input is externally dimmed and the remaining two are disabled, keep in mind that every rising edge of the enabling signal triggers a start-up phase (see the detailed **4.3 Input Buffer Section**) and the corresponding LSD conducts with a delay that depends both on the capacitor value between REF and GND and the filter output capacitor. (See figure 5 T_{LSD-ON}). A high REF to GND capacitor value is useful to damp the switching noise on the REF pin but gives long start-up times while, on the other hand, low values are useful for faster turn-on time but they have lower switching noise filtering capability.

4.5 Thermal Protection Section.

Overheating of the device due to an excessive power throughput or insufficient heat sinking is avoided by the Thermal Shutdown function. In case the junction temperature exceeds approximately 150°C the thermal shutdown protection shuts off the SMPS, cooling down the device. A thermal hysteresis of 10°C is guaranteed in order to avoid oscillation.

4.6 Low Side Driver (M1, M2, M3) Section.

The purpose of the low side drivers is to connect, when enabled, each LED array to ground creating a path for the current. Using external resistors, the current to flow into the LED arrays is set according to the following formula:

$$I_{ARRAY} = \frac{(V_{OUT} - V_{ARRAY})}{R_T + R_L + R_{(ON)}}$$

where:
R_L=R_{LT}, R_{LS} or R_{LR} (see figure 3)
R_T=R_{TT}, R_{TS} or R_{TR} (see figure 3)
$R_{(on)}$=Static drain to source LSD on resistance
V_{OUT}=Output Voltage
V_{ARRAY}=Expected LED array voltage drop

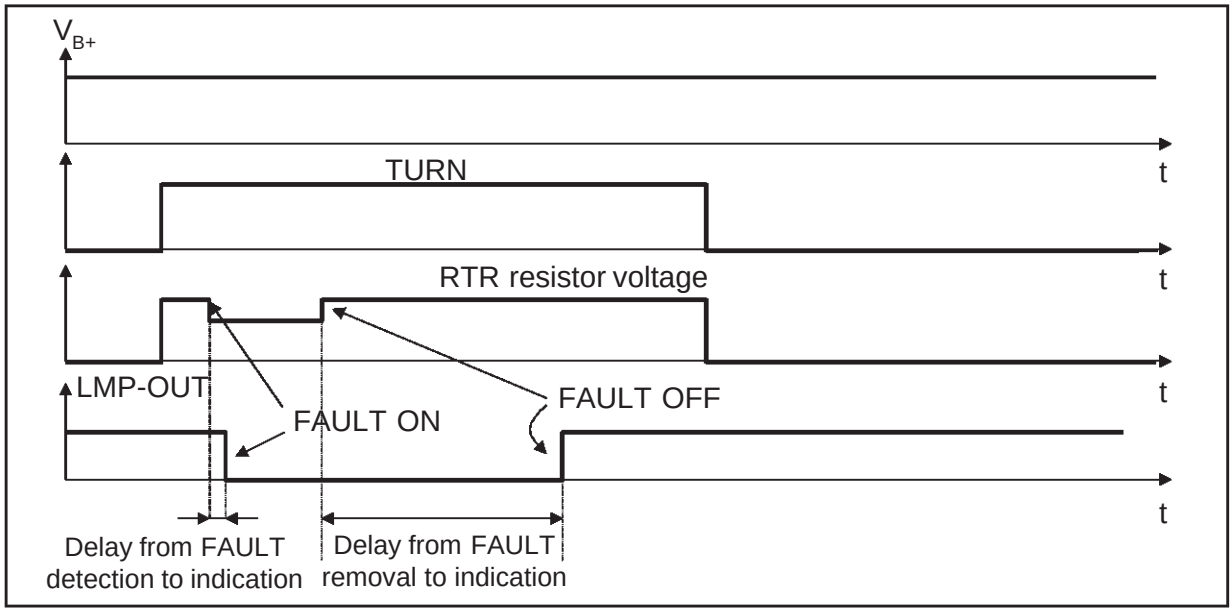
LSD over-current protection and under-current diagnostic (see **4.7 Lamp Outage Detection Section**) is performed by sensing the voltage on R_T resistors.

4.7 Lamp Outage Detect Section.

This internal block monitors the current flowing into each LSD, when active, by sensing the voltage drop across the R_T (R_{TS}, R_{TT}, R_{TR}) resistors (see figure 3).

Doing this, the LAMP OUTAGE block is able to detect either an over-current or an under-current (LED fail) condition.

Figure 6: Lamp Outage Section Behaviour (not to scale)



In fact, in case one or more LED fails, the current on the R_T resistor will drop due to the increased LED array equivalent resistance. If the voltage goes below an internal fixed threshold, a LED array fail condition is detected and the LMP-OUT pin will signal this fault status (LMP-OUT pin low). In order not to detect false fault conditions, due to the SMPS switching noise for example, a delay from fault detection to fault indication is guaranteed. For the same reason there is a time delay from the fault removal to the safe indication (LMP-OUT pin high). For the under-current diagnostic control logic timing see figure 6.

On the other hand if the current flowing into one LSD increases, the voltage on R_T increases too. An over-current condition is detected when the voltage drop on R_T exceeds an internal fixed threshold value. In this case the LSD average current is reduced by switching the corresponding LSD ON and OFF. The LAMP OUTAGE section is AND-ed with each input, that is, a fault condition can be detected only when the LED arrays are enabled.

4.8 Reference Section.

The device has an internal temperature stable bipolar band-gap voltage reference whose typical value is 1.24V. The internal logic circuitry is supplied with a voltage derived from the band-gap reference and it is externally available to the REF pin. A capacitor on this pin reduces the noise switching effect on the band-gap voltage reference.

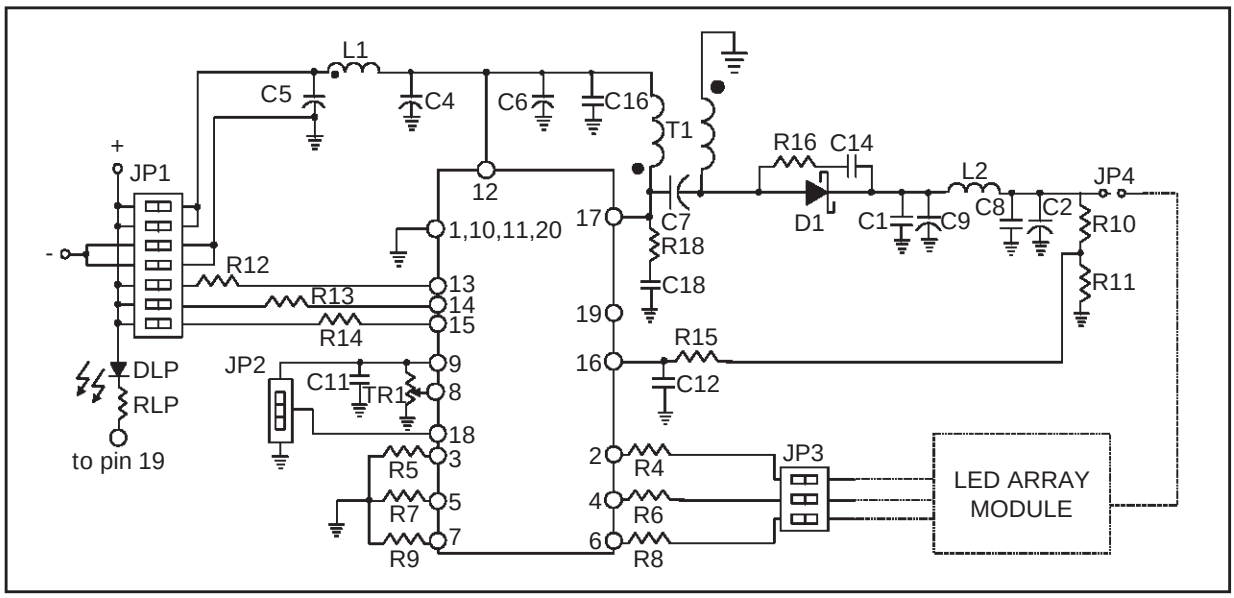
5. GENERAL DEMOBOARD CONSIDERATION.

The components placed on the STLC1 demoboard, whose schematic is shown in figure 7, have the following purposes:

C5, L1 and C4 are a pi-filter for the supply voltage and with C6 they represent the bulk energy storage elements for STLC1. C16 is a low ESR capacitor (X7R dielectric) used to reduce the voltage ripple on the B+ device supply pin.

Two coupled inductors compose T1, and together with C7 coupling capacitor, they form the so-called SEPIC topology. This converter configuration combines the best features of both the boost (continuous input current) and flyback topologies (any output voltage) and also reduces the converter ripple input current.

Figure 7: Demoboard Application Circuit



D1 is a power rectifier schottky diode, rated for an average current of 3A and 50V reverse blocking voltage, while C9, L2 and C8 are again a pi-filter for the output voltage and C1 and C2 are low ESR capacitors (X7R dielectric). This output filter smoothes output current from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces the output voltage ripple.

These capacitors must be selected with sufficient capacitance (C8, C9) and sufficiently low ESR to perform these functions. The output voltage is set by the R10 and R11 resistors according to the following formula:

$$V_{OUT} = V_{FDBK}\frac{R10 + R11}{R11}$$

In the proposed demoboard the output voltage is set at about 10V.

R15 and C12 are a low pass filter useful to damp the switching noise on the FDBK pin (pin 16).

The three couples (R4, R5), (R6, R7) and (R8, R9) are used to limit the current to each LSD, respectively TURN, STOP and TAIL (see paragraph **4.6 Low Side Drivers (M1, M2, M3) Section**).

R4, R6 and R8 have also the function of sensing resistors to detect both under and over current that flows into the corresponding LSD (see paragraph **4.7 Lamp Outage Detect Section**). Their value is

chosen as a trade off between the required sensibility in detecting anomolous working conditions (under and over current) and wasted electrical power.

C11 is an external bypass reference capacitor, while TR1 is a trimmer used to change the internal pulse width controller's duty cycle (see paragraph **4.4 LSD Control Section**) by partitioning the reference voltage. DLP is a LED diode that turns on when a fault condition is detected; RLP limits the current flowing into the DLP.

The RC couple R18, C18 is the simplest, but effective, non-polarized dissipative voltage snubber network. The main advantages of this snubber are that it damps the resonance of paracitic elements in the power circuit, thus reducing EMI issues and it also minimizes the power dissipation and stress of the internal power switch at turn off.

R16 and C14 are the same kind of snubber network and they are used here to minimize over voltages and to damp voltage ringing, which may result from the reverse recovery current of Schottky diode D1 and the leakage inductance.

R12, R13 and R14 resistors limit the current flowing into STLC1 inputs when enabled.

6. PCB LAYOUT RECOMMENDATION.

Any Switch Mode Power Supply requires a good design of the PCB (Printed Circuit Board) layout in order to achieve maximum performance in terms of system functionality and emitted radiations. Components placing, traces routing and width are the major issues.

Some fundamental rules will be given so that the PCB designer can produce a good layout.

All traces carrying current should be drawn on the PCB as short and thick as possible. This should be done to minimize resistive and inductive parasitic effects, gaining in system efficiency and radiated emissions.

Current return routing is another crucial issue. Signal ground and power ground must be routed separately and connected to a single ground point.

As a rule of thumb, traces carrying signal currents should run far away from traces carrying pulsed currents or quickly swinging voltages avoiding any coupling effect between them. Every unused space on the PCB could be filled with a ground plane helping to reduce noise emission.

Some sensitive points of the system, FDBK and P-OUT pins for example, may require some extra filtering and/or snubbering. In case high frequency filter capacitors are used (with ceramic or plastic film dielectric), they must be placed between these pins and the signal ground, as close to the IC as possible.

Table 3: Demoboard Application Circuit BOM

REFERENCE	DESCRIPTION
L1, L2	VK200
C4, C5, C6	22µF/35V Electrolytic Capacitor Low ESR
C16	220nF/35V Ceramic Capacitor X7R Dielectric
C7	47µF/35V Electrolytic Capacitor
C1, C2	4.7nF/35V Ceramic Capacitor X7RDielectric
C8, C9	220nF/35V Electrolytic Capacitor Low ESR
C14	560pF
C18	560pF/50V
C11	1µF/35V Tantalum Capacitor
C12	220pF Ceramic Capacitor
R10	9.1kΩ Resistor 0.125W/0.1%
R11	1.3kΩ Resistor 0.125W/0.1%
R15	4.7kΩ Resistor 0.125W/5%
R16	56Ω Resistor 0.125W/5%
R18	10Ω Resistor 0.125W/5%
R12, R13, R14	1.2kΩ 0.125W/5%
R4, R6, R8	2.2Ω Resistor 1W/5%
R5, R7, R9	1Ω 1W/5%
TR1	10kΩ Trimmer
RLP	1.5kΩ Resistor 0.125W/5%
D1	Schottky Diode STS3L4C939
DLP	LED Diode
T1	SEPIC Inductor, Toroid Horizontal THT 20µH@10ADC, 200-250KHz
JP1, JP2, JP3	Jumper

Figure 8: PCB Component Outline

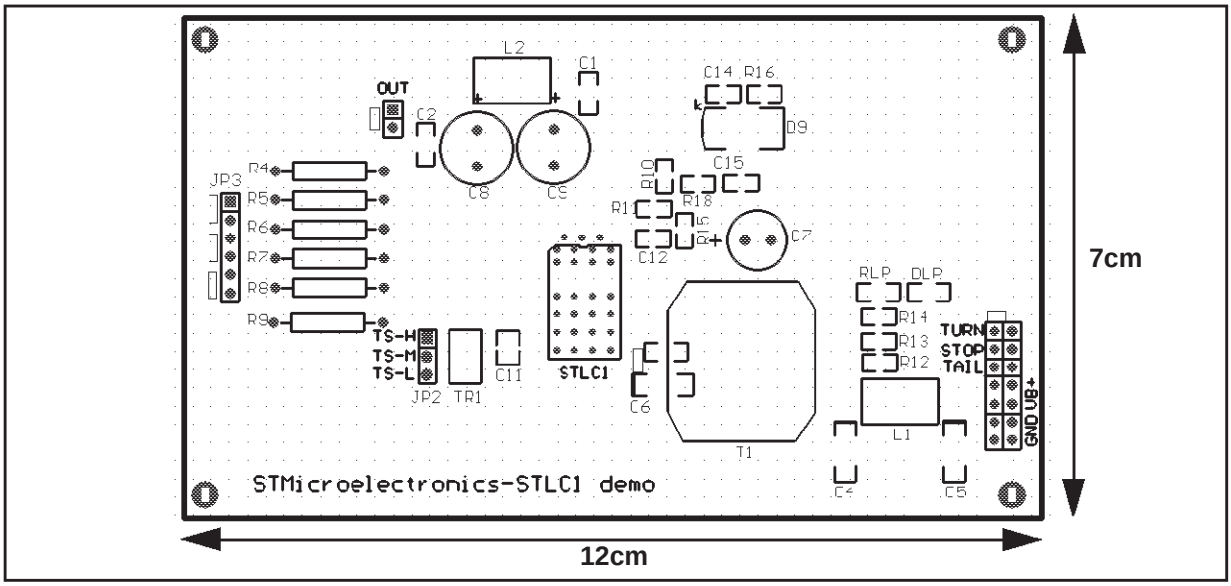


Figure 9: PCB Top Layer

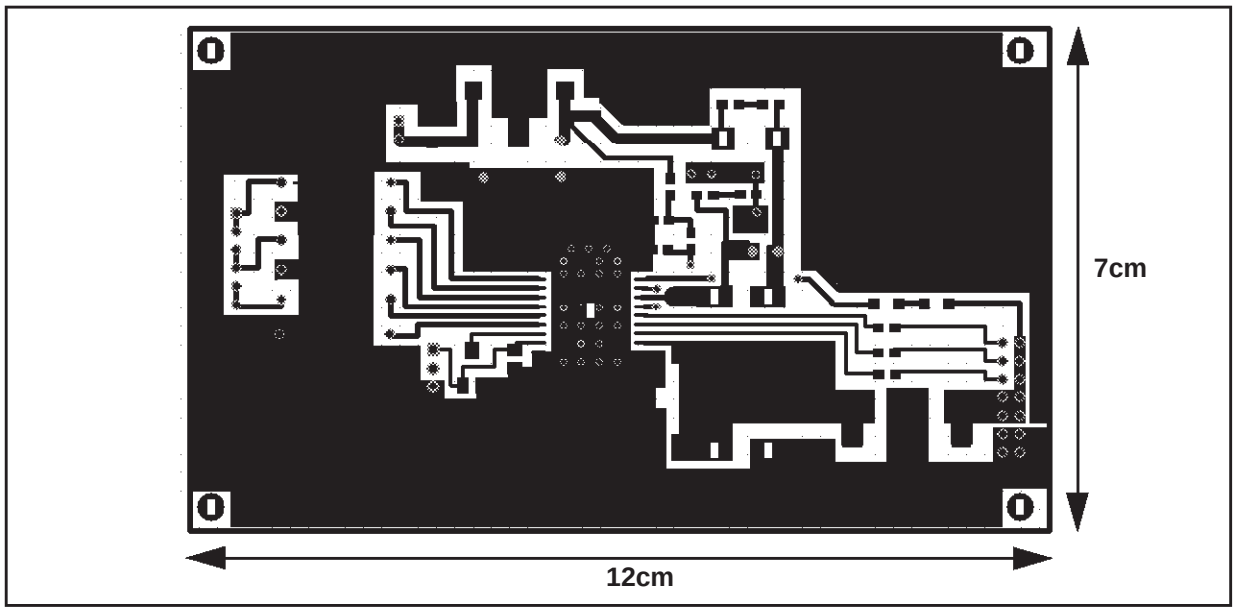
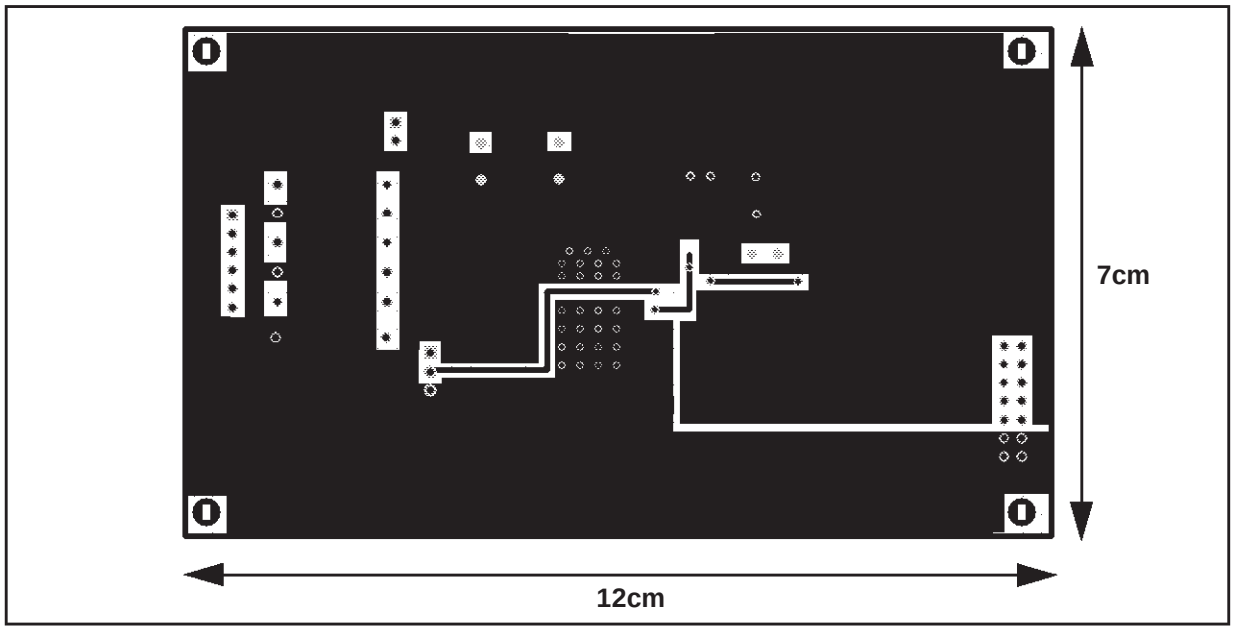


Figure 10: PCB Bottom Layer



7. CONCLUSION

A new device for rear LED lamps driving, STLC1, has been presented. Moreover, an in depth description of its functional blocks has been given together with some PCB layout suggestions.