



512K WORD × 16BIT LOW POWER PSEUDO SRAM

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1. GENERAL DESCRIPTION

W963A6BBN is a 8M bits CMOS pseudo static random access memory (Pseudo SRAM), organized as 512K words x 16 bits. Using advanced single transistor DRAM architecture and 0.175 μm process technology; W963L6BBN delivers fast access cycle time and low power consumption. It is suitable for mobile device application such as Cellular Phone and PDA, which high-density buffer is needed and power dissipation is most concerned.

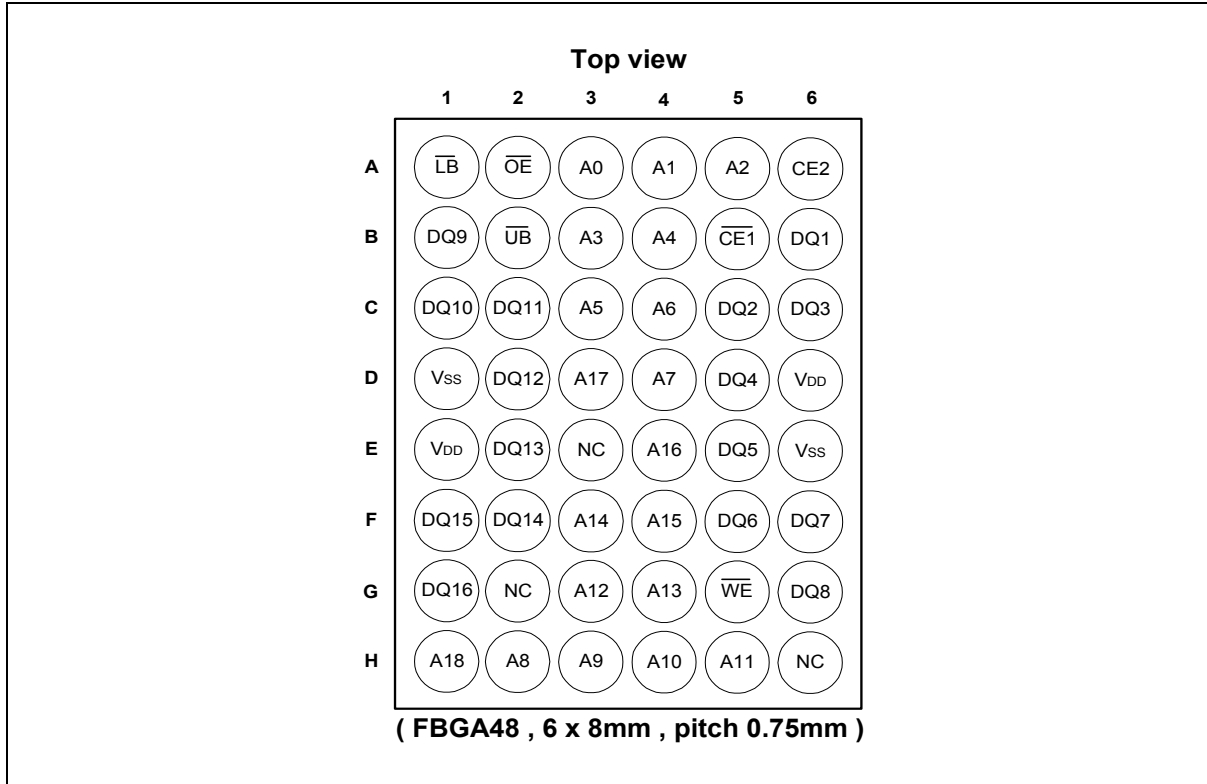
2. FEATURES

- Asynchronous SRAM interface
- Fast access cycle time:
 - $t_{RC} = 70 \text{ nS} (-70), 80 \text{ nS} (-80)$
- Low power consumption:
 - $I_{DDA1} = 20 \text{ mA Max.}$
 - $I_{DDS1} = 70 \mu\text{A Max.}$
- Byte write control
- Power supply:
 - $V_{DD} = +2.7\text{V to } +3.3\text{V}$
- Temperature:
 - $T_A = 0^\circ\text{C to } +70^\circ\text{C}$
 - $T_A = -25^\circ\text{C to } +85^\circ\text{C (Extended temperature)}$
 - $T_A = -40^\circ\text{C to } +85^\circ\text{C (Industrial temperature)}$

3. PRODUCT OPTIONS

PARAMETER	W963A6BBN70	W963A6BBN80
t_{RC}	70 nS Min.	80 nS Min.
I_{DDS1}	70 $\mu\text{A Max.}$	70 $\mu\text{A Max.}$
I_{DDA1}	20 mA	20 mA
V_{DD}	2.7V to 3.3V	2.7V to 3.3V

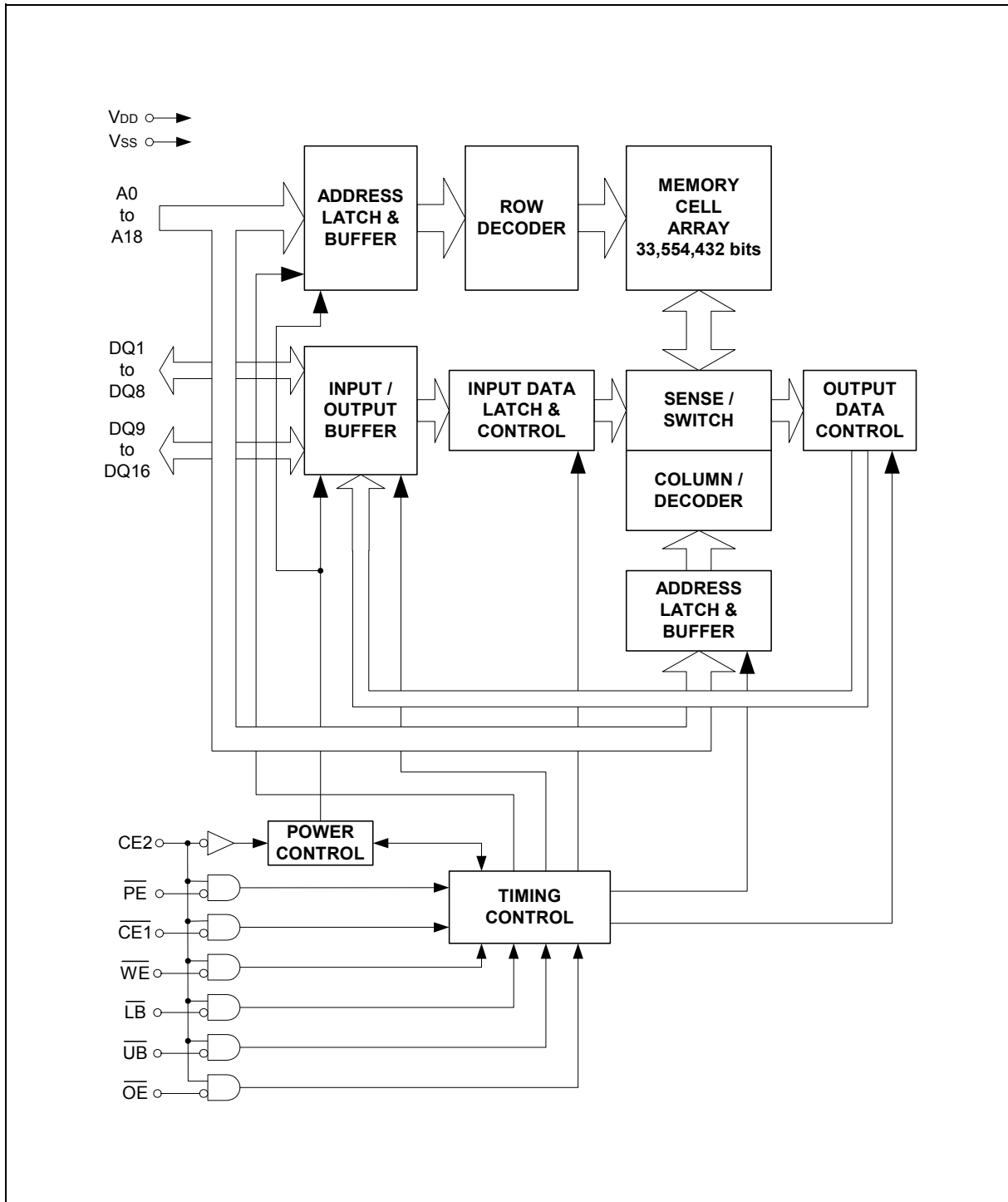
4. BALL CONFIGURATION



5. BALL DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A18	Address input
CE1	Chip Enable Input 1, Low: Enable
CE2	Chip Enable Input 2, High: Enable, Low: Enter Power Down mode
WE	Write enable input
OE	Output Enable input
LB	Lower byte write control
UB	Upper byte write control
I/O0 – I/O15	Data inputs/outputs
VDD	Power supply
VSS	Ground
NC	No Connection

6. BLOCK DIAGRAM





7. FUNCTION TRUTH TABLE

MODE	NOTE	CE2	$\overline{\text{CE1}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	A0-18	DQ1-8	DQ9-16	I _{DD}	DATA RETENTION
Standby (Deselect)		H	H	X	X	X	X	X	High-Z	High-Z	I _{DDs}	Yes
Output Disable	*1		L	H	H	X	X	*5	High-Z	High-Z	I _{DDA}	Yes
No Read				H	L	H	H	Valid	High-Z	High-Z		
Read	*2			L	L	*4	Valid	Output Valid	Output Valid			
Write (Upper Byte)				H	L	Valid	Invalid	Input Valid	Input Valid			
Write (Lower Byte)				L	H	L	H	Valid	Input Valid	Invalid		
Write (Word)				L	L	Valid	Input Valid	Input Valid	Input Valid			
Power Down	*3	L	X	X	X	X	X	X	High-Z	High-Z	I _{DDP}	No/Yes

Notes: L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High impedance, KEY = Key Address.

*1: Output Disable mode should not be kept longer than 1μs.

*2: Byte control at Read mode is not supported.

*3: Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. I_{DDP} current and data retention depend on the selection of Power Down Program.

*4: Either or both $\overline{\text{LB}}$ and $\overline{\text{UB}}$ must be Low for Read operation.

*5: Can be either V_{IL} or V_{IH} but must be valid before Read or Write.



8. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Voltage of V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.5 to +3.6	V
Voltage at Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to +3.6	V
Short Circuit Output Current	I _{OUT}	± 50	mA
Storage Temperature	T _{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

(Reference to V_{SS})

PARAMETER	NOTES	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage		V _{DD}	2.7	3.3	V
		V _{SS}	0	0	V
High Level Input Voltage	*1	V _{IH}	2.2	V _{DD} +0.3	V
Low Level Input Voltage	*2	V _{IL}	-0.3	0.5	V
Ambient Temperature		T _A	0	70	°C
Ambient Temperature		T _A	-25	85	°C
Ambient Temperature		T _A	-40	85	°C

Notes:

*1: Maximum DC voltage on input and I/O pins are V_{DD} +0.3V. During voltage transitions, inputs may positive overshoot to V_{DD} +1.0V for periods of up to 5ns.

*2: Minimum DC voltage on input and I/O pins are -0.3V. During voltage transitions, inputs may negative overshoot to -1.0V for periods of up to 5ns.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their Winbond representative beforehand.



Capacitance

Test conditions: $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

DESCRIPTION	SYMBOL	TEST SETUP	TYP.	MAX.	UNIT
Address Input Capacitance	CIN1	VIN = 0V	-	5	pF
Control Input Capacitance	CIN2	VIN = 0V	-	5	pF
Data Input/Output Capacitance	CIO	VIO = 0V	-	8	pF

DC Characteristics

(Under Recommended Operating Conditions unless otherwise noted) notes*1, *2, *3

PARAMETER	SYM.	TEST CONDITIONS	MIN.	MAX.	UNIT	
Input Leakage Current	ILI	VIN = VSS to VDD	-1.0	+1.0	μA	
Output Leakage Current	ILO	VOUT = VSS to VDD, Output Disable	-1.0	+1.0	μA	
Output High Voltage Level	VOH	VDD = VDD, IOH = -0.5 mA	2.2	-	V	
Output Low Voltage Level	VOL	IOL = 1 mA	-	0.4	V	
Standby Current	(TTL)	IDDS VDD = VDD Max., VIN = VIH or VIL CE1 = CE2 = VIH	-	3	mA	
	(CMOS)	IDDS1 VDD = VDD Max., VIN \leq 0.2V or VIN \geq VDD - 0.2V, CE1 = CE2 \geq VDD - 0.2V	-	70	μA	
Active Current	IDDA1	VDD = VDD Max., VIN = VIH or VIL, CE1 = VIL and CE2 = VIH, IOUT = 0 mA	t _{rc} / t _{wc} = minimum	-	20	mA
	IDDA2		t _{rc} / t _{wc} = 1 μs	-	3	mA

Notes:

- *1: All voltages are reference to Vss.
- *2: DC Characteristics are measured after following POWER-UP timing.
- *3: Iout depends on the output load conditions.



AC Characteristics

(Under Recommended Operating Conditions unless otherwise noted)

Read Operation

PARAMETER	SYM.	-70		-80		UNIT	NOTES
		Min.	Max.	Min.	Max.		
Read Cycle Time	t _{RC}	70	-	80	-	nS	
Chip Enable Access Time	t _{CE}	-	65	-	75	nS	*1, *3
Output Enable Access Time	t _{OE}	-	40	-	45	nS	*1
Address Access Time	t _{AA}	-	65	-	75	nS	*1
Output Data Hold Time	t _{OH}	5	-	5	-	nS	*1
$\overline{\text{CE1}}$ Low to Output Low-Z	t _{CLZ}	5	-	5	-	ns	*2
$\overline{\text{OE}}$ Low to Output Low-Z	t _{OLZ}	0	-	0	-	nS	*2
$\overline{\text{CE1}}$ High to Output High-Z	t _{CHZ}	-	20	-	25	nS	*2
$\overline{\text{OE}}$ High to Output High-Z	t _{OHZ}	-	20	-	25	nS	*2
Address Setup Time to $\overline{\text{CE1}}$ Low	t _{ASC}	-5	-	-5	-	nS	*4
Address Setup Time to $\overline{\text{OE}}$ Low	t _{ASO}	30	-	35	-	nS	*3, *5
	t _{ASO[ABS]}	10	-	10	-	nS	*6
$\overline{\text{LB}} / \overline{\text{UB}}$ Setup Time to $\overline{\text{CE1}}$ Low	t _{BSC}	-5	-	-5	-	nS	
$\overline{\text{LB}} / \overline{\text{UB}}$ Setup Time to $\overline{\text{OE}}$ Low	t _{BSO}	10	-	10	-	nS	
Address Invalid Time	t _{AX}	-	5	-	5	nS	
Address Hold Time from $\overline{\text{CE1}}$ Low	t _{CLAH}	70	-	80	-	nS	
Address Hold Time from $\overline{\text{OE}}$ Low	t _{OLAH}	40	-	45	-	nS	*9
Address Hold Time from $\overline{\text{CE1}}$ High	t _{CHAH}	-5	-	-5	-	nS	
Address Hold Time from $\overline{\text{OE}}$ High	t _{OHAH}	-5	-	-5	-	nS	
$\overline{\text{LB}} / \overline{\text{UB}}$ Hold Time from $\overline{\text{CE1}}$ High	t _{CHBH}	-5	-	-5	-	nS	
$\overline{\text{LB}} / \overline{\text{UB}}$ Hold Time from $\overline{\text{OE}}$ High	t _{OHBH}	-5	-	-5	-	nS	
$\overline{\text{CE1}}$ Low to $\overline{\text{OE}}$ Low Delay Time	t _{CLOL}	25	1000	30	1000	nS	*3, *5, *7, *8
$\overline{\text{OE}}$ Low to $\overline{\text{CE1}}$ High Delay Time	t _{OLCH}	35	-	40	-	nS	*7
$\overline{\text{CE1}}$ High Pulse Width	t _{CP}	12	-	15	-	nS	
$\overline{\text{OE}}$ High Pulse Width	t _{OP}	25	1000	30	1000	nS	*5, *7, *8
	t _{OP[ABS]}	12	-	15	-	nS	*6



Read Operation, Continued

Notes:

- *1: The output load is 30 pF
- *2: The output load is 5 pF.
- *3: The t_{CE} is applicable if \overline{OE} is brought to Low before $\overline{CE1}$ goes Low and is also applicable if actual value of both or either t_{ASO} or t_{CLOL} is shorter than specified value.
- *4: Applicable if \overline{OE} is brought to Low before $\overline{CE1}$ goes Low.
- *5: The t_{ASO} , $t_{CLOL}(\min)$ and $t_{OP}(\min)$ are reference values when the access time is determined by t_{OE} . If actual value of each parameter is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value.

For example, if actual t_{ASO} , $t_{ASO}(\text{actual})$, is shorter than specified minimum value, $t_{ASO}(\min)$, during \overline{OE} control access (ie., $\overline{CE1}$ stays Low), the t_{OE} become $t_{OE}(\max) + t_{ASO}(\min) - t_{ASO}(\text{actual})$.
- *6: The $t_{ASO}[\text{ABS}]$ and $t_{OP}[\text{ABS}]$ is the absolute minimum value during \overline{OE} control access.
- *7: If actual value of either t_{CLOL} or t_{OP} is shorter than specified minimum value, both t_{OLAH} and t_{OLCH} become $t_{RC}(\min) - t_{CLOL}(\text{actual})$ or $t_{RC}(\min) - t_{OP}(\text{actual})$.
- *8: Maximum value is applicable if $\overline{CE1}$ is kept at low.



AC Characteristics, Continued

Write Operation

PARAMETER	SYM.	-70		-80		UNIT	NOTES
		Min.	Max.	Min.	Max.		
Write Cycle Time	t _{WC}	70	-	80	-	nS	*1
Address Setup Time	t _{AS}	0	-	0	-	nS	*2
Address Hold Time	t _{AH}	35	-	40	-	nS	*2
$\overline{\text{CE1}}$ Write Setup Time	t _{CS}	0	1000	0	1000	nS	
$\overline{\text{CE1}}$ Write Hold Time	t _{CH}	0	1000	0	1000	nS	
$\overline{\text{WE}}$ Setup Time	t _{WS}	0	-	0	-	nS	
$\overline{\text{WE}}$ Hold Time	t _{WH}	0	-	0	-	nS	
$\overline{\text{LB}}$ and $\overline{\text{UB}}$ Setup Time	t _{BS}	-5	-	-5	-	nS	
$\overline{\text{LB}}$ and $\overline{\text{UB}}$ Hold Time	t _{BH}	-5	-	-5	-	nS	
$\overline{\text{OE}}$ Setup Time	t _{OES}	0	1000	0	1000	nS	*3
$\overline{\text{OE}}$ Hold Time	t _{OEH}	30	1000	35	1000	nS	*3, *4
	t _{OEH[ABS]}	12	-	15	-	nS	*5
$\overline{\text{OE}}$ High to $\overline{\text{CE1}}$ Low Setup Time	t _{OHCL}	-5	-	-5	-	nS	*6
$\overline{\text{OE}}$ High to Address Hold Time	t _{OH AH}	-5	-	-5	-	nS	*7
$\overline{\text{CE1}}$ Write Pulse Width	t _{CW}	45	-	50	-	nS	*1, *8
$\overline{\text{WE}}$ Write Pulse Width	T _{WP}	45	-	50	-	nS	*1, *8
$\overline{\text{CE1}}$ Write Recovery Time	t _{WRC}	10	-	15	-	nS	*1, *9
$\overline{\text{WE}}$ Write Recovery Time	t _{WR}	10	1000	15	1000	nS	*1, *3, *9
Data Setup Time	t _{DS}	15	-	20	-	nS	
Data Hold Time	t _{DH}	0	-	0	-	ns	
$\overline{\text{CE1}}$ High Pulse Width	t _{CP}	12	-	15	-	nS	*9



Write Operation, Continued

Notes:

- *1: Minimum value must be equal or greater than the sum of actual t_{CW} (or t_{WP}) and t_{WRC} (or t_{WR}).
- *2: New write address is valid from either $\overline{CE1}$ or \overline{WE} is brought to High.
- *3: The t_{OE} is specified from end of $t_{WC}(\min.)$. The $t_{OE}(\min)$ is a reference value when the access time is determined by t_{OE} .
If actual value, $t_{OE}(\text{actual})$ is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value.
- *4: The $t_{OE}(\max)$ is applicable if $\overline{CE1}$ is kept at Low and both \overline{WE} and \overline{OE} are kept at High.
- *5: The $t_{OE}[\text{ABS}]$ is the absolute minimum value if write cycle is terminated by \overline{WE} and $\overline{CE1}$ stays Low.
- *6: $t_{OHCL}(\min)$ must be satisfied if read operation is not performed prior to write operation.
In case \overline{OE} is disabled after $t_{OHCL}(\min.)$, \overline{WE} Low must be asserted after $t_{RC}(\min)$ from $\overline{CE1}$ Low. In other words, read operation is initiated if $t_{OHCL}(\min.)$ is not satisfied.
- *7: Applicable if $\overline{CE1}$ stays Low after read operation.
- *8: t_{CW} and t_{WP} is applicable if write operation is initiated by $\overline{CE1}$ and \overline{WE} , respectively.
- *9: t_{WRC} and t_{WR} is applicable if write operation is terminated by $\overline{CE1}$ and \overline{WE} , respectively.
The $t_{WR}(\min)$ can be ignored if $\overline{CE1}$ is brought to High together or after \overline{WE} is brought to High. In such case, the $t_{CP}(\min)$ must be satisfied.



AC Characteristics, Continued

Power Down and Power Down Program Parameters

PARAMETER	SYM.	-70		-80		UNIT	NOTES
		Min.	Max.	Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t _{CSP}	10	-	10	-	nS	
CE2 Low Hold Time after Power Down Entry	t _{C2LP}	70	-	80	-	nS	
CE1 High Setup Time following CE2 High after Power Down Exit	t _{CHS}	10	-	10	-	nS	

Other Timing Parameters

PARAMETER	SYM.	-70		-80		UNIT	NOTES
		Min.	Max.	Min.	Max.		
CE1 High to OE Invalid Time for Standby Entry	t _{CHOX}	10	-	10	-	nS	
CE1 High to WE Invalid Time for Standby Entry	t _{CHWX}	10	-	10	-	nS	*1
CE2 Low Hold Time after Power-up	t _{C2LH}	50	-	50	-	μS	*2
CE2 High Hold Time after Power-up	t _{C2HL}	50	-	50	-	μS	*3
CE1 High Hold Time following CE2 High after Power-up	t _{CHH}	350	-	350	-	μS	*2
Input Transition Time	t _r	1	25	1	25	nS	*4

Notes:

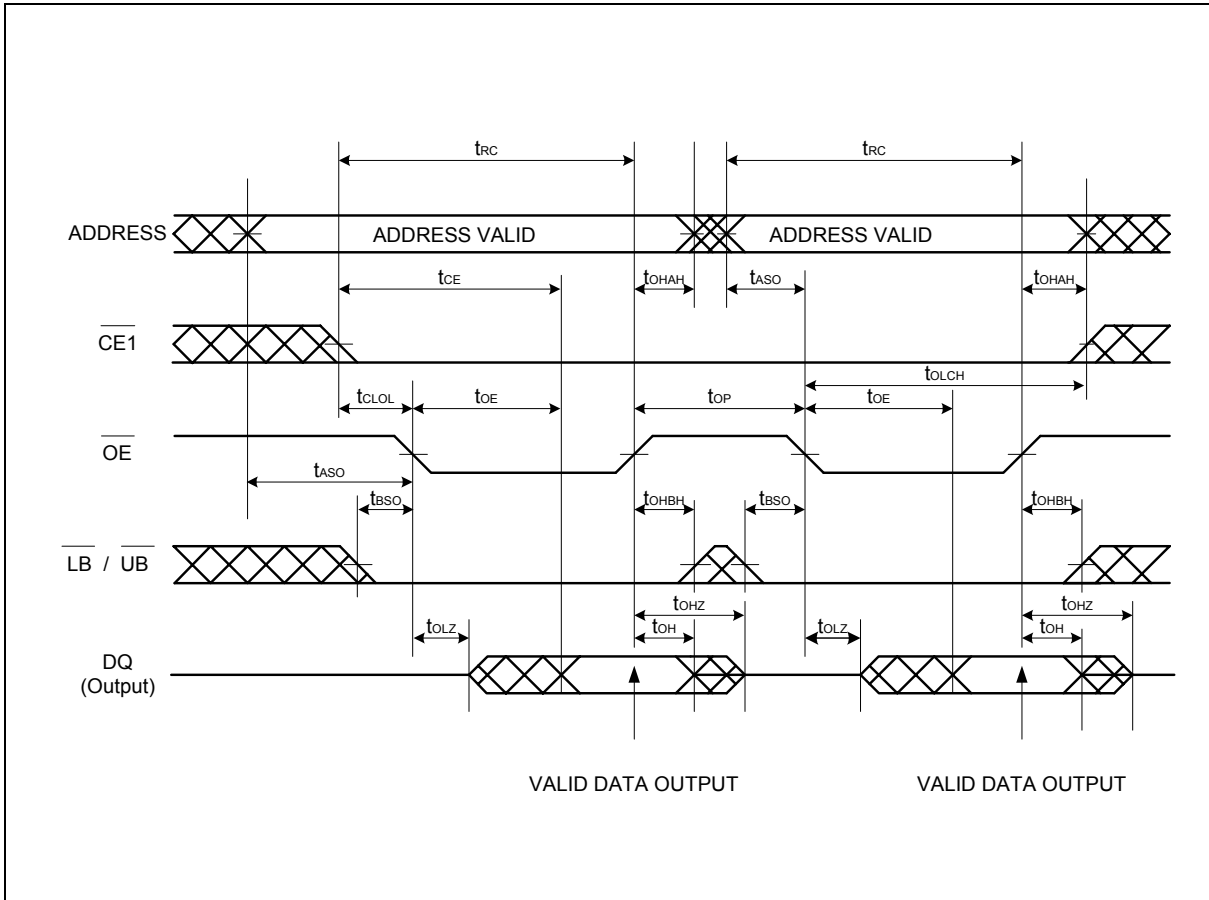
- *1: Some data might be written into any address location if t_{CHWX}(min) is not satisfied.
- *2: Must satisfy t_{CHH}(min) after t_{C2LH}(min).
- *3: Requires Power Down mode entry and exit after t_{C2HL}.
- *4: The Input Transition Time (t_r) at AC testing is 5ns as shown in below. If actual t_r is longer than 5ns, it may violate AC specified of some timing parameters.

AC Test Conditions

SYMBOL	DESCRIPTION	TEST SETUP	VALUE	UNIT	NOTE
V _{IH}	Input High Level	V _{DD} = 2.7V to 3.3V	2.3	V	
V _{IL}	Input Low Level	V _{DD} = 2.7V to 3.3V	0.5	V	
V _{REF}	Input Timing Measurement Level	V _{DD} = 2.7V to 3.3V	1.3	V	
T _T	Input Transition Time	Between V _{IL} and V _{IH}	5	nS	

9. TIMING WAVEFORMS

Read Timing #1 (\overline{OE} Control Access)



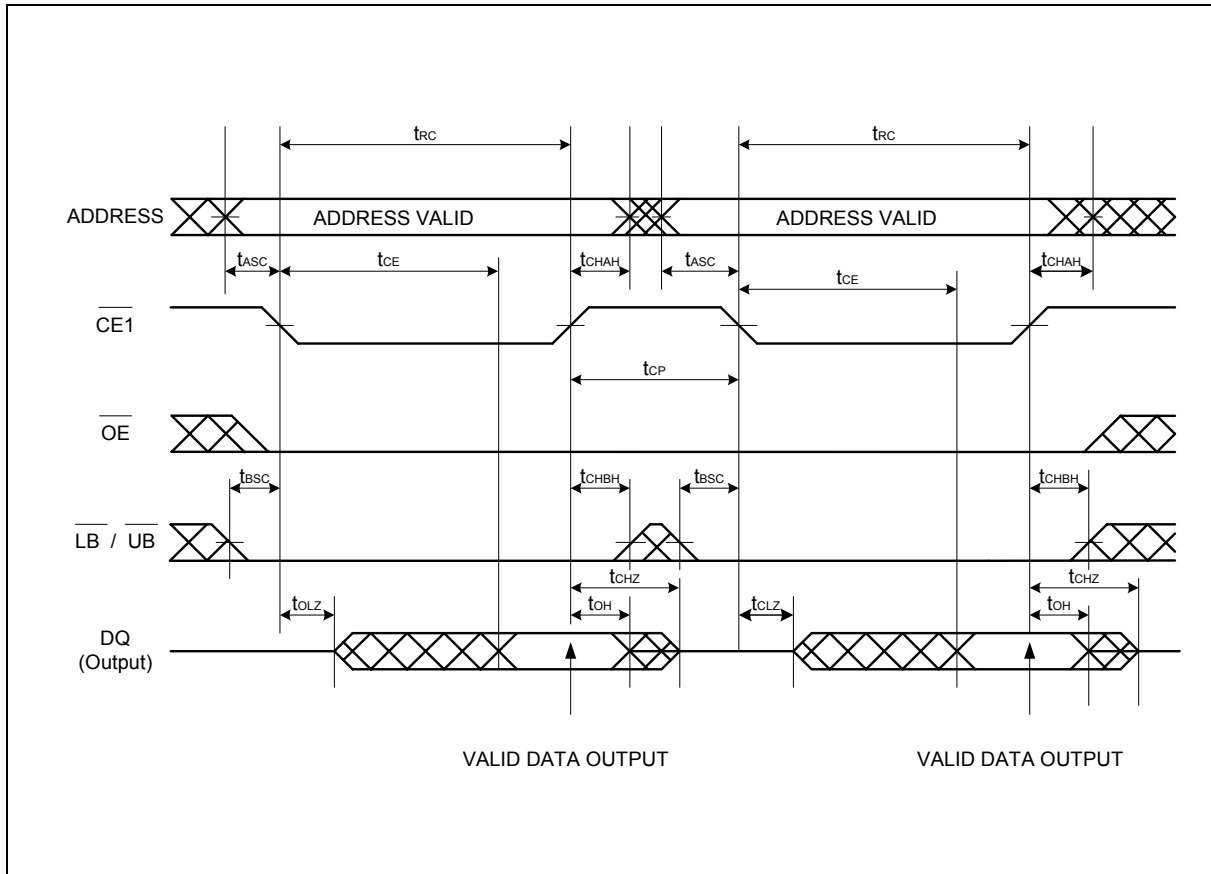
Note: $\overline{CE2}$, \overline{PE} and \overline{WE} must be High for entire read cycle.

Either or both \overline{LB} and \overline{UB} must be Low when both $\overline{CE1}$ and \overline{OE} are Low.



Timing Waveforms, continued

Read Timing #2 ($\overline{\text{CE1}}$ Control Access)



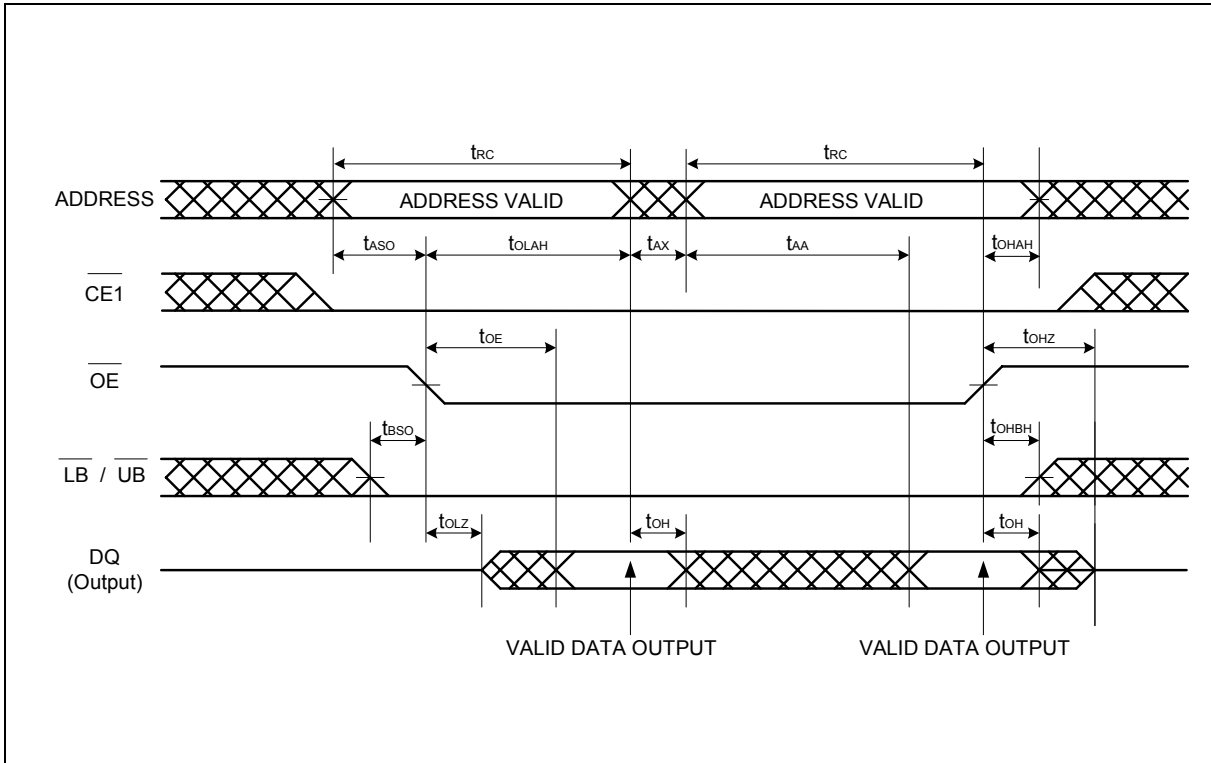
Note: $\overline{\text{CE2}}$, $\overline{\text{PE}}$ and $\overline{\text{WE}}$ must be High for entire read cycle.

Either or both $\overline{\text{LB}}$ and $\overline{\text{UB}}$ must be Low when both $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ are Low.



Timing Waveforms, continued

Read Timing #3 (Address Access after $\overline{\text{OE}}$ Control Access)



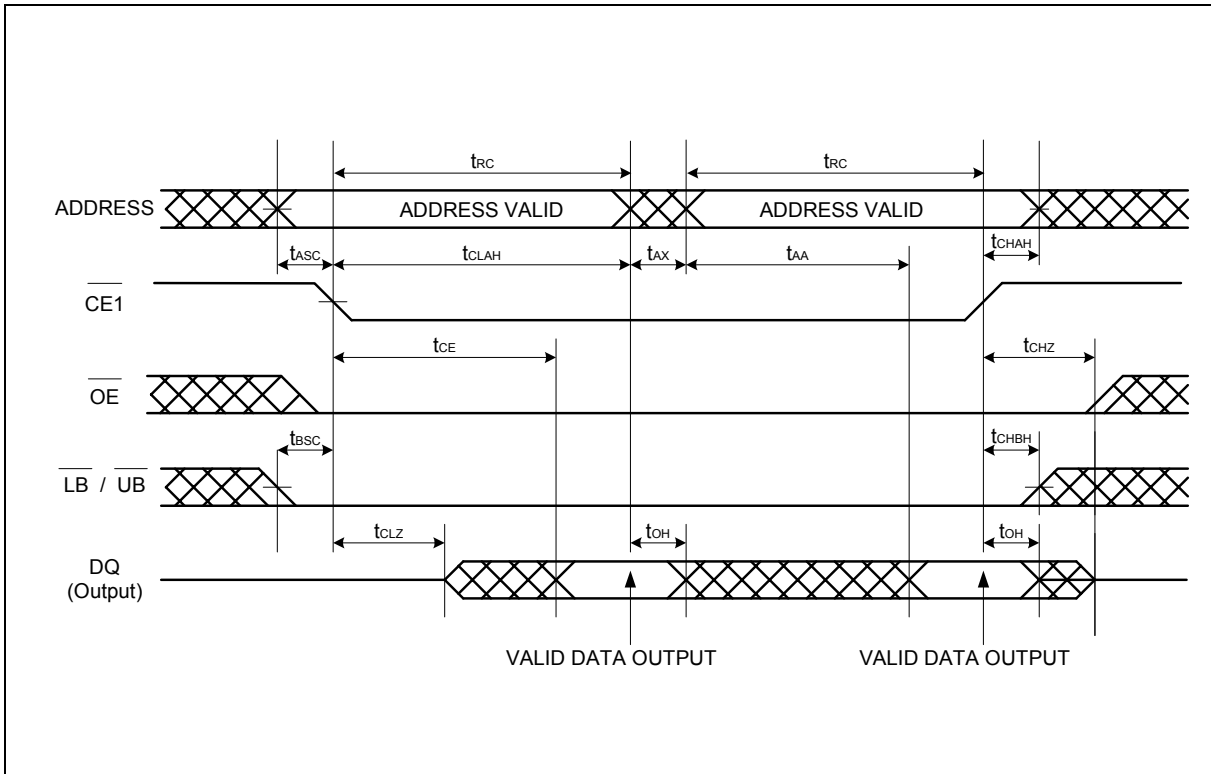
Note: $\overline{\text{CE2}}$, $\overline{\text{PE}}$ and $\overline{\text{WE}}$ must be High for entire read cycle.

Either or both $\overline{\text{LB}}$ and $\overline{\text{UB}}$ must be Low when both $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ are Low.



Timing Waveforms, continued

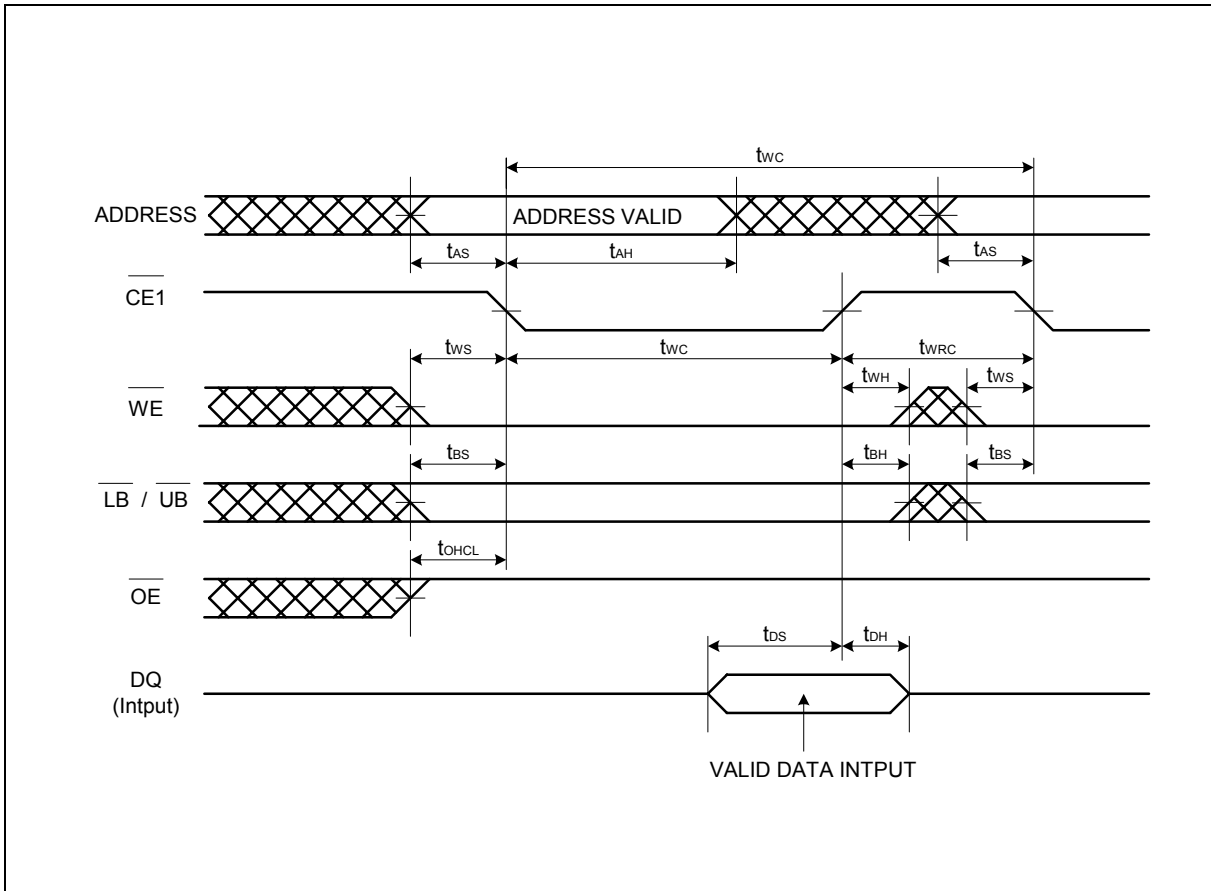
Read Timing #4 (Address Access after $\overline{\text{CE1}}$ Control Access)



Note: $\overline{\text{CE2}}$, $\overline{\text{PE}}$ and $\overline{\text{WE}}$ must be High for entire read cycle.
 Either or both $\overline{\text{LB}}$ and $\overline{\text{UB}}$ must be Low when both $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ are Low.

Timing Waveforms, continued

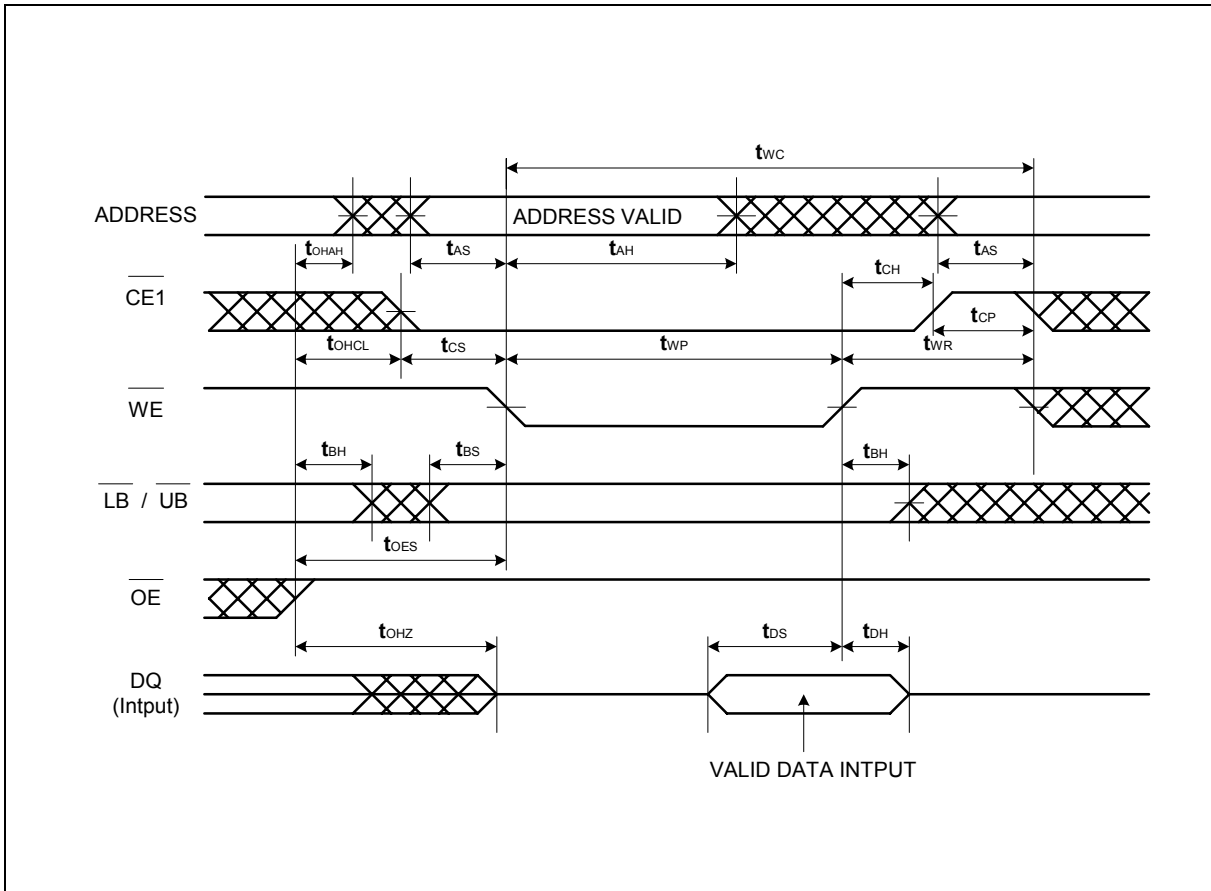
Write Timing #1 (CE1 Control)



Note: CE2 and PE must be High for entire write cycle.

Timing Waveforms, continued

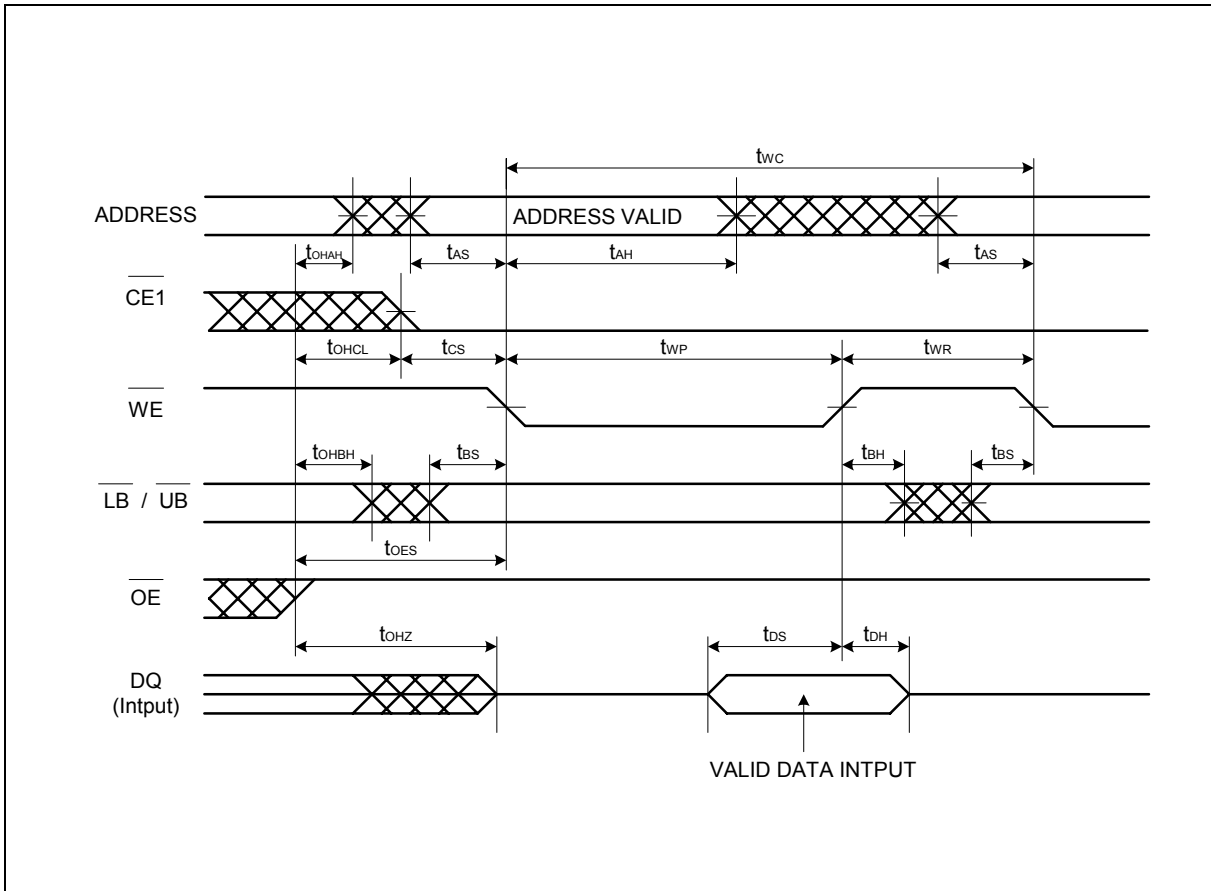
Write Timing #2-1 (WE Control, Single Write Operation)



Note: CE2 and PE must be High for entire write cycle.

Timing Waveforms, continued

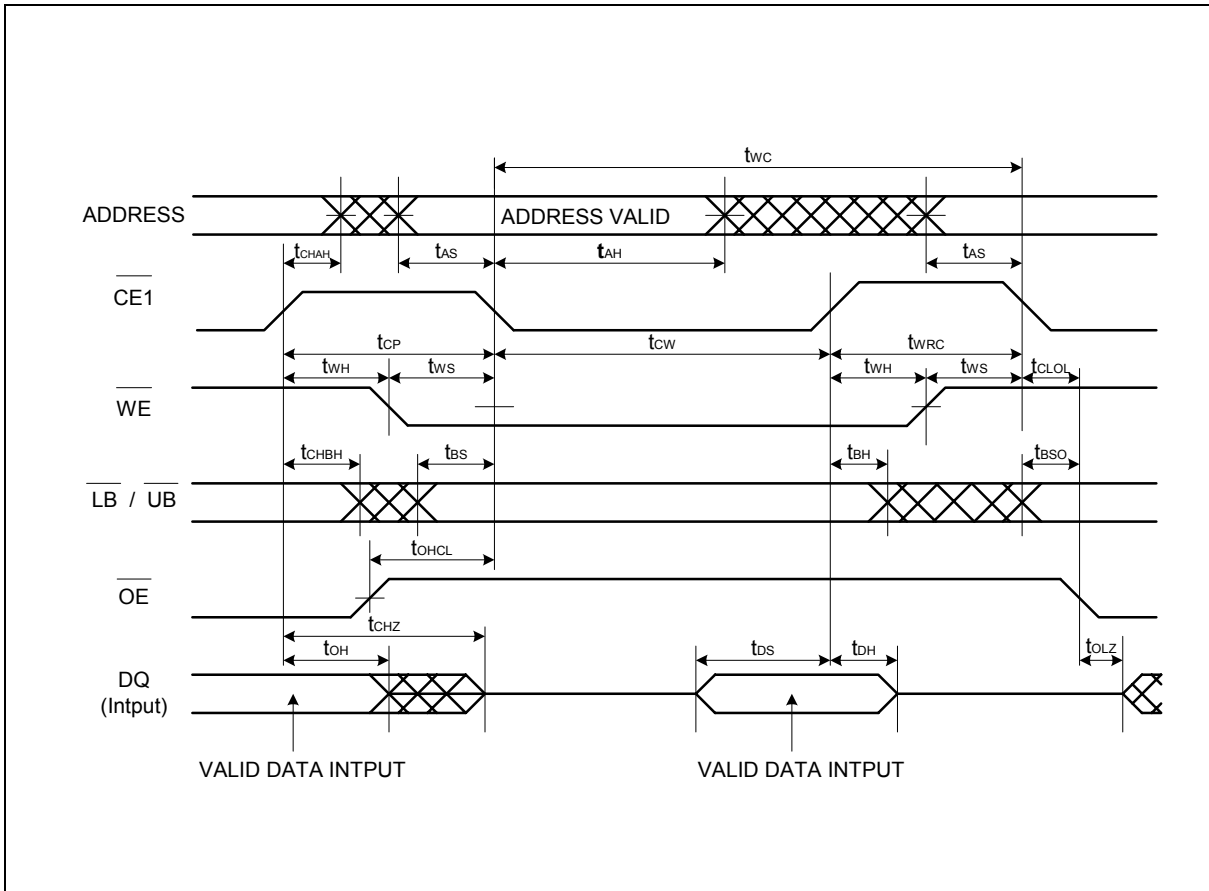
Write Timing #2 (WE Control, Continuous Write Operation)



Note: CE2 and PE must be High for entire write cycle.

Timing Waveforms, continued

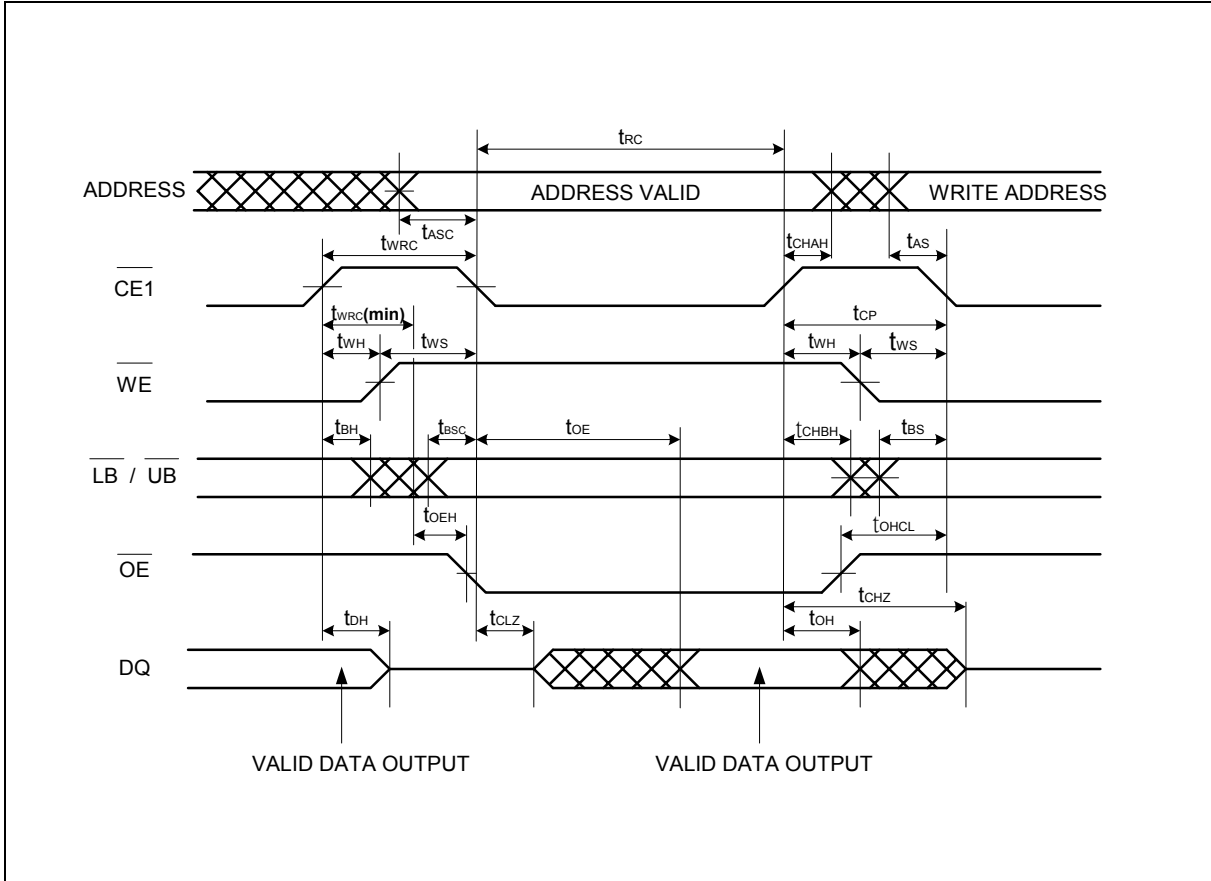
Read/Write Timing #1-1 (CE1 Control)



Note: Write address is valid from either $\overline{CE1}$ or \overline{WE} of last falling edge.

Timing Waveforms, continued

Read/Write Timing #1-2 (CE1 Control)

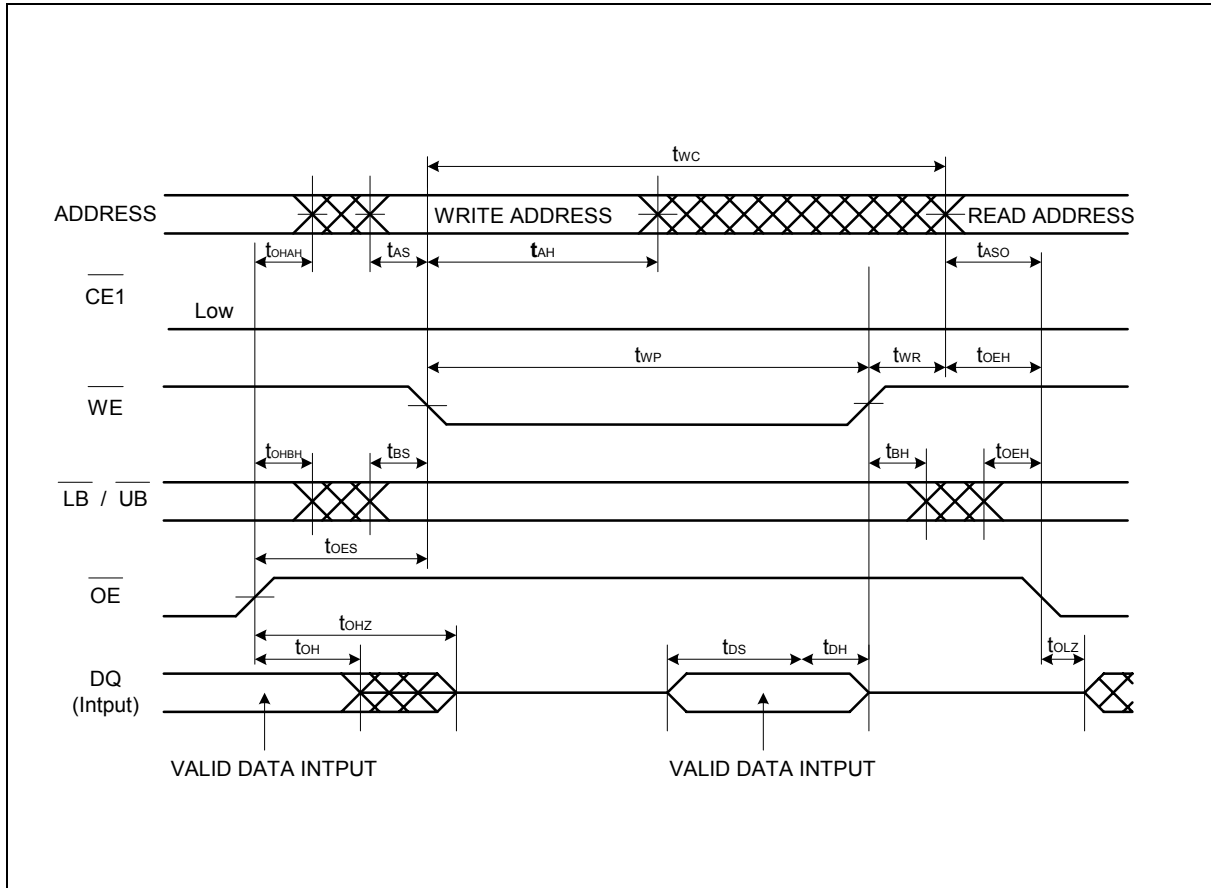


Note: The t_{OE} is specified from the time satisfied both t_{WRC} and $t_{WR(min)}$.



Timing Waveforms, continued

Read (\overline{OE} Control) / Write (\overline{WE} Control) Timing #2-1

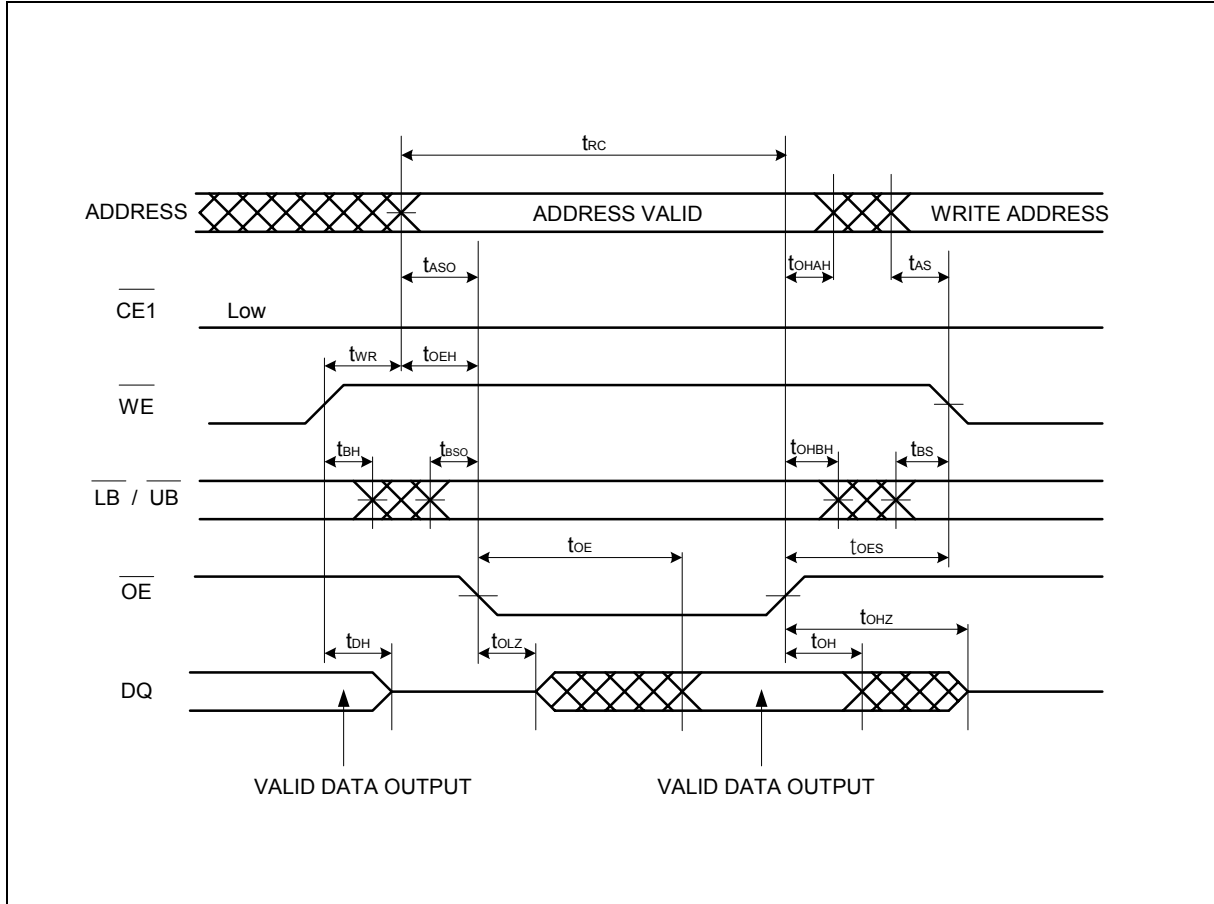


Note: $\overline{CE1}$ can be tied to Low for \overline{WE} and \overline{OE} controlled operation.

When $\overline{CE1}$ is tied to Low, output is exclusively controlled by \overline{OE} .

Timing Waveforms, continued

Read ($\overline{\text{OE}}$ Control) / Write ($\overline{\text{WE}}$ Control) Timing #2-2

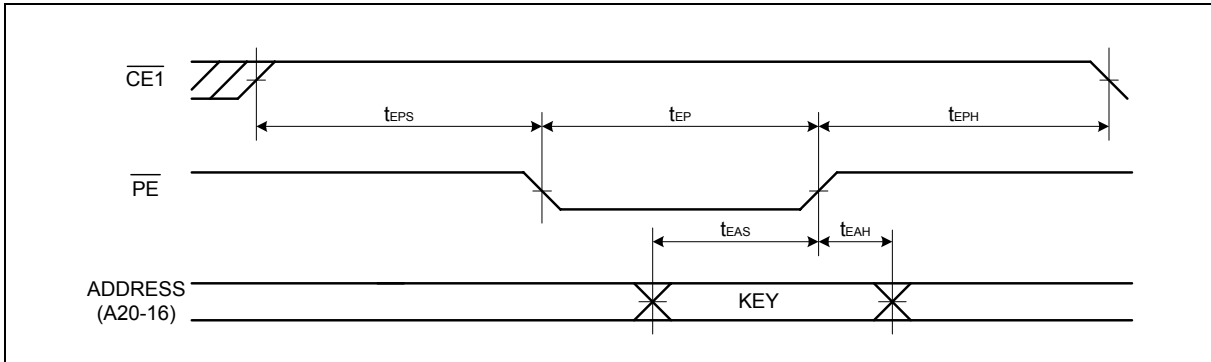


Note: $\overline{\text{CE1}}$ can be tied to Low for $\overline{\text{WE}}$ and $\overline{\text{OE}}$ controlled operation.
When $\overline{\text{CE1}}$ is tied to Low, output is exclusively controlled by $\overline{\text{OE}}$.



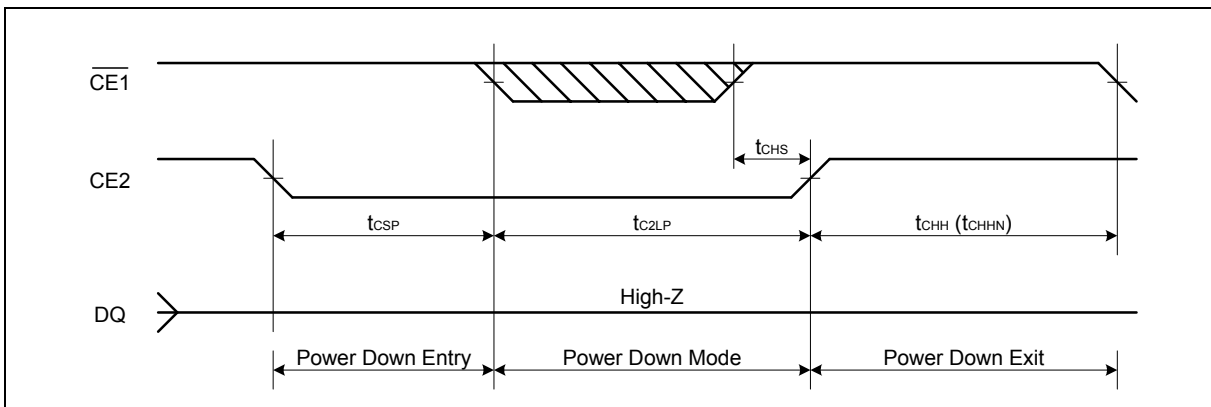
Timing Waveforms, continued

Power Down Program Timing



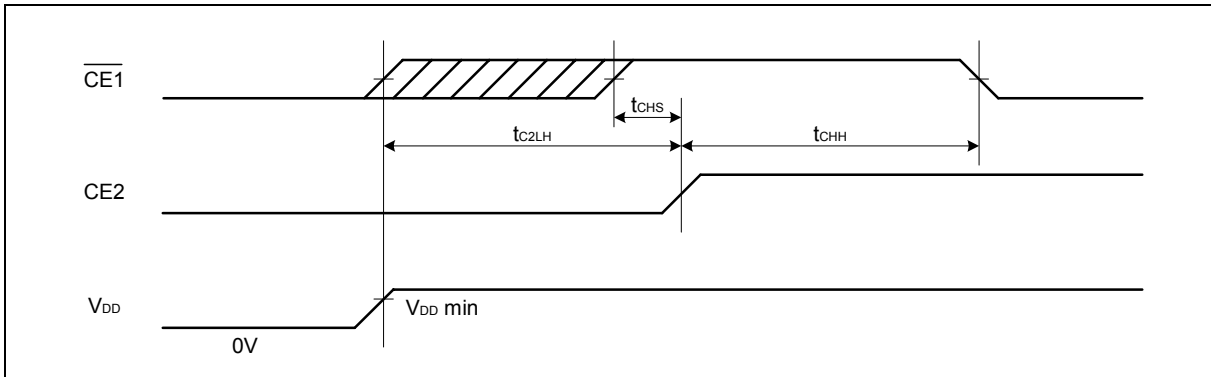
Note: CE2 must be High for Power Down Program operation.
Any other inputs not specified above can be either High or Low.

Power Down Entry and Exit Timing



Note: This Power Down mode can be also used for Power-up #2 below except that tCHHN can not be used at Power-up timing.

Power-up Timing #1

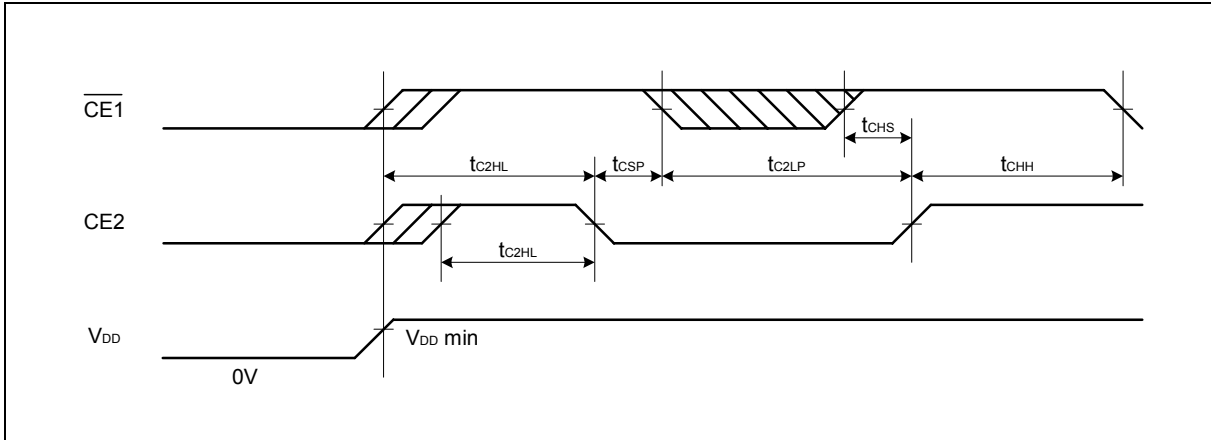


Note: The tC2LH specifies after VDD reaches specified minimum level.



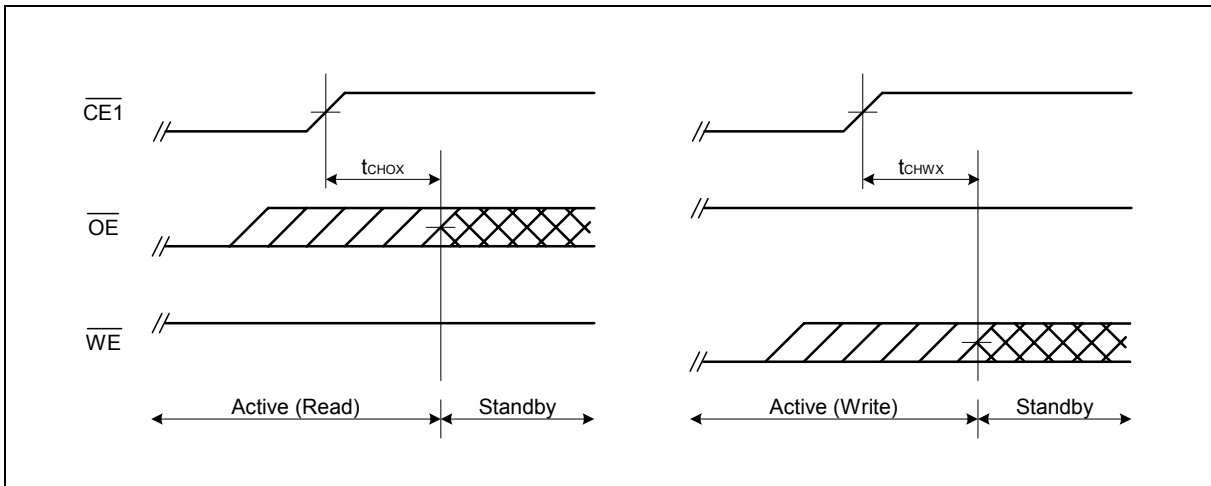
Timing Waveforms, continued

Power-up Timing #2



Note: The t_{c2HL} specifies from CE2 Low to High transition after V_{DD} reaches specified minimum level.
 $\overline{CE1}$ must be brought to High prior to or together with CE2 Low to High transition.

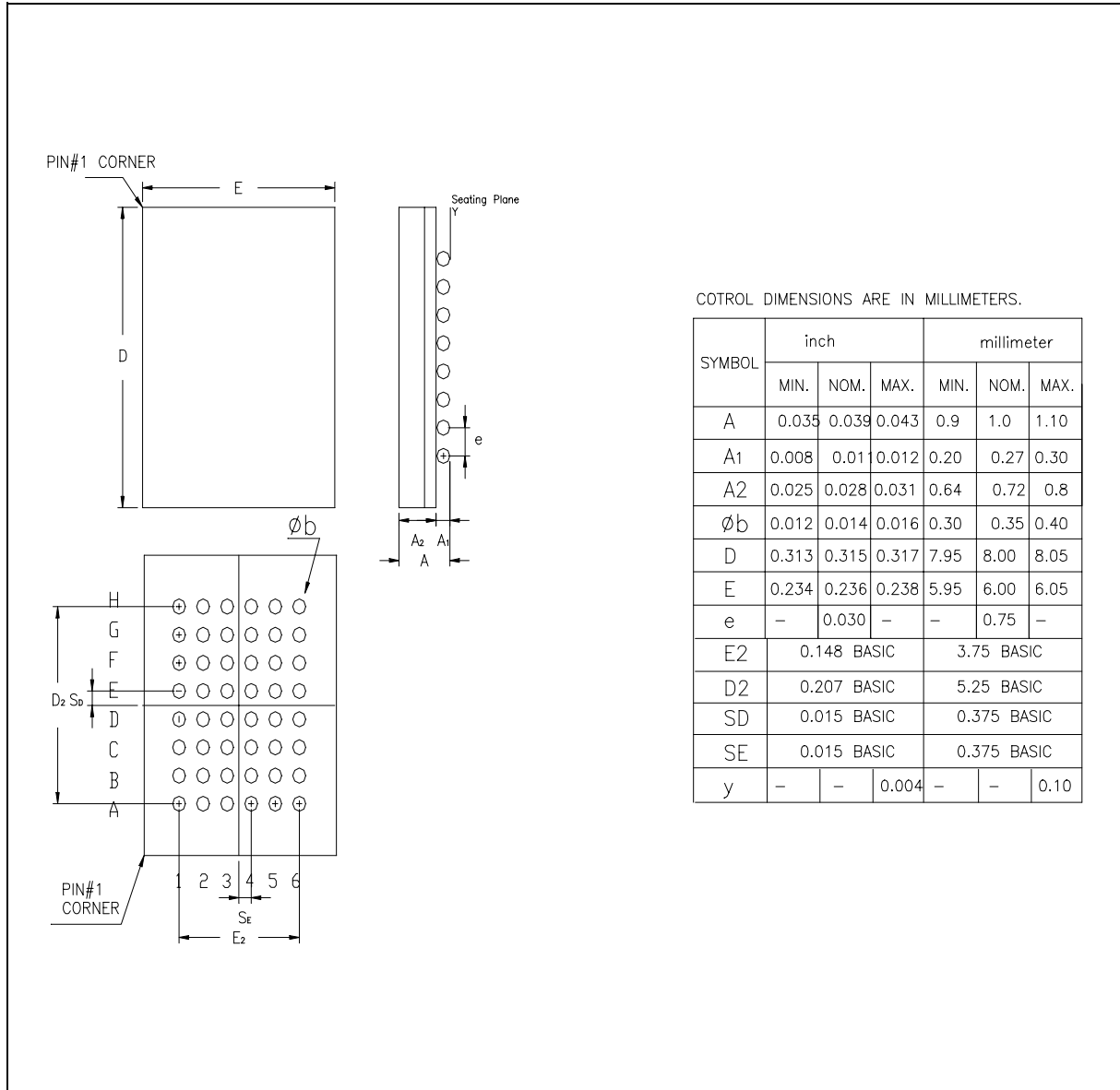
Standby Entry Timing after Read or Write



Note: Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes $t_{RC(min)}$ period from either last address transition of A0, A1 and A2, or $\overline{CE1}$ Low to High transition.

10. PACKAGE DIMENSION

TFBGA 48 Balls (6 x 8 mm², pitch 0.75 mm)





11. ORDERING INFORMATION

PART NO.	SPEED	OPERATING TEMPERATURE	PACKAGE
W963A6BBN70	70 nS	0 to 70	TFBGA 48, 6 mm x 8 mm, BALL PITCH 0.75 mm
W963A6BBN70E	70 nS	-25 to 85	TFBGA 48, 6 mm x 8 mm, BALL PITCH 0.75 mm
W963A6BBN70I	70 nS	-40 to 85	TFBGA 48, 6 mm x 8 mm, BALL PITCH 0.75 mm
W963A6BBN80	80 nS	0 to 70	TFBGA 48, 6 mm x 8 mm, BALL PITCH 0.75 mm
W963A6BBN80E	80 nS	-25 to 85	TFBGA 48, 6 mm x 8 mm, BALL PITCH 0.75 mm
W963A6BBN80I	80 nS	-40 to 85	TFBGA 48, 6 mm x 8 mm, BALL PITCH 0.75 mm

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.



12. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	March 10, 2003	-	Create new document



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