

MN103S97N

Type		MN103S97N (under development)	
Command ROM (×64-bit)		512 K-byte	
Data RAM (×32-bit)		24 K-byte	
Package		MBGA255-C-1111A *Lead-free	
Minimum Instruction Execution Time		16 ns (at 1.65 V to 1.95 V, 60 MHz)	
Interrupts		• RESET • IRQ × 11 • NMI • Key input • Timer × 40 • Input capture × 16 • PWM × 5 • SIF × 17 • DMA × 12 • WDT • A/D • System error	
Timer Counter		8-bit timer × 8 Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) 8-bit timer with PWM × 8 Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) PWM generating function 16-bit timer × 6 Up-down count Input capture function PWM generating function Compare/capture register 2-ch. 16-bit timer × 6 Reload-down count Watchdog timer × 1	
DMA Controller		Number of channels: 4 Unit of transfer: 8/16/32 bits Max. Transfer cycles: 65535 Staring factor: external interrupt, timer factor, PWM factor, serial transmission / reception factor, A/D conversion finish, software factor Transfer method: 2-bus cycle transfer Addressing modes: fixed, increment, decrement Transfer modes: word transfer, burst transfer, intermittent transfer	
Serial Interface		Serial 0, 1, 3 to 6: start-stop synchronization / synchronization commonly used, 6 lines Serial 2: start-stop synchronization / synchronization commonly used: 16 bytes containing transmission/reception FIFO I2CO: I ² C serial interface, multi master transmission/reception function	
I/O Pins	I/O	170	• Common use
	Input	25	• Common use
A/D Inputs		10-bit × 25-ch.	
PWM		12-, 14-bit resolution × 5-ch.	
ICR		28-bit × 13-ch. + 16-bit × 6-ch. (common with timer)	
OCR		16-bit × 12-ch. (common with timer)	
Timer Synchronous Output		4-bit (synchronous output) × 2-ch.	
ROM Collection		8-ch. (MN103SF66R : 12-ch.)	

Electrical Characteristics

Parameter		Symbol	Condition	Limit		Unit
				typ	max	
Operating Supply current	VDD	IDD1	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = 15 MHz, PLL = ON, LON = L	65(TBD)	100(TBD)	mA
	VDDH, AVDD	IDD6	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = 15 MHz, PLL = ON, LON = L	30(TBD)	55(TBD)	mA
Supply current at STOP	VDD	IDD5	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = oscillation stopped, LON = L Tj = 85°C		180(TBD)	μA
	VDDH, AVDD	VDD14	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = oscillation stopped, LON = L Tj = 85°C		10(TBD)	μA

(Ta = -20°C to +85°C, VSS = AVSS = 0.0 V)

A/D Converter Performance

Parameter	Condition	Limit			Unit
		min	typ	max	
Resolution				10	Bits
Non-linear error	AVDD = 3.3 V VSS = AVSS = 0.0 V			±4	LSB
A/D coversion time	IOCLK = 20 MHz, TAD = 200 ns	2.4			μs

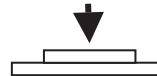
(Ta = 25°C, AVDD = 3.3 V, AVSS = 0.0 V)

TAD : A/D conversion clock cycle

Pin Assignment

N.D	PL4 / A12 / ADM12	PM1 / ICR1	PM0 / ICR0	PN0 / ICR8	PO1	PP4 / D4	PP7 / D7	PQ5 / D13	PQ7 / D15	PP5 / D5	PR5 / TM22IOB	PR7 / TM23IOB	PSS / BG	PT0 / A16	N.D	T
PL3 / A11 / ADM11	PL6 / A14 / ADM14	PM3 / ICR3	PM4 / ICR4	PM2 / ICR2	PN2 / ICR10	PP1 / D1	PQ1 / D9	PQ6 / D14	PR4 / TM22IOA	PR3 / TM21IOB	PS3 / WE2	PS2 / WDOVF	PT2 / A18	PU5 / A24 / K15	PU7 / K17	R
PK7 / A7 / ADM7	PL7 / A15 / ADM15	PM7 / ICR7	PM6 / ICR6	PM5 / ICR5	PN4 / ICR12	PP3 / D3	PQ3 / D11	PR1 / TM20IOB	PS1	PU1 / A20 / K11	PU3 / A22 / K13	PT1 / A17	PU2 / A21 / K12	P03 / D19 / SB11	PU0 / A19 / K10	P
PK5 / A5 / ADM5	PK4 / A4 / ADM4	PO0	PN1 / ICR9	PL5 / A13 / ADM13	PL1 / A9 / ADM9	PP0 / D0	PP6 / D6	PQ0 / D8	PQ4 / D12	PS4 / WE3	PR0 / TM20IOA	P01 / D17 / SB00	P05 / D21 / SBT1	P04 / D20 / SB01	P13 / D27 / SB03	N
PI5 / AS	PL0 / A8 / ADM8	PI3 / RE	PL2 / A10 / ADM10	PK6 / A6 / ADM6	PN3 / ICR11	PP2 / D2	PQ2 / D10	PR6 / TM23IOA	PR2 / TM21IOA	PS0 / PWM4	PU4 / A23 / K14	P07 / D23 / SB12	P12 / D26 / SB13	PU6 / A25 / K16	P00 / D16 / SB10	M
PI1 / CS1	PI4 / DK	PK3 / A3 / ADM3	PK1 / A1 / ADM1	PK2 / A2 / ADM2	PK0 / A0 / ADM0	VDDB	VDDB	VDDB	VSS	PS6 / BR	P10 / D24 / SBO2	P11 / D25 / SBT2	P14 / D28 / SBT3	P06 / D22	P02 / D18 / SBT0	L
*2 N.C [VREFH]	PI5 / RWSEL	PI1 / WE1	PI2 / SYSCLK	PI2 / CS2	PI0 / WE0	VSS	VDDH	VDD	VDD	P20 / SBI4	P21 / SBO4	*1 N.C (VDDH)	P16 / D30	VDDB	P15 / D29	K
AVDD	PG5 / AN21	PI0 / CS0	PI3 / CS3	PH0 / AN24	PI4 / CS4	VSS	VDDH	VDD	VSS	P31 / IRQ1	P36 / IRQ6	P24 / SBO5	P23 / SBI5	P22 / SBT4	P17 / D31	J
PG2 / AN18	PG4 / AN20	PG1 / AN17	PG6 / AN22	PG0 / AN16	PG3 / AN19	VSS	VDDH	VDD	VSS	P33 / IRQ3	P25 / SBT5	P34 / IRQ4	VSS	VDDH	OSCI	H
PF4 / AN12	PF0 / AN8	PG7 / AN23	PF6 / AN14	PF1 / AN9	PF5 / AN13	VSS	VDDH	VOUT	VSS	N.C ^{*3}	P35 / IRQ5	N.C ^{*3}	N.C ^{*3}	P32 / IRQ2	OSCO	G
PF2 / AN10	PE4 / AN4	PE7 / AN7	PE6 / AN6	PF3 / AN11	PE3 / AN3	P82 / SYOOT2	VSS	VSS	VSS	P41 / IRQ9	P37 / IRQ7	P50 / NMIRQ	MMOD1	P30 / IRQ0	N.C ^{*4}	F
PE2 / AN2	PE0 / AN0	PE1 / AN1	PF7 / AN15	PE5 / AN5	PB1 / TM11O / PWM2	P90 / SBI6	P80 / SYOOT0	P66 / TM36IO	P72 / TM12IO	N.C ^{*6} [TRCD1]	P70 / TM10IO	MMOD0	P53 / FRQS0	P42 / IRQ10	N.C ^{*5}	E
PD3 / TM25IOB	PD1 / TM24IOB	PCS / SCL0	PA0 / ADTRG	P94	P92 / SBT6	P84 / SY1OT0	P74 / TM14IO	P73 / TM13IO	P64 / TM34IO	P62 / TM32IO	N.C ^{*6} [EXTRG1]	N.C ^{*3}	P52 / EXMOD1	P51 / EXMOD0	P40 / IRQ8	D
PC1	AVSS	PD0 / TM24IOA	PB5 / TM5IO	PB7 / TM7IO	PB4 / TM4IO	P93	P85 / SY1OT1	P63 / TM33IO	N.C ^{*6} [EXTRG0]	N.C ^{*6} [TRCCLK]	TDO	N.C ^{*6} [TRCST]	NRST	FRQS1	N.D	C
PC3 / PWM0	PD2 / TM25IOA	PC4 / SDA0	PB3 / TM3IO	PB6 / TM6IO	P95	P87 / SY1OT3	P86 / SY1OT2	P75 / TM15IO	P65 / TM35IO	N.C ^{*6} [TRCD0]	P60 / TM30IO	N.C ^{*6} [TRCD3]	TMS	TRST	CKSEL / P55	B
N.D	PC2	PC0	PB2 / TM2IO / PWM3	PB0 / TM0IO / PWM1	P91 / SBO6	P83 / SYOOT3	P81 / SYOOT1	P71 / TM11IO	P67 / TM37IO	P61 / TM31IO	N.C ^{*6} [TRCD2]	TCK	TDI	LON	N.D	A
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Perspective



MBGA255-C-1111A *Lead-free

* ND has an electrode (pin) but NC is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

Each of VDD, VDDB, VDDH, and VSS has multiple electrodes (pins). Connect the same electrode names to the same power supply.

[]: Not available with MN103S97N.

*1 Connect the K4 pin to the VDDH power for the MN103SF66R.

*2 Connect the K16 pins to the AVDD power for the MN103SF66R.

*3 D4, G3, G4 and G6 pins have signal electrodes for the MN103SF66R. Perform the necessary pin processing.

*4 F1 pin should be pull-down, or pull-up to the VDDH power for the MN103SF66R.

*5 E1 pin should be open for the MN103SF66R.

*6 A5, B4, B6, C4, C6, C7, D5 and E6 pins are debugging pins. Perform the necessary pin processing.

Support Tool

■ On-board Development Tools	PX-ODBAMD (on-board debug unit)	
■ Flash Memory Built-in Type	Type	MN103SF66R (under development)
	Command ROM (× 64-bit)	1024 K-byte
	Data RAM (× 32-bit)	40 K-byte
	Minimum instruction execution time	16 ns (at 1.65 V to 1.95 V, 60 MHz)
	Package	MBGA255-C-1111A *Lead-free

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