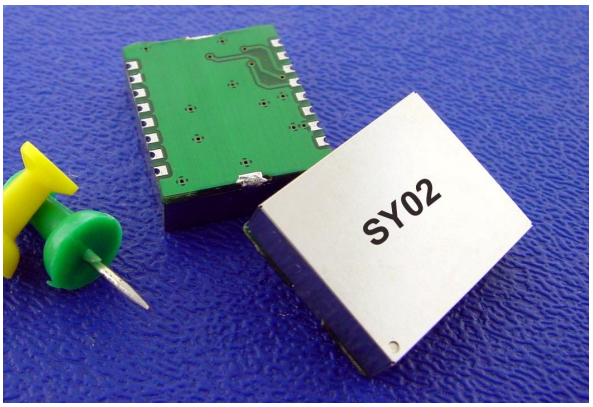
SY02-FEC

Date: January 7, 2003



• INTRODUCTION

The SY02-FEC is a high frequency crystal-based PLL synchronizer designed as a module level subsystem for easy incorporation into telecommunication equipment SONET/SDH/ATM/DWDM. Supports FEC (forward error Correction) or OC-N Frequencies.

• FEATURES

- Low jitter output from intrinsically low jitter VCXO or VCSO;
- User Selected one or two input references **up to 800MHz** (See Table on page 3)
- One high frequency LVPECL output with enable/disable function **up to 800MHz** (pre-select frequency value – upon order)
- Alarms status and VCXO monitor;
- The unit changes timing modes in response to external events;
- J-TAG service port for re-programming and servicing;
- 3.3V DC power supply
- Small dimensions: 0.8” x 1.00”

• APPLICATIONS

- ATM
- SDH
- PDH
- SONET
- DWDM
- FEC
- Other telecommunication equipment.

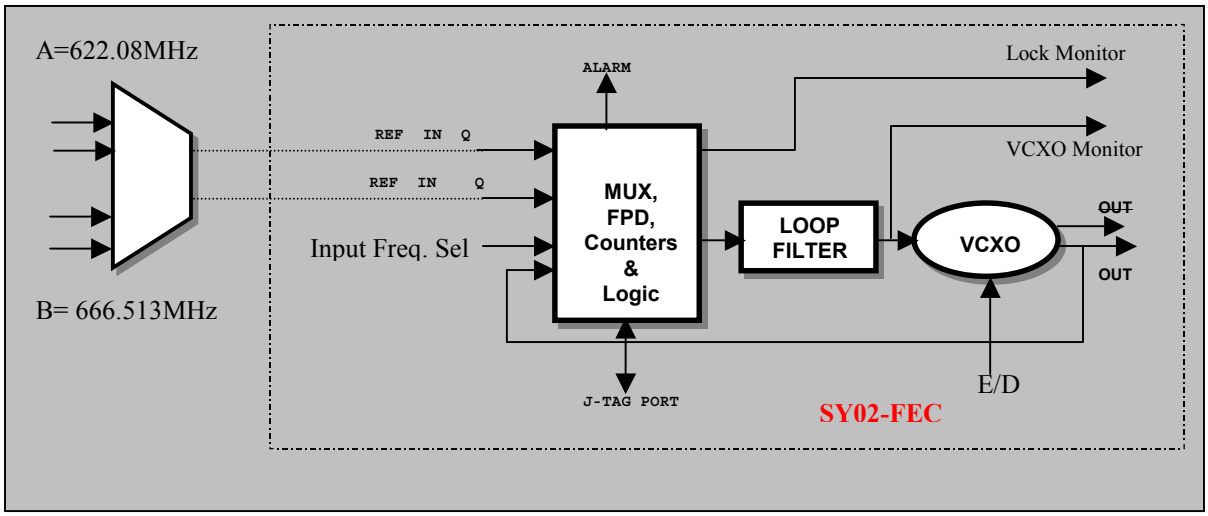


Figure 1 – Block Diagram (*Components outside the dotted line are user supplied)**

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• DESCRIPTION

The SY02-FEC is a High Frequency Phase Lock Loop has been designed as a module level subsystem for easy incorporation into telecommunication equipment. The module generates the high frequency (up to 800MHz) output from a low jitter VCXO (Crystal Based Oscillator) or VCSO (SAW based oscillators). The output can be disabled externally by setting OUTEN pin high. The SY02-FEC can be locked to a user defined input reference/s signal/s **(from 1.024MHz to 800MHz…for options please see table)**. Raltron's SY02-FEC device could be used as a frequency translator in PLL circuits or frequency re-generator device in cases where jitter cleaning and filtering is required. The module has a fast locking time and tolerates reference inputs with different duty cycles. The loop bandwidth is optimized in accordance with the VCXO used and required output performance. The ALARM output signals monitor the status of the phase lock loop and indicates LOLD (Loss of Lock Detect). If the reference REF IN is absent, the SY02-FEC will automatically switch to free run mode and LOLD will show "0" logic level. The SMD package dimensions are 0.80"x1.00" inch and powered by a supply of 3.3V.

- ALARM STATES

LOLD	ALARM
0	Module in Free-run
1	Module locked

- Input Reference Control select

CNT	Selected Option
0	Regenerated 622.08MHz into 622.08MHz
1	Translates 666.5143MHz into 622.08MHz

• PIN DESCRIPTION

	Name	Description	Signal Technology	VL			VH/ DC Voltage		
				Min	Typ	Max	Min	Typ	Max
1	Ref In	Input Reference Signal	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885
2	$\overline{\text{Ref In}}$	Input Reference Complimentary signal	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885
3	LOL	Lock Detect Alarm out – High when locked; Low when unlocked	DC	0	0.15	0.3	2.97	3.3	3.465
4	MNTR	VCXO Monitor out- DC control voltage offset indicator (when locked shall be within); 0.3<Vmntr<3.0 (for 3.3V supply)	DC				0.3<Vmntr<3.0		
6	N/C	No Connect	-----	-----	-----	----	------	------	------
7	GND	Ground	-----	-----	-----	----	------	------	------
8	Enable/Disable	Output Enable - > enables the output, active high or floating Disables the output, active low	DC	0	0.15	0.3	2.97	3.3	3.465
9	OUT	Oscillator Output -> Output of the module	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885
10	$\overline{\text{OUT}}$	Oscillator Complementary Output -> Output of the module	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885
11	N/C	No Connect	-----	-----	-----	----	------	------	------
12	CNT	Frequency Select; Low-Primary Frequency; High Secondary Frequency	DC	0	0.15	0.3	2.97	3.3	3.465
13	N/C	No Connect	-----	-----	-----	----	------	------	------
14	N/C	No Connect	-----	-----	-----	----	------	------	------
15	GND	Ground	-----	-----	-----	----	------	------	------
16	Vcc	Positive supply voltage	DC – 3.3V	-----	-----	----	2.97	3.3	3.465

• ORDERING INFORMATION

- Input/Output Frequencies available;

Frequency	Suffix	Frequency	Suffix
77.7600MHz	O3	168.0407MHz	C2
78.125MHz	B3	175.0000MHz	C3
78.6432MHz	B4	178.9440MHz	C4
82.9440MHz	B5	184.3200MHz	C5
92.6000MHz	U3	311.0400MHz	O6
100.000MHz	B6	622.0800MHz	O7
112.000MHz	B7	625.000MHz	C8
114.000MHz	B8	644.5312MHz	C9
125.000MHz	G2	666.5143MHz	C10
133.000MHz	G4	669.1281MHz	F1
139.264MHz	E6	669.3266MHz	F2
155.520MHz	O4	690.5692MHz	F3
156.250MHz	G6	710.9486MHz	F4
161.1328MHz	B9	719.7344MHz	F5
166.6286MHz	B10	777.6000MHz	F6
167.3316MHz	C1		

- **P/N System**

SY02-FEC – IP <Primary Input Frequency> - IS<Second Input Freq.>-OU<Output>S-T<Temp>

- See above Chart
If not listed Place **NL** and state the Freq.)

- See above chart (If not listed place **NL** and state the Freq. - must be higher in value than the primary Input reference)
If second Freq. Not applied place **NA**

- See above Chart
If not listed Place **NL** and state the Freq.)

- Supply Voltage;

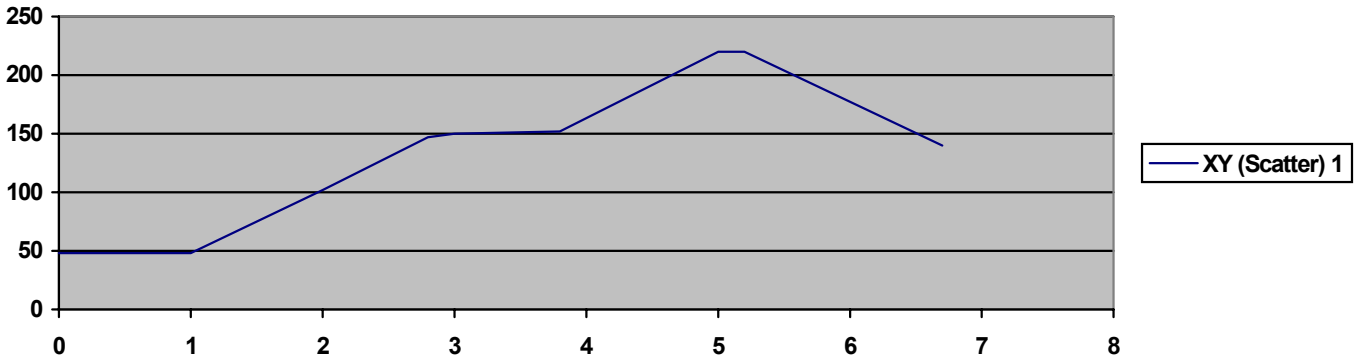
  4 – 3.3V

- Operating Temperature Range;
  C - 0°C to 70°C
  I - -40°C to +85°C

- **SPECIFICATION**

General Specifications	Mechanical	**1.000" x 0.800"x0.235"**	**SMT Module FR4 16 pins dual-in-line**
	Power Environment Internal Oscillators	3.3VDC +/-5%, <200mA Operating Temperature Humidity VCXO or VCSO	Regulated 0°C to 70°C or -40°C to +85°C 5% to 95% non-condensing Depends on the frequency
Input Signals	Number of Reference Inputs	2	
	Input reference frequency Signal Level	Per selected table on page 3 LVPECL	(other input frequencies available) Voh; 2.272V min ; Vol; 1.68Vmax
Output Signals	Number of Outputs	1	
	Output 1	Per selected table on page 3	other frequency contact Raltron
	Output 1 Signal Level	LVPECL (W/ Complimentary option)	Voh; 2.272V min ; Vol; 1.68Vmax
	Duty Cycle	50+/-10%	50%+/-5% available upon request
	Tracking/Capture Range	±50ppm APR min	
Signal Quality Performance	Jitter generation	<0.001UI RMS <0.001UI RMS <0.0001 UI RMS <0.0001 UI RMS	HPF 30Hz HPF 500Hz HPF 12KHz HPF 100KHz
	Jitter attenuation	-40dB -10dB	Fj=10Hz~1KHz Fj=1KHz~10MHz
	Jitter tolerance	2 µs, 10 Hz (0.05 UI @ 8KHz)	

- **REFLOW PROFILE**



- **OUTLINE DRAWING**