SONY

CXD3017Q

CD Digital Signal Processor with Built-in Digital Servo and DAC

Description

The CXD3017Q is a digital signal processor LSI for CD players. This LSI incorporates a digital servo, digital filter, zero detection circuit, 1-bit DAC and analog low-pass filter.

Features

Digital Signal Processor (DSP) Block
- 1×, 2×, 4× speed playback supported
- 16K-RAM
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- SEC strategy-based error correction
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry compensation circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Digital audio interface outputs
- Digital level meter, peak meter
- CD TEXT data demodulation

Digital Servo (DSSP) Block
- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment function
- Surf jump function supporting micro two-axis
- Tracking filter: 6 stages, focus filter: 5 stages

Digital Filter, DAC and Analog Low-pass Filter Blocks
- DBB (digital bass boost) function
- Double-speed playback supported
- Digital de-emphasis
- Digital attenuation
- 8Fs oversampling filter

Applications
CD players

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80 pin LQFP (Plastic)
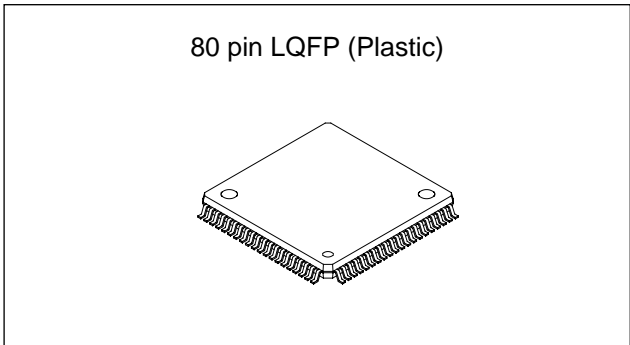
Structure
Silicon gate CMOS IC

Absolute Maximum Ratings
- Supply voltage V_{DD} −0.5 to +4.6   V
- Input voltage V_I −0.5 to +4.6   V
        (V_{SS} − 0.5V to V_{DD} + 0.5V)
- Output voltage V_O −0.5 to +4.6   V
        (V_{SS} − 0.5V to V_{DD} + 0.5V)
- Storage temperature T_{stg} −55 to +150   °C
- Supply voltage difference
        V_{SS} − AV_{SS} −0.3 to +0.3   V
        V_{DD} − AV_{DD} −0.3 to +0.3   V

Note) AV_{DD} includes XV_{DD} and AV_{SS} includes XV_{SS}.

Recommended Operating Conditions
- Supply voltage V_{DD} 2.7 to 3.6   V
- Operating temperature
        T_{opr} −20 to +75   °C

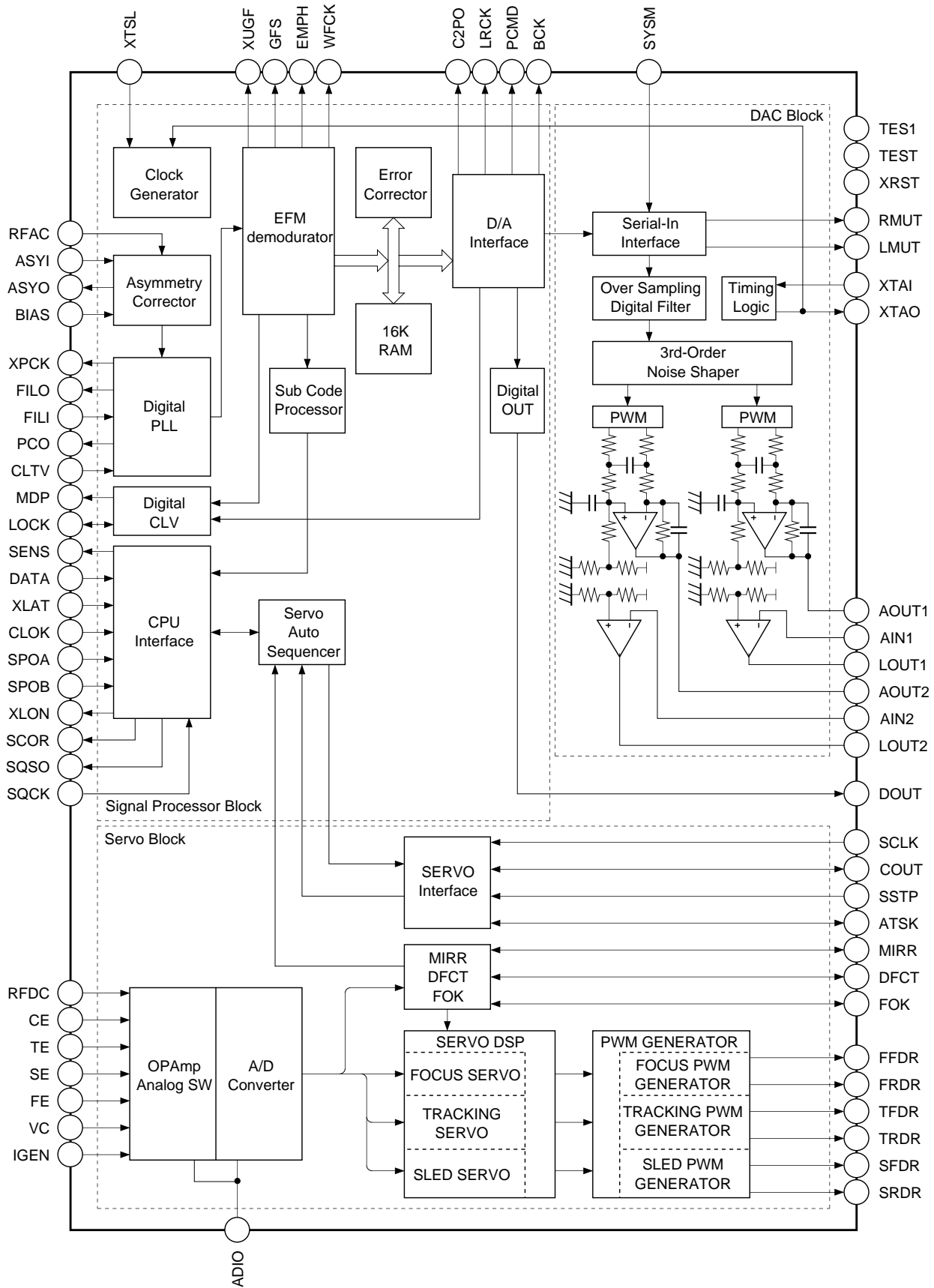| Playback speed	V_{DD} [V]	
	CD-DSP block	DAC block
4×	2.7 to 3.6	
2×	2.7 to 3.6	2.7 to 3.6
1×	2.7 to 3.6	2.7 to 3.6

I/O Capacitance
- Input pin C_I 9 (Max.)   pF
- Output pin C_O 11 (Max.)   pF
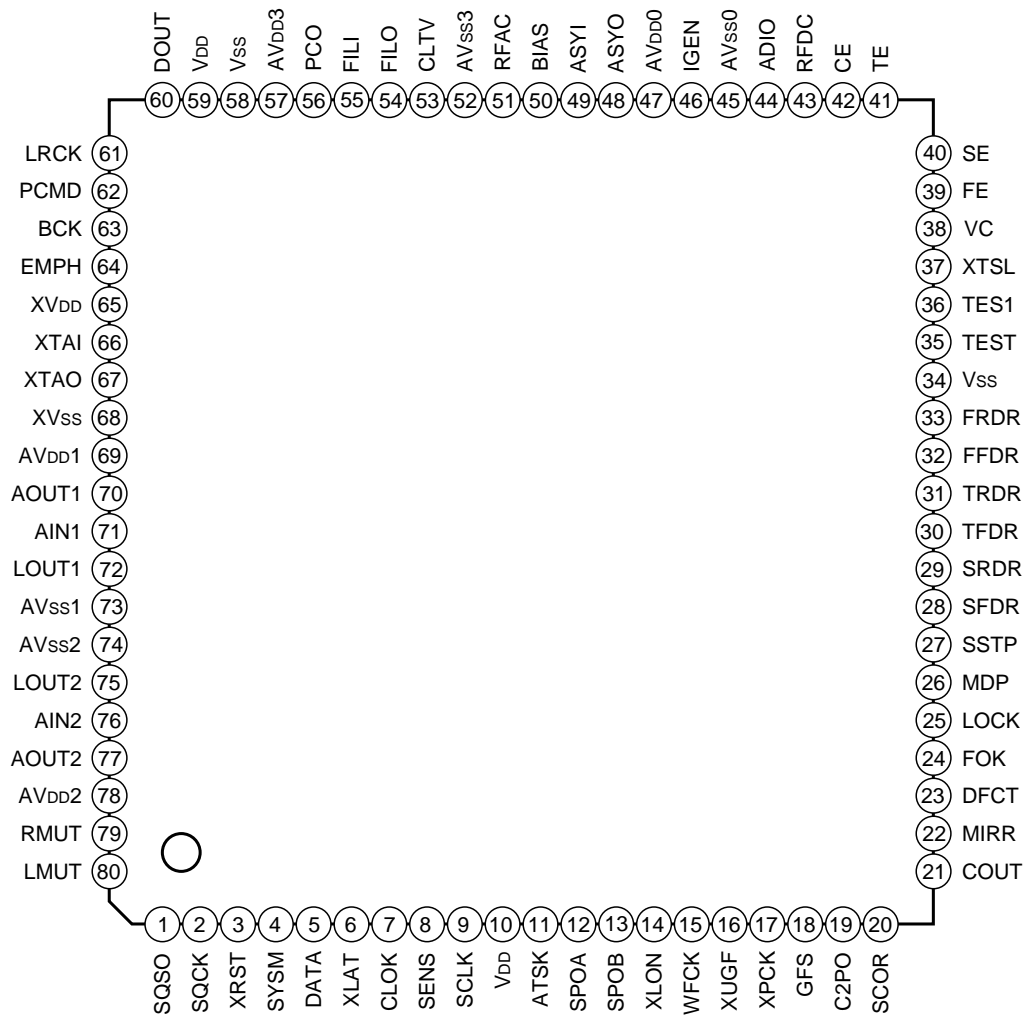- I/O pin $C_{I/O}$ 11 (Max.)   pF

Note) Measurement conditions $V_{DD} = V_I = 0V$
                       $f_M = 1MHz$

E99Y24B13

Block Diagram

Pin Configuration

Pin	Name
60	DOUT
59	VDD
58	VSS
57	AVDD3
56	PCO
55	FILI
54	FILO
53	CLTV
52	AVSS3
51	RFAC
50	BIAS
49	ASYI
48	ASYO
47	AVDD0
46	IGEN
45	AVSS0
44	ADIO
43	RFDC
42	CE
41	TE

Pin	Name
61	LRCK
62	PCMD
63	BCK
64	EMPH
65	XVDD
66	XTAI
67	XTAO
68	XVSS
69	AVDD1
70	AOUT1
71	AIN1
72	LOUT1
73	AVSS1
74	AVSS2
75	LOUT2
76	AIN2
77	AOUT2
78	AVDD2
79	RMUT
80	LMUT

Pin	Name
40	SE
39	FE
38	VC
37	XTSL
36	TES1
35	TEST
34	VSS
33	FRDR
32	FFDR
31	TRDR
30	TFDR
29	SRDR
28	SFDR
27	SSTP
26	MDP
25	LOCK
24	FOK
23	DFCT
22	MIRR
21	COUT

Pin	Name
1	SQSO
2	SQCK
3	XRST
4	SYSM
5	DATA
6	XLAT
7	CLOK
8	SENS
9	SCLK
10	VDD
11	ATSK
12	SPOA
13	SPOB
14	XLON
15	WFCK
16	XUGF
17	XPCK
18	GFS
19	C2PO
20	SCOR

Pin Description

Pin No.	Symbol	I/O	Output values	Description
1	SQSO	O	1, 0	Sub Q 80-bit, PCM peak and level data outputs. CD TEXT data output.
2	SQCK	I		SQSO readout clock input.
3	XRST	I		System reset. Reset when low.
4	SYSM	I		Mute input. Muted when high.
5	DATA	I		Serial data input from CPU.
6	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
7	CLOK	I		Serial data transfer clock input from CPU.
8	SENS	O	1, 0	SENS output to CPU.
9	SCLK	I		SENS serial data readout clock input.
10	V_{DD}	—	—	Digital power supply.
11	ATSK	I/O	1, 0	Anti-shock input/output.
12	SPOA	I		Microcomputer extension interface (input A)
13	SPOB	I		Microcomputer extension interface (input B)
14	XLON	O	1, 0	Microcomputer extension interface (output)
15	WFCK	O	1, 0	WFCK output.
16	XUGF	O	1, 0	XUGF output. MINT1 or RFCK is output by switching with the command.
17	XPCK	O	1, 0	XPCK output. MNT0 is output by switching with the command.
18	GFS	O	1, 0	GFS output. MNT3 or XROF is output by switching with the command.
19	C2PO	O	1, 0	C2PO output. GTOP is output by switching with the command.
20	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
21	COUT	I/O	1, 0	Track count signal input/output.
22	MIRR	I/O	1, 0	Mirror signal input/output.
23	DFCT	I/O	1, 0	Defect signal input/output.
24	FOK	I/O	1, 0	Focus OK signal input/output.
25	LOCK	I/O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Or input when LKIN = 1.
26	MDP	O	1, Z, 0	Spindle motor servo control output.
27	SSTP	I		Disc innermost track detection signal input.
28	SFDR	O	1, 0	Sled drive output.
29	SRDR	O	1, 0	Sled drive output.
30	TFDR	O	1, 0	Tracking drive output.
31	TRDR	O	1, 0	Tracking drive output.
32	FFDR	O	1, 0	Focus drive output.
33	FRDR	O	1, 0	Focus drive output.
34	V_{SS}	—	—	Digital GND.

Pin No.	Symbol	I/O	Output values	Description
35	TEST	I		Test pin. Normally, GND.
36	TES1	I		Test pin. Normally, GND.
37	XTSL	I		Crystal selection input. Low when the crystal is 16.9344MHz; high when the crystal is 33.8688MHz.
38	VC	I		Center voltage input.
39	FE	I		Focus error signal input.
40	SE	I		Sled error signal input.
41	TE	I		Tracking error signal input.
42	CE	I		Center servo analog input.
43	RFDC	I		RF signal input.
44	ADIO	O	Analog	Test pin. No connected.
45	AV$_{SS}$0	—	—	Analog GND.
46	IGEN	I		Operational amplifier constant current input.
47	AV$_{DD}$0	—	—	Analog power supply.
48	ASYO	O	1, 0	EFM full-swing output. (low = Vss, high = V$_{DD}$)
49	ASYI	I		Asymmetry comparator voltage input.
50	BIAS	I		Asymmetry circuit constant current input.
51	RFAC	I		EFM signal input.
52	AV$_{SS}$3	—	—	Analog GND.
53	CLTV	I		Multiplier VCO1 control voltage input.
54	FILO	O	Analog	Master PLL filter output. (slave = digital PLL)
55	FILI	I		Master PLL filter input.
56	PCO	O	1, Z, 0	Master PLL charge pump output.
57	AV$_{DD}$3	—	—	Analog power supply.
58	V$_{SS}$	—	—	Digital GND.
59	V$_{DD}$	—	—	Digital power supply.
60	DOUT	O	1, 0	Digital Out output.
61	LRCK	O	1, 0	D/A interface. LR clock output f = Fs.
62	PCMD	O	1, 0	D/A interface. Serial data output. (two's complement, MSB first)
63	BCK	O	1, 0	D/A interface. Bit clock output.
64	EMPH	O	1, 0	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
65	XV$_{DD}$	—	—	Master clock power supply.
66	XTAI	I		Crystal oscillation circuit input. Master clock is externally input from this pin.
67	XTAO	O		Crystal oscillation circuit output.
68	XV$_{SS}$	—	—	Master clock GND.

Pin No.	Symbol	I/O	Output values	Description
69	AVDD1	—	—	Analog power supply.
70	AOUT1	O		L ch analog output.
71	AIN1	I		L ch operational amplifier input.
72	LOUT1	O		L ch LINE output.
73	AVss1	—	—	Analog GND.
74	AVss2	—	—	Analog GND.
75	LOUT2	O		R ch LINE output.
76	AIN2	I		R ch operational amplifier output.
77	AOUT2	O		R ch analog output.
78	AVDD2	—	—	Analog power supply.
79	RMUT	O	1, 0	R ch zero detection flag.
80	LMUT	O	1, 0	L ch zero detection flag.

Notes) • PCMD is a MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- XPCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136μs.
- C2PO represents the data error status.
- XROF is generated when the 16K RAM exceeds the ±4F jitter margin.

Monitor Pin Output Combinations

Command bit		Output data			
MTSL1	MTSL0				
0	0	XUGF	XPCK	GFS	C2PO
0	1	MNT1	MNT0	MNT3	C2PO
1	0	RFCK	XPCK	XROF	GTOP

Electrical Characteristics

1. DC Characteristics

$(V_{DD} = AV_{DD} = 3.3 \pm 0.3V,\ V_{SS} = AV_{SS} = 0V,\ T_{opr} = -20\ \text{to}\ +75°C)$

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level	V_{IH1}		$0.7V_{DD}$			V	*1, *9
	Low level	V_{IL1}				$0.2V_{DD}$	V	
Input voltage (2)	High level	V_{IH2}	$V_I \leq 5.5V$	$0.8V_{DD}$			V	*2
	Low level	V_{IL2}				$0.2V_{DD}$	V	
Input voltage (3)	High level	V_{IH3}	$V_I \leq 5.5V$ Schmitt input	$0.8V_{DD}$			V	*3
	Low level	V_{IL3}				$0.2V_{DD}$	V	
Input voltage (4)		V_{IN4}	Analog input	V_{SS}		V_{DD}	V	*4, *5
Output voltage (1)	High level	V_{OH1}	$I_{OH} = -4mA$ $I_{OL} = 4mA$	$V_{DD} - 0.4$		V_{DD}	V	*6, *8, *9
	Low level	V_{OL1}		0		0.4	V	
Output voltage (2)	High level	V_{OH2}	$I_{OH} = -0.28mA$ $I_{OL} = 0.36mA$	$V_{DD} - 0.5$		V_{DD}	V	*7
	Low level	V_{OL2}		0		0.4	V	
Input leak current (1)		I_{LI1}	$V_I = V_{SS}$ or V_{DD}	−10		10	µA	*1
Input leak current (2)		I_{LI2}	$V_I = 0$ to $5.5V$	−10		10	µA	*2, *3
Input leak current (3)		I_{LI3}	$V_I = V_{SS}$ or V_{DD}	−40		40	µA	*9
Input leak current (4)		I_{LI4}	$V_I = 0.25V_{DD}$ to $0.75V_{DD}$	−40		40	µA	*5
Tri-state pin output leak current		I_{LO}	$V_I = V_{SS}$ or V_{DD}	−40		40	µA	*8

1-1. Applicable pins and classification

*1 CMOS level input pins (1):
     TEST, TES1
*2 CMOS level input pins (2):
     SYSM, DATA, XLAT, SSTP, XTSL
*3 CMOS Schmitt input pins:
     SQCK, XRST, CLOK, SCLK, SPOA, SPOB
*4 Analog input pins (1):
     ASYI, CLTV, FILI, RFAC
*5 Analog input pins (2):
     VC, FE, SE, TE, CE, RFDC
*6 Normal output pins (1):
     SQSO, XLON, WFCK, XUGF, XPCK, GFS, C2PO, SCOR, SFDR, SRDR, TFDR, TRDR, FRDR, ASYO,
     DOUT, LRCK, PCMD, BCK, EMPH, RMUT, LMUT
*7 Normal output pin (2):
     FILO
*8 Tri-state output pins:
     SENS, MDP, FFDR, PCO
*9 Normal input/output pins:
     ATSK, COUT, MIRR, DFCT, FOK, LOCK

Note) When the external pull-down resistors are connected to the pins *2 and *3, the resistance applied to
        these pins should be 5kΩ or less in total.

2. AC Characteristics

(1) XTAI pin

(a) When using self-excited oscillation

(Topr = −20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(b) When inputting pulses to XTAI pin

(Topr = −20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1000	ns
Input high level	V_{IHX}	$0.7V_{DD}$			V
Input low level	V_{ILX}			$0.2V_{DD}$	V
Rise time, fall time	t_R, t_F			10	ns
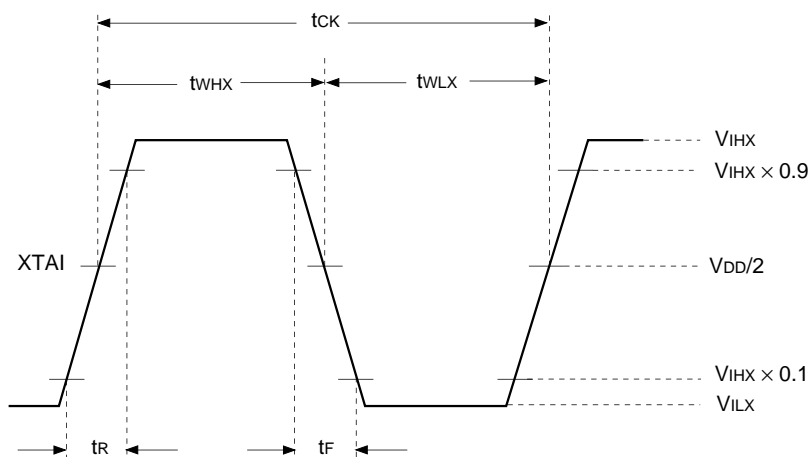
(c) When inputting sine waves to XTAI pin via a capacitor

(Topr = −20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	unit
Input amplitude	V_I	$0.5V_{DD}$		V_{DD} + 0.3	Vp-p

(2) CLOK, DATA, XLAT and SQCK pin

(V_{DD} = AV_{DD} = 3.3 ± 0.3V, V_{SS} = AV_{SS} = 0V, Topr = −20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
SQCK frequency	f_T			0.65 **Note)**	MHz
SQCK pulse width	t_{WT}	750 **Note)**			ns
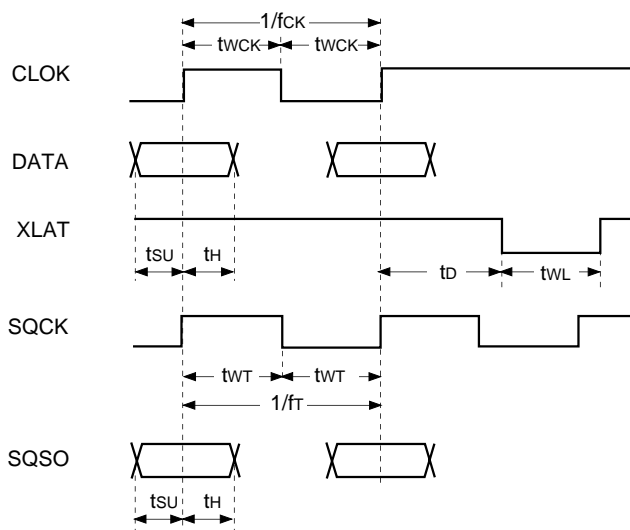
Note) In quasi double-speed playback mode, except when SQSO is Sub Q Read, the SQCK maximum operating frequency is 300kHz and its minimum pulse width is 1.5µs.
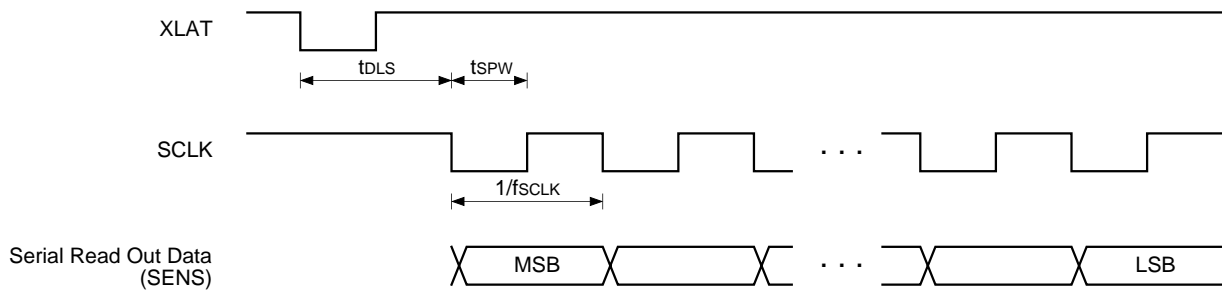
(3) SCLK pin

| Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			μs

(4) COUT, MIRR and DFCT pins

Operating frequency

$(V_{DD} = AV_{DD} = 3.3 \pm 0.3V, V_{SS} = AV_{SS} = 0V, T_{opr} = -20$ to $+75°C)$

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
COUT maximum operating frequency	f_{COUT}	40			kHz	*1
MIRR maximum operating frequency	f_{MIRR}	40			kHz	*2
DFCT maximum operating frequency	f_{DFCTH}	5			kHz	*3

*1 When using a high-speed traverse TZC.

*2
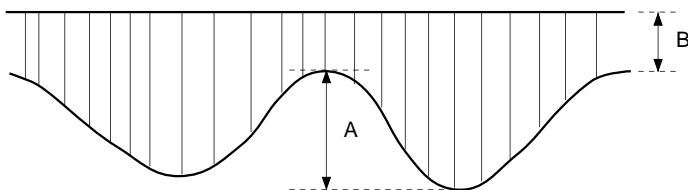
When the RF signal continuously satisfies the following conditions during the above traverse.

- $A = 0.11V_{DD}$ to $0.23V_{DD}$

- $\dfrac{B}{A + B} \le 25\%$

*3 During complete RF signal omission.
   When settings related to DFCT signal generation are Typ.

1-bit DAC and LPF Block Analog Characteristics

Analog characteristics (V_{DD} = AV_{DD} = 3.3V, V_{SS} = AV_{SS} = 0V, Ta = 25°C)

| Item	Symbol	Conditions	Crystal	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data	384Fs		0.0080	0.0120	%
			768Fs		0.0080	0.0120	
Signal-to-noise ratio	S/N	1kHz, 0dB data when AMUT ON (Using A-weighting filter)	384Fs	98	102		dB
			768Fs	98	102		

Fs = 44.1kHz in all cases.

The total harmonic distortion and signal-to-noise ratio measurement circuits are shown below.

Note) The external load capacitance connect to the LPF block should be 30pF or less in total.
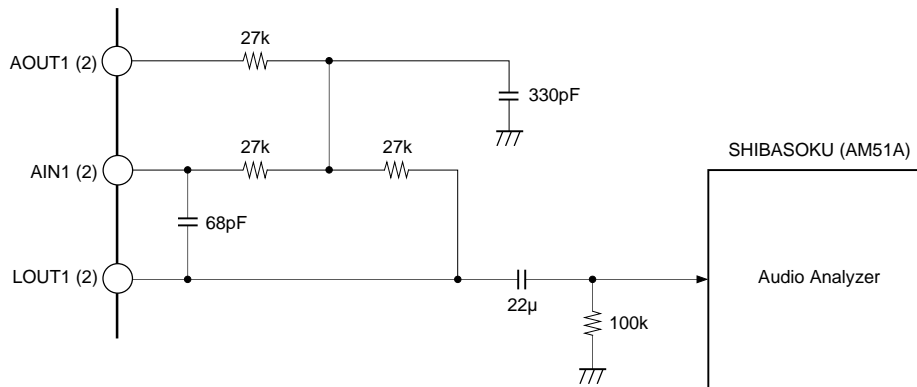
LPF external circuit diagram
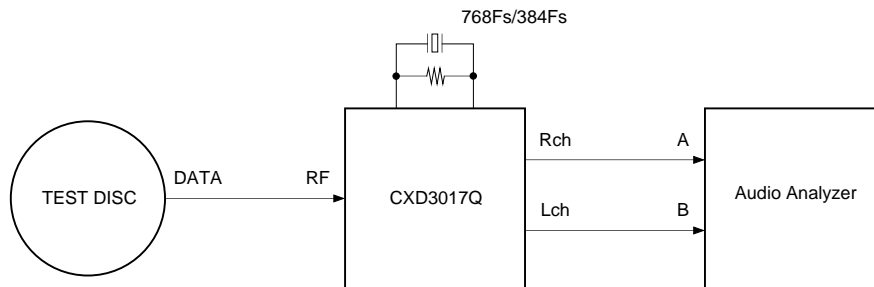
Block diagram of analog characteristics measurement

(V_{DD} = AV_{DD} = 3.3V, V_{SS} = AV_{SS} = 0V, Topr = −20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Applicable pins
Output voltage	V_{OUT}		0.71		Vrms	*1
Load resistance	R_L	20			kΩ	*1
Load capacitance	C_L			30	pF	*1, *2

* Measurement is conducted for the LPF external circuit diagram with the sine wave output of 1kHz and 0dB.

Applicable pins
*1 LOUT1, LOUT2
*2 AOUT1, AOUT2

Contents

Explanation of abbreviations   AVRG: Average
                               AGCNTL: Auto gain control
                               FCS: Focus
                               TRK: Tracking
                               SLD: Sled
                               DFCT: Defect

§1. CPU Interface

§1-1. CPU Interface Timing

• CPU interface
This interface uses DATA, CLOK and XLAT to set the modes.
The interface timing chart is shown below.
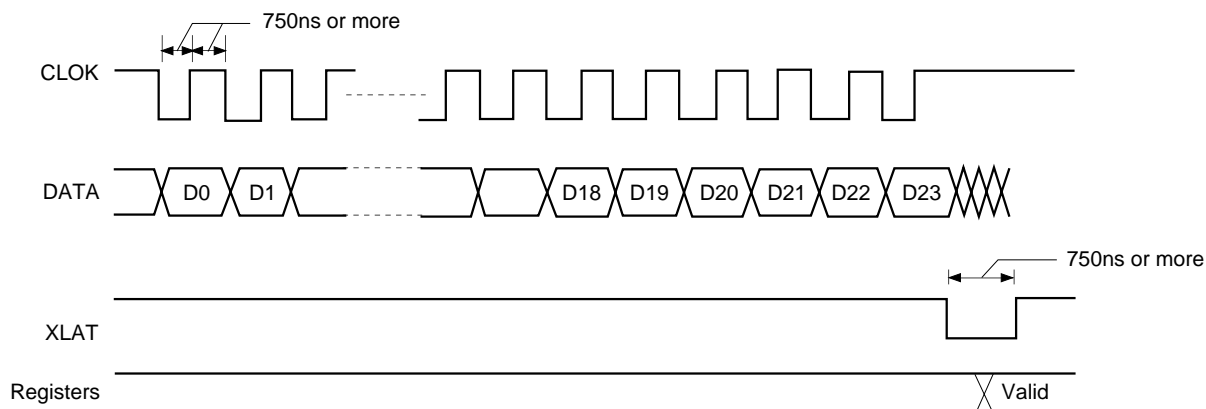
• The internal registers are initialized by a reset when XRST = 0.
Note) Be sure to set SQCK to high when XLAT is low.

§1-2. CPU Interface Command Table

Total bit length for each register

Register	Total bit length
0 to 2	8 bits
3	8 to 24 bits
4 to 6	8 bits
7	20 bits
8	28 bits
9	24 bits
A	28 bits
B	16 bits
C	8 bits
D	16 bits
E	20 bits

Command Table ($0X to 1X)

Register	Command	Address D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
0	FOCUS CONTROL	0 0 0 0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
			0	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEARCH VOLTAGE DOWN
			0	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEARCH VOLTAGE UP
			1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK ON
			0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK OFF
1	TRACKING CONTROL	0 0 0 1	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE ON
			—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE OFF
			—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN NORMAL
			—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP
			—	—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
			—	—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 2

—: Don't care

Command Table ($2X to 3X)

Register	Command	Address D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
				Data 1				Data 2				Data 3				Data 4				Data 5			
2	TRACKING MODE	0 0 1 0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF
			0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO ON
			1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD TRACK JUMP
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE TRACK JUMP
			—	—	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO OFF
			—	—	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO ON
			—	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD SLED MOVE
			—	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE SLED MOVE

Register	Command	Address D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
				Data 1				Data 2				Data 3				Data 4				Data 5			
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)
			0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±2 × basic value)
			0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±3 × basic value)
			0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±4 × basic value)

—: Don't care

Command Table ($340X)

Register	Command	Address 1 (D23 to D20)	Address 2 (D19 to D16)	Address 3 (D15 to D12)	Address 4				Data 1					Data 2			
					D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 0 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K00) SLED INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K01) SLED LOW BOOST FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K02) SLED LOW BOOST FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K03) SLED LOW BOOST FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K04) SLED LOW BOOST FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K05) SLED OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K06) FOCUS INPUT GAIN
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K07) SLED AUTO GAIN
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K08) FOCUS HIGH CUT FILTER A
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K09) FOCUS HIGH CUT FILTER B
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN

Command Table ($341X)

Register	Command	Address 1 D23 to D20	Address 2 D19 to D16	Address 3 D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 0 1	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K10) FOCUS PHASE COMPENSATE FILTER B
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K11) FOCUS OUTPUT GAIN
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K12) ANTI SHOCK INPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K13) FOCUS AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K14) HPTZC / AUTO GAIN HIGH PASS FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K15) HPTZC / AUTO GAIN HIGH PASS FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K16) ANTI SHOCK HIGH PASS FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K17) HPTZC / AUTO GAIN LOW PASS FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K18) FIX
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K19) TRACKING INPUT GAIN
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1A) TRACKING HIGH CUT FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1B) TRACKING HIGH CUT FILTER B
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1C) TRACKING LOW BOOST FILTER A-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1D) TRACKING LOW BOOST FILTER A-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1E) TRACKING LOW BOOST FILTER B-H
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1F) TRACKING LOW BOOST FILTER B-L

Note: Columns D11 to D8 form **Address 4**; columns D7 to D4 form **Data 1**; columns D3 to D0 form **Data 2**.

Command Table ($342X)

Register	Command	Address 1 (D23 to D20)	Address 2 (D19 to D16)	Address 3 (D15 to D12)	Address 4				Data 1				Data 2				
					D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 1 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K22) TRACKING OUTPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K23) TRACKING AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2E) Not used
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2F) Not used

Command Table ($343X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 1 1	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K30) SLED INPUT GAIN (when SFSK = 1 TG up2)
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K31) ANTI SHOCK LOW PASS FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K32) Not used
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K33) ANTI SHOCK HIGH PASS FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K34) ANTI SHOCK HIGH PASS FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K35) ANTI SHOCK FILTER COMPARATE GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K36) TRACKING GAIN UP2 HIGH CUT FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K37) TRACKING GAIN UP2 HIGH CUT FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K38) TRACKING GAIN UP2 LOW BOOST FILTER A-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K39) TRACKING GAIN UP2 LOW BOOST FILTER A-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3A) TRACKING GAIN UP2 LOW BOOST FILTER B-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3B) TRACKING GAIN UP2 LOW BOOST FILTER B-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3C) TRACKING GAIN UP PHASE COMPENSATE FILTER A
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3D) TRACKING GAIN UP PHASE COMPENSATE FILTER B
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3E) TRACKING GAIN UP OUTPUT GAIN
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3F) Not used

Command Table ($344X)

Register	Command	Address 1 D23 to D20	Address 2 D19 to D16	Address 3 D15 to D12	Address 4 D11	D10	D9	D8	Data 1 D7	D6	D5	D4	D3	Data 2 D2	D1	D0	Description
3	SELECT	0 0 1 1	0 1 0 0	0 1 0 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K40) TRACKING HOLD FILTER INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K41) TRACKING HOLD FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K42) TRACKING HOLD FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K43) TRACKING HOLD FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K44) TRACKING HOLD FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K45) TRACKING HOLD FILTER OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K46) TRACKING HOLD FILTER INPUT GAIN (when THSK = 1 TG up2)
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K47) Not used
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K48) FOCUS HOLD FILTER INPUT GAIN
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K49) FOCUS HOLD FILTER A-H
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4A) FOCUS HOLD FILTER A-L
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4B) FOCUS HOLD FILTER B-H
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4C) FOCUS HOLD FILTER B-L
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4D) FOCUS HOLD FILTER OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4E) Not used
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4F) Not used

Command Table ($348X to 34FX)

Register	Command	Address 1	Address 2	Address 3				Data 1				Data 2				Data 3				
		D23 to D20	D19 to D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	1	0	0	0	0	0	PFOK1	PFOK0	0	0	0	MRS	MRT1	MRT0	0	0	PFOK, RFAC
				1	0	1	1	SFBK1	SFBK2	0	0	0	0	0	0	0	0	0	0	Booster Surf Brake
				1	1	0	0	THBON	FHBON	TLB1ON	FLB1ON	TLB2ON	0	HBST1	HBST0	LB1S1	LB1S0	LB2S1	LB2S0	Booster
				1	1	1	0	IDFS3	IDFS2	IDFS1	IDFS0	0	0	IDFT1	IDFT0	0	0	0	INVRFDC	DFCT
				D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
								1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—	FCS Bias Limit
				1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—	FCS Bias Data
				1	1	0	0	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0	Traverse Center Data

Command Table ($35X to 3FX)

Register 3 — SELECT — D23 to D20 = 0 0 1 1

Command (function)	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
System GAIN	1	1	1	1	1	0	0	0	SYG3	SYG2	SYG1	SYG0	FZB3	FZB2	FZB1	FZB0	FZA3	FZA2	FZA1	FZA0
FOCUS SEARCH SPEED/VOLTAGE/AUTO GAIN	0	1	0	1	FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0
DTZC/TRACK JUMP VOLTAGE/AUTO GAIN	0	1	1	0	0	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0
FZSL/SLED MOVE/Voltage/AUTO GAIN	0	1	1	1	FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT
LEVEL/AUTO GAIN/DFSW/ (Initialize)	1	0	0	0	VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0
SERIAL DATA READ MODE/SELECT	1	0	0	1	DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0	0	0	0	0	0	0	0	0
FOCUS BIAS	1	0	1	0	0	FBON	0	0	0	0	FZC	0	FPS1	FPS0	TPS1	TPS0	SVDA	0	0	0
Operation for MIRR/ DFCT/FOK	1	0	1	1	SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	0	0	0	0	0	0	0	0
TZC/COUT BOTTOM/MIRR	1	1	0	0	COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0
SLED FILTER	1	1	0	1	SFID	SFSK	THID	THSK	ABEF	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0
Filter	1	1	1	0	F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D
Others	1	1	1	1	0	AGG4	XT4D	XT2D	AGSD	DRR2	DRR1	DRR0	0	ASFG	FTQ	1	SRO1	0	AGHF	ASOT

—: Don't care

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Instruction Table

Register	Command	Addr D3	Addr D2	Addr D1	Addr D0	D1 D3	D1 D2	D1 D1	D1 D0	D2 D3	D2 D2	D2 D1	D2 D0	D3 D3	D3 D2	D3 D1	D3 D0	D4 D3	D4 D2	D4 D1	D4 D0	D5 D3	D5 D2	D5 D1	D5 D0	D6 D3	D6 D2	D6 D1	D6 D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C)	0	1	0	1	0.18ms	0.09ms	0.05ms	0.02ms	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	Brake (B)					0.36ms	0.18ms	0.09ms	0.05ms	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	Kick (D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	—	—	—	—	—	—	—	—
8	Mode specification	1	0	0	0	CDROM	DOUT Mute	DOUT ON/OFF	WSEL	VCO SEL1	0	SOCT	0	KSL3	KSL2	1	0	0	VCO1 CS0	0	0	0	0	0	0	TXON	TXOUT	OUTL1	OUTL0
9	Function specification	1	0	0	1	0	DSPB ON/OFF	0	0	0	0	0	0	OPSL1 0	MCSL	0	0	ZDPL	ZMUT	0	0	—	—	—	—	—	—	—	—
9	Function specification	1	0	0	1	0	DSPB ON/OFF	0	0	0	0	0	0	OPSL1 1	MCSL	0	0	ZDPL	ZMUT	0	0	0	DCOF	0	DAC PWDN	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	0	0	OPSL2 0	EMPH	SMUT	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—
A	Audio CTRL	1	0	1	1	0	0	Mute	ATT	0	0	OPSL2 1	EMPH	SMUT	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FMUT	LRWO	BSBST	BBSL
A	Sleep setting	1	0	1	1	1	1	0	1	ADCPS	DSP SLEEP	DSSP SLEEP	ASYM SLEEP	0	LPF SLEEP	0	0	—	—	—	—	—	—	—	—	—	—	—	—
B	Serial bus CTRL	1	0	1	1	SL1	SL0	CPUSR	0	TRM1	TRM0	MTSL1	MTSL0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
C	Spindle servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	TB	TP	Gain CLVS	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—

§1-3. CPU Command Presets

Command Preset Table ($0X to 34X)

Bit grouping — Address: D23 to D20, D19, D18; Data 1: D17, D16; Data 2: D15, D14, D13, D12; Data 3: D11, D10, D9, D8; Data 4: D7, D6, D5, D4, D3; Data 5: D2, D1, D0.

Register	Command	D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Notes
0	FOCUS CONTROL	0 0 0 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
1	TRACKING CONTROL	0 0 0 1	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
2	TRACKING MODE	0 0 1 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF SLED SERVO OFF

Bit grouping — Address 1: D23 to D20, D19, D18; Data 1: D17, D16; Data 2: D15, D14, D13, D12; Data 3: D11, D10, D9, D8; Data 4: D7, D6, D5, D4, D3; Data 5: D2, D1, D0.

Register	Command	D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Notes
3	—	0 0 1 1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)
3	SELECT	0 0 1 1	0	1	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	KRAM DATA ($3400XX to $344fXX)

(For the SELECT / KRAM DATA row, the data portion: See "Coefficient ROM Preset Values Table".)

—: Don't care

Command Preset Table ($348X to 34FX)

Register	Command	Address 1 (D23 to D20)	Address 2 (D19 to D16)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
3	SELECT	0 0 1 1	0 1 0 0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PFOK, RFAC
				1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Booster Surf Brake
				1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Booster
				1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Servo DAC output
				1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	DFCT
				1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	—	FCS Bias Limit
				1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	—	FCS Bias Data
				1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Traverse Center Data

—: Don't care

Command Preset Table ($35X to 3FX)

Register 3 — Command: SELECT

System GAIN

Register	Command	Address 1					Address 2				Data 1						Data 2						Data 3		
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D2	D1	D0
		0 0 1 1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register 3 — Command: SELECT (D23 to D20 = 0 0 1 1)

Function	Address								Data 1					Data 2					Data 3			Data 4					
	D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
FOCUS SEARCH SPEED/ VOLTAGE AUTO GAIN	0 0 1 1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1						
DTZC/TRACK JUMP VOLTAGE AUTO GAIN	0 0 1 1	0	1	1	0	0	0	0	0	1	1	1	1	0	0	1	0	1	1	1	0						
FZSL/SLED MOVE/ Voltage/AUTO GAIN	0 0 1 1	0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	1	0						
LEVEL/AUTO GAIN/ DFSW/ (Initialize)	0 0 1 1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
SERIAL DATA READ MODE/SELECT	0 0 1 1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0						
FOCUS BIAS	0 0 1 1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
Operation for MIRR/ DFCT/FOK	0 0 1 1	1	0	1	1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0						
TZC/COUT BOTTOM/MIRR	0 0 1 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
SLED FILTER	0 0 1 1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0						
Filter	0 0 1 1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0						
Others	0 0 1 1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						

—: Don't care

Reset Initialization

Register	Command	Addr D3	Addr D2	Addr D1	Addr D0	D1 D3	D1 D2	D1 D1	D1 D0	D2 D3	D2 D2	D2 D1	D2 D0	D3 D3	D3 D2	D3 D1	D3 D0	D4 D3	D4 D2	D4 D1	D4 D0	D5 D3	D5 D2	D5 D1	D5 D0	D6 D3	D6 D2	D6 D1	D6 D0
		Address				Data 1				Data 2				Data 3				Data 4				Data 5				Data 6			
4	Auto sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C), Brake (B),	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	Kick (D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	1	0	○	○	○	○	—	—	—	—	—	—	—	—
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○
9	Function specification	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	1	0	0	0	1	1	0	○	○	○	○	○	○	○	○	○	○	○	○
A	Sleep setting	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
B	Serial bus CTRL	1	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
C	Spindle servo coefficient setting	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—

<Coefficient ROM Preset Values Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	Not used
K2F	00	Not used

* Fix indicates that normal preset values should be used.

<Coefficient ROM Preset Values Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	Not used
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	Not used
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is accessed with THSK = 1.)
K47	00	Not used
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	Not used
K4F	00	Not used

§1-4. Description of SENS Signals and Commands

SENS output

Microcomputer serial register (latching not required)	SENS output	Output data length
$0X	FZC	—
$1X	AS (Anti Shock)	—
$2X	TZC	—
$30 to 37	SSTP	—
$38	AGOK	—
$38	XAVEBSY	—
$3904	TE Avrg Reg.	9 bit
$3908	FE Avrg Reg.	9 bit
$390C	VC Avrg Reg.	9 bit
$391C	TRVSC Reg.	9 bit
$391D	FB Reg.	9 bit
$391F	RFDC Avrg Reg.	8 bit
$3A	FBIAS count STOP	—
$3B to 3F	SSTP	—
$4X	XBUSY	—
$5X	FOK	—
$6X, 7X, 8X, 9X	0	—
$AX	GFS	—
$BX	0	—
$CX	COUT frequency division	—
$DX	0	—
$EX	OV64	—
$FX	0	—

Notes) • The SENS output can be read from the SQSO pin when SOCT = 0, SL1 = 1 and SL0 = 0.
$38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement.
SSTP is output in all other cases.
• The signals output by $0X to $3X in the table above cannot be read during the auto sequence operation.

Description of SENS Signals

SENS output	
XBUSY	Low while the auto sequencer is in operation, high when the operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the regenerated frame sync is obtained with the correct timing.
COUT	Counts the number of tracks with frequeny division ratio set by $B. High when $B is latched, and toggles each time COUT is counted just for the frequency diviison ratio set by $B.
OV64	Low when the EFM signal is lengthened by 64 channel clock pulses or more after passing through the sync detection filter.

The meaning of the data for each address is explained below.

$4X commands

Command	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS-ON	0	1	1	1
1 TRACK JUMP	1	0	0	RXF
10 TRACK JUMP	1	0	1	RXF
2N TRACK JUMP	1	1	0	RXF
N TRACK MOVE	1	1	1	RXF

RXF = 0 FORWARD
RXF = 1 REVERSE

- When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the Track jump/move commands ($48 to $4F) are canceled, $25 is sent and the auto sequence is interrupted.

$5X commands

Auto sequence timer setting

Setting timers: A, E, C, B

Command	D3	D2	D1	D0
Blind (A, E), Over flow (C)	0.18ms	0.09ms	0.05ms	0.02ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.05ms

Ex.) D2 = D0 = 1, D3 = D1 = 0 (Initial Reset)

A = E = C = 0.11ms
B = 0.23ms

$6X commands

Auto sequence timer setting

Setting timer: D

Command	D3	D2	D1	D0
KICK (D)	11.6ms	5.8ms	2.9ms	1.45ms

Ex.) D3 = 0, D2 = D1 = D0 = 1 (Initial Reset)

D = 10.15ms

$7X commands

Auto sequence track jump/move count setting (N)

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

This command is used to set N when a 2N-track jump and an N-track move are executed for auto sequence.

- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.
- The number of tracks jumped is counted according to the COUT signals.

$8X commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
MODE specification	CDROM	DOUT Mute	DOUT ON/OFF	WSEL	VCO SEL1	0	SOCT	0	KSL3	KSL2	1	0

See the $BX commands.

	Data 4				Data 5				Data 6			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
	0	VCO1 CS0	0	0	0	0	0	0	TXON	TXOUT	OUTL1	OUTL0

Command bit	C2PO timing	Processing
CDROM = 1	See Timing Chart 1-1.	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	See Timing Chart 1-1.	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	Digital Out output is muted. (DA output is not muted.)
DOUT Mute = 0	When no other mute conditions are set, Digital Out output is not muted.

Command bit	Processing
DOUT ON/OFF = 1	Digital Out is output from the DOUT pin.
DOUT ON/OFF = 0	Digital Out is not output from the DOUT pin.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock[1]	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

[1] In normal-speed playback, channel clock = 4.3218MHz.

Command bit			Processing
VCOSEL1	KSL3	KSL2	
0	0	0	Multiplier PLL VCO1 is set to 1× speed, and the output is 1/1 frequency-divided.
0	0	1	Multiplier PLL VCO1 is set to 1× speed, and the output is 1/2 frequency-divided.
0	1	0	Multiplier PLL VCO1 is set to 1× speed, and the output is 1/4 frequency-divided.
0	1	1	Multiplier PLL VCO1 is set to 1× speed, and the output is 1/8 frequency-divided.
1	0	0	Multiplier PLL VCO1 is set to about 2× speed, and the output is 1/1 frequency-divided.
1	0	1	Multiplier PLL VCO1 is set to about 2× speed, and the output is 1/2 frequency-divided.
1	1	0	Multiplier PLL VCO1 is set to about 2× speed, and the output is 1/4 frequency-divided.
1	1	1	Multiplier PLL VCO1 is set to about 2× speed, and the output is 1/8 frequency-divided.

Command bit	Processing
VCO1CS0 = 0	Multiplier PLL VCO1 low speed is selected.
VCO1CS0 = 1	Multiplier PLL VCO1 high speed is selected.

* The CXD3017Q has two VCO1s, and this command selects one of these VCO1s.

* **Block Diagram of VCO Internal Path**
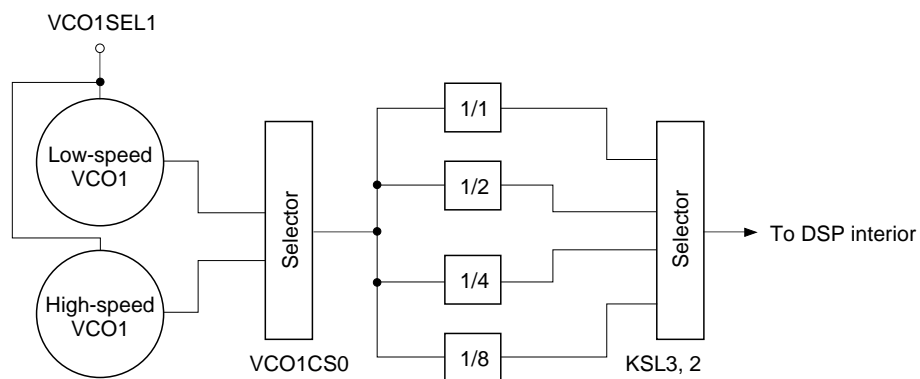
VCO1 Internal Path

Command bit	Processing
TXON = 0	When CD TEXT data in not demodulated, set TXON to 0.
TXON = 1	When CD TEXT data in demodulated, set TXON to 1.

* See "§3-13. CD TEXT Data Demodulation"

Command bit	Processing
TXOUT = 0	Various signals except for CD TEXT is output from the SQSO pin.
TXOUT = 1	CD TEXT data is output from the SQSO pin.

* See "§3-13. CD TEXT Data Demodulation"

Command bit	Processing
OUTL1 = 0	WFCK and XPCK are output.
OUTL1 = 1	WFCK and XPCK outputs are low.

Command bit	Processing
OUTL0 = 0	PCMD, BCK, LRCK and EMPH are output.
OUTL0 = 1	PCMD, BCK, LRCK and EMPH outputs are low.

* OUTL0 is the command which controls the PCMD, BCK, LRCK and EMPH external outputs.
   The IC internal PCMD, BCK, LRCK and EMPH are connected to the built-in DAC regardless of OUTL0=1 or 0.

Timing Chart 1-1

LRCK

CDROM = 0
C2PO

Rch 16-bit C2 Pointer
Lch 16-bit C2 Pointer

If C2 Pointer = 1, data is NG

CDROM = 1
C2PO

C2 Pointer for upper 8bits | C2 Pointer for lower 8bits
C2 Pointer for upper 8bits | C2 Pointer for lower 8bits

Rch C2 Pointer
Lch C2 Pointer
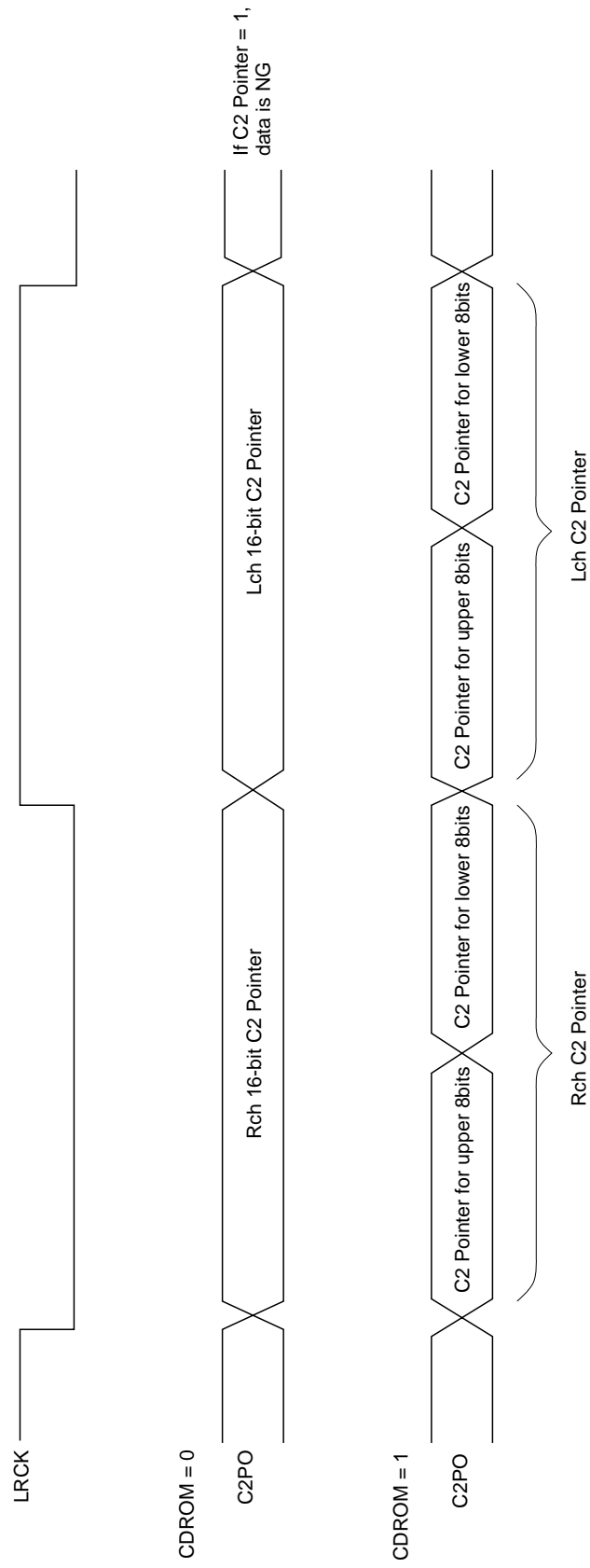
$9X commands (OPSL1= 0) * Data 2 D0 and subsequent data are for DF/DAC function settings.

Command	Data 1				Data 2		Data 3				Data 4			
	D3	D2	D1	D0	D3 to D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Function specification	0	DSPB ON/OFF	0	0	000	0	0	MCSL	0	0	ZDPL	ZMUT	—	—

OPSL1

Data 5			
D3	D2	D1	D0
—	—	—	—

$9X commands (OPSL1= 1) * Data 2 D0 and subsequent data are for DF/DAC function settings.

Command	Data 1				Data 2		Data 3				Data 4			
	D3	D2	D1	D0	D3 to D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Function specification	0	DSPB ON/OFF	0	0	000	0	1	MCSL	0	0	ZDPL	ZMUT	0	0

OPSL1

Data 5			
D3	D2	D1	D0
0	DCOF	0	DAC PWDN

Command bit	Processing
DSPB = 1	Double-speed playback (CD-DSP block)
DSPB = 0	Normal-speed playback (CD-DSP block)

Command bit	Processing
OPSL1 = 1	DCOF,DACPWDN can be set.
OPSL1 = 0	DCOF,DACPWDN cannot be set.

Command bit	Processing
MCSL = 1	DF/DAC block master clock selection. Crystal = 768Fs (33.8688MHz)
MCSL = 0	DF/DAC block master clock selection. Crystal = 384Fs (16.9344MHz)

Command bit	Processing
ZDPL = 1	LMUT and RMUT pins are high when muted.
ZDPL = 0	LMUT and RMUT pins are low when muted.

* See "Mute flag output" for the mute flag output conditions.

Command bit	Processing
ZMUT = 1	Zero detection mute is on.
ZMUT = 0	Zero detection mute is off.

* Set ZDPL to 1 when zero detection mute is on.

Command bit	Processing
DCOF = 1	DC offset is off.
DCOF = 0	DC offset is on.

* DCOF can be set when OPSL1 = 1.
* Set DC offset to off when zero detection mute is on.

Command bit	Processing
DACPWDN = 0	Normal operation.
DACPWDN = 1	DAC block clock is stopped. This makes it possible to reduce power consumption.

$AX commands (OPSL2 = 0)   * Data 2 and subsequent data are for DF/DAC function settings.

Command	Data 1				Data 2				Data 3	
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2
Audio CTRL	0	0	Mute	ATT	0	0	0	EMPH	SMUT	AD10

OPSL2

Data 3		Data 4				Data 5				Data 6			
D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—

$AX commands (OPSL2 = 1)   * Data 2 and subsequent data are for DF/DAC function settings.

Command	Data 1				Data 2				Data 3	
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2
Audio CTRL	0	0	Mute	ATT	0	0	1	EMPH	SMUT	AD10

OPSL2

Data 3		Data 4				Data 5				Data 6			
D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FMUT	LRWO	BSBST	BBSL

Command bit	Processing
Mute = 1	CD-DSP block mute is on. 0 data is output from the CD-DSP block.
Mute = 0	CD-DSP block mute is off.

Command bit	Processing
ATT = 1	CD-DSP block output is attenuated (–12dB).
ATT = 0	CD-DSP block output attenuation is off.

Command bit	Meaning
OPSL2 = 1	FMUT, LRWO, BSBST and BBSL can be set.
OPSL2 = 0	FMUT, LRWO, BSBST and BBSL cannot be set.

Command bit	Processing
EMPH = 1	De-emphasis is on.
EMPH = 0	De-emphasis is off.

* If either the EMPHI pin or EMPH is high, de-emphasis is on.

Command bit	Processing
SMUT = 1	Soft mute is on.
SMUT = 0	Soft mute is off.

* If either the SMUT pin or SMUT is high, soft mute is on.

Command bit	Meaning
AD10 to AD0	Attenuation data.

The attenuation data consists of 11 bits, and is set as follows.

Attenuation data	Audio output
400h	0dB
3FFh	–0.0085dB
3FEh	–0.0170dB
:	
001h	–60.206dB
000h	– ∞

The attenuation data (AD10 to AD0) consists of 11bits, and can be set in 1024 different ways in the range of 000h to 400h.

The audio output from 001h to 400h is obtained using the following equation.

$$\text{Audio output} = 20\log \frac{\text{Attenuation data}}{1024} \text{ [dB]}$$

Command bit	Meaning
FMUT = 1	Forced mute is on.
FMUT = 0	Forced mute is off.

* FMUT can be set when OPSL2 = 1.

Command bit	Meaning
LRWO = 1	Forced synchronization mode **Note)**
LRWO = 0	Normal operation.

* LRWO can be set when OPSL2 = 1.

Note) Synchronization is performed at the first falling edge of LRCK during reset, so there is normally no need to set this mode. However, synchronization can be forcibly performed by setting LRWO = 1.

Command bit	Processing
BSBST = 1	Bass boost is on.
BSBST = 0	Bass boost is off.

* BSBST can be set when OPSL2 = 1.

Command bit	Processing
BBSL = 1	Bass boost is Max.
BBSL = 0	Bass boost is Mid.

* BBSL can be set when OPSL2 = 1.

$AD commands (preset: $AD00)

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
AD (Sleep setting)	1	1	0	1	ADCPS	DSP SLEEP	DSSP SLEEP	ASYM SLEEP	0	LPF SLEEP	0	0				

ADCPS:　　　This bit sets the operation mode of the DSSP block A/D converter.

　　　　　　When 0, the operation mode of the DSSP block A/D converter is set to normal. (default)

　　　　　　When 1, the operation mode of the DSSP block A/D converter is set to power saving.

DSP SLEEP:　This bit sets the operation mode of the DSP block.

　　　　　　When 0, the DSP block operates normally. (default)

　　　　　　When 1, the DSP block clock is stopped. This makes it possible to reduce power consumption.

DSSP SLEEP:　This bit sets the operation mode of the DSSP block.

　　　　　　When 0, the DSSP block operates normally. (default)

　　　　　　When 1, the DSSP block clock is stopped. In addition, the A/D converter and operational amplifier in the DSSP block are set to standby mode. This makes it possible to reduce power consumption.

ASYM SLEEP:　This bit sets the operation mode of the asymmetry correction circuit and VCO1.

　　　　　　When 0, the asymmetry correction circuit and VCO1 operate normally. (default)

　　　　　　When 1, the operational amplifier in the asymmetry correction circuit is set to standby mode. In addition, the multiplier PLL VCO1 oscillation is stopped. This makes it possible to reduce power consumption.

LPF SLEEP:　This bit sets the operation mode of the analog low-pass filter block.

　　　　　　When 0, the analog low-pass filter block operates normally. (default)

　　　　　　When 1, the analog low-pass filter block is set to standby mode. This makes it possible to reduce power consumption.

* The DAC block clock can be stopped by setting $9 command DACPWDN (when OPSL1 = 1).

$BX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Serial bus CTRL	SL1	SL0	CPUSR	0	TRM1	TRM0	MTSL1	MTSL0	0	0	0	0

SOCT	SL1	SL0	mode
0	0	0	SubQ
0	0	1	Peak meter
0	1	0	SENS
0	1	1	D
1	0	0	SubQ
1	0	1	A
1	1	0	B
1	1	1	C

The SQSO pin output can be switched to the various signals by setting the SOCT command of $8X and the SL1 and SL0 commands of $BX. Set SQCK to high at the falling edge of XLAT.

Except for Sub Q and peak meter, the signals are loaded to the register when they are set at the falling edge of XLAT. Sub Q is loaded to the register with each SCOR, and Peak meter is loaded when a peak is detected.

—: don't care

Timing diagram signals:

- **XLAT**
- **SQCK**
- **mode A**: PER0, PER1, PER2, PER3, PER4, PER5, PER6, PER7, C1F1, C1F2, C2F1, C2F2, 0, FOK, GFS, LOCK, EMPH, ALOCK, —, —, —, —, —
- **mode B**: —, —, —, —, —, —, —, —, —, ALOCK, C1F1, C1F2, 0, C2F1, C2F2, 0, FOK, GFS, LOCK, EMPH, —, —, —
- **mode C**: PER0, PER1, PER2, PER3, PER4, PER5, PER6, PER7, 0, C1F1, C1F2, 0, C2F1, C2F2, 0, FOK, GFS, LOCK, EMPH, —, —, —, —
- **mode D**: SPOA, SPOB, 0, 0, WFCK, SCOR, GFS, GTOP, EMPH, FOK, LOCK, RFCK, XRAOF, C1F1, C1F2, C2F1, C2F2
- **Peak meter**: L0, L1, L2, L3, L4, L5, L6, L7, R0, R1, R2, R3, R4, R5, R6, R7

Signal	Description
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460Hz; when GFS is high, a high signal is output. If GFS is low eight consecutive samples, a low signal is output.
EMPH	High when the playback disc has emphasis.
ALOCK	GFS is sampled at 460Hz; when GFS is high eight consecutive samples, a high signal is output. If GFS is low eight consecutive samples, a low signal is output.
SPOA, B	SPOA and B pin inputs.
WFCK	Write frame clock output.
SCOR	High when either subcode sync S0 or S1 is detected.
GTOP	High when the sync protection window is open.
RFCK	Read frame clock output.
XRAOF	Low when the built-in 16K RAM exceeds the ±4 frame jitter margin.
L0 to L7, R0 to R7	Peak meter register output. L0 to 7 are the left-channel and R0 to 7 are the right-channel peak data. L0 and R0 are LSB.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single Error Correction
1	1	Irretrievable Error

C2F1	C2F2	C2 correction status
0	0	No Error
1	0	Single Error Correction
1	1	Irretrievable Error

Command bit	Processing
CPUSR = 1	XLON pin is high.
CPUSR = 0	XLON pin is low.

Peak meter

XLAT

SQCK

SQSO

L0 L1 L2 L3 L4 L5 L6 L7 R0 R1 R2 R3 R4 R5 R6 R7

(Peak meter)
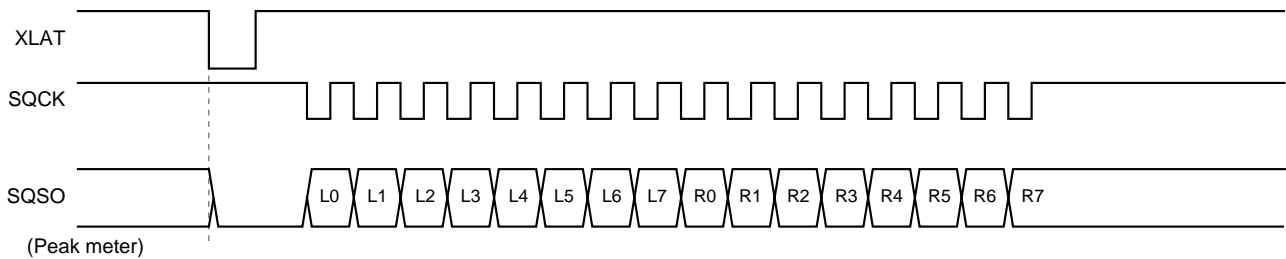
Setting the SOCT command of $8X to 0 and the SL1 and SL0 commands of $BX to 0 and 1, respectively, results in peak detection mode. The SQSO output is connected to the peak register. The maximum PCM data values (absolute value, upper 8bits) for the left and right channels can be read from SQSO by inputting 16 clocks to SQCK. Peak detection is not performed during SQCK input, and the peak register does not change during readout. This SQCK input judgment uses a retriggerable monostable multivibrator with a time constant of 270µs to 400µs. The time during which SQCK input is high should be 270µs or less. Also, peak detection is restarted 270µs to 400µs after SQCK input.

The peak register is reset with each readout (16 clocks input to SQCK).
The maximum value in peak detection mode is detected and held in this status until the next readout. When switching to peak detection mode, readout should be performed one time initially to reset the peak register.

Peak detection can also be performed for previous value hold and average value interpolation data.

Traverse monitor count value setting
These bits are set when monitoring the traverse condition of the SENS output according to the COUT frequency division.

Command bit		Processing
TRM1	TRM0	
0	0	1/64 frequency division
0	1	1/128 frequency division
1	0	1/256 frequency division
1	1	1/512 frequency division

Monitor output switching
The monitor output can be switched to the various signals by setting the MTSL1 and MTSL0 commands of $B.

Command bit		Output data			
	Symbol	XUGF	XPCK	GFS	C2PO
MTSL1	MTSL0				
0	0	XUGF	XPCK	GFS	C2PO
0	1	MNT1	MNT0	MNT3	C2PO
1	0	RFCK	XPCK	XROF	GTOP

* It is necessary for the SRO1 command of $3F to be set to 0.

$CX commands

Command	D3	D2	D1	D0
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0
CLV CTRL ($DX)				Gain CLVS

• CLV mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	−12dB
0	0	1	−6dB
0	1	0	−6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

• CLVP mode gain setting: GMDP: GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	−6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	−6dB
0	1	0dB
1	0	+6dB

$DX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV CTRL	0	TB	TP	Gain CLVS	1	1	1	0	0	0	0	0

See the $CX commands.

Command bit	Description
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS mode.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS mode.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

$EX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0	0	0	0	0	0	0	0	0

Data 4			
D3	D2	D1	D0
0	0	0	0

Command bit				Mode	Description
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.[1]
1	0	0	0	KICK	Spindle forward rotation mode.[1]
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR = 0 in any mode.[1]
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

[1] See Timing Charts 1-2 and 1-3.

Timing Chart 1-2
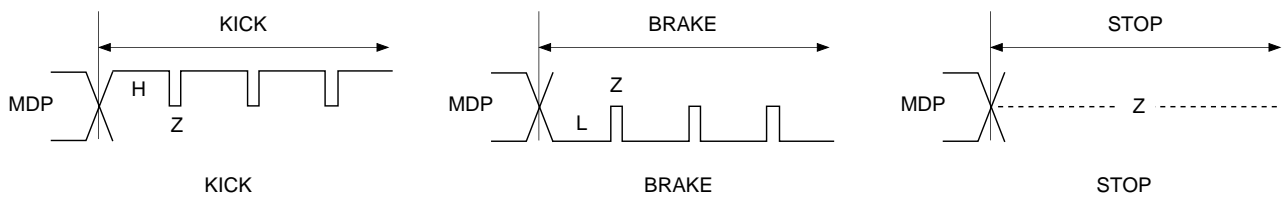
Timing Chart 1-3
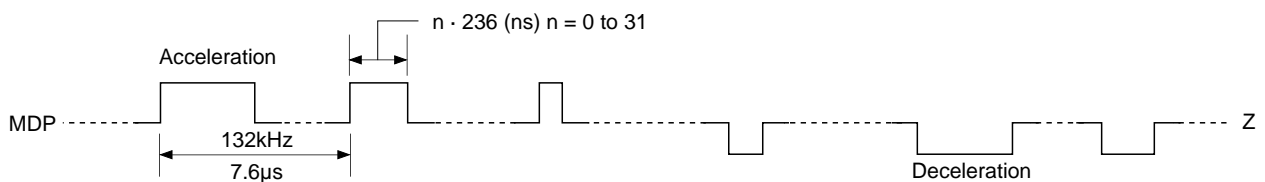
§2. Subcode Interface

In the CXD3017Q, only SubQ can be readout.

The subcodes P and R to W cannot be readout.

Sub Q can be read out after checking CRC of the 80 bits in the subcode frame.

Sub Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

§2-1. 80-bit Sub Q Readout

Fig. 2-1 shows the peripheral block of the 80-bit Sub Q register.

• First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.

• 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80 bits are loaded into the parallel/serial register.

  When SQSO goes high 400μs (monostable multivibrator time constant) or more after subcode readout, the CPU determines that the new data (which passed the CRC check) has been loaded.

• The CRCF reset is performed by inputting SQCK. When the subcode data is discontinuous after track jump, etc. CRCF is reset by inputting SQCK. Then, if CRCF =1, the CPU determines that the new data has been loaded.

• When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.

• Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.

  The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.

• The retriggerable monostable multivibrator has a time constant from 270 to 400μs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.

• While the monostable multivibrator is being reset, data cannot be loaded in the 80-bit parallel/serial register. In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others. (See Timing Chart 2-2.)

• The high and low intervals for SQCK should be between 750ns and 120μs.

Block Diagram 2-1

Timing Chart 2-2

WFCK

SCOR

Order
Inversion

SQSO

CRCF1 CRCF2

Determined by mode

L

80 Clock

SQCK

Registere load forbidder

270 to 400μs when SQCK = high.

750ns to 120μs

Mono/multi (Internal)

1 2 3 ...... 91 92 93 94 95 96 97 98

1 2 3

SQCK

SQSO

CRCF ADR0 ADR1 ADR2 ADR3 CTL0 CTL1 CTL2 CTL3

300ns max

§3. Description of Other Functions

§3-1. Channel Clock Regeneration by the Digital PLL Circuit

• The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.

Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.

In an actual player, a PLL is necessary for regenerating the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 3-1.

The CXD3017Q has a built-in three-stage PLL.

• The first-stage PLL regenerates the high-frequency clock needed by the second-stage digital PLL.

• The second-stage PLL is a digital PLL that regenerates the actual channel clock.

Block Diagram 3-1

§3-2. Frame Sync Protection

• In normal-speed playback, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

• In the CXD3017Q, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths; one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. Concretely, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync.

In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.

§3-3. Error Correction

• In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.

For C2 correction, the code is created with 24-byte information and 4-byte parity.

Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.

• The CXD3017Q's SEC strategy uses powerful frame sync protection and C1 and C2 error correction to achieve high playability.

• The correction status can be monitored externally. See Table 3-2.

• When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT1	MNT0	Description
0	0	0	No C1 errors
0	0	1	One C1 error corrected
0	1	1	C1 correction impossible
1	0	0	No C2 errors
1	0	1	One C2 error corrected
1	1	0	C2 correction impossible

Table 3-2

Timing Chart 3-3

Normal-speed PB

t = Dependent on error condition

MNT3

C1 correction | C2 correction

MNT1

MNT0

Strobe | Strobe
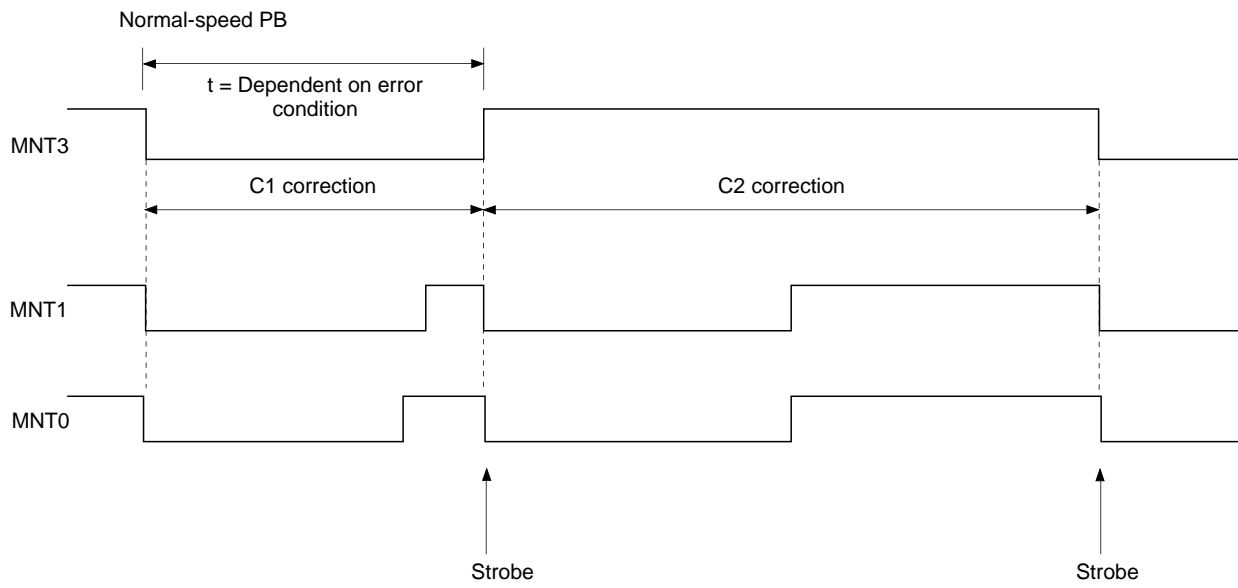
§3-4. DA Interface

• The CXD3017Q's DA interface is as follows:
  Interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first.
  When LRCK is high, the data is for the left channel.

Timing Chart 3-4

48-bit slot Normal-Speed Playback

LRCK
(44.1k)

BCK
(2.12M)

PCMD

48-bit slot Double-Speed Playback

LRCK
(88.2k)

BCK
(4.23M)

PCMD

– 52 –
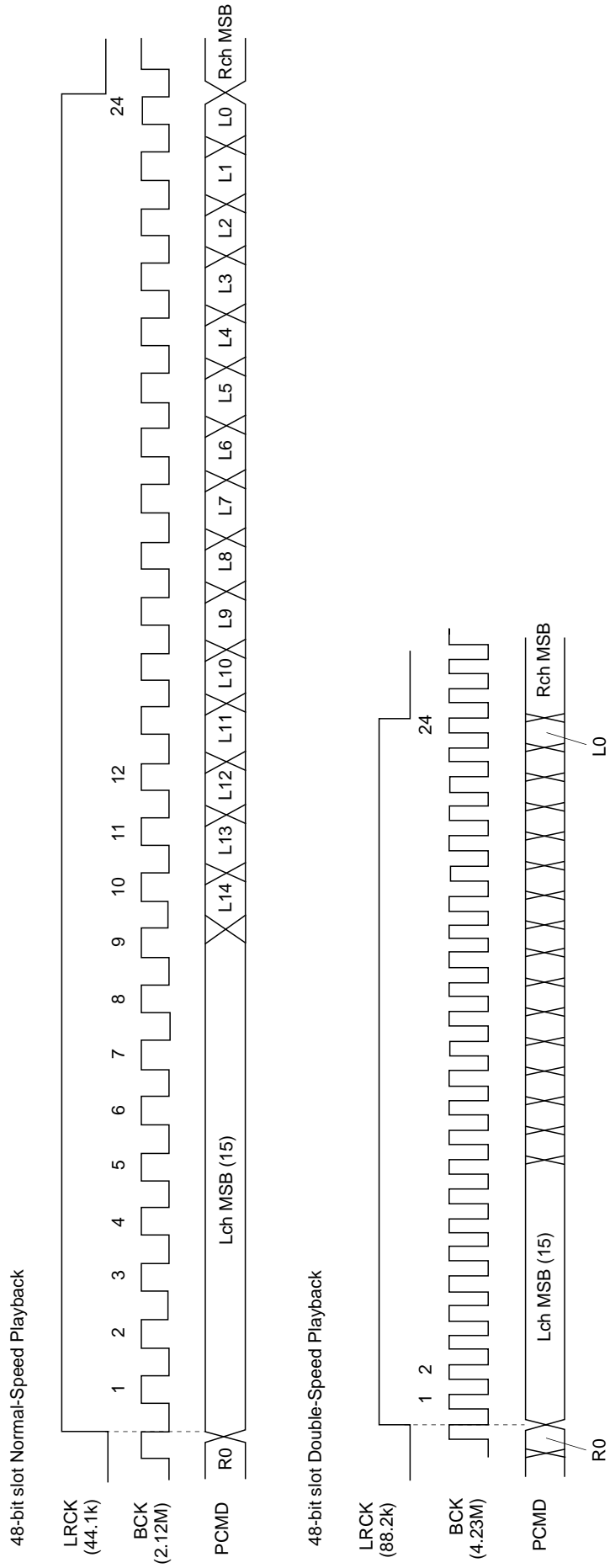
§3-5. Digital Out

There are three Digital Out: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.
The CXD3017Q supports type 2 form 1.
Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3) of the channel status.
When Mute = 1 in $AX commands, the channel status is pre-value hold.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	◄─	From sub Q		─►	0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32																
48																
								0								
176																

Bits 0 to 3 Sub Q control bits that matched twice with CRCOK
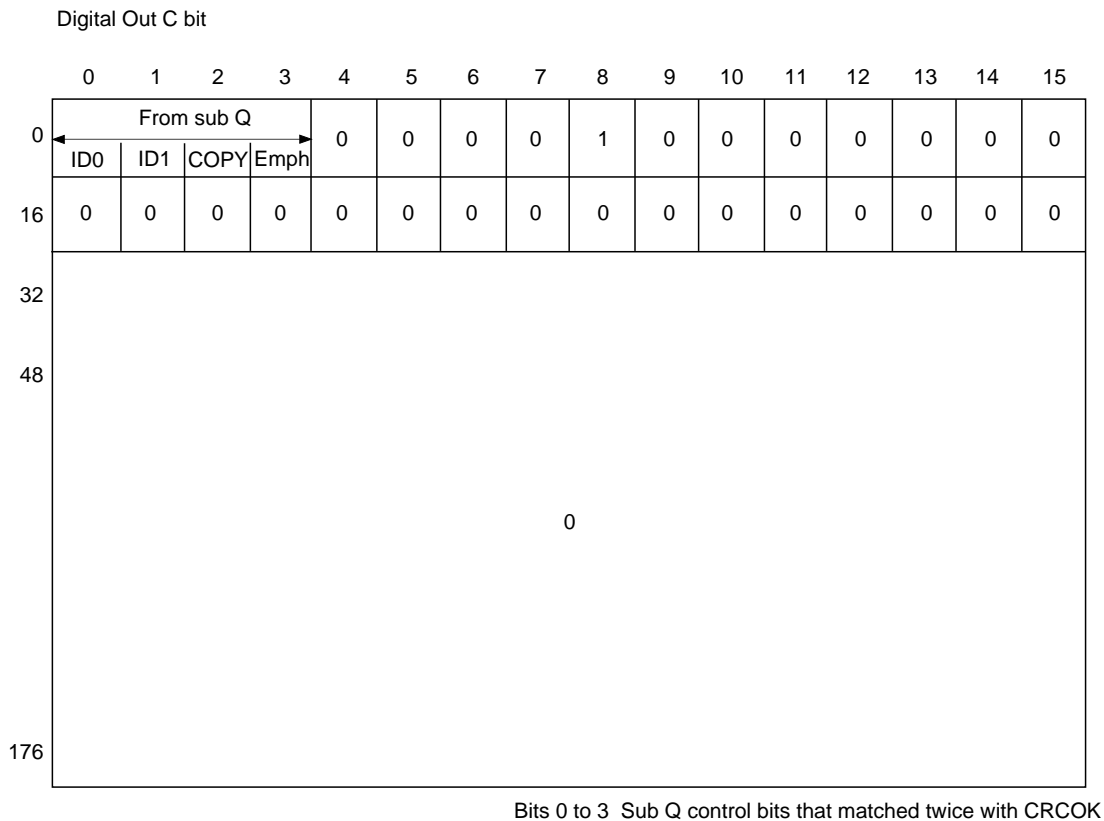
Table 3-5

§3-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jump and N-track move are executed automatically.
The commands which enable transfer to the CXD3017Q during the execution of auto sequence are $4X to $EX.
When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point.

(a) Auto focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 3-6. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.
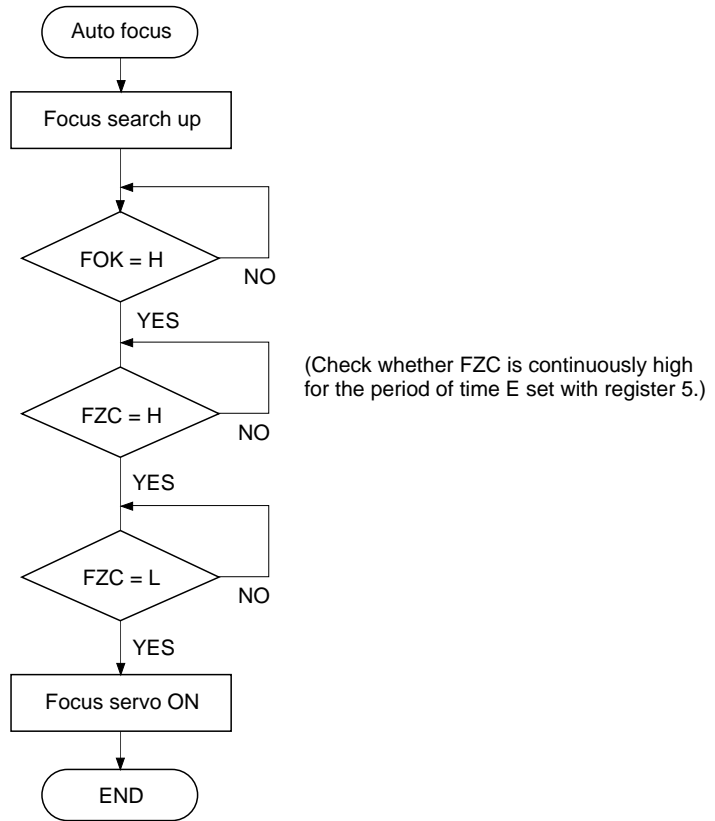
Fig. 3-6-(a). Auto Focus Flow Chart
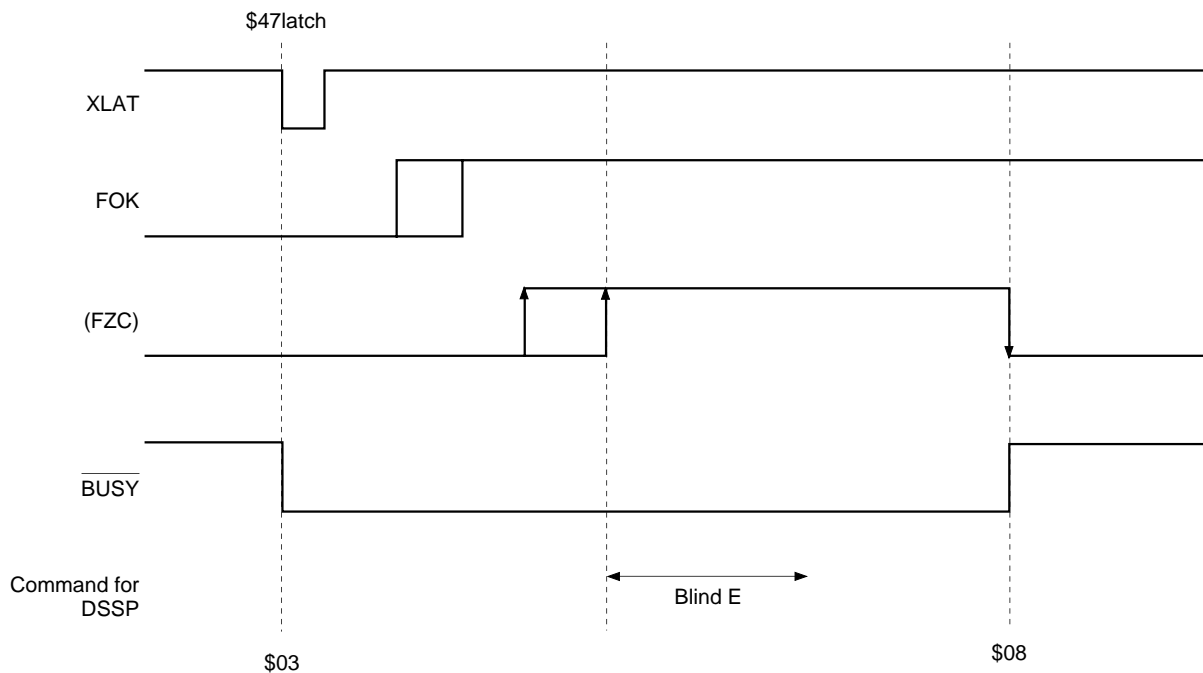
Fig. 3-6-(b). Auto Focus Timing Chart

(b) Track jump

1, 10 and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on should be sent beforehand because they are not involved in this sequence.

• 1-track jump

When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 3-7. Set blind A and brake B with register 5.

• 10-track jump

When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 3-8. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.

• 2N-track jump

When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 3-9. The track jump count N is set with register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps.

Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.

• N-track move

When $4E ($4F for REV) is received from the CPU, a FWD (REV) N-track move is performed in accordance with Fig. 3-10. N can be set to 2^{16} tracks. COUT is used for counting the number of jumps. The N-track move is executed only by moving the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks.
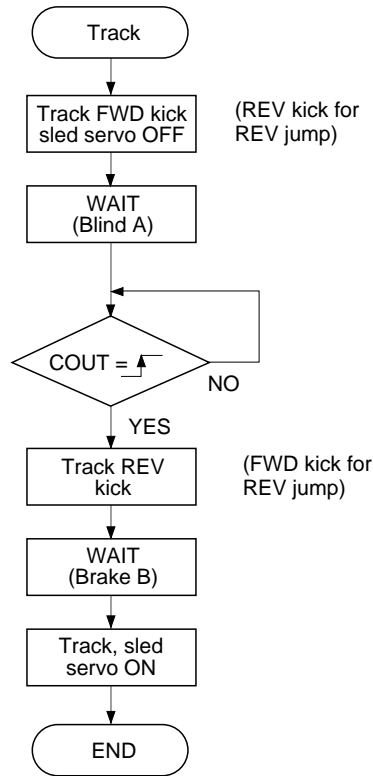
Fig. 3-7-(a). 1-Track Jump Flow Chart
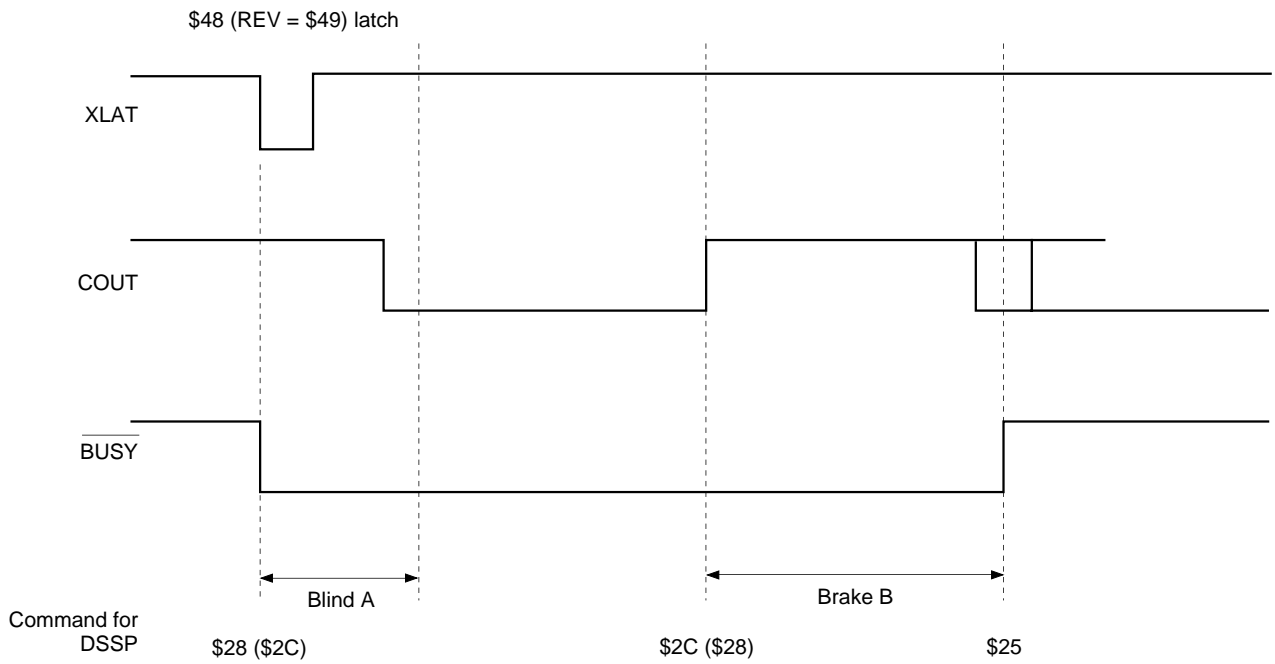
Fig. 3-7-(b). 1-Track Jump Timing Chart
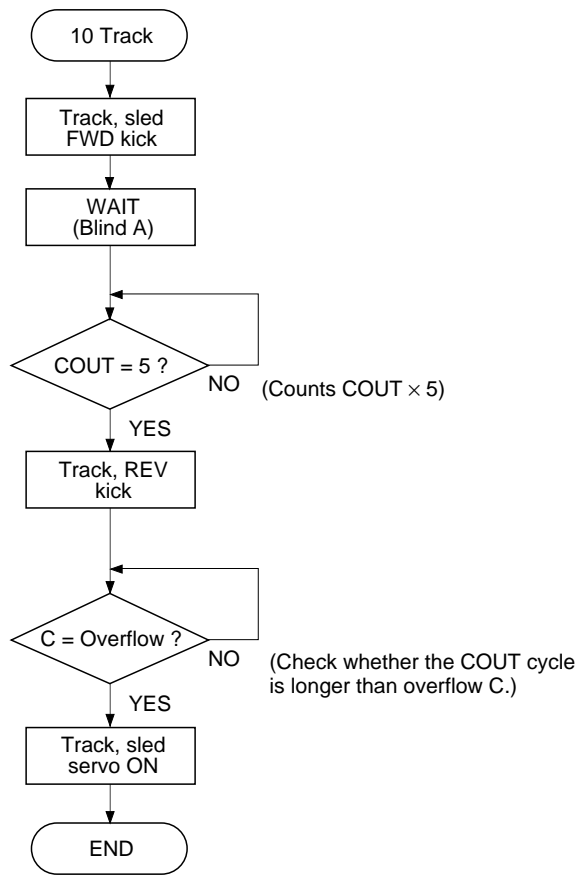
Fig. 3-8-(a). 10-Track Jump Flow Chart
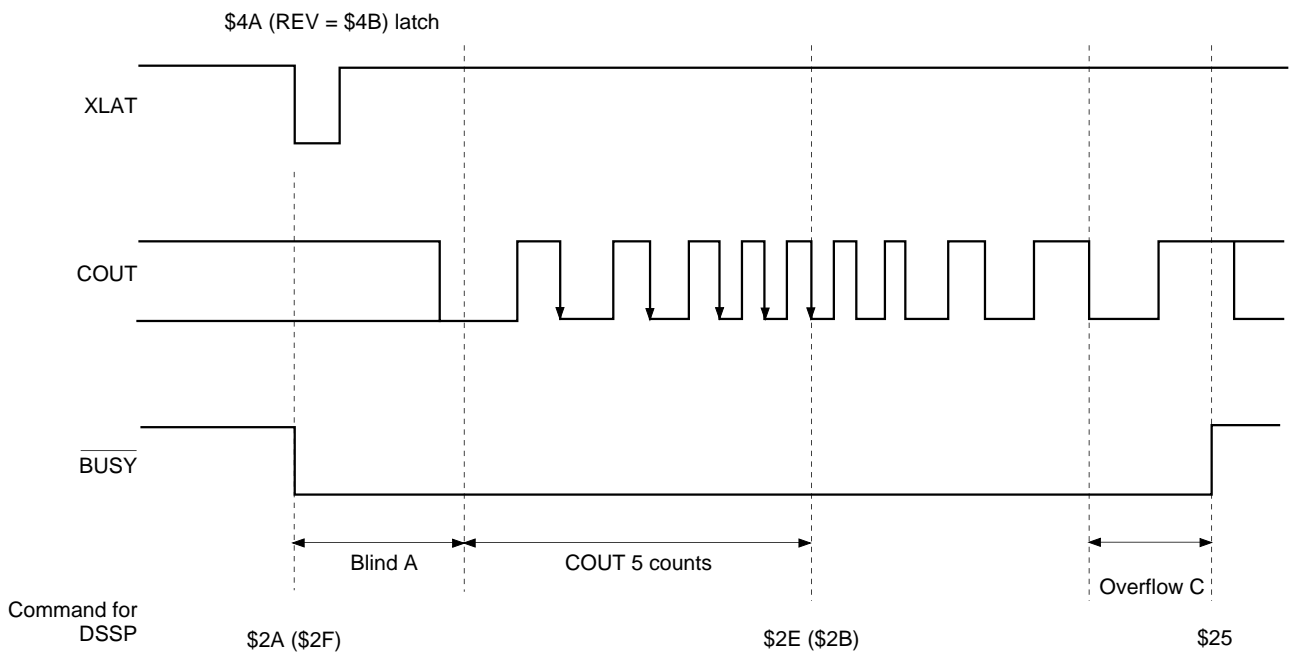
Fig. 3-8-(b). 10-Track Jump Timing Chart
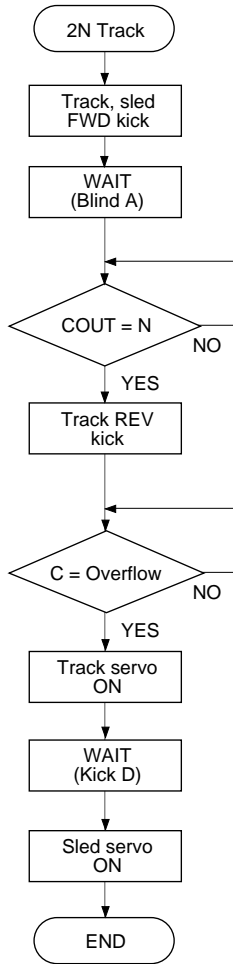
Fig. 3-9-(a). 2N-Track Jump Flow Chart
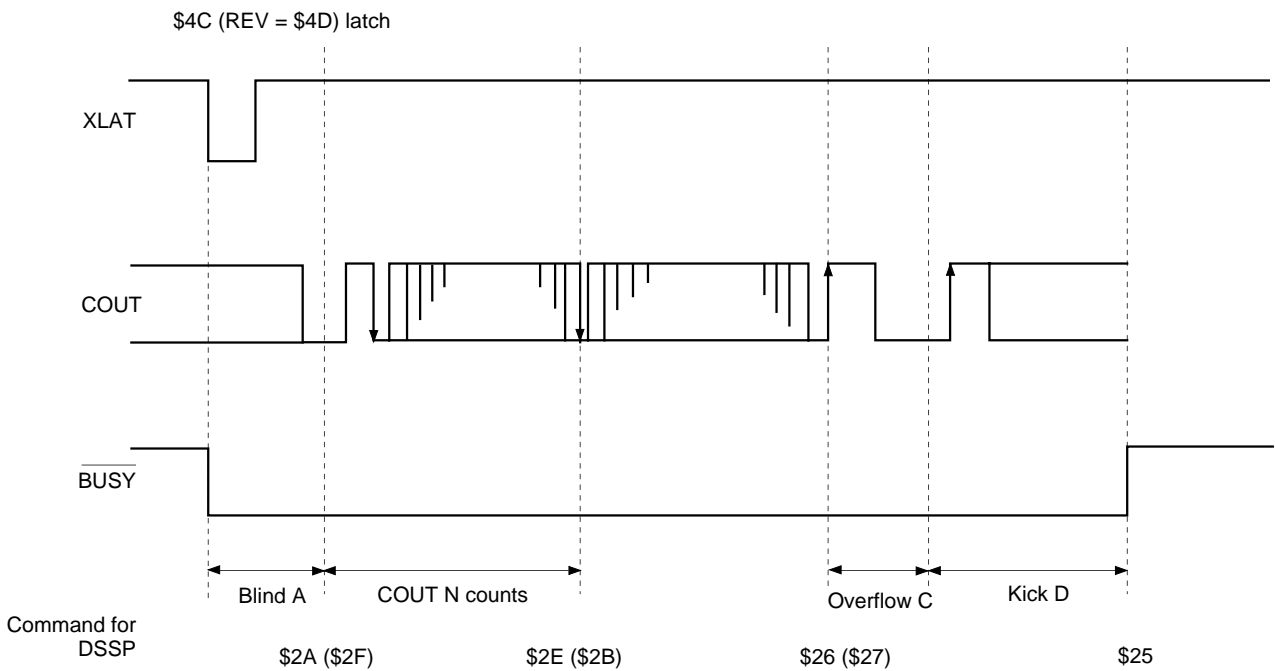
Fig. 3-9-(b). 2N-Track Jump Timing Chart
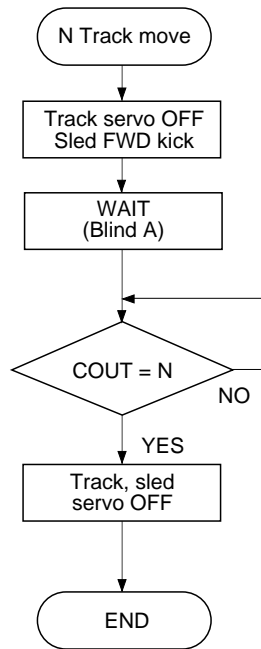
Fig. 3-10-(a). N-Track Move Flow Chart
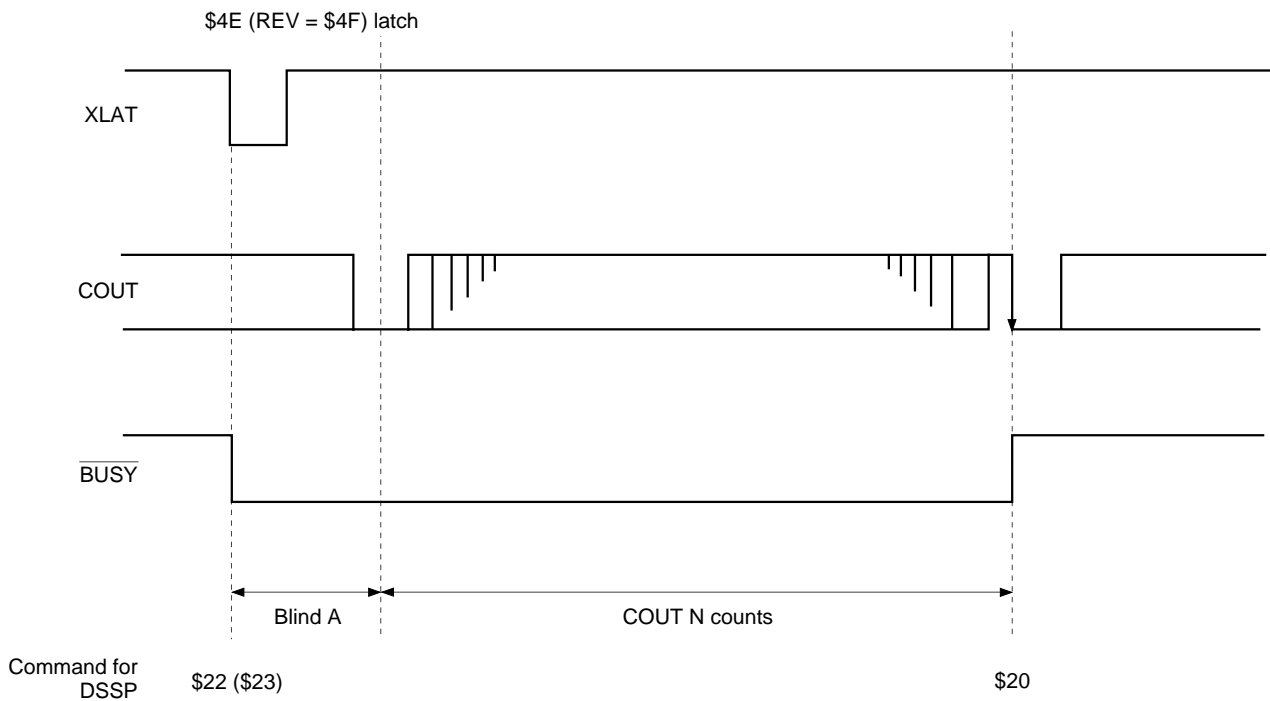
Fig. 3-10-(b). N-Track Move Timing Chart

§3-7. Digital CLV

Fig. 3-11 shows the block diagram. Digital CLV outputs MDS error and MDP error signals with PWM, with the sampling frequency increased up to 130kHz during normal-speed playback in CLVS, CLVP and other modes. In addition, the digital spindle servo gain is variable.

Digital CLV
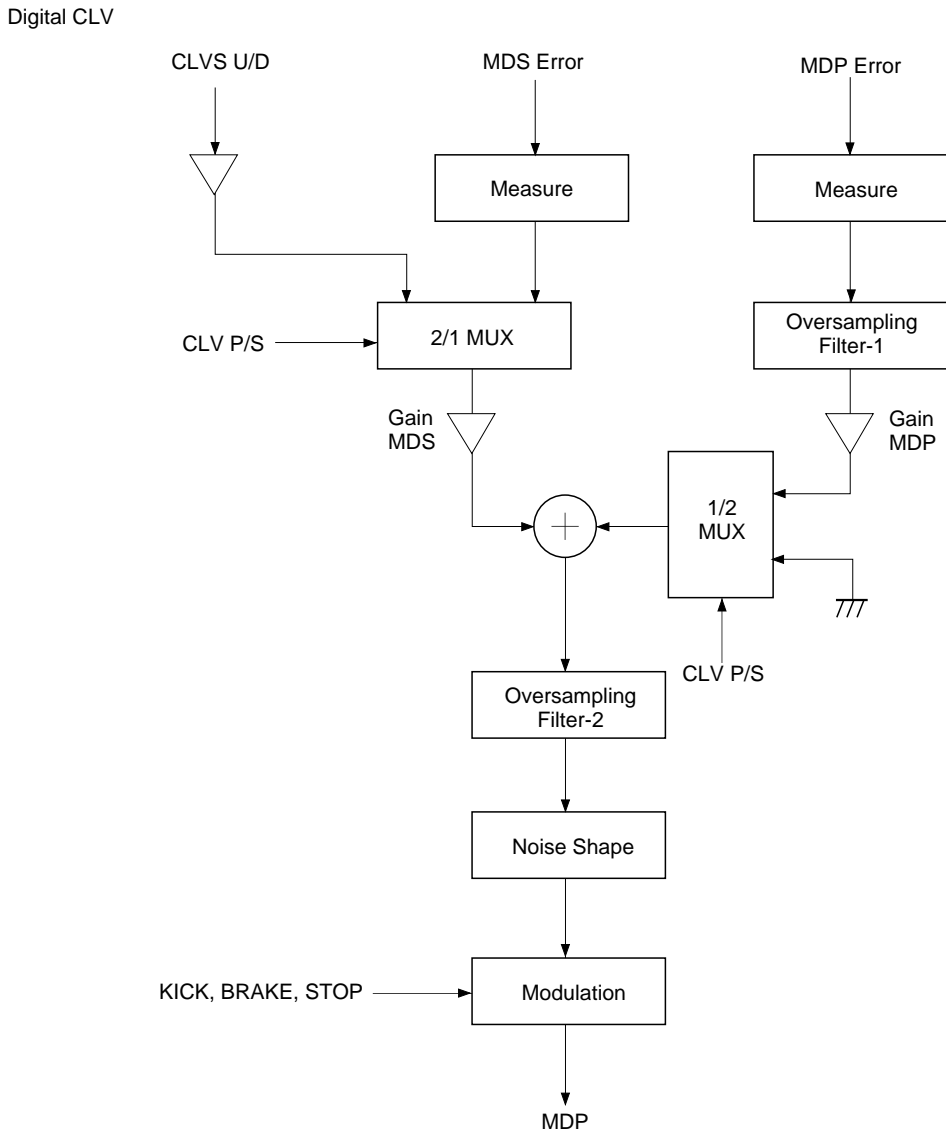
CLVS U/D: Up/down signal from CLVS servo
MDS error: Frequency error for CLVP servo
MDP error: Phase error for CLVP servo

Fig. 3-11. Block Diagram

§3-8. CD-DSP Block Playback Speed

In the CXD3017Q, the following playback modes can be selected through different combinations of the crystal, XTSL pin and the DSPB command of $9X.

CD-DSP block playback speed

Crystal	XTSL	DSPB	CD-DSP block playback speed
768Fs	0	1	4×[*1]
768Fs	1	0	1×
768Fs	1	1	2×
384Fs	0	0	1×
384Fs	0	1	2×
384Fs	1	1	1×[*2]

Fs = 44.1kHz.

[*1] In 4× speed playback, the timer value for the auto sequence is halved.

[*2] Low power consumption mode. The CD-DSP processing speed is halved, allowing power consumption to be reduced.

§3-9. DAC Block Playback Speed

The operation speed for the DAC block is determined by the crystal and the MCSL command of $9X regardless of the CD-DSP operating conditions noted above. This allows the playback modes for the DAC and CD-DSP blocks to be set independently.

1-bit DAC block playback speed

Crystal	MCSL	DAC block playback speed
768Fs	1	1×
768Fs	0	2×
384Fs	0	1×

Fs = 44.1kHz.

§3-10. Description of DAC Block Functions

Zero data detection

When the condition where the lower 4 bits of the input data are DC and the remaining upper bits are all "0" or all "1" has continued about for 300ms, zero data is detected. Zero data detection is performed independently for the left and right channels.

Mute flag output

The LMUT and RMUT pins go active when any one of the following conditions is met.
The polarity can be selected with the ZDPL command of $9X.

- When zero data is detected
- When a high signal is input to the SYSM pin
- When the SMUT command of $AX is set

Attenuation operation

Assuming attenuation data X1, X2 and X3 (X1 > X3 > X2), the corresponding audio outputs are Y1, Y2 and Y3 (Y1 > Y3 > Y2). First, X1 is sent, followed by X2. If X2 is sent before X1 reaches Y1 (A in the figure), X1 continues approaching Y2. Next, if X3 is sent before X1 reaches Y2 (B or C in the figure), X1 then approaches Y3 from the value (B or C in the figure) at that point.
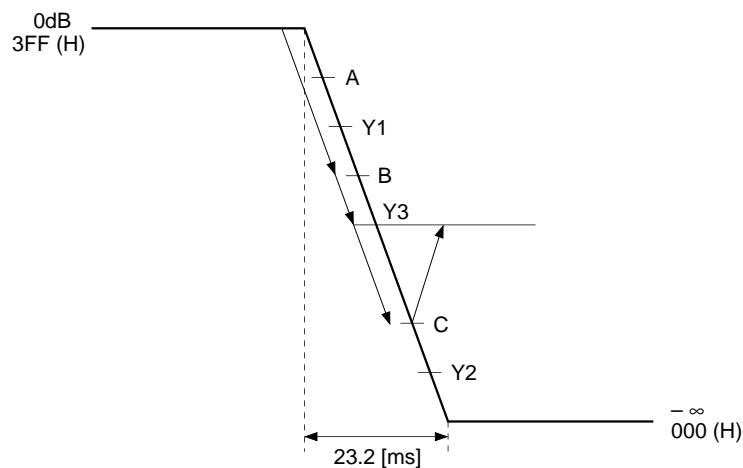
DAC block mute operation

Soft mute

Soft mute results and the input data is attenuated to zero when any one of the following conditions is met.

- When attenuation data of "000" (high) is set
- When the SMUT command of $AX is set to 1
- When a high signal is input to the SYSM input pin
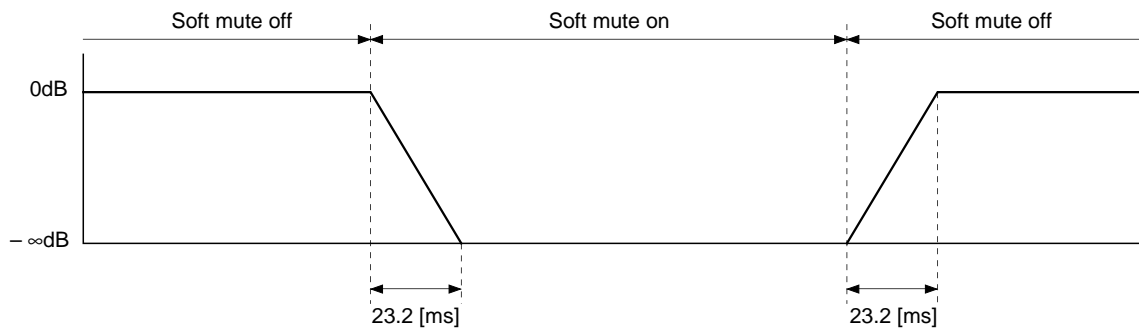
Forced mute

Forced mute results when the FMUT command of $AX is set to 1.

Forced mute fixes the PWM output that is input to the LPF block to low.

* When setting FMUT, set OPSL2 to 1. (See the $AX commands.)

Zero detection mute

When the ZMUT command of $9X is set to 1 and the zero data is detected for the left or right channel, the analog mute is applied to the each channel.

(See "Zero data detection".)

When the ZMUT command of $9X is set to 1, the analog mute is applied even if the mute flag output condition is met. When the zero detection mute is on, set the DCOF, ZDPL command of $9X to 1.

LRCK Synchronization

Synchronization is performed at the first falling edge of the LRCK input during reset.

After that, synchronization is lost when the LRCK input frequency changes and resynchronization must be performed.

The LRCK input frequency changes when the master clock of the LSI is switched and the playback speed changes such as the following cases.

- When the XTSL pin switches between high and low
- When the DSPB command of $9X setting changes
- When the MCSL command of $9X setting changes

LRCK switching may also be performed if there are other ICs between the CD-DSP block and the DAC block. Resynchronization must be performed in this case as well.

For resynchronization, set the LRWO command of $AX to 1, wait for one LRCK cycle or more, and then set LRWO to 0.

* When setting LRWO, set OPSL2 to 1. (See the $AX commands.)

Digital Bass Boost

Bass boost without external parts is possible using the built-in digital filter. The boost strength has two levels: Mid. and Max. BSBST and BBSL of address A are used for the setting.

See Graph 3-12 for the digital bass boost frequency response.

Digital Bass Boost Frequency Response [Hz]
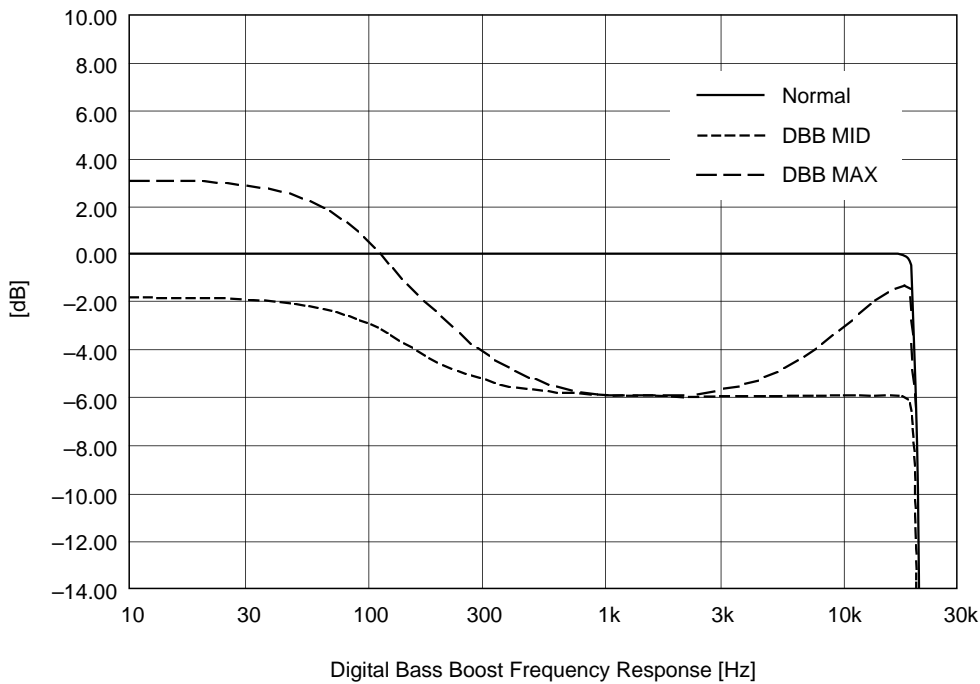
Graph 3-12

§3-11. LPF Block

The CXD3017Q contains an initial-stage secondary active LPF with numerous resistors and capacitors and an operational amplifier with reference voltage.
The resistors and capacitors are attached externally, allowing the cut-off frequency fc to be determined flexibly.
The reference voltage (V_C) is (AV$_{DD}$ – AV$_{SS}$) $\times$ 0.45.

The LPF block application circuit is shown below.
In this circuit, the cut-off frequency is fc $\approx$ 40kHz.

LPF Block Application Circuit
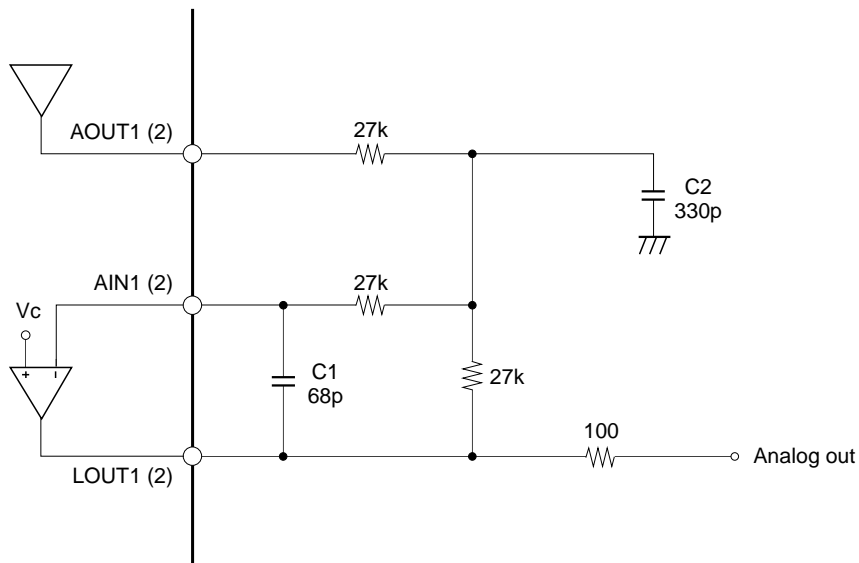
Fig. 3-13. LPF External Circuit

§3-12. Asymmetry Compensation

Fig. 3-14 shows the block diagram and circuit example.

$$\frac{R1}{R2} = \frac{2}{5}$$
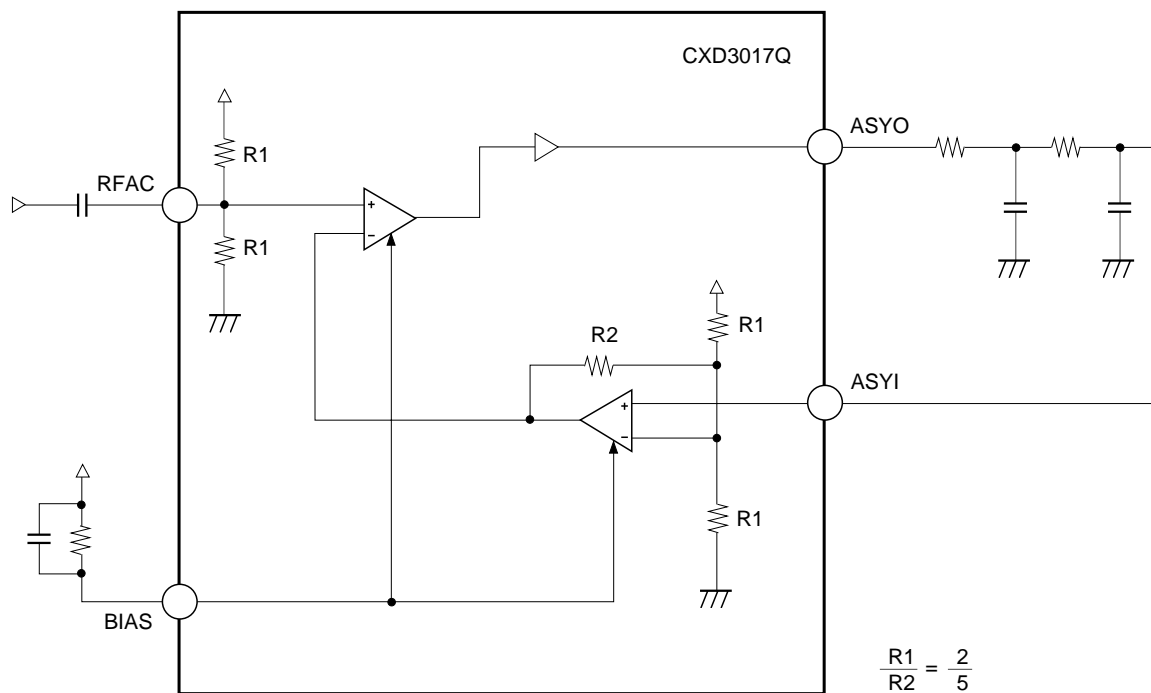
Fig. 3-14. Asymmetry Compensation Application Circuit

§3-13. CD TEXT Data Demodulation

• In order to demodulate the CD TEXT data, set the command $8 Data 6 D3 TXON to 1.
  It requires 26.7ms (max.) to demodulate the CD TEXT data correctly after TXON is set to 1.
• The CD TEXT data is output by switching the SQSO pin with the command. The CD TEXT data output is enabled by setting the command $8 Data 6 D2 TXOUT to 1. To read data, the readout clock should be input to SQCK.
• The readable data are the CRC counting results for the each pack and the CD TEXT data (16 bytes) except for CRC data.
• When the CD TEXT data is read, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
• Data which can be stored in the LSI is 1 packet (4 packs).
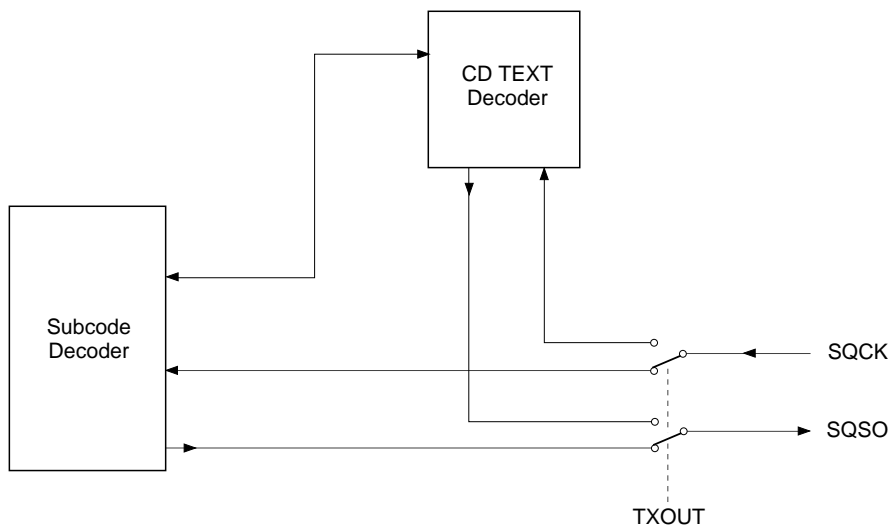
Fig. 3-15. Block Diagram of CD TEXT Demodulation Circuit
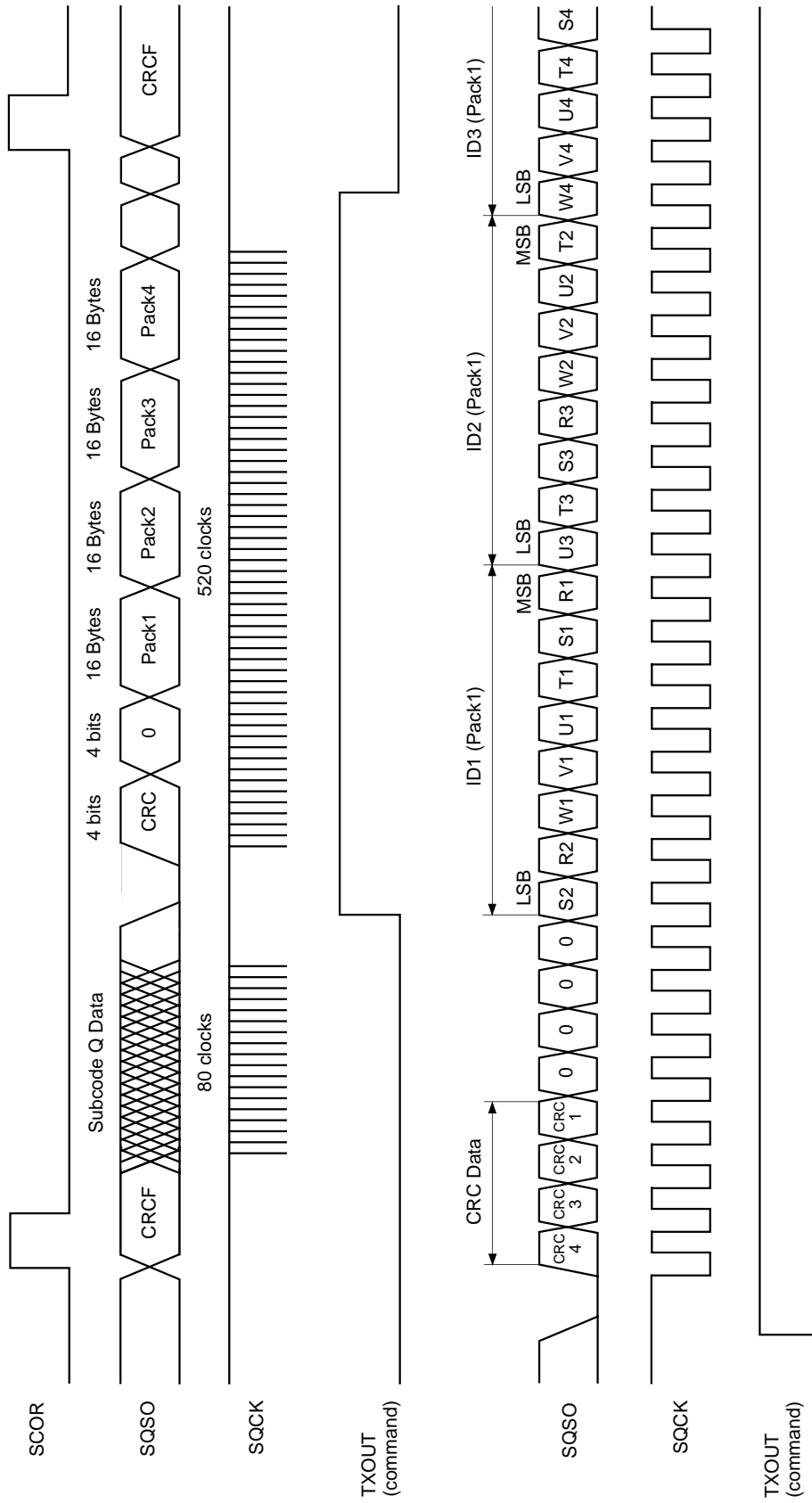
Fig. 3-16. CD TEXT DATA Timing Chart

§4. Description of Servo Signal Processing System Functions and Commands

§4-1. General Description of Servo Signal Processing System (V$_{DD}$: Supply voltage)

Focus servo

   Sampling rate: 88.2kHz (when MCK = 128Fs)

   Input range: 1/4V$_{DD}$ to 3/4V$_{DD}$

   Output format: 7-bit PWM

   Other: Offset cancel

                         Focus bias adjustment

                         Focus search

                         Gain-down function

                         Defect countermeasure

                         Auto gain control

Tracking servo

   Sampling rate: 88.2kHz (when MCK = 128Fs)

   Input range: 1/4V$_{DD}$ to 3/4V$_{DD}$

   Output format: 7-bit PWM

   Other: Offset cancel

                         E:F balance adjustment

                         Track jump

                         Gain-up function

                         Defect countermeasure

                         Drive cancel

                         Auto gain control

                         Vibration countermeasure

Sled servo

   Sampling rate: 345Hz (when MCK = 128Fs)

   Input range: 1/4V$_{DD}$ to 3/4V$_{DD}$

   Output format: 7-bit PWM

   Other: Sled move

FOK, MIRR, DFCT signal generation

   RF signal sampling rate: 1.4MHz (when MCK = 128Fs)

   Input range: 1/4V$_{DD}$ to 3/4V$_{DD}$

   Other: RF zero level automatic measurement

§4-2. Digital Servo Block Master Clock (MCK)

The clock with 2/3 frequency of the crystal is supplied to the digital servo block.

XT4D and XT2D are $3F commands, and XT1D is a $3E command. (Default is 0 for each command)

The digital servo block is designed with an MCK frequency of 5.6448MHz (128Fs) as typical.

Mode	XTAI	FSTO	XTSL	XT4D	XT2D	XT1D	Frequency division ratio	MCK
1	384Fs	256Fs	*	*	*	1	1	256Fs
2	384Fs	256Fs	*	*	1	0	1/2	128Fs
3	384Fs	256Fs	0	0	0	0	1/2	128Fs
4	768Fs	512Fs	*	*	*	1	1	512Fs
5	768Fs	512Fs	*	*	1	0	1/2	256Fs
6	768Fs	512Fs	*	1	0	0	1/4	128Fs
7	768Fs	512Fs	1	0	0	0	1/4	128Fs

Fs = 44.1kHz, *: don't care

Table 4-1

§4-3. DC Offset Cancel [AVRG (Average) Measurement and Compensation] (See Fig. 4-3.)

The CXD3017Q can measure the averages of RFDC, VC, FE and TE and compensate these signals using the measurement results to control the servo effectively. This AVRG measurement and compensation is necessary to initialize the CXD3017Q, and is able to cancel the DC offset.

AVRG measurement takes the levels applied to the VC, FE, RFDC and TE pins as the digital average values of 256 samples, and then loads these values into each AVRG register.

The AVRG measurement commands are D15 (VCLM), D13 (FLM), D11 (RFLM) and D4 (TLM) of $38.

Measurement is on when the respective command is set to 1.

AVRG measurement requires approximately 2.9ms to 5.8ms (when MCK = 128Fs) after the command is received.

The completion of AVRG measurement operation can be monitored by the SENS pin. (See Timing Chart 4-2.)

Monitoring requires that the upper 8 bits of the command register are 38 (h).
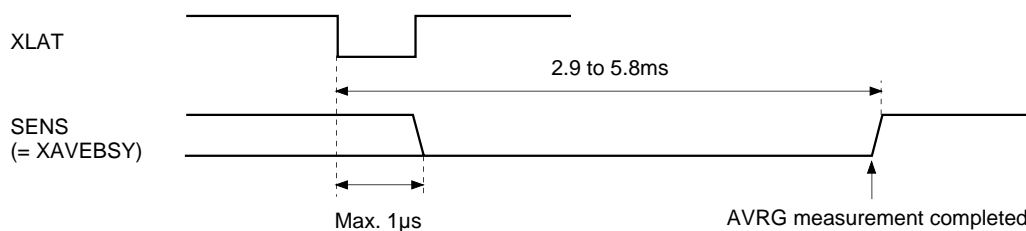
Timing Chart 4-2

<Measurement>

VC AVRG: The VC DC offset (VC AVRG) which is the center voltage for the system is measured and used to compensate the FE, TE and SE signals.

FE AVRG: The FE DC offset (FE AVRG) is measured and used to compensate the FE and FZC signals.

TE AVRG: The TE DC offset (TE AVRG) is measured and used to compensate the TE and SE signals.

RF AVRG: The RF DC offset (RF AVRG) is measured and used to compensate the RFDC signal.

<Compensation>

RFLC: (RF signal – RF AVRG) is input to the RF In register.
          "00" is input when the RF signal is lower than RF AVRG.
TCL0:   (TE signal – VC AVRG) is input to the TRK In register.
TCL1:   (TE signal – TE AVRG) is input to the TRK In register.
VCLC: (FE signal – VC AVRG) is input to the FCS In register.
FLC1:   (FE signal – FE AVRG) is input to the FCS In register.
FLC0:   (FE signal – FE AVRG) is input to the FZC register.

Two methods of canceling the DC offset are assumed for the CXD3017Q. These methods are shown in Figs. 4-3a and 4-3b.

An example of AVRG measurement and compensation commands is shown below.

$38 08 00 (RF AVRG measurement)
$38 20 00 (FE AVRG measurement)
$38 00 10 (TE AVRG measurement)
$38 14 0A (Compensation on [RFLC, FLC0, FLC1, TLC1]; corresponds to Fig. 4-3a.)

See the description of $38 for these commands.

§4-4. E:F Balance Adjustment Function (See Fig. 4-3.)

When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS search, the traverse waveform appears in the TE signal due to disc eccentricity.

In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of $38 to 1.

The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to 0.

Next, setting D2 (TLC2) of $38 to 1 compensates the values obtained from the TE and SE input pins with the TRVSC register value (subtraction), allowing the E:F balance offset to be adjusted. (See Fig. 4-3.)

§4-5. FCS Bias (Focus Bias) Adjustment Function

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of $3A to 1. (See Fig. 4-3.)

When D11 = 0 and D10 = 1 is set by $34F, the FBIAS register value can be written using the 9-bit value of D9 to D1 (D9: MSB).

In addition, the RF jitter can be monitored by setting the $8 command SOCT to 1. (See "DSP Block Timing Chart".)
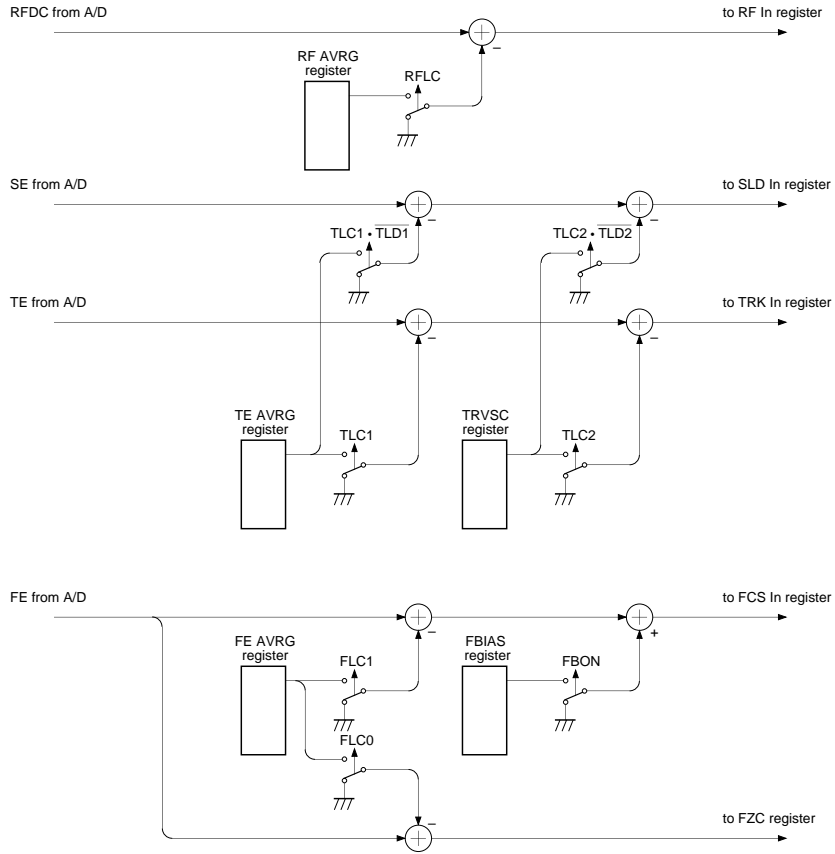
Fig. 4-3a
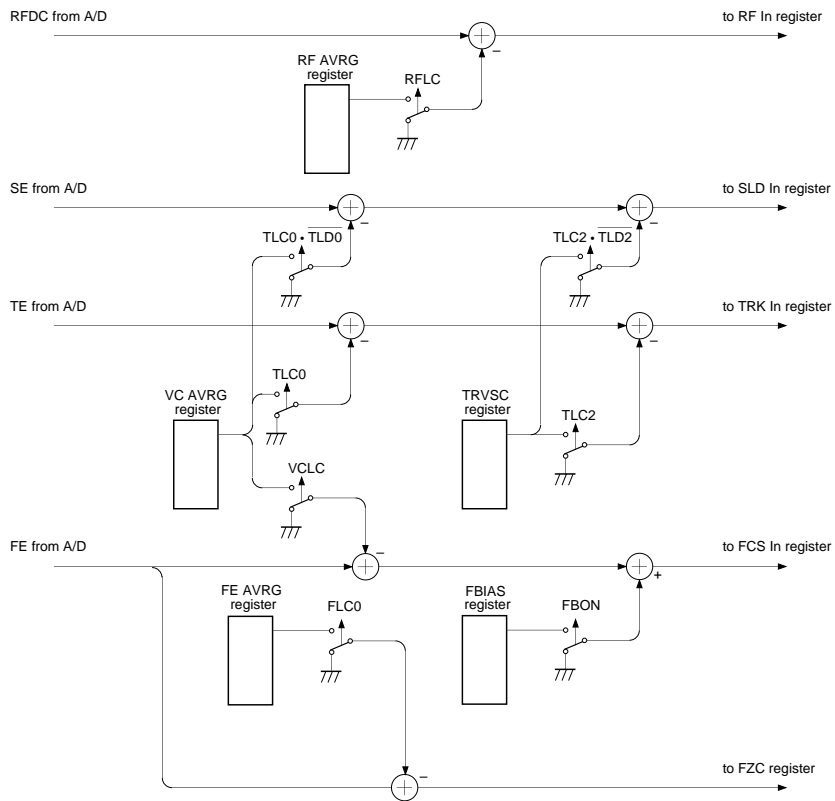
Fig. 4-3b

§4-6. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate servo loop gain. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.

The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the command register are 38 (h), the completion of AGCNTL operation can be confirmed by monitoring the SENS pin. (See Timing Chart 4-4 and "Description of SENS Signals".)

Setting D9 and D8 of $38 to 1 sets FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.

XLAT

Max. 11.4μs

SENS
(= AGOK)

AGCNTL completion
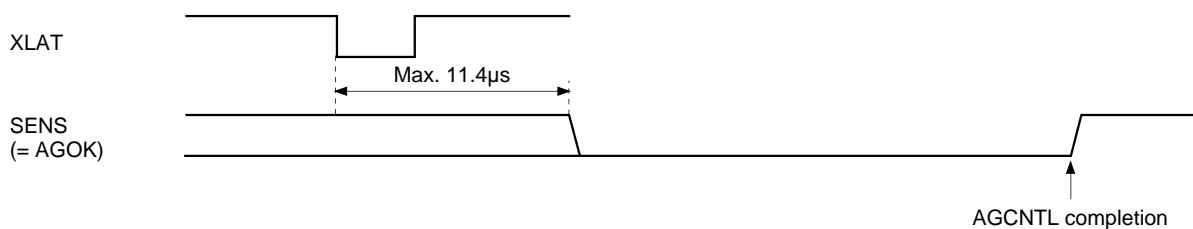
Timing Chart 4-4

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 change for AGT (tracking AGCNTL) due to AGCNTL.

These coefficients change from 01 to 7F (h), and they must also be set within this range when written externally. After AGCNTL operation has completed, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related settings

The following settings can be changed with $35, $36 and $37.

FG6 to FG0; AGF convergence gain setting, effective setting range: 00 to 57 (h)

TG6 to TG0; AGT convergence gain setting, effective setting range: 00 to 57 (h)

AGS;   Self-stop on/off

AGJ;   Convergence completion judgment time

AGGF;   Internally generated sine wave amplitude (AGF)

AGGT;   Internally generated sine wave amplitude (AGT)

AGV1;   AGCNTL sensitivity 1 (during rough adjustment)

AGV2;   AGCNTL sensitivity 2 (during fine adjustment)

AGHS;   Rough adjustment on/off

AGHT;   Fine adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to FG0 and TG6 to TG0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0 dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL default operation has two stages.

In the first stage, rough adjustment is performed with high sensitivity for a certain period of time (select 256/128ms with AGHT, when MCK = 128Fs), and the AGCNTL coefficient approaches the appropriate value. The sensitivity at this time can be selected from two types with AGV1.

In the second stage, the AGCNTL coefficient is finely adjusted with relatively low sensitivity to further approach the appropriate value. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD3017Q confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ, when MCK = 128Fs), and then completes AGCNTL operation. (Self-stop mode) This self-stop mode can be canceled by setting AGS to 0.

In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.

An example of AGCNTL coefficient transitions during AGCNTL operation with various settings is shown in Fig. 4-5.
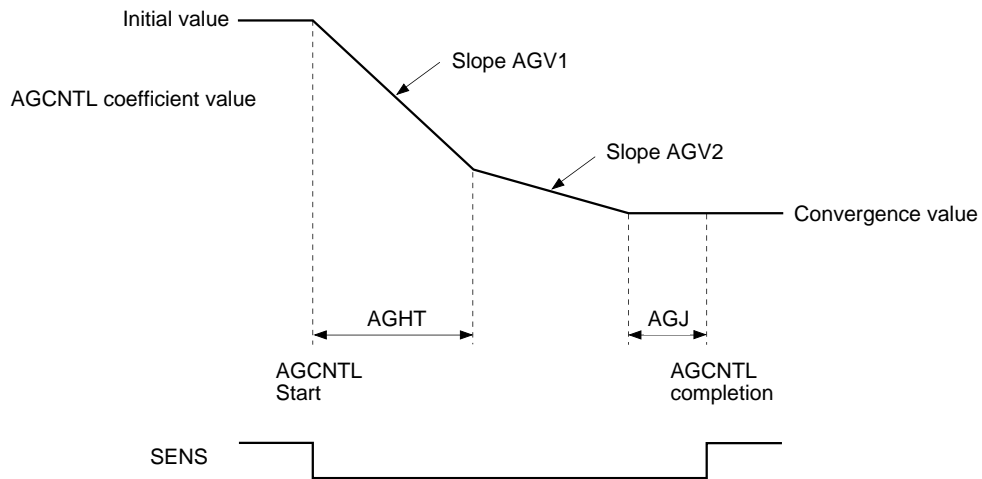
Fig. 4-5

Note) Fig. 4-5 shows the case where the AGCCNTL coefficient converges from the initial value to a smaller value.

§4-7. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command $0X. (See Table 4-6.)

Register name	Command	D23 to D20	D19 to D16	
0	FOCUS CONTROL	0 0 0 0	1 0 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1 1 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0 ∗ 0 ∗	FOCUS SERVO OFF, 0V OUT
			0 ∗ 1 ∗	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0 ∗ 1 0	FOCUS SEARCH VOLTAGE DOWN
			0 ∗ 1 1	FOCUS SEARCH VOLTAGE UP

∗: don't care

Table 4-6

FCS Search

FCS search is required in the course of turning on the FCS servo.

Fig. 4-7 shows the signals for sending commands $00 → $02 → $03 and performing only FCS search operation.
Fig. 4-8 shows the signals for sending $08 (FCS on) after that.
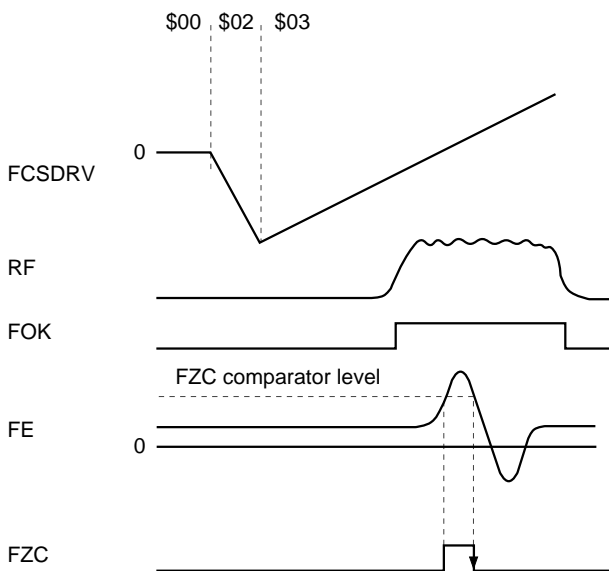
Fig. 4-7
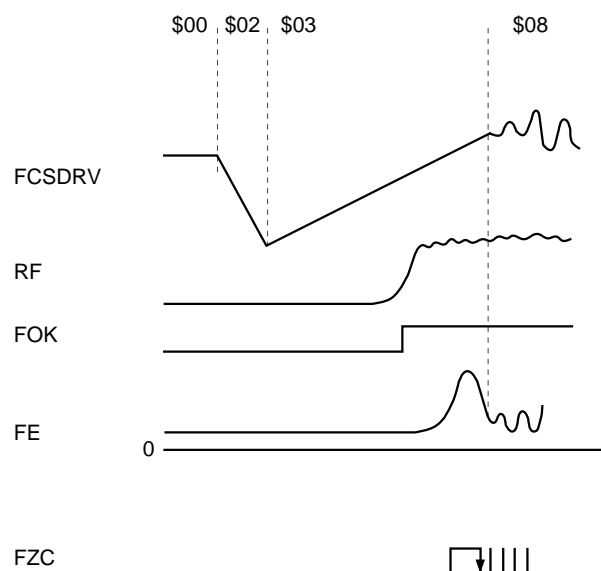
Fig. 4-8

§4-8. TRK (Tracking) and SLD (Sled) Servo Control

The TRK and SLD servos are controlled by the 8-bit command $2X. (See Table 4-9.)
When the upper 4 bits of the serial data are 2 (h), TZC is output to the SENS pin.

Register name	Command	D23 to D20	D19 to D16	
2	TRACKING MODE	0 0 1 0	0 0 ∗ ∗	TRACKING SERVO OFF
			0 1 ∗ ∗	TRACKING SERVO ON
			1 0 ∗ ∗	FORWARD TRACK JUMP
			1 1 ∗ ∗	REVERSE TRACK JUMP
			∗ ∗ 0 0	SLED SERVO OFF
			∗ ∗ 0 1	SLED SERVO ON
			∗ ∗ 1 0	FORWARD SLED MOVE
			∗ ∗ 1 1	REVERSE SLED MOVE

∗: don't care

Table 4-9

TRK Servo

The TRK JUMP (track jump) level can be set with 6 bits (D13 to D8) of $36.
In addition, when the TRK servo is on and D17 of $1 is set to 1, the TRK servo filter switches to gain-up mode.
The filter also switches to gain-up mode when the LOCK signal goes low or when vibration is detected with the anti-shock circuit (described hereafter) enabled.
The CXD3017Q has 2 types of gain-up filter structures in TRK gain-up mode which can be selected by setting D16 of $1. (See Table 4-17.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from 6 bits (D13 to D8) of $37, is determined by multiplying this value by 1×, 2×, 3×, or 4× set using D17 and D16 when D18 = D19 = 0 is set with $3. (See Table 4-10.)
SLD MOV must be performed continuously for 50µs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the TRK servo switches to gain-up mode and the SLD servo is turned off. These operations are disabled by setting D6 (LKSW) of $38 to 1.

Register name	Command	D23 to D20	D19 to D16	
3	SELECT	0 0 1 1	0 0 0 0	SLED KICK LEVEL (basic value × ±1)
			0 0 0 1	SLED KICK LEVEL (basic value × ±2)
			0 0 1 0	SLED KICK LEVEL (basic value × ±3)
			0 0 1 1	SLED KICK LEVEL (basic value × ±4)

Table 4-10

§4-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz (when MCK = 128Fs) and loaded. The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.

An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of this envelope waveform.

The MIRR signal is generated by comparing the waveform generated by subtracting the bottom hold value from the peak hold value with this MIRR comparator level. (See Fig. 4-11.)

The bottom hold speed and mirror sensitivity can be selected from four values using D7 and D6, and D5 and D4, respectively, of $3C.
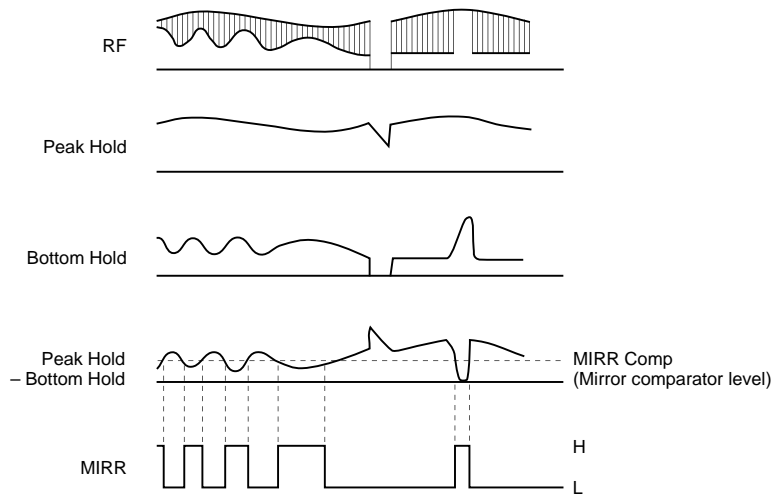
Fig. 4-11

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 4-12.)

The DFCT comparator level can be selected from four values using D13 and D12 of $3B.
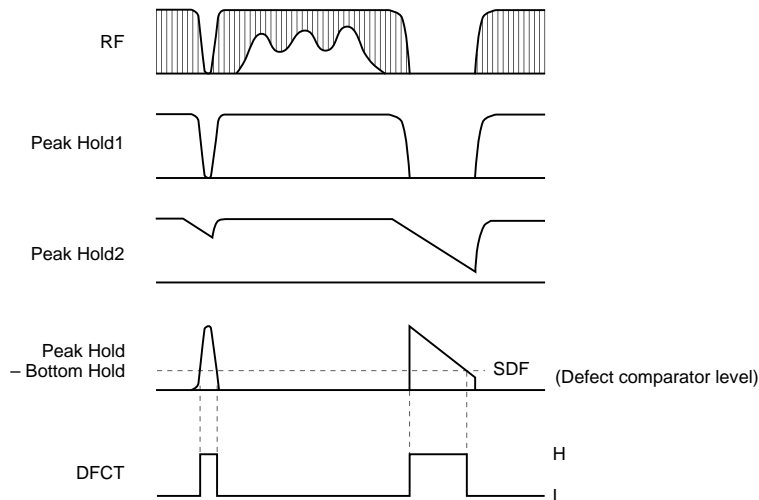
Fig. 4-12

§4-10. DFCT Countermeasure Circuit

The DFCT countermeasure circuit maintains the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.

Specifically, this operation is achieved by detecting scratches and defects with the DFCT signal generation circuit, and when DFCT goes high, applying the low-frequency component of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 4-13.)

In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of $38 to 1.
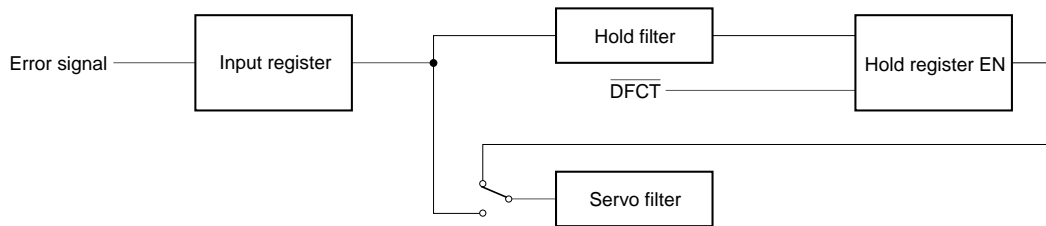
Fig. 4-13

§4-11. Anti-Shock Circuit

When vibrations occur in the CD player, this circuit forces the TRK filter to switch to gain-up mode so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures.

Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 4-14.)

The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by adjusting the value of the anti-shock filter output coefficient K35.

This function can be turned on and off by D19 of $1 when the brake circuit (described hereafter) is off. (See Table 4-17.)

This circuit can also support an external vibration detection circuit, and can set the TRK servo filter to gain-up mode by inputting high level to the ATSK pin.

When the upper 4 bits of the command register are 1 (h), vibration detection can be monitored from the SENS pin. It can also be monitored from the ATSK pin by setting $3F command ASOT to 1.
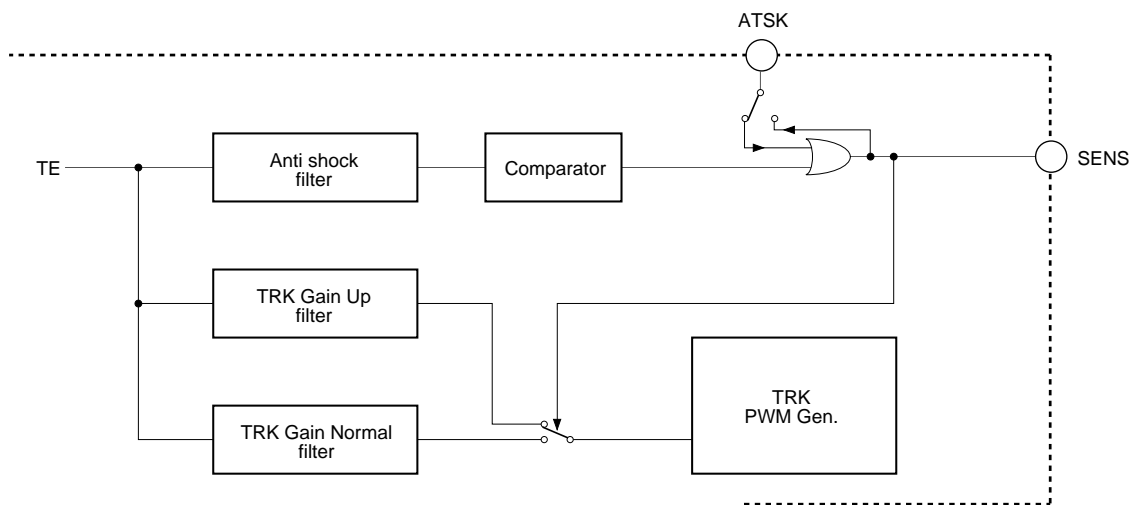
Fig. 4-14

§4-12. Brake Circuit

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

In principle, the brake circuit uses the tracking drive as a brake by cutting the unnecessary portions utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 4-15 and 4-16.)

Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of $1. (See Table 4-17.)

In addition, the low frequency for the tracking drive after masking can be boosted. (SFBK1, 2 of $34B)

Inner track → Outer track

Outer track → Inner track
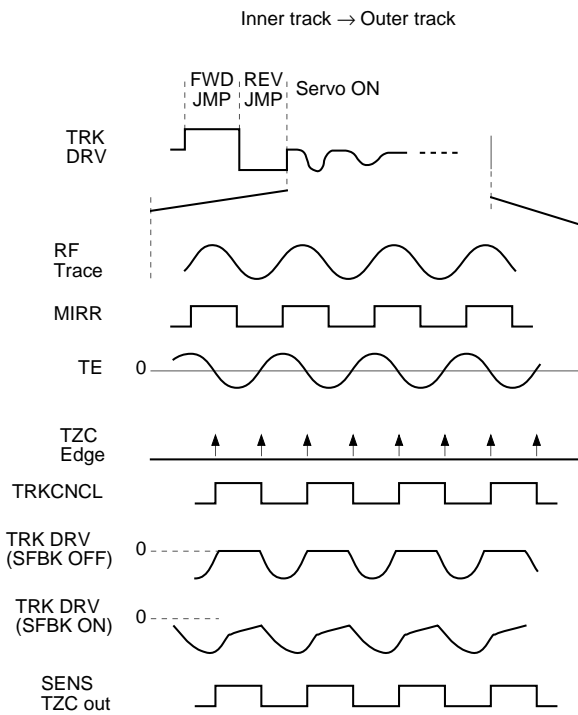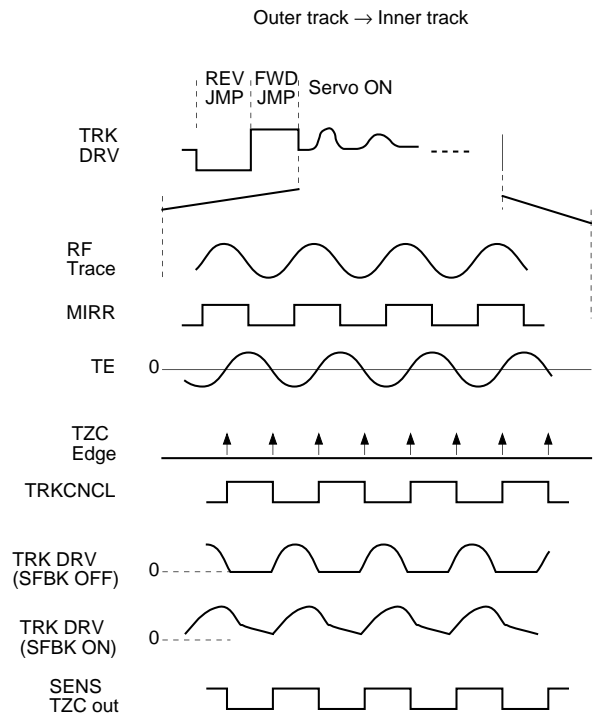
Fig. 4-15

Fig. 4-16

Register name	Command	D23 to D20	D19 to D16	
1	TRACKING CONTROL	0 0 0 1	1 0 ∗ ∗	ANTI SHOCK ON
			0 ∗ ∗ ∗	ANTI SHOCK OFF
			∗ 1 ∗ ∗	BRAKE ON
			∗ 0 ∗ ∗	BRAKE OFF
			∗ ∗ 0 ∗	TRACKING GAIN NORMAL
			∗ ∗ 1 ∗	TRACKING GAIN UP
			∗ ∗ ∗ 1	TRACKING GAIN UP FILTER SELECT 1
			∗ ∗ ∗ 0	TRACKING GAIN UP FILTER SELECT 2

∗: don't care

Table 4-17

§4-13. COUT Signal

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. The used TZC signal can be selected from among three different phases according to the COUT signal application.

- • HPTZC: For 1-track jumps
      Fast phase COUT signal generation with a fast phase TZC signal. (The TZC phase is advanced by a cut-off 1kHz digital HPF; when MCK = 128Fs.)
- • STZC: For COUT generation when MIRR is externally input and for applications other than COUT generation. This is generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
- • DTZC: For high-speed traverse
      Reliable COUT signal generation with a delayed phase STZC signal.

Since it takes some time to generate the MIRR signal, it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.
The COUT signal output method is switched with D15 and D14 of $3C.

    When D15 = 1:   STZC
    When D15 = 0 and D14 = 0: HPTZC
    When D15 = 0 and D14 = 1: DTZC

When DTZC is selected, the delay can be selected from two values with D14 of $36.

§4-14. Serial Readout Circuit

The following measurement and adjustment results specified beforehand by serial command $39 can be read out from the SENS pin by inputting the readout clock to the SCLK pin. (See Fig. 4-18, Table 4-19 and "Description of SENS Signals".)

Specified commands
    $390C: VC AVRG measurement result $3953: FCS AGCNTL coefficient result
    $3908: FE AVRG measurement result $3963: TRK AGCNTL coefficient result
    $3904: TE AVRG measurement result $391C: TRVSC adjustment result
    $391F: RF AVRG measurement result $391D: FBIAS register value
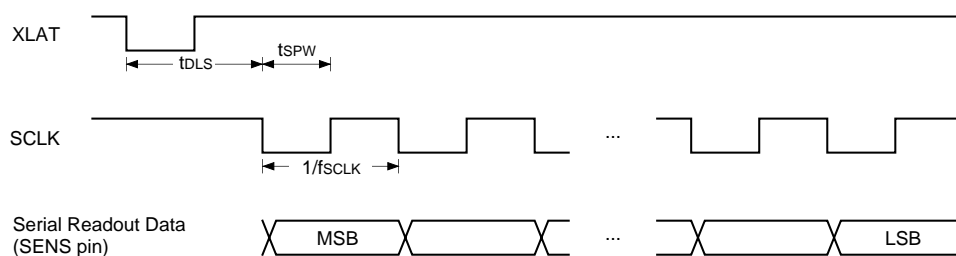
Fig. 4-18

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			μs

Table 4-19

During readout, the upper 8 bits of the command register must be 39 (h).

§4-15. Writing to Coefficient RAM

The coefficient RAM can be rewritten by $34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40μs (when MCK = 128Fs) after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)

After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.

The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of $34 as the address (D15 = 0) and D7 to D0 as the data. Coefficient rewriting is completed 11.3μs (when MCK = 128Fs) after the command is received. When rewriting multiple coefficients continuously, be sure to wait 11.3μs (when MCK = 128Fs) before sending the next rewrite command.

§4-16. PWM Output

FCS, TRK and SLD PWM format outputs are described below.

In particular, FCS and TRK use a double oversampling noise shaper.

Timing Chart 4-20 and Fig. 4-21 show examples of output waveforms and drive circuits.

$$t_{MCK} = \frac{1}{5.6448MHz} \approx 180ns$$
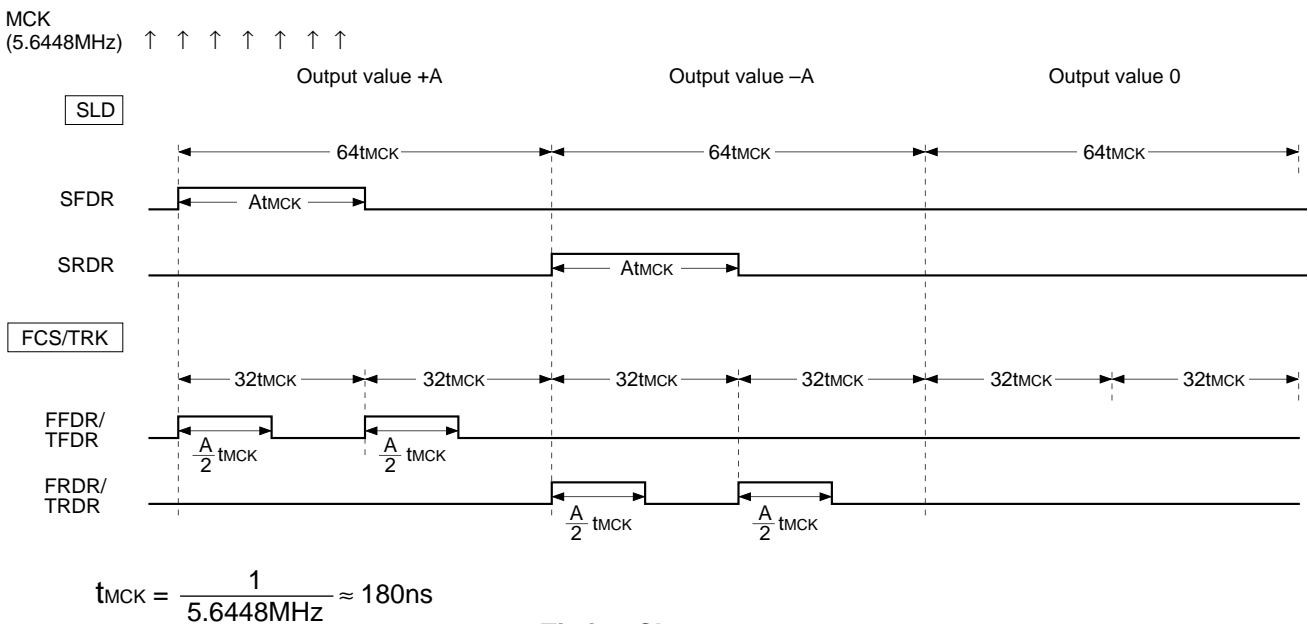
Timing Chart 4-20
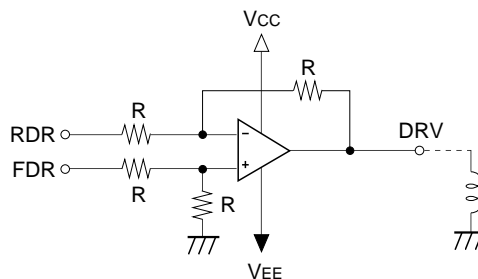
Fig. 4-21. Drive Circuit

§4-17. Servo Status Changes Produced by LOCK Signal

When the LOCK signal becomes low, the TRK servo switches to the gain-up mode and the SLD servo turns off in order to prevent SLD free-running.
Setting D6 (LKSW) of $38 to 1 deactivates this function.
In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low.
This enables microcomputer control.

§4-18. Description of Commands and Data Sets

$34

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	KA6	KA5	KA4	KA3	KA2	KA1	KA0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

When D15 = 0.
   KA6 to KA0: Coefficient address
   KD7 to KD0: Coefficient data

$348 (preset: $348 000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PFOK1	PFOK0	0	0	0	MRS	MRT1	MRT0	0	0

These commands set the FOK signal hold time. See $3B for the FOK slice level.
These are the values when MCK = 128Fs, and the hold time is inversely proportional to the MCK setting.

PFOK1	PFOK0	Processing
0	0	High when the RFDC value is higher than the FOK slice level, low when lower than the FOK slice level.
0	1	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 4.35ms or more.
1	0	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 10.16ms or more.
1	1	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 21.77ms or more.

MRS: This command switches the time constant for generating the MIRR comparator level of the MIRR generation circuit.
              When 0, the time constant is normal. (default)
              When 1, the time constant is longer than normal.
              The time during which MIRR = high due to the effects of RFDC signal pulse noise, etc., can be suppressed by setting MRS = 1.

MRT1, 0:   These commands limit the time while MIRR = high.

	MRT1	MRT0	MIRR maximum time [ms]
∗	0	0	No time limit
	0	1	1.10
	1	0	2.20
	1	1	4.00

∗: preset

$34B (preset: $34B 000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	SFBK1	SFBK2	0	0	0	0	0	0	0	0	0	0

The low frequency can be boosted for brake operation.
See §4-12 for brake operation.

SFBK1:   When 1, brake operation is performed by setting the LowBooster-1 input to 0.
         This is valid only when TLB1ON = 1. Preset is 0.
SFBK2:   When 1, brake operation is performed by setting the LowBooster-2 input to 0.
         This is valid only when TLB2ON = 1. Preset is 0.

$34C (preset: $34C 000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	THBON	FHBON	TLB1ON	FLB1ON	TLB2ON	0	HBST1	HBST0	LB1S1	LB1S0	LB2S1	LB2S0

These bits turn on the boost function. (See §4-20. Filter Composition.)
There are five boosters (three for the TRK filter and two for the FCS filter) which can be turned on and off independently.

THBON: When 1, the high frequency is boosted for the TRK filter. Preset is 0.
FHBON: When 1, the high frequency is boosted for the FCS filter. Preset is 0.
TLB1ON: When 1, the low frequency is boosted for the TRK filter. Preset is 0.
FLB1ON: When 1, the low frequency is boosted for the FCS filter. Preset is 0.
TLB2ON: When 1, the low frequency is boosted for the TRK filter. Preset is 0.

The difference between TLB1ON and TLB2ON is the position where the low frequency is boosted.
For TLB1ON, the low frequency is boosted before the TRK jump, and for TLB2ON, after the TRK jump.

The following commands set the boosters. (See §4-20. Filter Composition.)

HBST1, HBST0: TRK and FCS HighBooster setting.
              HighBooster has the configuration shown in Fig. 4-22a, and can select three different
              combinations of coefficients BK1, BK2 and BK3. (See Table 4-23a.)
              An example of characteristics is shown in Fig. 4-24a.
              These characteristics are the same for both the TRK and FCS filters.
              The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB1S1, LB1S0: TRK and FCS LowBooster-1 setting.
              LowBooster-1 has the configuration shown in Fig. 4-22b, and can select three different
              combinations of coefficients BK4, BK5 and BK6. (See Table 4-23b.)
              An example of characteristics is shown in Fig. 4-24b.
              These characteristics are the same for both the TRK and FCS filters.
              The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB2S1, LB2S0: TRK LowBooster-2 setting.
              LowBooster-2 has the configuration shown in Fig. 4-22c, and can select three different
              combinations of coefficients BK7, BK8 and BK9. (See Table 4-23c.)
              An example of characteristics is shown in Fig. 4-24c.
              This booster is used exclusively for the TRK filter.
              The sampling frequency is 88.2kHz (when MCK = 128Fs).

              Note) Fs = 44.1kHz
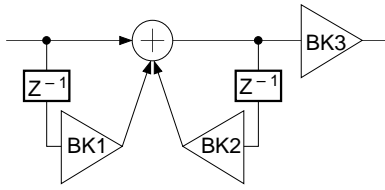
Fig. 4-22a

HBST1	HBST0	HighBooster setting		
		BK1	BK2	BK3
0	—	−120/128	96/128	2
1	0	−124/128	112/128	2
1	1	−126/128	120/128	2

Table 4-23a
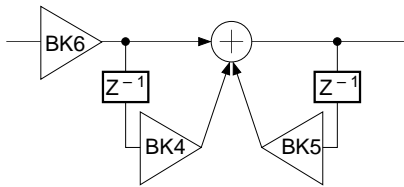
Fig. 4-22b

LB1S1	LB1S0	LowBooster-1 setting		
		BK4	BK5	BK6
0	—	−255/256	1023/1024	1/4
1	0	−511/512	2047/2048	1/4
1	1	−1023/1024	4095/4096	1/4

Table 4-23b
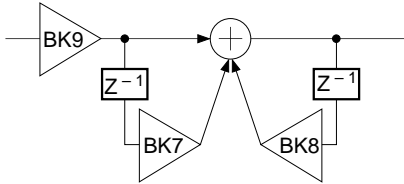
Fig. 4-22c

LB2S1	LB2S0	LowBooster-2 setting		
		BK7	BK8	BK9
0	—	−255/256	1023/1024	1/4
1	0	−511/512	2047/2048	1/4
1	1	−1023/1024	4095/4096	1/4

Table 4-23c
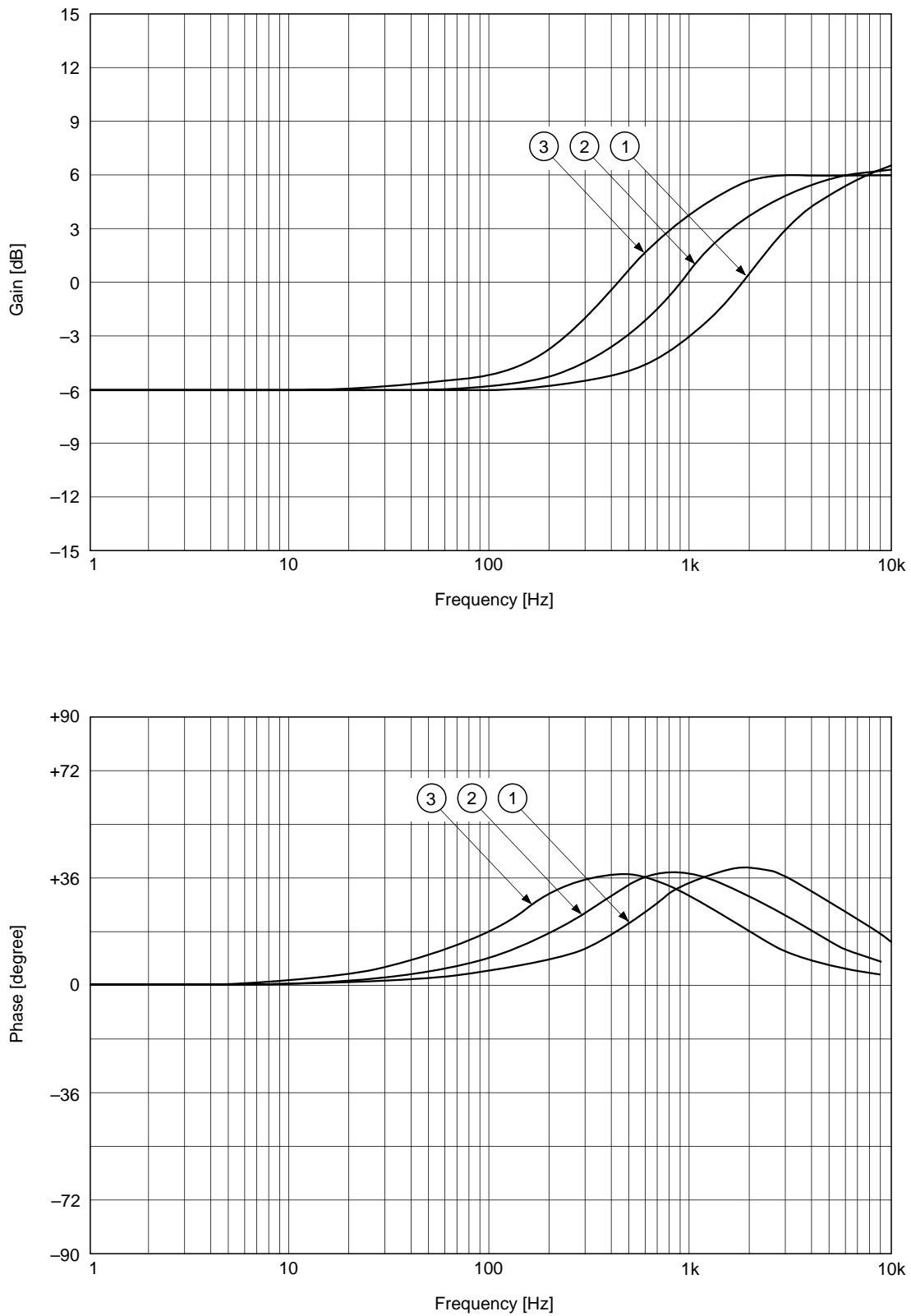
Fig. 4-24a. Servo HighBooster characteristics [FCS, TRK] (MCK = 128Fs)

① HBST1 = 0   ② HBST1 = 1, HBST0 = 0   ③ HBST1 = 1, HBST0 = 1
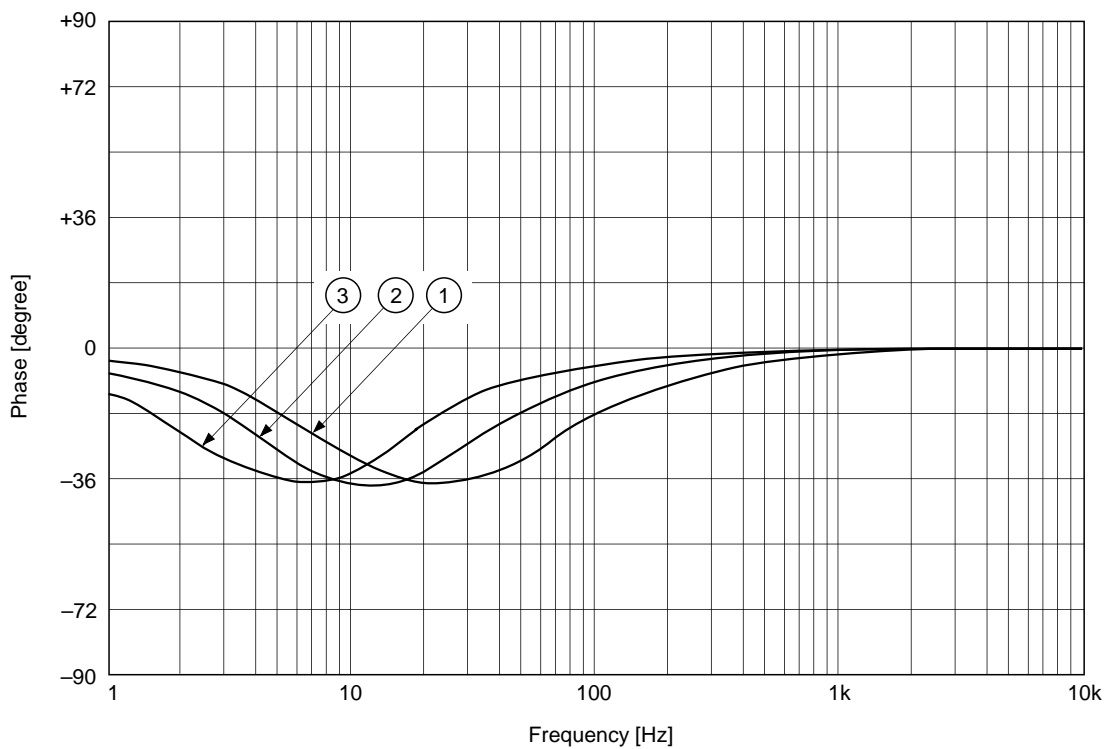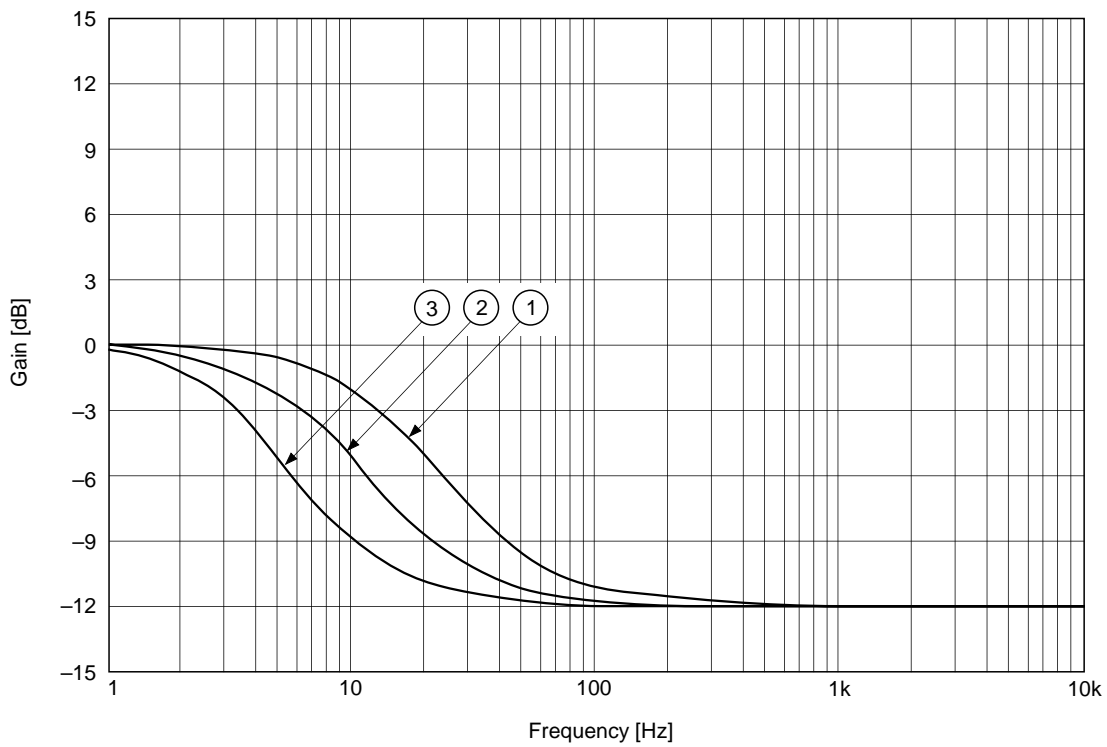
Fig. 4-24b. Servo LowBooster-1 characteristics [FCS, TRK] (MCK = 128Fs)

① LB1S1 = 0   ② LB1S1 = 1, LB1S0 = 0   ③ LB1S1 = 1, LB1S0 = 1
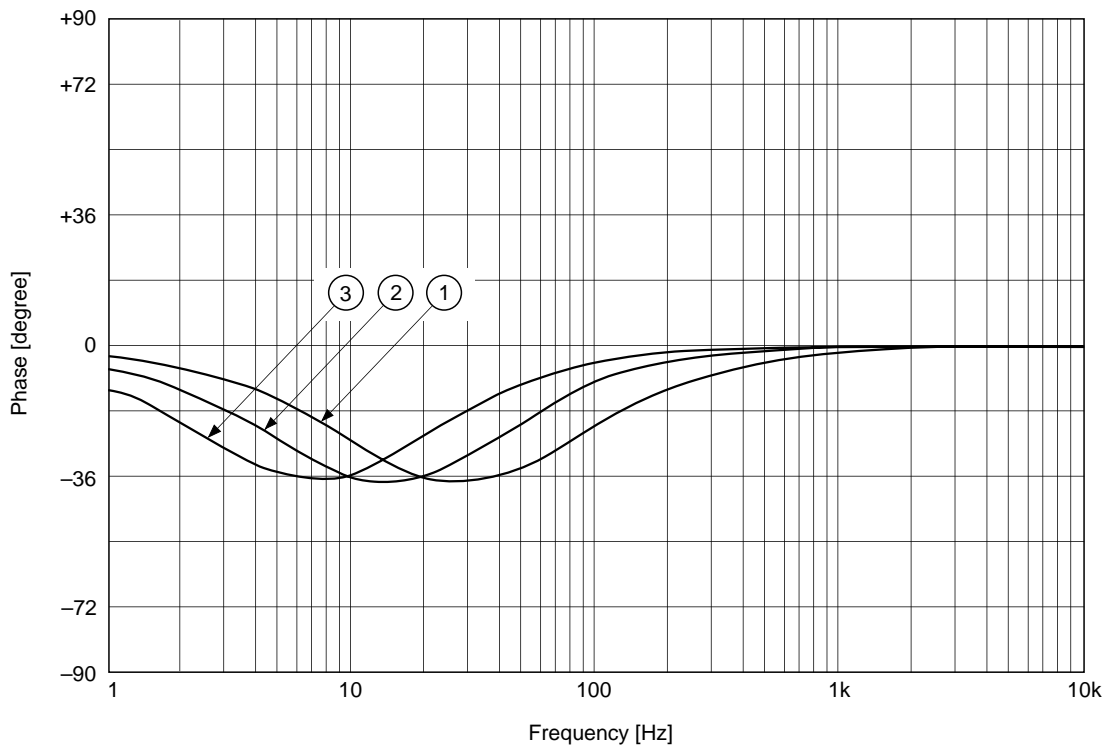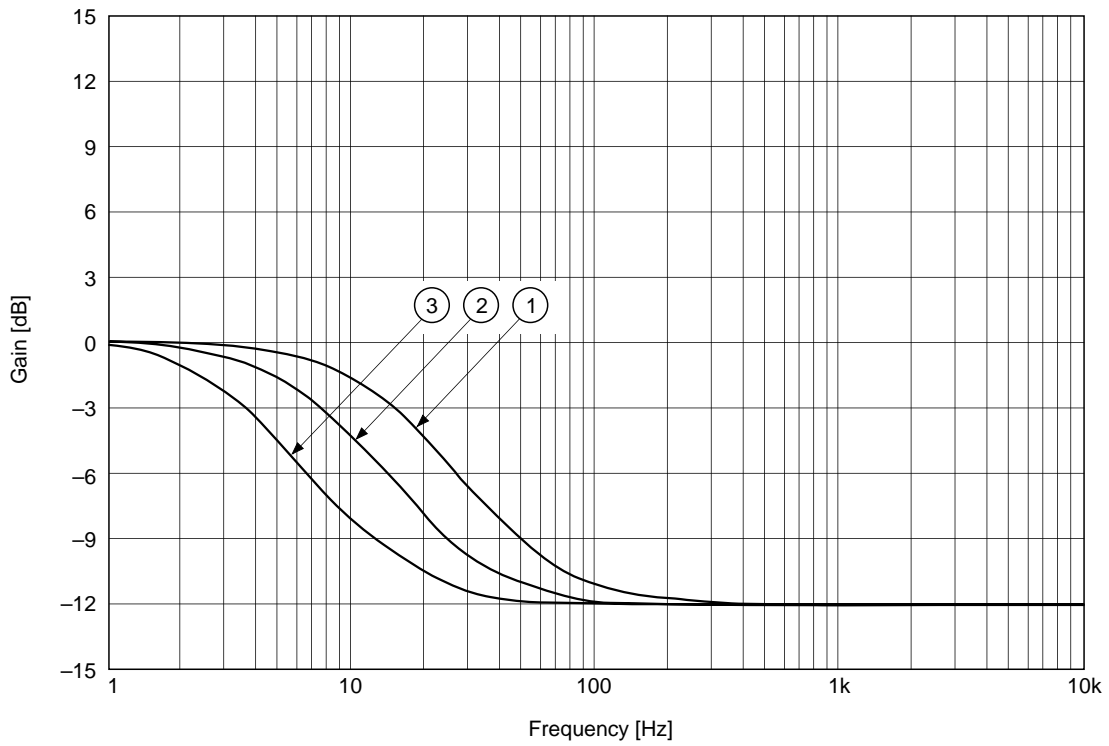
Fig. 4-24c. Servo LowBooster-2 characteristics [TRK] (MCK = 128Fs)

① LB2S1 = 0   ② LB2S1 = 1, LB2S0 = 0   ③ LB2S1 = 1, LB2S0 = 1

$34E (preset: $34E000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	IDFSL3	IDFSL2	IDFSL1	IDFSL0	0	0	IDFT1	IDFT0	0	0	0	INVRFDC

IDFSL3:   New DFCT detection output setting.

When 0, only the DFCT signal described in §4-9 is detected and output from the DFCT pin. (default)

When 1, the DFCT signal described in §4-9 and the new DFCT signal are switched and output from the DFCT pin.

The switching timing is as follows.

When the §4-9 DFCT signal is low, the new DFCT signal is output from the DFCT pin.

When the §4-9 DFCT signal is high, this DFCT signal is output from the DFCT pin.

In addition, the time at which the new DFCT signal can be output after the §4-9 DFCT signal switches to low can also be set. (See IDFT1, 0 of $34E.)

IDFSL3	§4-9 DFCT	DFCT pin
0	L	§4-9 DFCT
0	H	§4-9 DFCT
1	L	New DFCT
1	H	§4-9 DFCT

IDFSL2:   New DFCT detection time setting.

DFCT = high is held for a certain time after new DFCT detection. This command sets that time.

When 0, a long hold time. (default)

When 1, a short hold time.

IDFSL1:   New DFCT detection sensitivity setting.

When 0, a high detection sensitivity. (default)

When 1, a low detection sensitivity.

IDFSL0:   New DFCT release sensitivity setting.

When 0, a high release sensitivity. (default)

When 1, a low release sensitivity.

IDFT1, 0:   These commands set the time at which the new DFCT signal can be output (output prohibited time) after the §4-9 DFCT signal switches to low.

IDFT1	IDFT0	New DFCT signal output prohibited time
0	0	204.08μs
0	1	294.78μs
1	0	408.16μs
1	1	612.24μs

∗: preset

INVRFDC: RFDC signal polarity inverted input setting.

When 0, the RFDC signal polarity is set to non-inverted. (default)

When 1, the RFDC signal polarity is set to inverted.

$34F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—

When D15 = D14 = D13 = D12 = D11 = 1 ($34F)

    D10 = 0

    FBIAS LIMIT register write

    FBL9 to FBL1: Data; data compared with FB9 to FB1, FBL9 = MSB.

              When using the FBIAS register in counter mode, counter operation stops when the

              value of FB9 to FB1 matches with FBL9 to FBL1.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—

When D15 = D14 = D13 = D12 = 1 ($34F)

    D11 = 0, D10 = 1

    FBIAS register write

    FB9 to FB1: Data;   two's complement data, FB9 = MSB.

              For FE input conversion, FB9 to FB1 = 011111111 corresponds to $255/256 \times V_{DD}/4$

              and FB9 to FB1 = 100000000 to $-256/256 \times V_{DD}/4$ respectively. (V_{DD}: supply voltage)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0

When D15 = D14 = D13 = D12 = 1 ($34F)

    D11 = 0, D10 = 0

    TRVSC register write

    TV9 to TV0: Data;   two's complement data, TV9 = MSB.

              For TE input conversion, TV9 to TV0 = 0011111111 corresponds to $255/256 \times V_{DD}/4$

              and TV9 to TV0 = 1100000000 to $-256/256 \times V_{DD}/4$ respectively. (V_{DD}: supply voltage)

Notes) • When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to
      each bit TV8 to TV0 during external write are read out.

     • When reading out internally measured values and then writing these values externally, set TV9 the
      same as TV8.

$35 (preset: $35 58 2D)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0

FT1, FT0, FTZ: Focus search-up speed

Default value: 010 ($0.673 \times V_{DD}$V/s)

Focus drive output conversion

FT1	FT0	FTZ	Focus search speed [V/s]
0	0	0	$1.35 \times V_{DD}$
0	1	0	$0.673 \times V_{DD}$
1	0	0	$0.449 \times V_{DD}$
1	1	0	$0.336 \times V_{DD}$
0	0	1	$1.79 \times V_{DD}$
0	1	1	$1.08 \times V_{DD}$
1	0	1	$0.897 \times V_{DD}$
1	1	1	$0.769 \times V_{DD}$

∗ (second row marked preset)

∗: preset, V_{DD}: PWM driver supply voltage

FS5 to FS0: Focus search limit voltage

Default value: 011000 ($(1 \pm 24/64) \times V_{DD}/2$, V_{DD}: PWM driver supply voltage)

Focus drive output conversion

FG6 to FG0: AGF convergence gain setting value

Default value: 0101101

$36 (preset: $36 0E 2E)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0

DTZC: DTZC delay (8.5/4.25μs, when MCK = 128Fs)

Default value: 0 (4.25μs)

TJ5 to TJ0: Track jump voltage

Default value: 001110 ($(1 \pm 14/64) \times V_{DD}/2$, V_{DD}: PWM driver supply voltage)

Tracking drive output conversion

SFJP: Surf jump mode on/off

The tracking PWM output is generated by adding the tracking filter output and TJReg (TJ5 to TJ0), by setting D7 to 1 (on)

TG6 to TG0: AGT convergence gain setting value

Default value: 0101110

$37 (preset: $37 50 BA)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT

FZSH, FZSL: FZC (Focus Zero Cross) slice level

Default value: 01 (1/8 × V_{DD}/2, V_{DD}: supply voltage); FE input conversion

	FZSH	FZSL	Slice level
	0	0	1/4 × V_{DD}/2
∗	0	1	1/8 × V_{DD}/2
	1	0	1/16 × V_{DD}/2
	1	1	1/32 × V_{DD}/2

∗: preset

SM5 to SM0: Sled move voltage

Default value: 010000 ((1 ± 16/64) × V_{DD}/2, V_{DD}: PWM driver supply voltage)

Sled drive output conversion

AGS: AGCNTL self-stop on/off

Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms, when MCK = 128Fs)

Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

		FE/TE input conversion
AGGF	0 (small)	1/32 × V_{DD}/2
	1 (large)∗	1/16 × V_{DD}/2
AGGT	0 (small)	1/16 × V_{DD}/2
	1 (large)∗	1/8 × V_{DD}/2

∗: preset

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low

Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low

Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off

Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms, when MCK = 128Fs)

Default value: 0 (256ms)

$38 (preset: $38 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0

DC offset cancel. See §4-3.
* VCLM: VC level measurement (on/off)
  VCLC: VC level compensation for FCS In register (on/off)
* FLM: Focus zero level measurement (on/off)
  FLC0: Focus zero level compensation for FZC register (on/off)
* RFLM: RF zero level measurement (on/off)
  RFLC: RF zero level compensation (on/off)

Automatic gain control. See §4-6.
  AGF: Focus auto gain adjustment (on/off)
  AGT: Tracking auto gain adjustment (on/off)

Misoperation prevention circuit
  DFSW: Defect disable switch (on/off)
    Setting this switch to 1 (on) disables the defect countermeasure circuit.
  LKSW: Lock switch (on/off)
    Setting this switch to 1 (on) disables the sled free-running prevention circuit.

DC offset cancel. See §4-3.
  TBLM: Traverse center measurement (on/off)
* TCLM: Tracking zero level measurement (on/off)
  FLC1: Focus zero level compensation for FCS In register (on/off)
  TLC2: Traverse center compensation (on/off)
  TLC1: Tracking zero level compensation (on/off)
  TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with ∗ are accepted every 2.9ms. (when MCK = 128Fs)
    All commands are on when 1.

$39 (preset: $390000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0	0	0	0	0	0	0	0	0

When $3A command SVDA = 0

DAC: Serial data readout DAC mode setting.

When 0, serial data cannot be read out. (default)

When 1, serial data can be read out.

SD6 to SD0: These bits select the serial readout data.

D14	D13	D12	D11	D10	D9	D8	Readout data	Readout data length
SD6	SD5	SD4	SD3	SD2	SD1	SD0		
1			Coefficient RAM address				Coefficient RAM data	8 bits
0	1			Data RAM address			Data RAM data	16 bits
0	0	1	1	1	1	1	RF AVRG register	8 bits
0	0	1	1	1	1	0	RFDC input signal	8 bits
0	0	1	1	1	0	1	FCS Bias register	9 bits
0	0	1	1	1	0	0	TRVSC register	9 bits
0	0	1	0	1	0	0	DFCT count	8 bits
0	0	1	0	0	1	1	RFDC (Bottom)	8 bits
0	0	1	0	0	1	0	RFDC (Peak)	8 bits
0	0	1	0	0	0	1	RFDC (Peak – Bottom)	8 bits
0	0	0	1	1	∗	∗	VC AVRG register	9 bits
0	0	0	1	0	∗	∗	FE AVRG register	9 bits
0	0	0	0	1	∗	∗	TE AVRG register	9 bits
0	0	0	0	0	1	1	FE input signal	8 bits
0	0	0	0	0	1	0	TE input signal	8 bits
0	0	0	0	0	0	1	SE input signal	8 bits
0	0	0	0	0	0	0	VC input signal	8 bits

∗: don't care

Note) When $3A SVDA is changed, select the readout data again.

The DFCT count counts the number of times the DFCT signal rises while $3994 is set.

Readout outputs the DFCT count at that time.

When $3A command SVDA = 1

DAC: This command selects whether to set readout data for the left or right channel.

When 0, right channel readout data is selected. (default)

When 1, left channel readout data is selected.

SD6 to SD0: These bits select the data to be output from the left or right channel.

D14	D13	D12	D11	D10	D9	D8	Readout data	Readout data length
SD6	SD5	SD4	SD3	SD2	SD1	SD0		
0	1	Data RAM address					Data RAM data	16 bits
0	0	1	1	1	1	1	RF AVRG register	8 bits
0	0	1	1	1	1	0	RFDC input signal	8 bits
0	0	1	1	1	0	1	FCS Bias register	9 bits
0	0	1	1	1	0	0	TRVSC register	9 bits
0	0	0	1	1	*	*	VC AVRG register	9 bits
0	0	0	1	0	*	*	FE AVRG register	9 bits
0	0	0	0	1	*	*	TE AVRG register	9 bits
0	0	0	0	0	1	1	FE input signal	8 bits
0	0	0	0	0	1	0	TE input signal	8 bits
0	0	0	0	0	0	1	SE input signal	8 bits
0	0	0	0	0	0	0	VC input signal	8 bits

*1 (marks FE AVRG register row)
*2 (marks TE AVRG register row)

∗: don't care

*1 Right channel preset

*2 Left channel preset

Note) Coefficient RAM data cannot be output from the audio DAC side.

Do not output RFDC (peak, bottom, peak-bottom) or the DFCT count from the audio DAC side.

When $3A SVDA is changed, select the readout data again.

$3A (preset: $3A0000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	FBON	0	0	0	0	FIFZC	0	FPS1	FPS0	TPS1	TPS0	SVDA	0	0	0

FBON: FBIAS (focus bias) register operation setting.

FBON	Processing
0	FBIAS (focus bias) register addition off.
1	FBIAS (focus bias) register addition on.

FIFZC: This selects the FZC slice level setting command.

When 0, the FZC slice level is determined by the $37 FZSH and FZSL setting values. (default)

When 1, the FZC slice level is determined by the $3F8 FIFZB3 to FIFZB0 and FIFZA3 to FIFZA0 setting values.

This allows more detailed setting and the addition of hysteresis compared to the $37 FZSH and FZSL setting.

FPS1, FPS0:   Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0:   Gain setting when transferring data from the tracking filter to the PWM block.

These are effective for increasing the overall gain in order to widen the servo band, etc.

Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus and tracking by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

	FPS1	FPS0	Relative gain		TPS1	TPS0	Relative gain	
*	0	0	0dB		0	0	0dB	*
	0	1	+6dB		0	1	+6dB	
	1	0	+12dB		1	0	+12dB	
	1	1	+18dB		1	1	+18dB	

∗: preset

SVDA: This allows the data set by the $39 command to be output through the audio DAC.

When 0, audio is output. (default)

When 1, the data set by the $39 command is output.

$3B (preset: $3B E0 50)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	0	0	0	0

SFOX, SFO2, SFO1:

FOK slice level

Default value: 011 ($28/256 \times V_{DD}/2$, V_{DD} = supply voltage)

RFDC input conversion

	SFOX	SFO2	SFO1	Slice level
	0	0	0	$16/256 \times V_{DD}/2$
	0	0	1	$20/256 \times V_{DD}/2$
	0	1	0	$24/256 \times V_{DD}/2$
*	0	1	1	$28/256 \times V_{DD}/2$
	1	0	0	$32/256 \times V_{DD}/2$
	1	0	1	$40/256 \times V_{DD}/2$
	1	1	0	$48/256 \times V_{DD}/2$
	1	1	1	$56/256 \times V_{DD}/2$

∗: preset

SDF2, SDF1: DFCT slice level

Default value: 10 ($0.0313 \times V_{DD}$)

RFDC input conversion

	SDF2	SDF1	Slice level
	0	0	$0.0156 \times V_{DD}$
	0	1	$0.0234 \times V_{DD}$
*	1	0	$0.0313 \times V_{DD}$
	1	1	$0.0391 \times V_{DD}$

∗: preset, V_{DD}: supply voltage

MAX2, MAX1: DFCT maximum time (MCK = 128Fs)

Default value: 00 (no timer limit)

	MAX2	MAX1	DFCT maximum time
*	0	0	No timer limit
	0	1	2.00ms
	1	0	2.36
	1	1	2.72

∗: preset

BTF: Bottom hold double-speed count-up mode for MIRR signal generation

On/off (default: off)

On when 1.

D2V2, D2V1: Peak hold 2 for DFCT signal generation

Count-down speed setting

Default value: 01 (0.086 × V_{DD}/ms, 44.1kHz)

[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D2V2	D2V1	Count-down speed	
		[V/ms]	[kHz]
0	0	0.0431 × V_{DD}	22.05
0	1	0.0861 × V_{DD}	44.1
1	0	0.172 × V_{DD}	88.2
1	1	0.344 × V_{DD}	176.4

∗: preset, V_{DD}: supply voltage

D1V2, D1V1: Peak hold 1 for DFCT signal generation

Count-down speed setting

Default value: 01 (0.688 × V_{DD}/ms, 352.8kHz)

[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D1V2	D1V1	Count-down speed	
		[V/ms]	[kHz]
0	0	0.344 × V_{DD}	176.4
0	1	0.688 × V_{DD}	352.8
1	0	1.38 × V_{DD}	705.6
1	1	2.75 × V_{DD}	1411.2

∗: preset, V_{DD}: supply voltage

$3C (preset: $3C 00 80)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0

COSS, COTS: These select the TZC signal used when generating the COUT signal.

	COSS	COTS	TZC
	1	—	STZC
*	0	0	HPTZC
	0	1	DTZC

*: preset, —: don't care

STZC is the TZC generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
DTZC is the delayed phase STZC. (The delay time can be selected by D14 of $36.)
HPTZC is the fast phase TZC passed through a HPF with a cut-off frequency of 1kHz.
See §4-13.

CETZ: Normally, the input from the TE pin enters the TRK filter and is used to generate the TZC
              signal. However, the input from the CE pin can also be used. This function is for the center
              error servo.
              When 0, the TZC signal is generated by using the signal input to the TE pin.
              When 1, the TZC signal is generated by using the signal input to the CE pin.
CETF: When 0, the signal input to the TE pin is input to the TRK servo filter.
              When 1, the signal input to the CE pin is input to the TRK servo filter.

These commands output the TZC signal.
COT2, COT1:   The COUT signal is replaced by the TZC signal. Concretely, the TZC signal is output from the
              COUT pin and the TZC signal is used for auto sequence instead of the COUT signal.

	COT2	COT1	COUT pin output
	1	—	STZC
	0	1	HPTZC
*	0	0	COUT

*: preset, —: don't care

MOT2:   The MIRR signal is replaced by the STZC signal. Concretely, the STZC signal is output from
              the MIRR pin and the STZC signal is used for generating the COUT signal instead of the MIRR
              signal.

These commands set the MIRR signal generation circuit.
BTS1, BTS0:   These set the count-up speed for the bottom hold value of the MIRR generation circuit.
              The time per step is approximately 708ns (when MCK = 128Fs). The preset value is BTS1 = 1,
              BTS0 = 0 like the CXD2586R. These bits are valid only when BTF of $3B is 0.
MRC1, MRC0:   These set the minimum pulse width for masking the MIRR signal of the MIRR generation circuit.
              As noted in §4-9, the MIRR signal is generated by comparing the waveform obtained by
              subtracting the bottom hold value from the peak hold value with the MIRR comparator level.
              Strictly speaking, however, for MIRR to become high, these levels must be compared
              continuously for a certain time. These bits set that time.
              The preset value is MRC1 = 0, MRC0 = 0 like the CXD2586R.

	BTS1	BTS0	Number of count-up steps per cycle
	0	0	1
	0	1	2
*	1	0	4
	1	1	8

MRC1	MRC0	Setting time [µs]
0	0	5.669 *
0	1	11.338
1	0	22.675
1	1	45.351

*: preset (when MCK = 128Fs)

$3D (preset: $3D 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFID	SFSK	THID	THSK	ABEF	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0

SFID: SLED servo filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When the low frequency component of the tracking error signal obtained from the RF amplifier is attenuated, the low frequency can be amplified and input to the SLD servo filter.

SFSK: Only during TRK servo gain up2 operation, coefficient K30 is used instead of K00. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M00 can be kept uniform by adjusting the K30 value even during the above switching.

THID: TRK hold filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When signals other than the tracking error signal from the RF amplifier are input to the SE input pin, the signal transmitted from the TE pin can be obtained as TRK hold filter input.

THSK: Only during TRK servo gain up2 operation, coefficient K46 is used instead of K40. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M18 can be kept uniform by adjusting the K46 value even during the above switching.
* See "§4-20. Filter Composition" regarding the SFID, SFSK, THID and THSK commands.

ABEF: The focus error (FE) and tracking error (TE) can be generated internally.
When 0, the FE and TE signal input mode results. Input each error signal through the FE and TE pins. (default)
When 1, the FE and TE signal generation mode results and the FE and TE signals are generated internally.

TLD2 to 0: These turn on and off SLD filter correction independently of the TRK filter.
See $38 (TLC2 to TLC0) and Fig. 4-3.

	TLC2	TLD2	Traverse center correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

	TLC1	TLD1	Tracking zero level correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

	TLC0	TLD0	VC level correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

∗: preset, —: don't care

• Input coefficient sign inversion when SFID = 1 and THID = 1

The preset coefficients for the TRK filter are negative for input and positive for output. With this, the CXD3017Q outputs servo drives which have the reversed phase of input errors.
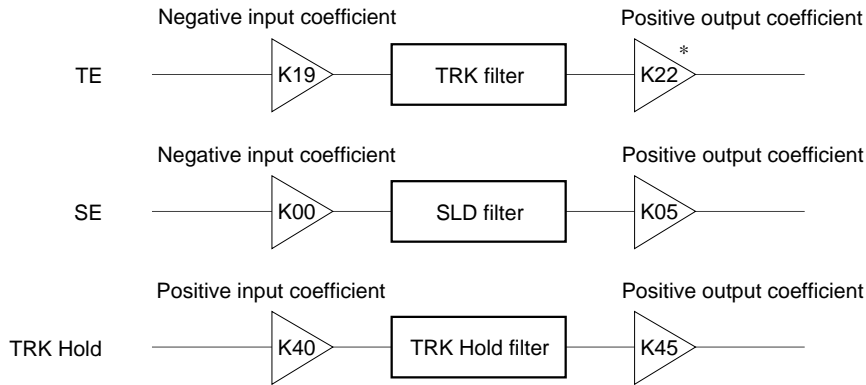
When SFID = 1, the TRK filter negative input coefficient is applied to the SLD filter, so the SLD input coefficient (K00) sign must be inverted. (For example, inverting the sign for coefficient K00: E0h results in 20h.)
For the same reason, when THID = 1, the TRK hold input coefficient (K40) sign must be inverted.
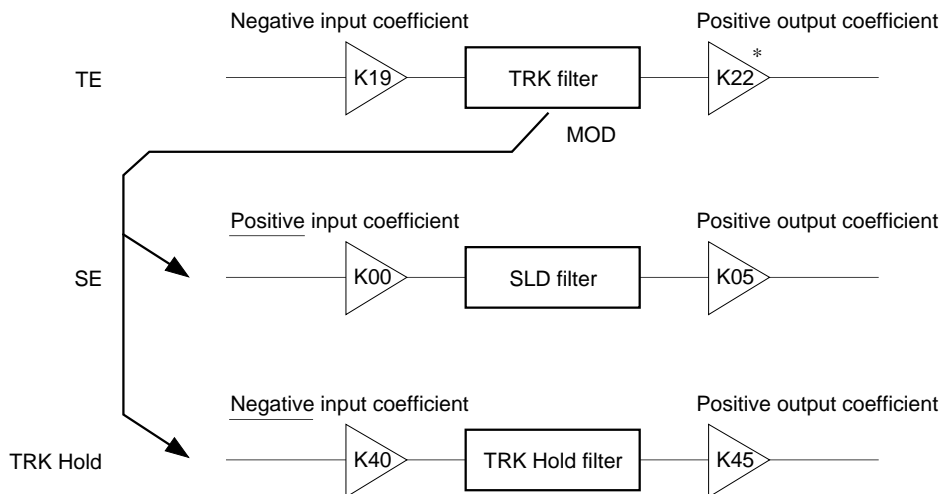
* For TRK servo gain normal
See §4-20. Filter Composition".

$3E (preset: $3E 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
On when 1; default is 0.
F1NM: Gain normal
F1DM: Gain down
T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
On when 1; default is 0.
T1NM: Gain normal
T1UM: Gain up
F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
On when 1; default is 0.
Generally, the advance amount of the phase increases by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
F3NM: Gain normal
F3DM: Gain down
T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
On when 1; default is 0.
Generally, the advance amount of the phase increases by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
T3NM: Gain normal
T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.
See "§4-20 Filter Composition" at the end of this specification concerning quasi double accuracy.

DFIS: FCS hold filter input extraction node selection
0: M05 (Data RAM address 05); default
1: M04 (Data RAM address 04)
TLCD: This command masks the TLC2 command set by D2 of $38 only when FOK is low.
On when 1; default is 0
LKIN: When 0, the internally generated LOCK signal is output to the LOCK pin. (default)
When 1, the LOCK signal can be input from an external source to the LOCK pin.
COIN: When 0, the internally generated COUT signal is output to the COUT pin. (default)
When 1, the COUT signal can be input from an external source to the COUT pin.

The MIRR, DFCT and FOK signals can also be input from an external source.
MDFI: When 0, the MIRR, DFCT and FOK signals are generated internally. (default)
When 1, the MIRR, DFCT and FOK signals can be input from an external source through the MIRR, DFCT and FOK pins.
MIRI: When 0, the MIRR signal is generated internally. (default)
When 1, the MIRR signal can be input from an external source through the MIRR pin.

	MDFI	MIRI	
*	0	0	MIRR, DFCT and FOK are all generated internally.
	0	1	MIRR only is input from an external source.
	1	—	MIRR, DFCT and FOK are all input from an external source.

∗: preset, —: don't care

XT1D: The input to the servo master clock is used without being frequency-divided by setting XT1D to 1. This command takes precedence over the XTSL pin, XT2D and XT4D. See the description of $3F for XT2D and XT4D.

$3F (preset: $3F 00 10)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	AGG4	XT4D	XT2D	AGSD	DRR2	DRR1	DRR0	0	ASFG	FTQ	1	SRO1	0	AGHF	ASOT

AGG4: This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC.
When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

AGG4	AGGF	AGGT	Sin wave amplitude	
			FE input conversion	TE input conversion
0	0	—	$1/32 \times V_{DD}/2$	—
	1	—	$1/16 \times V_{DD}/2^*$	—
	—	0	—	$1/16 \times V_{DD}/2$
	—	1	—	$1/8 \times V_{DD}/2^*$
1	0	0	$1/64 \times V_{DD}/2$	
	0	1	$1/32 \times V_{DD}/2$	
	1	0	$1/16 \times V_{DD}/2$	
	1	1	$1/8 \times V_{DD}/2$	

∗: preset, —: don't care

See $37 for AGGF and AGGT. The presets are AGG4 = 0, AGGF = 1 and AGGT = 1.

XT4D, XT2D: MCK (digital servo master clock) frequency division ratio setting
This command forcibly sets the frequency division ratio to 1/4, 1/2 or 1/1 when MCK is generated.
See the description of $3E for XT1D. Also, see "§4-2. Digital Servo Block Master Clock (MCK)".

XT1D	XT2D	XT4D	Frequency division ratio
0	0	0	According to XTSL
1	—	—	1/1
0	1	—	1/2
0	0	1	1/4

∗: preset, —: don't care

AGSD: This command is used to determine whether the result of the tracking auto gain adjustment is reflected on the sled. See §4-6 for the auto gain adjustment.
When AGSD = 0, the result of the tracking auto gain adjustment is reflected on the sled.
In other words, the coefficient K07 = K23. (preset)
When AGSD = 1, the result of the tracking auto gain adjustment is not reflected on the sled.
In other words, the coefficient K07 is not affected by K23.

DRR2 to DRR0: Partially clears the Data RAM values (0 write).

The following values are cleared when 1 (on) respectively; default is 0

DRR2: M08, M09, M0A

DRR1: M00, M01, M02

DRR0: M00, M01, M02 only when LOCK = low

Note) Set DRR1 and DRR0 on for 50μs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, the FCS servo filter is forcibly set to gain normal status.

On when 1; default is 0

FTQ: The slope of the output during focus search is 1/4 the conventional output slope. On when 1; default is 0

SRO1:   This command is used to continuously externally output various data inside the digital servo block which have been specified with the $39 command. (However, D15 (DAC) of $39 must be set to 1.)

Digital output (SOCK, XOLT and SOUT) can be obtained from three specified pins by setting this command to 1.

	SRO1 = 1
SOCK	Output from LMUT pin.
XOLT	Output from WFCK pin.
SOUT	Output from RMUT pin.

AGHF: This halves the frequency of the internally generated sine wave during AGC.

ASOT: The anti-shock signal, which is internally detected, is output from the ATSK pin. Output when 1; default is 0.

Vibration detection when a high signal is output for the anti-shock signal output.

$3F8 (preset: $3F8800)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SYG3	SYG2	SYG1	SYG0	FIFZB3	FIFZB2	FIFZB1	FIFZB0	FIFZA3	FIFZA2	FIFZA1	FIFZA0

SYG3 to SYG0: These simultaneously set the focus drive, tracking drive and sled drive output gains. See the $CX commands for the spindle drive output gain setting.

	SYG3	SYG2	SYG1	SYG0	GAIN
	0	0	0	0	0 (−∞dB)
	0	0	0	1	0.125 (−18.1dB)
	0	0	1	0	0.250 (−12.0dB)
	0	0	1	1	0.375 (−8.5dB)
	0	1	0	0	0.500 (−6.0dB)
	0	1	0	1	0.625 (−4.1dB)
	0	1	1	0	0.750 (−2.5dB)
	0	1	1	1	0.875 (−1.2dB)
*	1	0	0	0	1.000 (0.0dB)
	1	0	0	1	1.125 (+1.0dB)
	1	0	1	0	1.250 (+1.9dB)
	1	0	1	1	1.375 (+2.8dB)
	1	1	0	0	1.500 (+3.5dB)
	1	1	0	1	1.625 (+4.2dB)
	1	1	1	0	1.750 (+4.9dB)
	1	1	1	1	1.875 (+5.5dB)

∗: preset

FIFZB3 to FIFZB0:

This sets the slice level at which FZC changes from high to low.

FIFZA3 to FIFZA0:

This sets the slice level at which FZC changes from low to high.

The FIFZB3 to FIFZB0 and FIFZA3 to FIFZA0 setting values are valid only when $3A FIFZC is 1.

Set so that the FIFZB3 to FIFZB0 ≤ FIFZA3 to FIFZA0.

Hysteresis can be added to the slice level by setting FIFZB3 to FIFZB0 < FIFZA3 to FIFZA0.

$$\text{FZC slice level} = \frac{\text{FIFZB3 to FIFZB0 or FIFZA3 to FIFZA0 setting value}}{32} \times 0.5 \times V_{DD} \text{ [V]}$$

Description of Data Readout

Data is connected to the 7-segment LED
by 4-bits at a time. This enables Hex
display using four 7-segment LEDs.
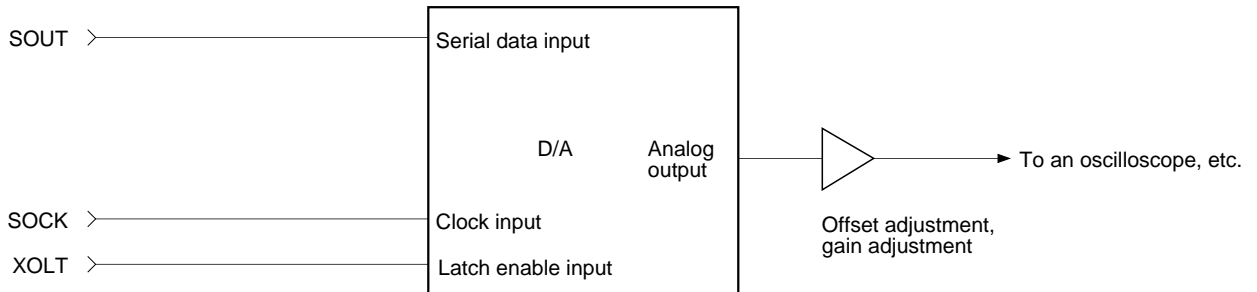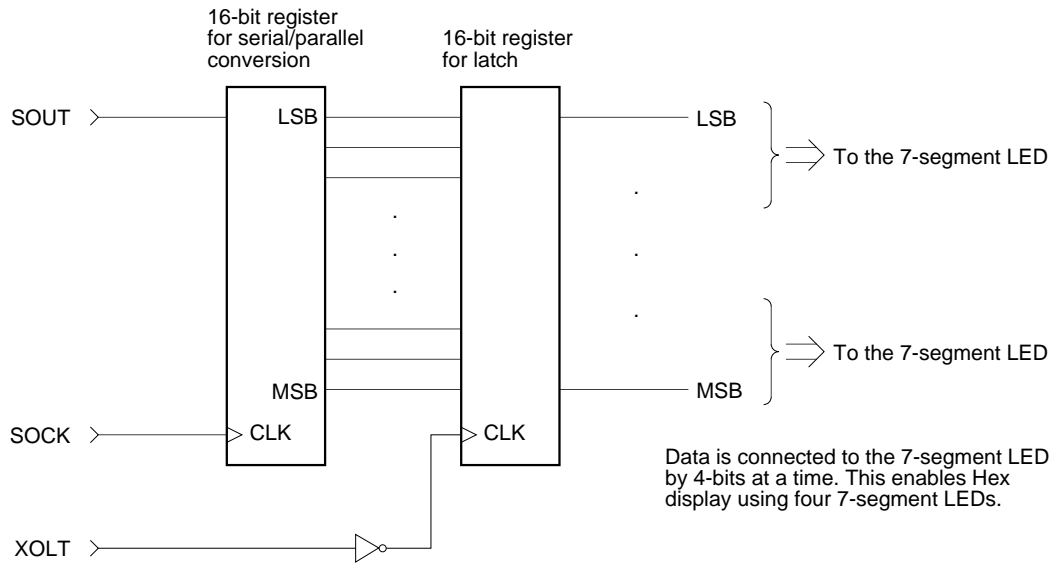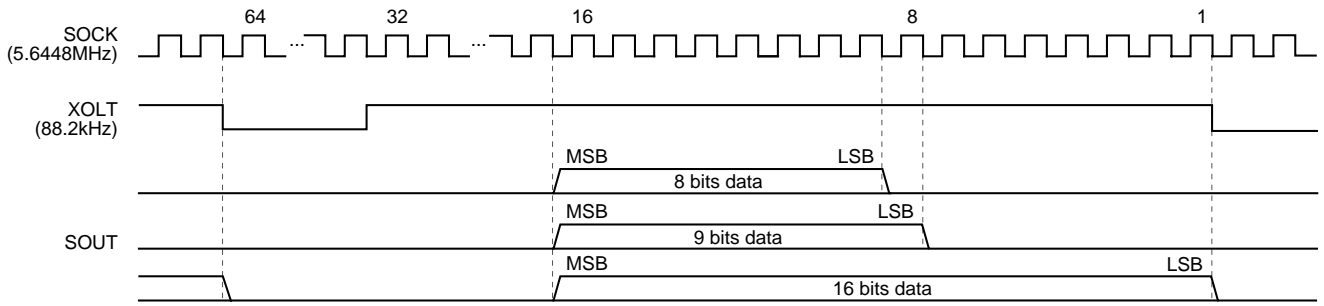
Waveforms can be monitored with an oscilloscope using a serial
input-type D/A converter as shown above.

§4-19. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	Not used
K2F	00	Not used

* Fix indicates that normal preset values should be used.

<Coefficient Preset Value Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK gain up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	Not used
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	Not used
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK gain up2 is accessed with THSK = 1.)
K47	00	Not used
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	Not used
K4F	00	Not used

§4-20. Filter Composition

The internal filter composition is shown below.
K∗∗**: Coefficient RAM address, M**∗∗**: Data RAM address**

FCS Servo Gain Normal fs = 88.2kHz

FCS Servo Gain Down fs = 88.2kHz

FCS Hold Reg2

FCS In Reg

Sin ROM

DFCT

2^{-1}

AGFON

K06

K06

M03

Z^{-1}

K08

M04

Z^{-1}

K09

K0A

K0B

2^{-7}

M1F To FCS Hold

K0F

M05

Z^{-1}

K0C

K0D

K0E

2^{-7}

M1E To FCS Hold

K0F

M06

Z^{-1}

K10

K11

M07

K13

FCS AUTO Gain

Note) Set the MSB bit of the K0B and K0D coefficients to 0.

FCS Hold Reg2

FCS In Reg

DFCT

2^{-1}

K06

M03

Z^{-1}

K24

M04

Z^{-1}

K25

K26

K27

2^{-7}

M1F To FCS Hold

K2B

M05

Z^{-1}

K28

K29

K2A

2^{-7}

M1E To FCS Hold

K2B

M06

Z^{-1}

K2C

K2D

M07

K13

FSC AUTO Gain

Note) Set the MSB bit of the K27 and K29 coefficients to 0.

2^7

PWM

FPS1, 0

Z^{-1}

BK1

BK2

Z^{-1}

BK3

BK6

Z^{-1}

BK4

BK5

Z^{-1}

FCS SRCH

TRK Servo Gain Normal fs = 88.2kHz

TRK Servo Gain Up1 fs = 88.2kHz

TRK Servo Gain Up2 fs = 88.2kHz

Note) Set the MSB bit of the K1D and K1F coefficients to 0.

Note) Set the MSB bit of the K39 and K3B coefficients to 0.

FCS Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EAXX0)
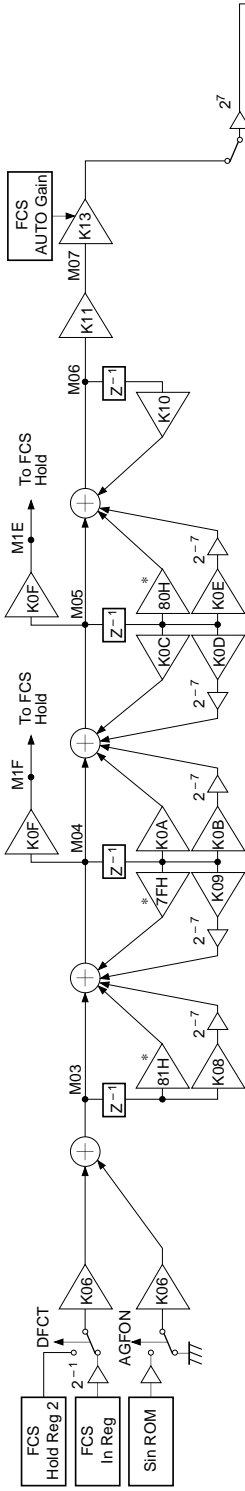
Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K08, K09 and K0E coefficients during quasi double accuracy to 0.

FCS Servo Gain Down; fs = 88.2kHz, during quasi double accuracy (Ex.: $3E5XX0)
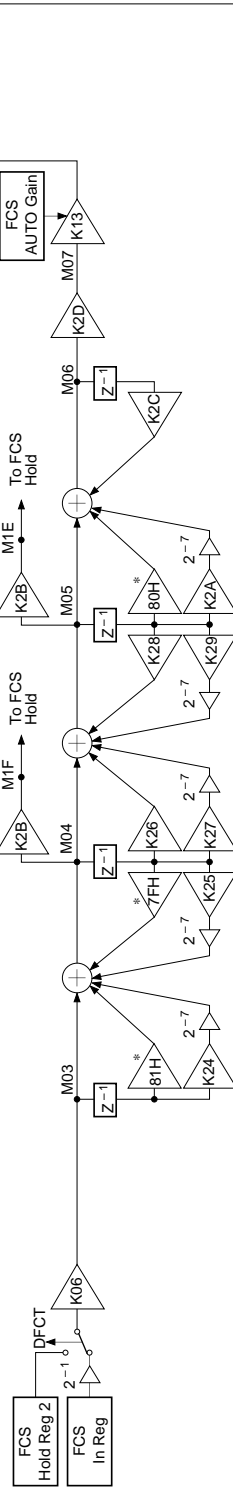
Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to 0.

* 81h, 7Fh and 80h are each Hex display 8-bit fixed values
  when set to quasi double accuracy.

TRK Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EXAX0)
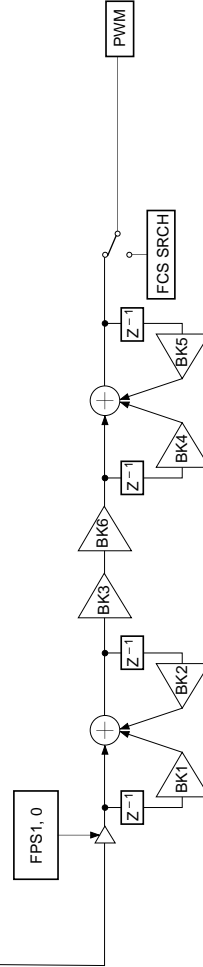
Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.
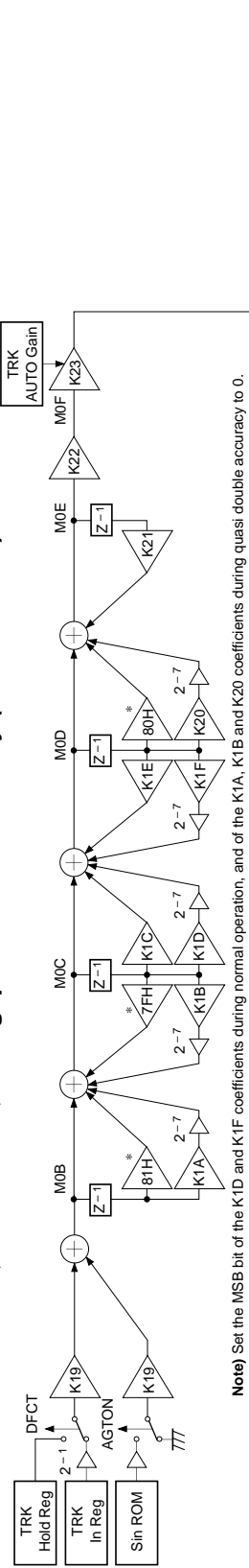
TRK Servo gain up1; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EX5X0)

Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.
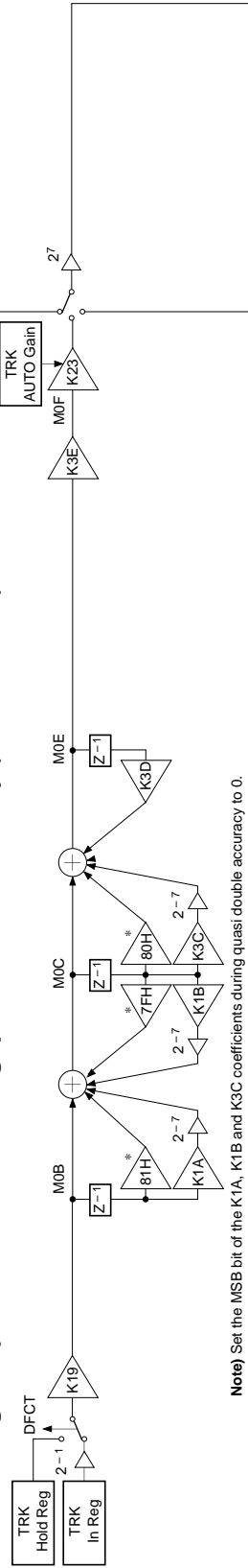
TRK Servo gain up2; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EX5X0)

Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K36, K37 and K3C coefficients during quasi double accuracy to 0.
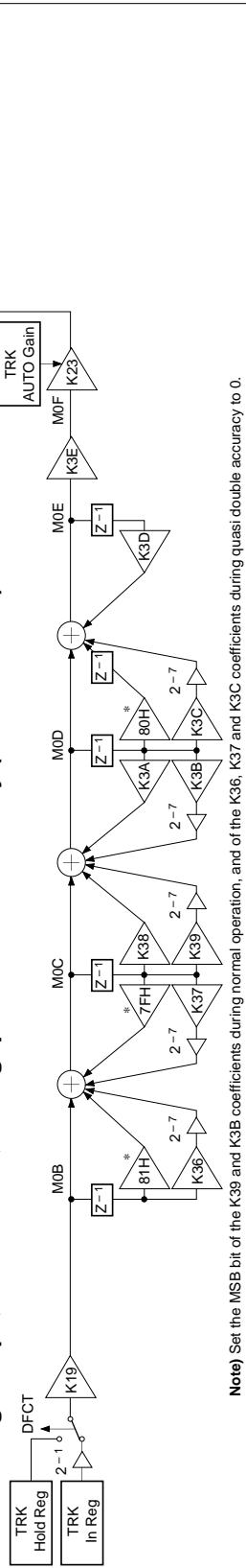
* 81h, 7Fh and 80h are each Hex display 8-bit fixed values when set to quasi double accuracy.
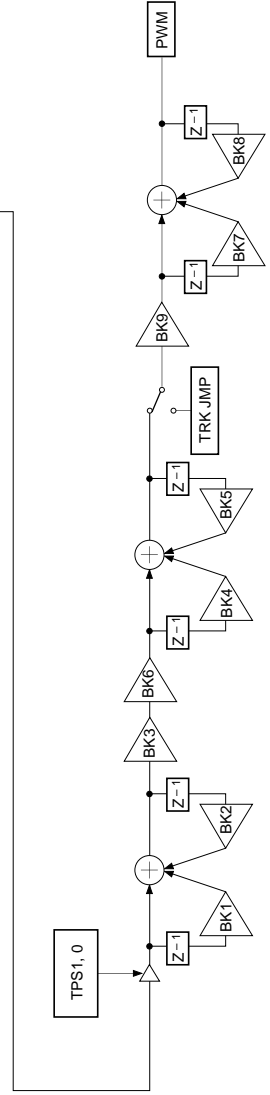
SLD Servo fs = 345Hz

TRK SERVO FILTER
Second-stage output
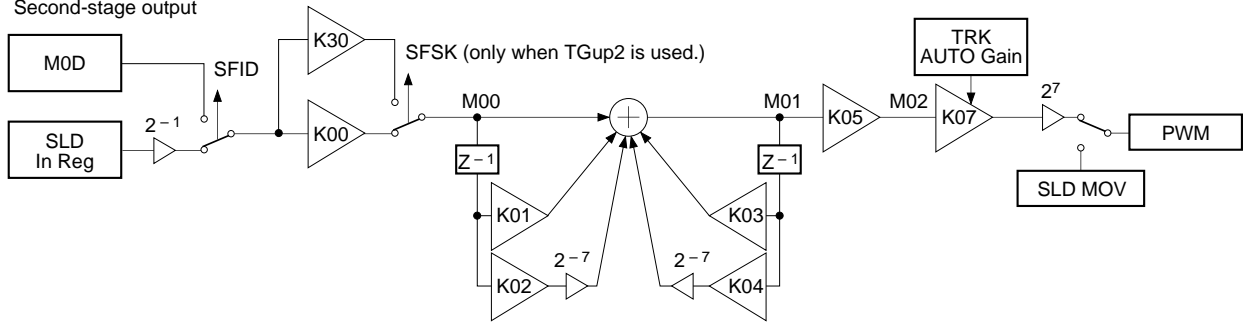
Note) Set the MSB bit of the K02 and K04 coefficients to 0.

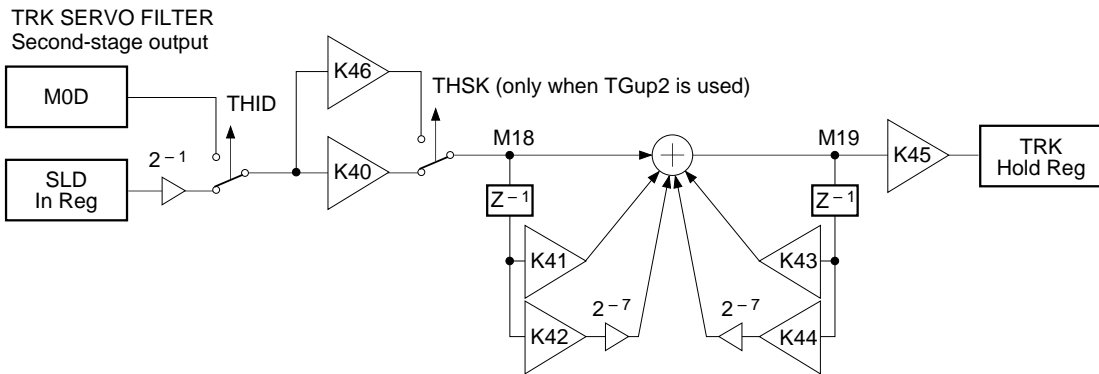## HPTZC/Auto Gain fs = 88.2kHz
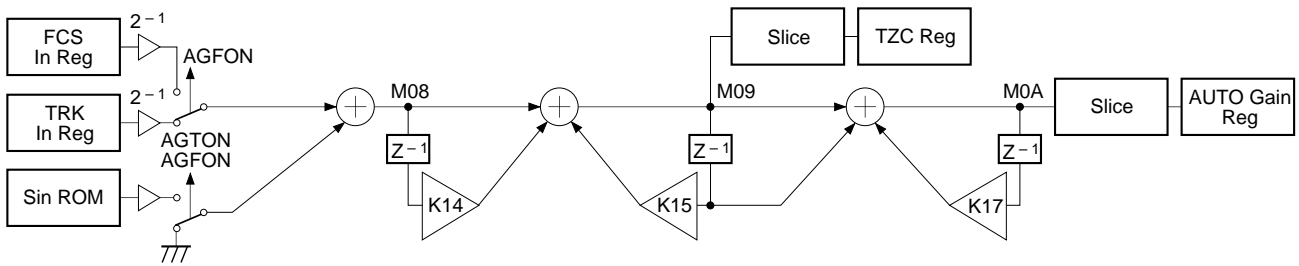
Anti Shock fs = 88.2kHz
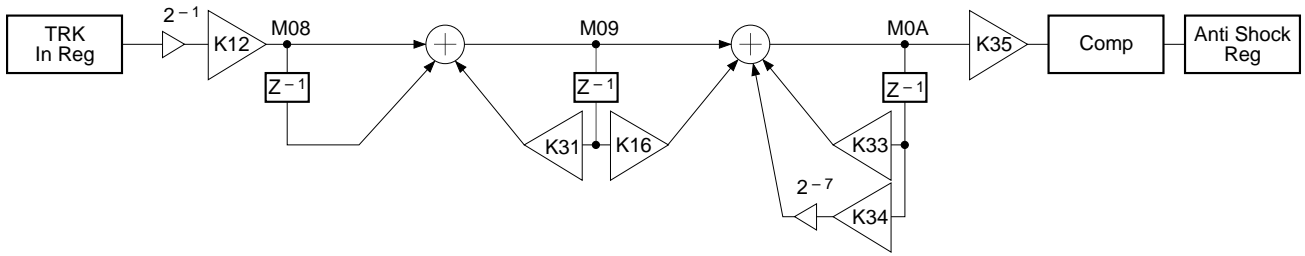
Note) Set the MSB bit of the K34 coefficient to 0.

The comparator level is 1/16 the maximum amplitude of the comparator input.
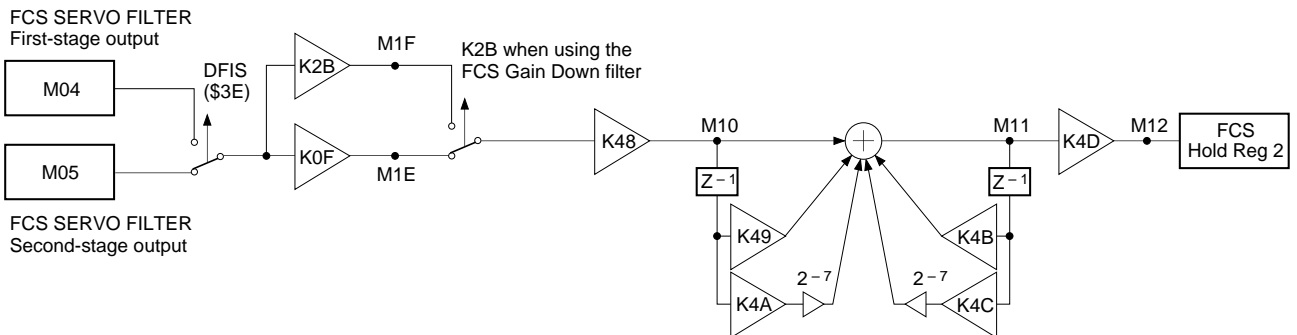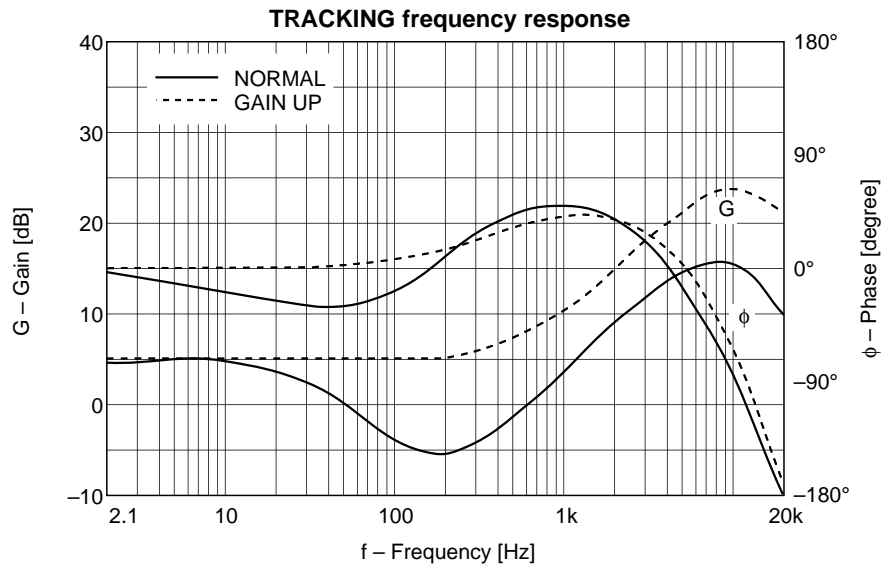
AVRG fs = 88.2kHz
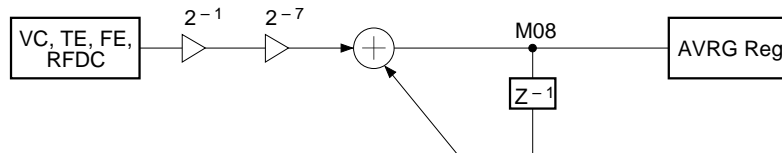
TRK Hold fs = 345Hz

Note) Set the MSB bit of the K42 and K44 coefficients to 0.
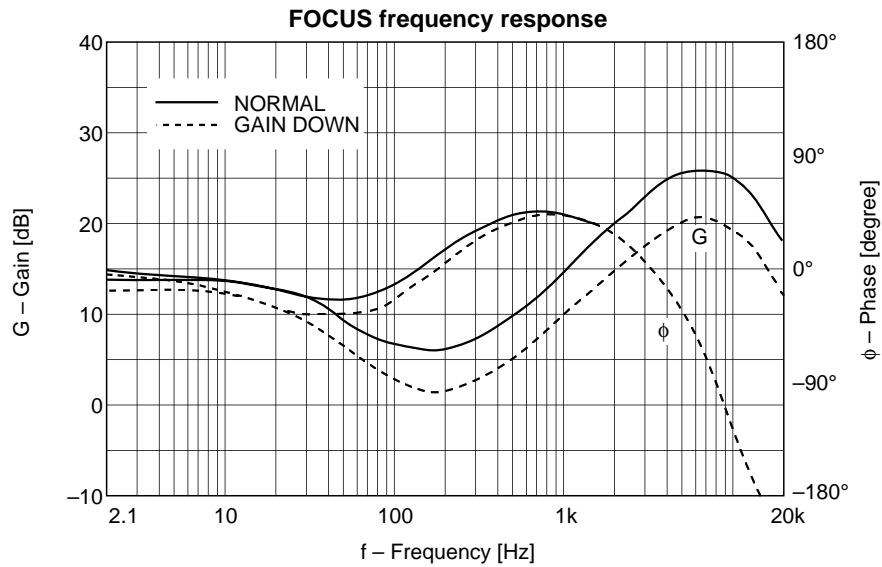
FCS Hold fs = 345Hz

Note) Set the MSB bit of the K4A and K4C coefficients to 0.
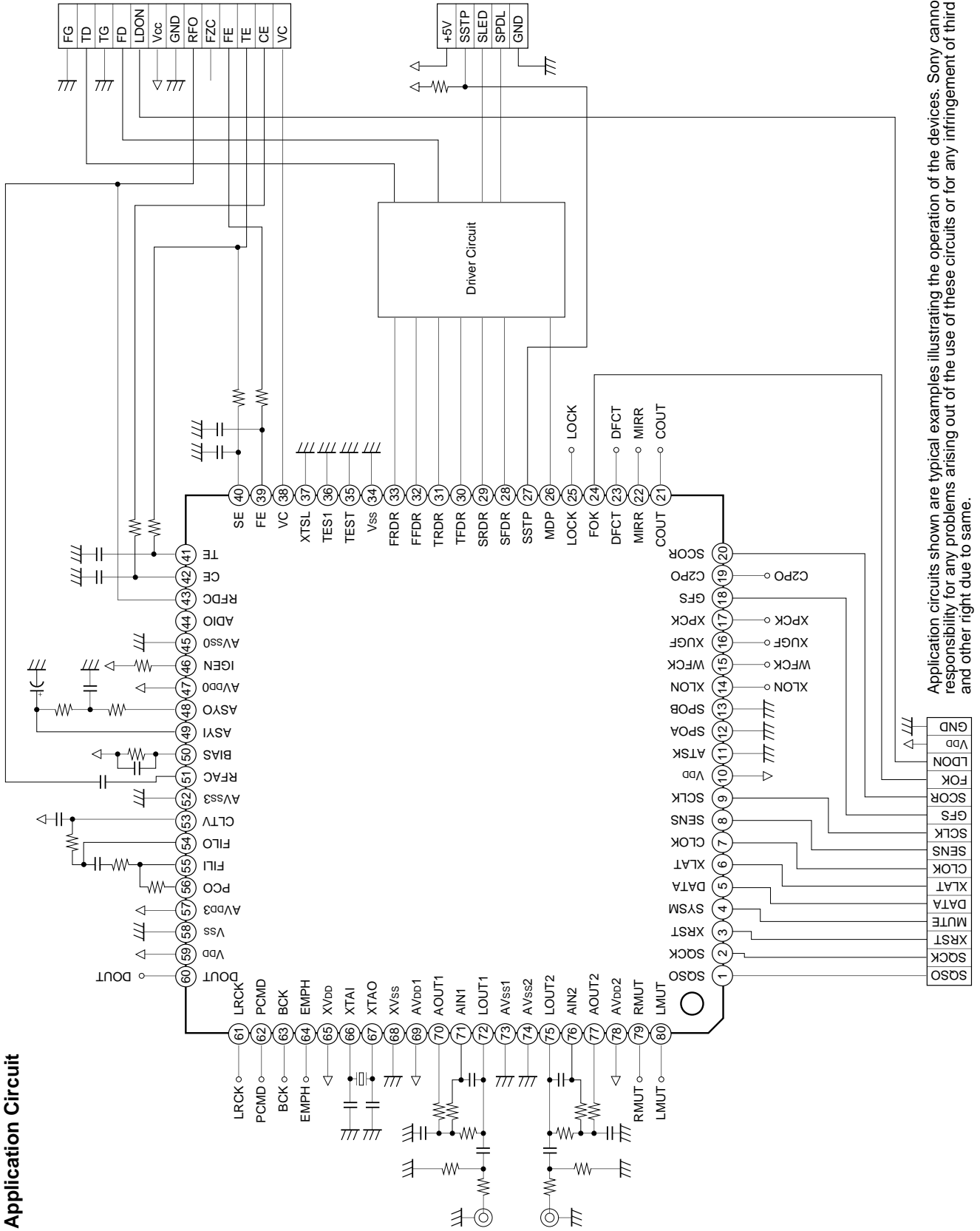
§4-21. TRACKING and FOCUS Frequency Response

TRACKING frequency response

When using the preset coefficients with the boost function off.

FOCUS frequency response

When using the preset coefficients with the boost function off.

§5. Application Circuit

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline   Unit: mm

80PIN QFP (PLASTIC)

□ 16.0 ± 0.4

+ 0.4
□ 14.0 − 0.1

60   41

61   40

80   21

1   20

0.65

+ 0.15
0.3 − 0.1

⊕ | 0.24 Ⓜ

+ 0.35
1.5 − 0.15

+ 0.1
0.127 − 0.05

0.1

(15.0)

+ 0.15
0.1 − 0.1

0.5 ± 0.2

0° to 10°
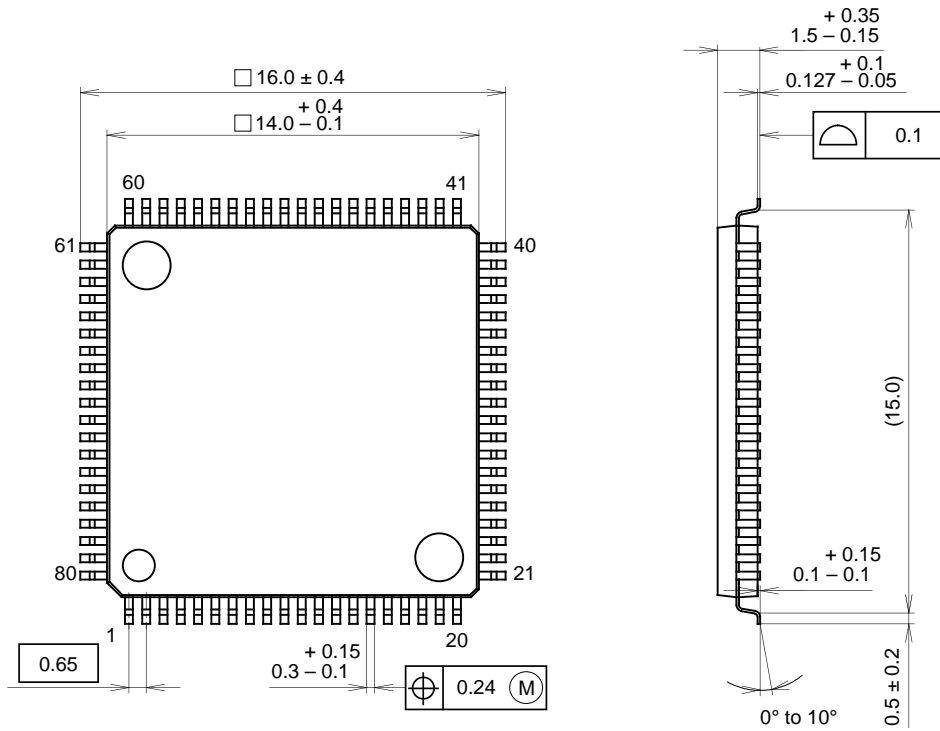
SONY CODE	QFP-80P-L03
EIAJ CODE	QFP080-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g