HARRIS SEMICONDUCTOR

ACS03MS

Radiation Hardened Quad 2-Input NAND Gate with Open Drain

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RAD(Si)/s, 20ns Pulse
- Cosmic Ray Upset Immunity <1 x 10^{-11} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels II ≤ 1μA at VOL, VOH

Description

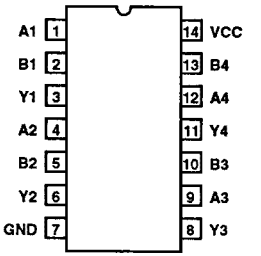
The Harris ACS03MS is a Radiation Hardened quad 2-input NAND gate with open drain outputs. The open drain output can drive resistance loads from a separate supply voltage.

The ACS03MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

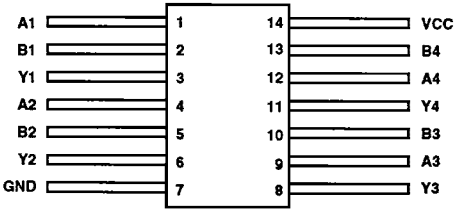
The ACS03MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP3-F14, LEAD FINISH C
TOP VIEW

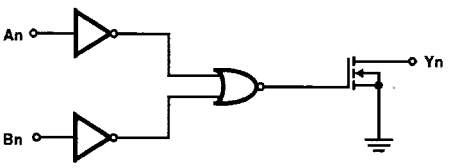


Truth Table

INPUTS		OUTPUT
An	Bn	Yn
L	L	Z*, H**
L	H	Z*, H**
H	L	Z*, H**
H	H	L

L = Low
H = High
Z = High Impedance
* Without Pull-up Resistor
** With Pull-up Resistor

Functional Diagram



7 LOGIC

File Number 3064

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +6.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flatpack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . VCC to 70% of VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	5	µA
			2, 3	+125°C, -55°C	-	100	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-1	±1	µA
			2, 3	+125°C, -55°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	V

NOTES:
1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	15	ns
Propagation Delay	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	10	ns
			10, 11	+125°C, -55°C	2	11	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Transition Time	TTHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	9	ns
			10, 11	+125°C, -55°C	1	10	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	Typical 10		pF
				+125°C	Typical 10		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	1M LIMITS MIN	1M LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.10	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V	+25°C	4.0	0.5	V
Propagation Delay	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	15	ns
Propagation Delay	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	11	ns
Transition Time	TTHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	10	ns

NOTE:

1. All voltages referenced to device GND.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±1μA
IOL/IOH	5	±15%
IOZ	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	VCC = 6V ± 0.5V	$^1/_2$VCC = 3V ± 0.5V	OSCILLATOR	
				50KHz	25KHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	14	-	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14	3, 6, 8, 11	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	14	3, 6, 8, 11	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

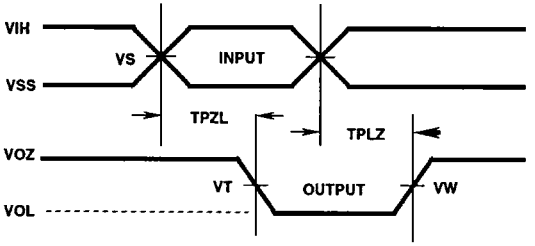
1. Each pin except VCC and GND will have a series resistor of 10K ± 5%
2. Each pin except VCC and GND will have a series resistor of 1K ± 5%

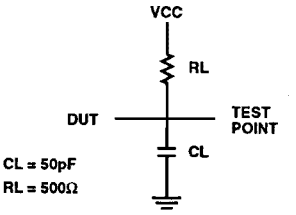
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

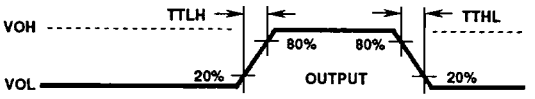
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Tri-State Low Timing Diagram and Load Circuit





TRANSITION TIMING DIAGRAM



TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
68 x 79 mils
1730mm x 2010mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 6.75kÅ Min., 8.25kÅ Max.
Metal 2 Thickness: 9kÅ Min., 11kÅ Max.

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.3 x 4.3 mils

Metallization Mask Layout

ACS03MS