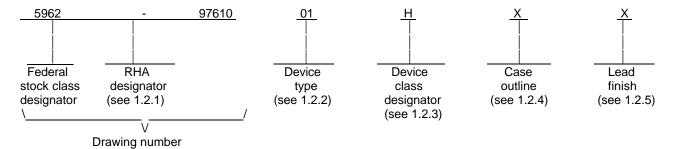
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1. SCOPE

- 1.1 <u>Scope</u>. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowered high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.
 - 1.2 PIN. The PIN shall be as shown in the following example:



- 1.2.1 <u>Radiation hardness assurance (RHA) designator</u>. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
 - 1.2.2 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Generic number	Circuit function	Access time
WMF2M16-150	FLASH EPROM, 2M x 16-bit	150 ns
WMF2M16-120	FLASH EPROM, 2M x 16-bit	120 ns
WMF2M16-90	FLASH EPROM, 2M x 16-bit	90 ns
	WMF2M16-150 WMF2M16-120	WMF2M16-150 FLASH EPROM, 2M x 16-bit WMF2M16-120 FLASH EPROM, 2M x 16-bit

1.2.3 <u>Device class designator</u>. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class

Device performance documentation

D, E, G, H, or K

Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
X	See figure 1	56	Ceramic flatpack, lead formed

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

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.3 Absolute maximum ratings. 1/	
Supply voltage range (V _{CC}) 2/	-2.0 V dc to +7.0 V dc -2.0 V dc to +7.0 V dc 0.33 W maximum at 5 MHz -65°C to +150°C +300°C 10 years minimum 10,000 cycles minimum -2.0 V dc to +12.5 V dc <u>3</u> /
.4 Recommended operating conditions.	
Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc -0.5 V dc to +0.8 V dc +2.0 V dc to V _{CC} + 0.5 V dc -55°C to +125°C

+11.5 V dc to +12.5 V dc

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

- 1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- $\underline{2}'$ Minimum DC voltage in input or I/O pins is -0.5 V dc. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V dc for periods up to 20 ns. Maximum DC voltage on output and I/O pins V_{CC} +0.5 V dc. During voltage transitions, outputs may overshoot to V_{CC} +2.0 V dc for periods up to 20 ns.
- 3/ Minimum DC input voltage on RESET, OE, and A9 is -0.5 V dc. During voltage transitions, RESET, OE, and A9 may overshoot V_{SS} to -2.0 V dc for periods up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to +14.0 V dc for periods up to 20 ns.

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HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturer may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.
 - 3.2.1 <u>Case outline(s)</u>. The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.
 - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.
 - 3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.
 - 3.2.4 Timing diagrams. The timing diagram(s) shall be specified on figures 4, 5, and 6.
 - 3.2.5 Block diagram. The block diagram shall be as specified on figure 7.
 - 3.2.6 Output load circuit. The output load circuit shall be as specified on figure 8.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 <u>Programming procedure</u>. The programming procedure shall be as specified by the manufacturer and shall be available upon request.
- 3.6 <u>Marking of Device(s)</u>. Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.
- 3.7 <u>Data</u>. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

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- 3.8 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.
- 3.9 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.
- 3.10 <u>Endurance</u>. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the intial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendors procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.
- 3.11 <u>Data retention</u>. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for the initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall gurantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

STANDARD
MICROCIRCUIT DRAWING

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		TABLE I. <u>Electrical performance</u>	characteristic	<u>'S</u> .			
Test	Symbol	Conditions $\underline{1}/\underline{2}/$ $-55^{\circ}C \leq T_{C} \leq +125^{\circ}C$ unless otherwise specified	Group A subgroups	Device type		Limits	Unit
					Min	Max	
DC parameters							
Input leakage current	ILI	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	μА
Output leakage current	I _{LO}	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	μА
V _{CC} active current for read	I _{cc} 1	$\overline{\text{CS}} = \text{V}_{\text{IL}}, \overline{\text{OE}} = \text{V}_{\text{IH}},$ $\text{f} = 5 \text{MHz}, \text{V}_{\text{CC}} = 5.5 \text{V dc}$	1,2,3	All		80	mA
V _{CC} active current for Program or erase <u>3</u> /	I _{CC} 2	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH},$ $V_{CC} = 5.5 \text{ V dc}$	1,2,3	All		120	mA
V _{CC} standby current	I _{CC} 3	V_{CC} = 5.5 V dc, \overline{CS} = V _{IH} , \underline{f} = 5 MHz, RESET = V_{CC} \pm 0.3 V	1,2,3	All		0.50	mA
Input low level 3/	V _{IL}		1,2,3	All	-0.5	0.8	V
Input high level 3/	V _{IH}		1,2,3	All	2.0	V _{CC} + 0.5 V	V
Output low voltage	V _{OL}	$V_{CC} = 4.5 \text{ V dc}, I_{OL} = 12.0 \text{ mA}$	1,2,3	All		0.45	V
Output high voltage	V _{OH}	$V_{CC} = 4.5 \text{ V dc}, I_{OH} = -2.5 \text{ mA}$	1,2,3	All	0.85 x V _{CC}		V
Low V _{CC} , lockout voltage	V _{LKO}		1,2,3	All	3.2	4.2	V
Dynamic characteristics							
Address capacitance 3/	C _{AD}	$V_{IN} = 0 \text{ V dc, f} = 1.0 \text{ MHz,}$ $T_A = +25^{\circ}\text{C}$	4	All		25	pF
Output enable 3/ Capacitance	C _{OE}	$V_{IN} = 0 \text{ V dc, f} = 1.0 \text{ MHz,}$ $T_A = +25^{\circ}\text{C}$	4	All		25	pF

See footnotes at end of table.

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	TABLE I	. Electrical performance chara	<u>acteristics</u> - Co	ntinued.			
Test	Symbol	Conditions $\underline{1}/\underline{2}/$ $-55^{\circ}C \le T_{C} \le +125^{\circ}C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic characterisitics - conf	tinued		T	T		_	T
Write enable <u>3</u> / Capacitance	C _{WE}	$V_{IN} = 0 \text{ V dc}, f = 1.0 \text{ MHz},$ $T_A = +25^{\circ}\text{C}$	4	All		25	pF
Chip select capacitance 3/	C _{CS}	$V_{IN} = 0 \text{ V dc, f} = 1.0 \text{ MHz,}$ $T_A = +25^{\circ}\text{C}$	4	All		15	pF
Data I/O capacitance 3/	C _{I/O}	$V_{IN} = 0 \text{ V dc, f} = 1.0 \text{ MHz,}$ $T_A = +25^{\circ}\text{C}$	4	All		15	pF
Functional testing	T						
Functional tests		See 4.3.1c	7,8A,8B	All			
Read cycle AC timing characte	eristics		T	1			T
Read cycle time 3/	t _{RC}	See figure 4	9,10,11	01 02 03	150 120 90		ns
Address access time	t _{ACC}	See figure 4	9,10,11	01 02 03		150 120 90	ns
Chip select access time	t _{CE}	See figure 4	9,10,11	01 02 03		150 120 90	ns
Output enable to output valid	t _{OE}	See figure 4	9,10,11	01 02 03		55 50 40	ns
O <u>utp</u> ut <u>hol</u> d from address, CS or OE change, <u>3</u> / Whichever is first	t _{ОН}	See figure 4	9,10,11	All	0		ns

See footnotes at end of table.

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	TABLE I	. Electrical performance chara	acteristics - Co	ntinued.			
Test	Symbol	Conditions $\underline{1}/\underline{2}/$ -55°C \leq T _C \leq +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write/Erase/ Program AC timi	ng characte	ristics WE controlled	T	1			1
Write cycle time 3/	t _{WC}	See figure 5	9,10,11	01 02 03	150 120 90		ns
Chip select setup time	t _{CS}	See figure 5	9,10,11	All	0		ns
Write enable pulse width	t _{WP}	See figure 5	9,10,11	01,02	50		ns
				03	45		
Address setup time	t _{AS}	See figure 5	9,10,11	All	0		ns
Data setup time	t _{DS}	See figure 5	9,10,11	01,02	50		ns
				03	45		
Data hold time	t _{DH}	See figure 5	9,10,11	All	0		ns
Address hold time	t _{AH}	See figure 5	9,10,11	01,02	50		ns
				03	45		
Write enable pulse width 3/	t _{WPH}	See figure 5	9,10,11	All	20		ns
Write/Erase/Program AC timin	g character	istics CS controlled					
Write cycle time 3/	t _{WC}	See figure 6	9,10,11	01 02 03	150 120 90		ns
Write enable setup time	tws	See figure 6	9,10,11	All	0		ns

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-97610
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TABLE I. <u>Electrical performance characteristics</u> - Continued.							
Test	Symbol	Conditions $\underline{1}/\underline{2}/$ -55°C \leq T _C \leq +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write/Erase/ Program AC timir	ng characte	ristics CS controlled - continue	ed	ı		Ī-	
Chip select pulse width	t _{CP}	See figure 6	9,10,11	01,02	50		ns
				03	45		
Address setup time	t _{AS}	See figure 6	9,10,11	All	0		ns
Data hold time	t _{DH}	See figure 6	9,10,11	All	0		ns
Data setup time	t _{DS}	See figure 6	9,10,11	01,02	50		ns
				03	45		
Address hold time	t _{AH}	See figure 6	9,10,11	01,02	50		ns
				03	45		
Chip select pulse width 3/ High	t _{CPH}	See figure 6	9,10,11	All	20		ns

- Unless otherwise specified, 4.5 V dc \leq VcC \leq 5.5 V dc and Vss = 0 V.
- Unless otherwise specified, the DC test conditions are as follows:

Input pulse levels: $V_{IH} = V_{CC} - 0.3 \text{ V}$ and $V_{IL} = 0.3 \text{ V}$.

Unless otherwise specified, the AC test conditions are as follows: Input pulse levels: $V_{IL} = 0$ V and $V_{IH} = 3.0$ V. Input rise and fall times: 5 nanoseconds. Input and output timing reference levels: 1.5 V.

Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.

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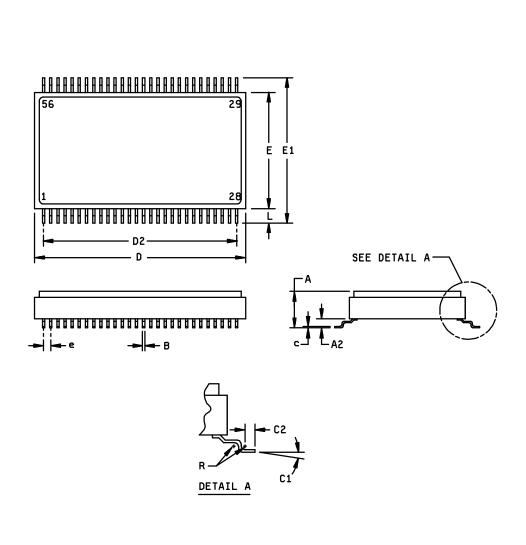


FIGURE 1. Case outline.

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Symbol	Millimeters		Inc	hes
	Min	Max	Min	Max
А		4.06		.160
A2	0.38	0.64	.033	.047
В	0.20	0.30	.008	.012
С	0.13	0.23	.006	.010
C1	0°	-4°	0°	-4°
C2	0.51 TYP		.020 TYP	
D	23.37	23.88	.920	.940
D2	21.59 TYP			.540 TYP
E	12.80	13.11	.504	
				.516
E1	16.00 16.26		.630 .640	
e	0.80 TYP		.315 TYP	
L	1.58 TYP		.063 TYP	
R	0.18	TYP	.007	' TYP

NOTES:

 The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - continued.

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Device Types	All	Device types	All	Device Types	All	Device types	All
Case Outline	Х	Case outline	Х	Case Outline	Х	Case outline	Х
Terminal number	Terminal Symbol	Terminal number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal number	Terminal Symbol
1	CS	17	I/O14	33	I/O2	49	А3
2	A12	18	1/07	34	NC	50	A2
3	A13	19	I/O15	35	NC	51	A1
4	A14	20	RY/BY	36	NC	52	A9
5	A15	21	ŌĒ	37	A0	53	A10
6	NC	22	WE	38	I/O0	54	A11
7	CS2	23	NC	39	I/O8	55	RESET
8	NC	24	I/O13	40	I/O1	56	NC
9	A20	25	I/O5	41	I/O9		
10	A19	26	I/O12	42	VCC		
11	A18	27	I/O4	43	A8		
12	A17	28	Vcc	44	GND		
13	A16	29	GND	45	A7		
14	Vcc	30	I/O11	46	A6		
15	GND	31	I/O3	47	A5		
16	I/O6	32	I/O10	48	A4		

NOTE: NC is a no connection

FIGURE 2. <u>Terminal connections</u>.

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CS	OE	WE	I/O	MODE
V _{IL}	\vee_{IL}	V _{IH}	D _{OUT}	Read
V _{IL}	\vee_{IH}	\vee_{IL}	D _{IN}	Write
V _{IH}	Х	Х	High Z	Standby
V _{IL}	V _{IH}	V _{IH}	High Z	Output disable

NOTES:

- 1. V_{IH} = High logic level
- 2. V_{IL} = Low logic level
- 3. X = Do not care (either high or low)4. High Z = High impedance state

FIGURE 3. Truth table.

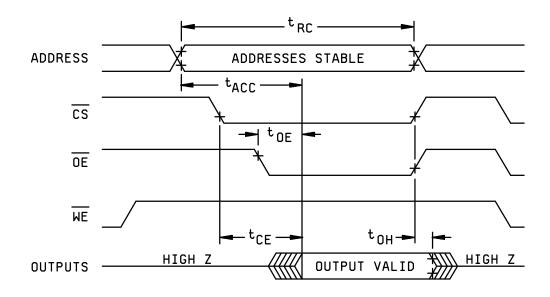


FIGURE 4. Read cycle timing diagram.

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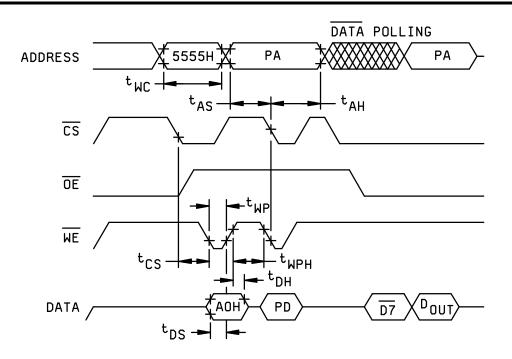


FIGURE 5. Write cycle timing diagram, WE controlled.

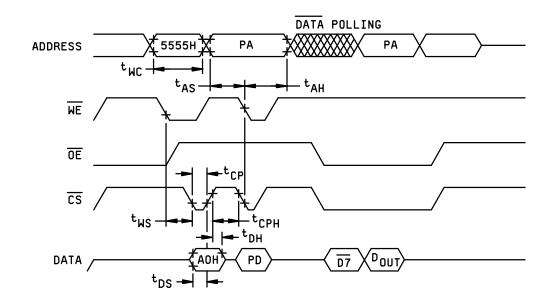


FIGURE 6. Write cycle timing diagram, CS controlled.

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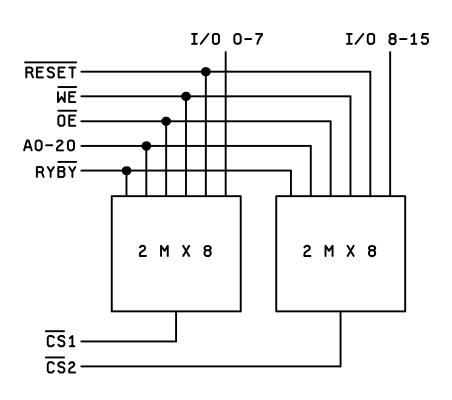
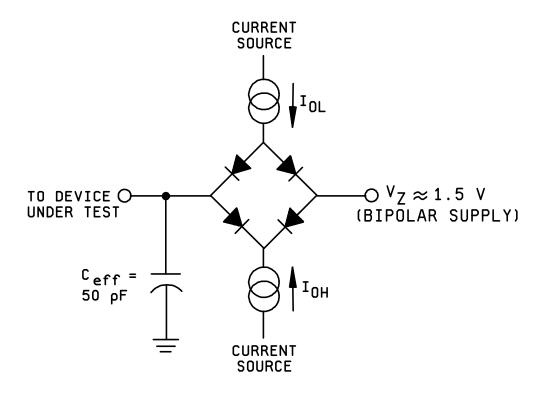


FIGURE 7. Block diagram.

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Parameter	Тур.	Unit
Input pulse level	V _{IL} = 0 V, V _{IH} = 3.0 V	V
Input rise and fall	5	ns
Input and output reference level	1.5	٧
Timing reference level	1.5	V

NOTES:

- 1. V_Z is programmable from +2 V to +7 V.
- 2. $I_{\mbox{OL}}$ and $I_{\mbox{OH}}$ are programmable from 0 to 16 mA.
- 3. Tester impedance is $Z_0 = 75$ ohms.
- 4. V_Z is typically the midpoint of V_{OL} and V_{OH} .
- 5. $I_{\mbox{OL}}$ and $I_{\mbox{OH}}$ are adjusted to simulate a typical resistive load circuit.
- 6. ATE tester includes jig capacitance.

FIGURE 8. Output load circuit.

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*, 2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

^{*} PDA applies to subgroup 1.

4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
 - 4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 <u>Conformance and periodic inspections</u>. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.
 - 4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 5 and 6 shall be omitted.
 - c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

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- 4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.
- 4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.
- 4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.
- 5. PACKAGING
- 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.
- 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.
- 6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.
- 6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.8 herein) to DSCC-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-07-18

Approved sources of supply for SMD 5962-97610 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard	Vendor	Vendor
microcircuit drawing	CAGE	Similar
PIN <u>1</u> /	number	PIN <u>2</u> /
5962-9761001HXA	54230	WMF2M16-150DAQ5
5962-9761001HXC	54230	WMF2M16-150DAQ5
5962-9761002HXA	54230	WMF2M16-120DAQ5
5962-9761002HXC	54230	WMF2M16-120DAQ5
5962-9761003HXA	54230	WMF2M16-90DAQ5
5962-9761003HXC	54230	WMF2M16-90DAQ5

- The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
Number

Vendor name
and address

54230

White Electronic Designs Corporation
3601 East University Drive.
Phoenix, AZ 85034

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.