Silicon PNP Power Transistors 3CD6D

DESCRIPTION

- With TO-3 package
- Low collector saturation voltage

APPLICATIONS

- For power amplifier and low speed switching applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=℃)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-110	V
V_{CEO}	Collector-emitter voltage	Open base	-110	V
V_{EBO}	Emitter-base voltage	Open collector	-4	V
I_C	Collector current		-5	A
P_C	Collector power dissipation	T_C=75℃	50	W
T_j	Junction temperature		150	℃
T_{stg}	Storage temperature		-55~150	℃

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CHARACTERISTICS

Tj=25℃ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=-10mA ;I_B=0	-110			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=-1mA ;I_B=0	-4			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-2.5A; I_B=-0.5A		-1.0	-1.5	V
V_{BEsat}	Base-emitter saturation voltage	I_C=-2.5A; I_B=-0.5A			-2.0	V
I_{CBO}	Collector cut-off current	V_{CB}=-110V; I_E=0			-0.1	mA
I_{CEO}	Collector cut-off current	V_{CE}=-110V; I_E=0			-1.0	mA
I_{EBO}	Emitter cut-off current	V_{EB}=-4V; I_C=0			-0.1	mA
h_{FE}	DC current gain	I_C=-2.5A ; V_{CE}=-10V	10		180	

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PACKAGE OUTLINE

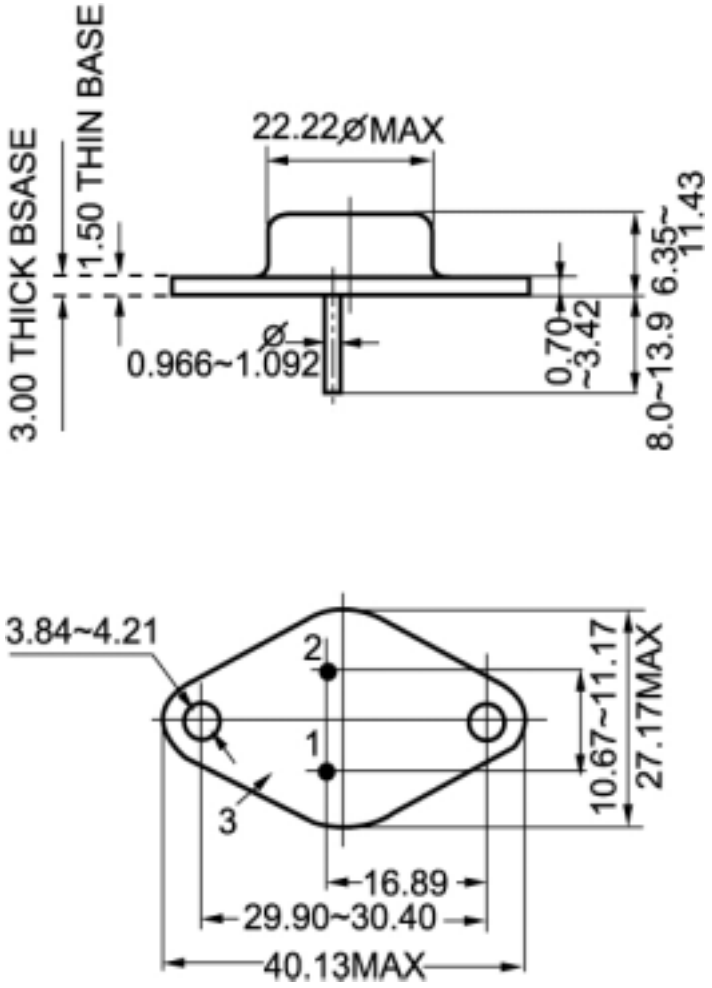

Fig.2 outline dimensions (unindicated tolerance:±0.1mm)