

256 Bit

X25401

16 x 16 Bit

SPI Serial AUTOSTORE™ NOVRAM

FEATURES

- 1MHz Clock Rate
- AUTOSTORE™ NOVRAM
 - Automatically Performs a Store Operation Upon Loss of V_{CC}
- Single 5 Volt Supply
- Ideal for use with Single Chip Microcomputers
 - Minimum I/O Interface
 - SPI Mode (0,0 & 1,1) Serial Port Compatible
 - Easily Interfaced to Microcontroller Ports
- Software and Hardware Control of Nonvolatile Functions
- Auto Recall on Power-Up
- TTL and CMOS Compatible
- Low Power Dissipation
 - Active Current: 10mA
 - Standby Current: 50 μ A
- 8-Lead PDIP and 8-Lead SOIC Packages
- High Reliability
 - Store Cycles: 1,000,000
 - Data Retention: 100 Years

DESCRIPTION

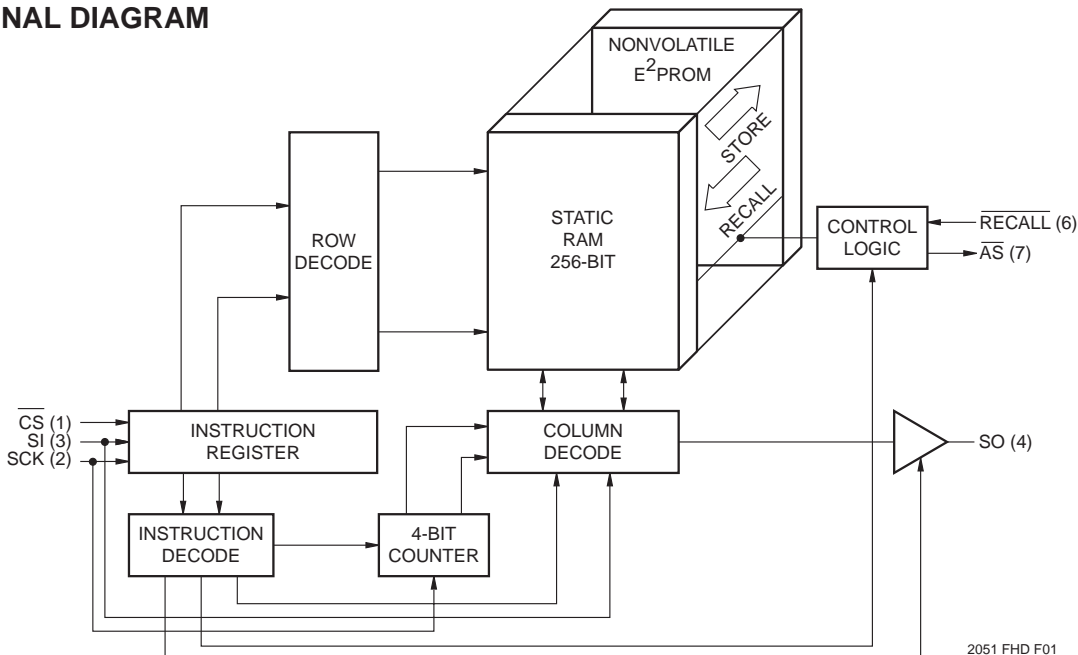
The Xicor X25401 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit-by-bit with a nonvolatile E²PROM array. The X25401 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select (\overline{CS}) input, allowing any number of devices to share the same bus.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E²PROM) is completed in 5ms or less and a recall operation (E²PROM data to RAM) is completed in 2 μ s or less.

The X25401 also includes the AUTOSTORE feature, a user selectable feature that automatically performs a store operation when V_{CC} falls below a preset threshold.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years.

FUNCTIONAL DIAGRAM



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 COPS is a trademark of National Semiconductor Corp.

X25401

PIN DESCRIPTIONS

Chip Select (\overline{CS})

The Chip Select input must be LOW to enable all read/write operations. \overline{CS} must remain LOW following a Read or Write command until the data transfer is complete. \overline{CS} HIGH places the X25401 in the low power standby mode and resets the instruction register. Therefore, \overline{CS} must be brought HIGH after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SCK)

The Serial Clock input is used to clock all data into and out of the device.

Serial Data In (SI)

SI is the serial data input.

Serial Data Out (SO)

SO is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

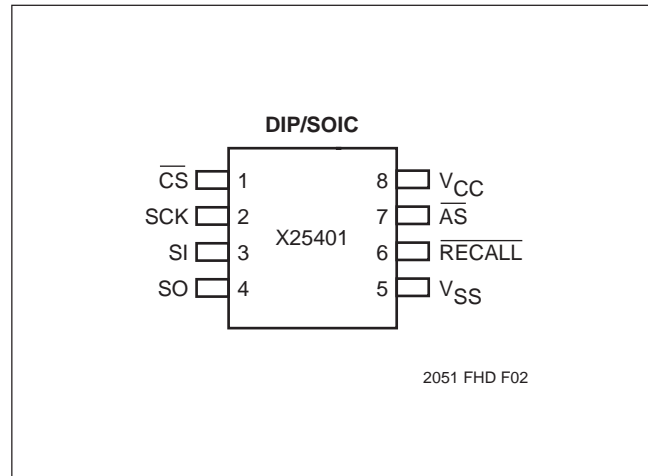
AUTOSTORE Output (\overline{AS})

\overline{AS} is an open drain output which, when asserted indicates V_{CC} has fallen below the AUTOSTORE threshold (V_{ASTH}). \overline{AS} may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller or as an input to a low power reset circuit.

\overline{RECALL}

\overline{RECALL} LOW will initiate an internal transfer of data from E²PROM to the RAM array.

PIN CONFIGURATION



PIN NAMES

| Symbol | Description |
|---------------------|------------------|
| \overline{CS} | Chip Enable |
| SCK | Serial Clock |
| SI | Serial Data In |
| SO | Serial Data Out |
| \overline{RECALL} | Recall Input |
| \overline{AS} | AUTOSTORE Output |
| V_{CC} | +5V |
| V_{SS} | Ground |

2051 PGM T01

X25401

DEVICE OPERATION

The X25401 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. \overline{CS} must be LOW during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address bits (A) or don't cares (X) and bits 2 through 0 are the operation codes. The X25401 requires the instruction to be shifted in with the MSB first.

After \overline{CS} is LOW, the X25401 will not begin to interpret the data stream until a logic "1" has been shifted in on SI. Therefore, \overline{CS} may be brought LOW with SCK running and SI LOW. SI must then go HIGH to indicate the start condition of an instruction before the X25401 will begin any action.

In addition, the SCK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

RCL and \overline{RECALL}

Either a software RCL instruction or a LOW on the \overline{RECALL} input will initiate a transfer of E²PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is

reset upon power-up and must be intentionally set by the user to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

WRDS and WREN

Internally the X25401 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E²PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E²PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

STO

The software STO instruction will initiate a transfer of data from RAM to E²PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

- STO instruction issued.
- The internal "write enable" latch must be set (WREN instruction issued).
- The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

TABLE 1. INSTRUCTION SET

| Instruction | Format, I ₂ I ₁ I ₀ | Operation |
|------------------|--|---|
| WRDS (Figure 3) | 1XXXX000 | Reset Write Enable Latch (Disables Writes and Stores) |
| STO (Figure 3) | 1XXXX001 | Store RAM Data in E ² PROM |
| ENAS | 1XXXX010 | Enable AUTOSTORE Feature |
| WRITE (Figure 2) | 1AAAA011 | Write Data into RAM Address AAAA |
| WREN (Figure 3) | 1XXXX100 | Set Write Enable Latch (Enables Writes and Stores) |
| RCL (Figure 3) | 1XXXX101 | Recall E ² PROM Data into RAM |
| READ (Figure 1) | 1AAAA11X | Read Data from RAM Address AAAA |

X = Don't Care
A = Address

2051 PGM T11

X25401

WRITE

The WRITE instruction contains the 4-bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. \overline{CS} must remain LOW during the entire operation. \overline{CS} must go HIGH before the next rising edge of SCK. If \overline{CS} is brought HIGH prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If \overline{CS} is kept LOW for more than 24 SCK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

READ

The READ instruction contains the 4-bit address of the word to be accessed. Unlike the other six instructions, I_0 of the instruction word is a “don’t care”. This provides two advantages. In a design that ties both SI and SO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SCK clock cycle.

All data bits are clocked by the falling edge of SCK (refer to Read Cycle Diagram).

LOW POWER MODE

When \overline{CS} is HIGH, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

AUTOSTORE Feature

The AUTOSTORE instruction (ENAS) sets the “AUTOSTORE enable” latch, allowing the X25401 to automatically perform a store operation when V_{CC} falls below the AUTOSTORE threshold (V_{ASTH}).

WRITE PROTECTION

The X25401 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Up Condition

Upon power-up the “write enable” and “AUTOSTORE enable” latches are in the reset state, disabling any store operation.

Unknown Data Store

The “previous recall” latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

SYSTEM CONSIDERATIONS

Power-Up Recall

The X25401 performs a power-up recall that transfers the E²PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the “previous recall” latch. During this power-up recall operation, all commands are ignored. Therefore, the host should delay any operations with the X25401 a minimum of t_{PUR} after V_{CC} is stable.

X25401

Figure 1. RAM Read

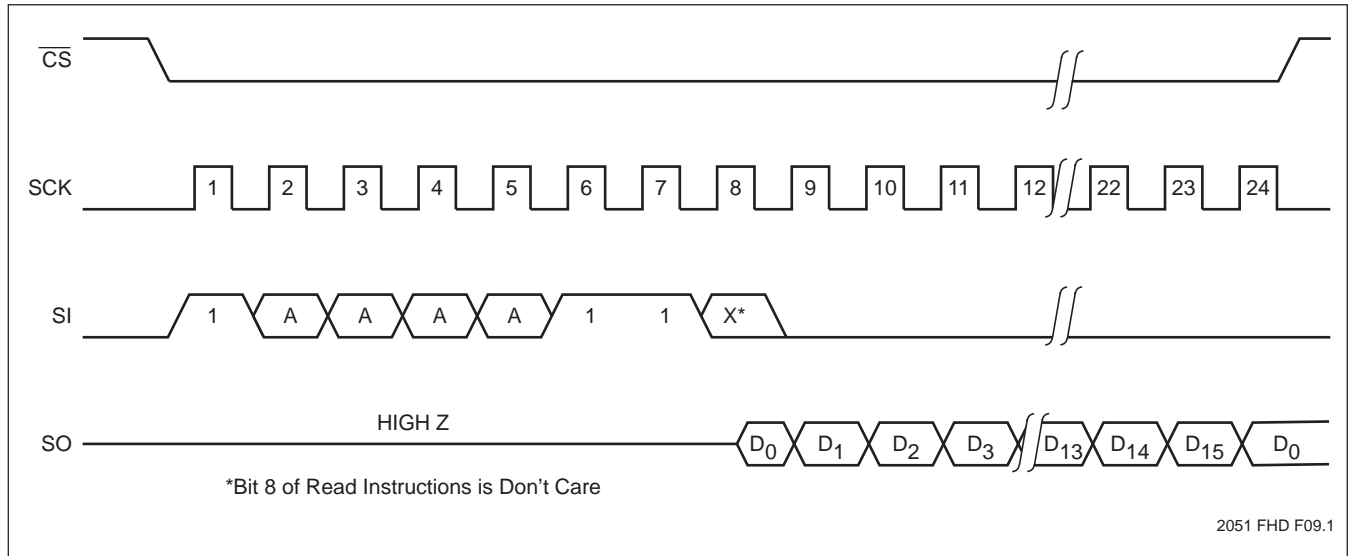


Figure 2. RAM Write

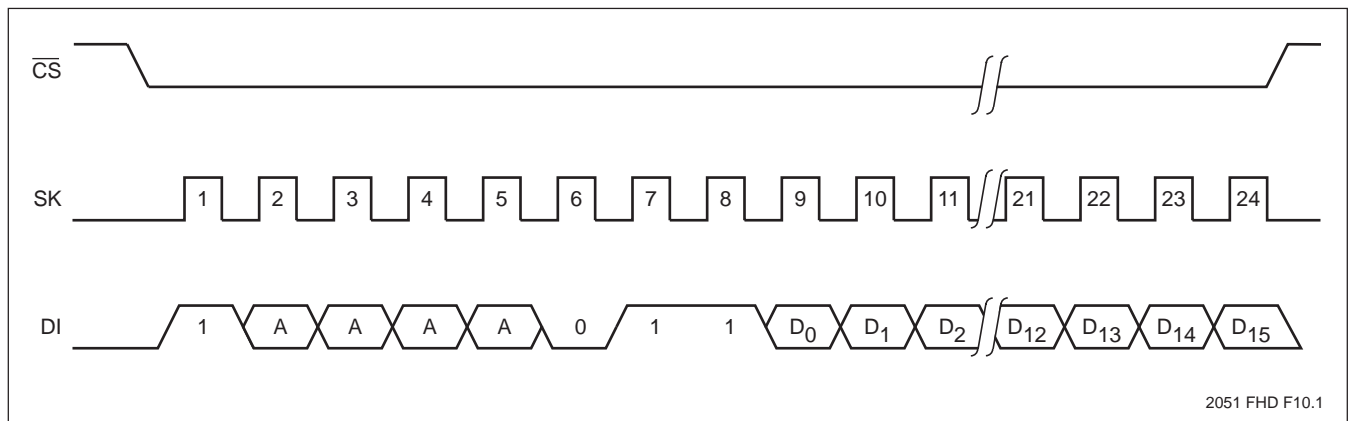
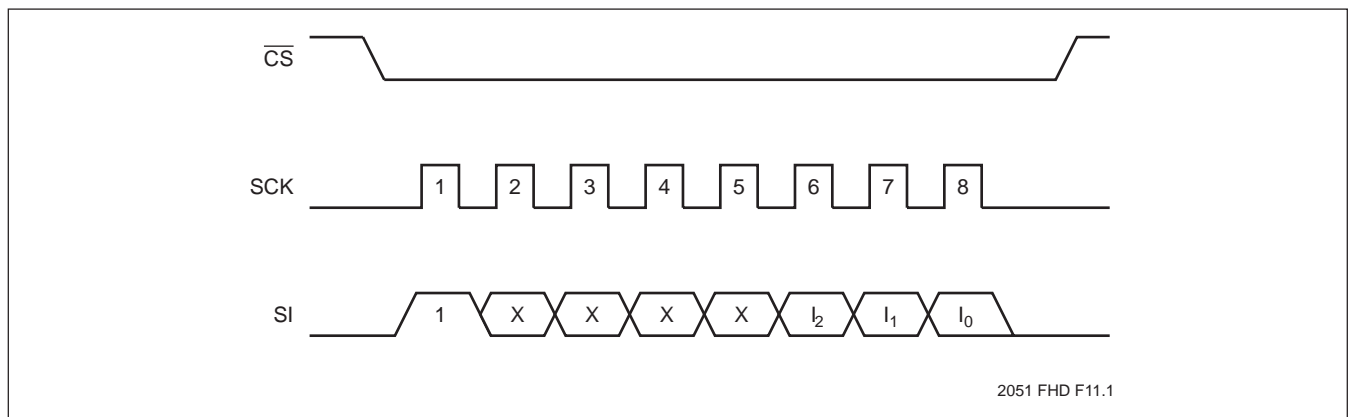
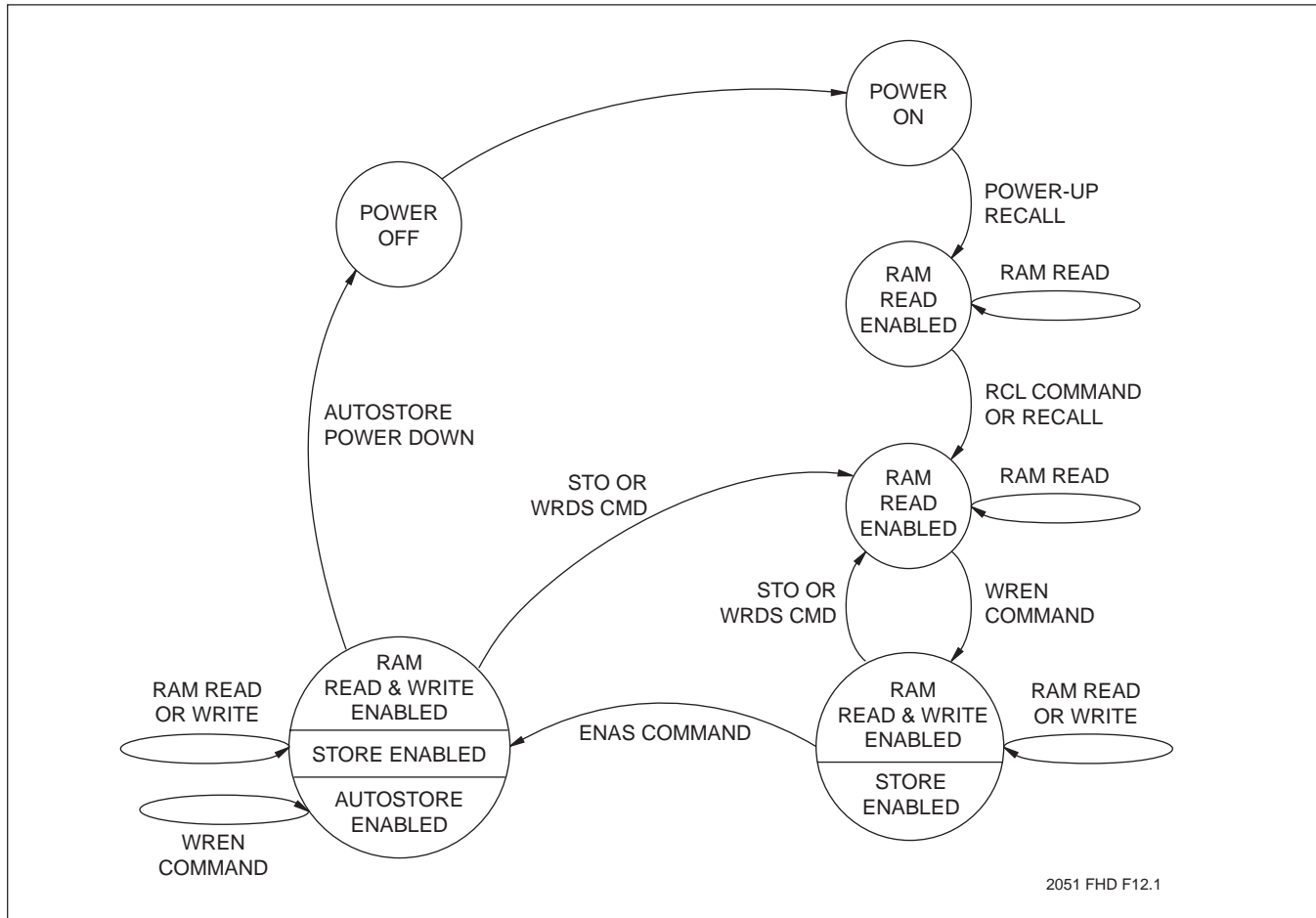


Figure 3. Non-Data Operations



X25401

Figure 4. X25401 State Diagram



X25401

ABSOLUTE MAXIMUM RATINGS*

| | |
|--|-----------------|
| Temperature under Bias | -65°C to +135°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on any Pin with Respect to V_{SS} | -1V to +7V |
| D.C. Output Current | 5mA |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Temperature | Min. | Max. |
|-------------|-------|--------|
| Commercial | 0°C | +70°C |
| Industrial | -40°C | +85°C |
| Military | -55°C | +125°C |

2051 PGM T02.1

| Supply Voltage | Limits |
|----------------|---------|
| X25401 | 5V ±10% |

2051 PGM T03.2

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | Units | Test Conditions |
|----------------|--|--------|--------------|-------|---|
| | | Min. | Max. | | |
| I_{CC1} | V_{CC} Supply Current (TTL Inputs) | | 10 | mA | SCK = 0.4V/2.4V Levels @ 1MHz, SO = Open, All Other Inputs = V_{IH} |
| I_{CC2} | V_{CC} Supply Current (During AUTOSTORE) | | 2 | mA | All Inputs = V_{IH} , $\overline{CS} = V_{IL}$, SO = Open, $V_{CC} = 4.3V$ |
| I_{SB1} | V_{CC} Standby Current (TTL Inputs) | | 1 | mA | SO = Open, $\overline{CS} = V_{IL}$, All Other Inputs = V_{IH} |
| I_{SB2} | V_{CC} Standby Current (CMOS Inputs) | | 50 | μA | SO = Open, $\overline{CS} = V_{SS}$, All Other Inputs = $V_{CC} - 0.3V$ |
| I_{LI} | Input Load Current | | 10 | μA | $V_{IN} = V_{SS}$ to V_{CC} |
| I_{LO} | Output Leakage Current | | 10 | μA | $V_{OUT} = V_{SS}$ to V_{CC} |
| $V_{IL}^{(1)}$ | Input LOW Voltage | -1 | 0.8 | V | |
| $V_{IH}^{(1)}$ | Input HIGH Voltage | 2 | $V_{CC} + 1$ | V | |
| V_{OL} | Output LOW Voltage | | 0.4 | V | $I_{OL} = 4.2mA$ |
| V_{OH} | Output HIGH Voltage | 2.4 | | V | $I_{OH} = -2mA$ |
| $V_{OL(AS)}$ | Output LOW Voltage (AS) | | 0.4 | V | $I_{OL(AS)} = 1mA$ |

2051 PGM T04.3

ENDURANCE AND DATA RETENTION

| Parameter | Min. | Units |
|----------------|-----------|----------------------|
| Endurance | 100,000 | Data Changes Per Bit |
| Store Cycles | 1,000,000 | Store Cycles |
| Data Retention | 100 | Years |

2051 PGM T05

CAPACITANCE $T_A = +25^\circ C$, $f = 1MHz$, $V_{CC} = 5V$

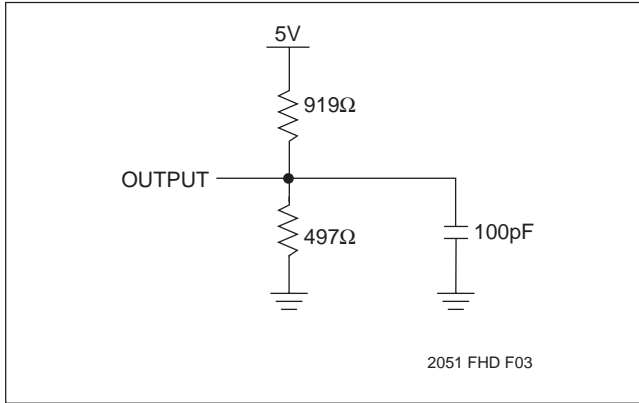
| Symbol | Parameter | Max. | Units | Test Conditions |
|-----------------|--------------------|------|-------|-----------------|
| $C_{OUT}^{(2)}$ | Output Capacitance | 8 | pF | $V_{OUT} = 0V$ |
| $C_{IN}^{(2)}$ | Input Capacitance | 6 | pF | $V_{IN} = 0V$ |

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

2051 PGM T06.2

X25401

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

| | |
|--------------------------------|----------|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 10ns |
| Input and Output Timing Levels | 1.5V |

2051 PGM T07.1

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read and Write Cycle Limits

| Symbol | Parameter | Min. | Max. | Units |
|----------------|------------------------------|------|------|---------|
| $F_{SK}^{(3)}$ | SCK Frequency | | 1 | MHz |
| t_{SCKH} | SCK Positive Pulse Width | 400 | | ns |
| t_{SCKL} | SCK Negative Pulse Width | 400 | | ns |
| t_{DS} | Data Setup Time | 400 | | ns |
| t_{DH} | Data Hold Time | 80 | | ns |
| t_{PD1} | SCK to Data Bit 0 Valid | | 375 | ns |
| t_{PD} | SCK to Data Valid | | 375 | ns |
| t_z | Chip Select to Output High Z | | 1 | μs |
| t_{CSS} | Chip Select Setup | 800 | | ns |
| t_{CSH} | Chip Select Hold | 350 | | ns |
| t_{CDS} | Chip Deselect | 800 | | ns |

2051 PGM T08.1

POWER-UP TIMING

| Symbol | Parameter | Max. | Units |
|-----------------|--------------------------------------|------|---------|
| $t_{PUR}^{(4)}$ | Power-up to Read Operation | 200 | μs |
| $t_{PUW}^{(4)}$ | Power-up to Write or Store Operation | 5 | ms |

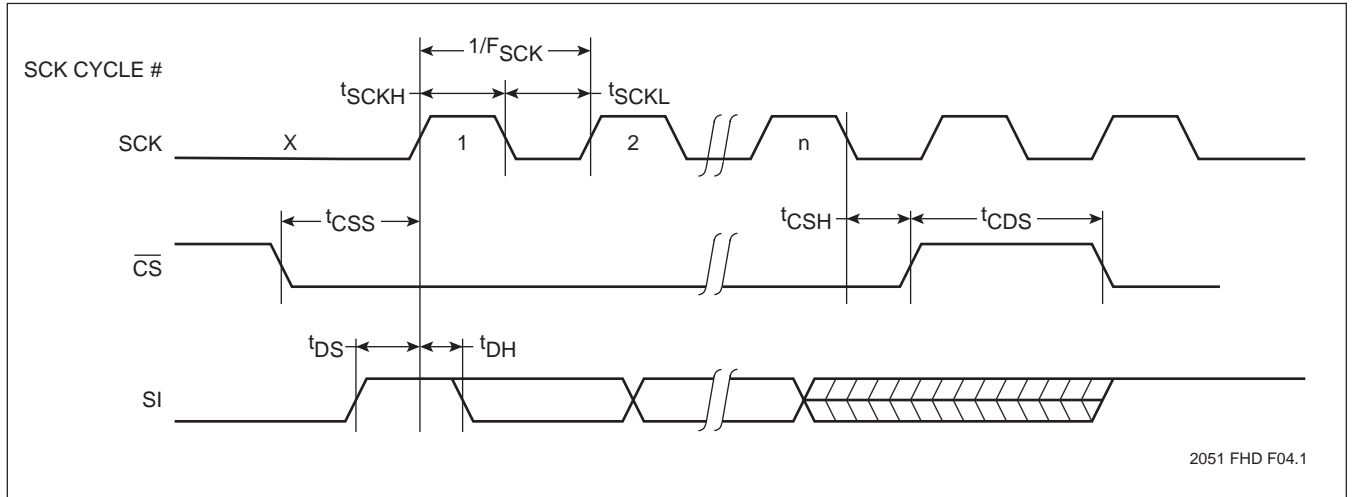
2051 PGM T09

Notes: (3) SCK rise and fall times must be less than 50ns.

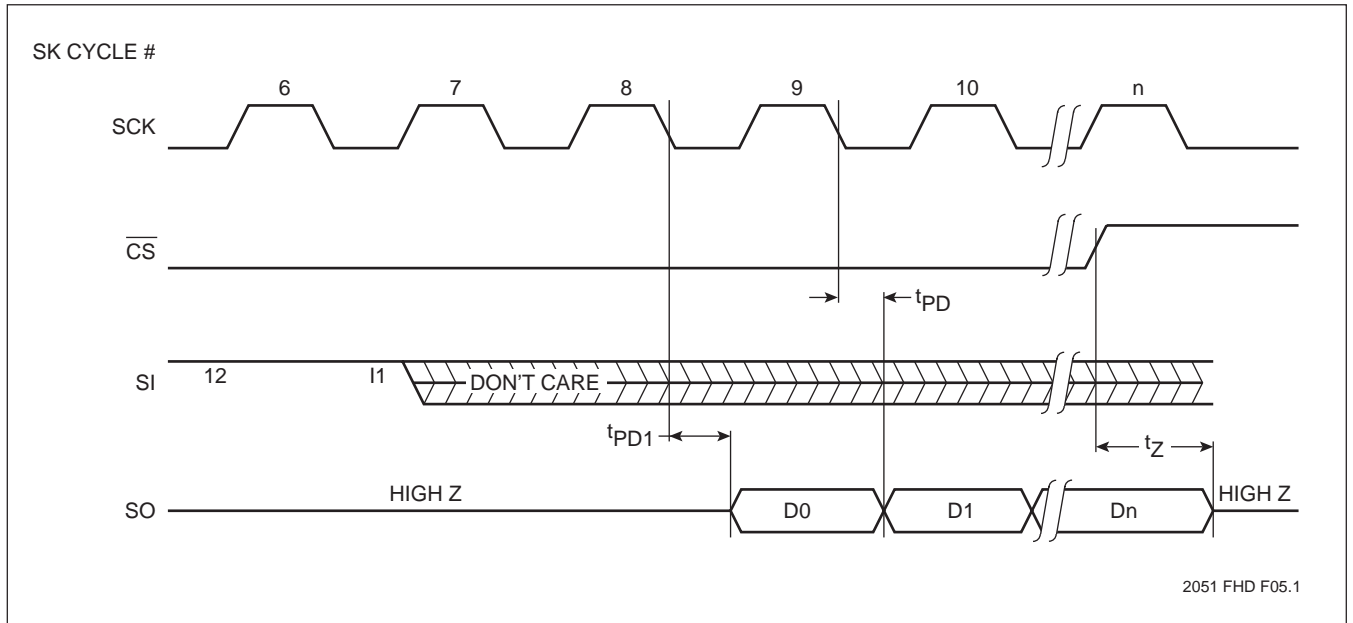
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X25401

Write Cycle



Read Cycle



X25401

NONVOLATILE OPERATIONS

| Operation | $\overline{\text{RECALL}}$ | Software Instruction | Write Enable Latch State | Previous Recall Latch State |
|-----------------|----------------------------|----------------------|--------------------------|-----------------------------|
| Hardware Recall | 0 | NOP ⁽⁵⁾ | X | X |
| Software Recall | 1 | RCL | X | X |
| Software Store | 1 | STO | SET | SET |

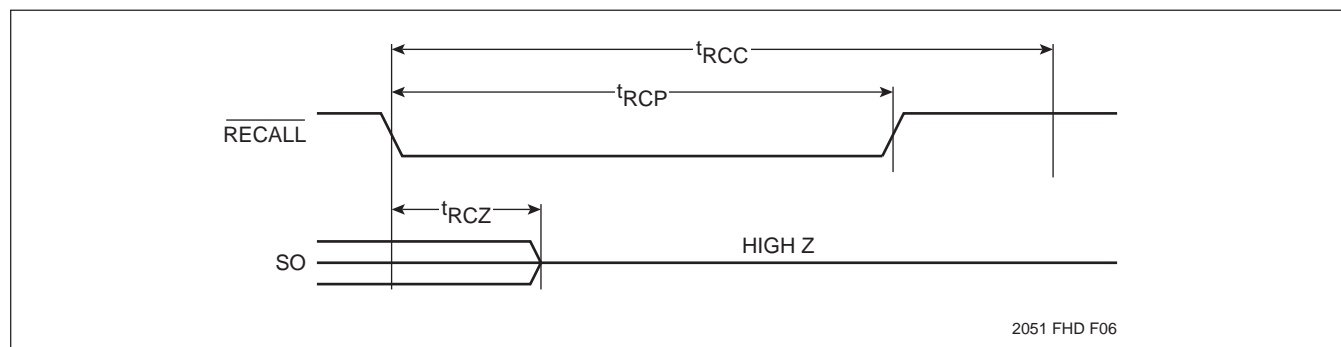
2051 PGM T10

ARRAY RECALL LIMITS

| Symbol | Parameter | Min. | Max. | Units |
|------------------|-----------------------------------|------|------|---------------|
| t_{RCC} | Recall Cycle Time | 2 | | μs |
| t_{RCP} | Recall Pulse Width ⁽⁶⁾ | 500 | | ns |
| t_{RCZ} | Recall to Output in High Z | | 500 | ns |

2051 PGM T11

Recall Timing



SOFTWARE STORE CYCLE LIMITS

| Symbol | Parameter | Min. | Typ. ⁽⁷⁾ | Max. | Units |
|-----------------|---|------|---------------------|------|-------|
| t_{ST} | Store Time After Clock 8 of STO Command | | 2 | 5 | ms |

2051 PGM T12.1

Notes: (5) NOP designates when the X25401 is not currently executing an instruction.

(6) Recall rise time must be $<10\mu\text{s}$.

(7) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

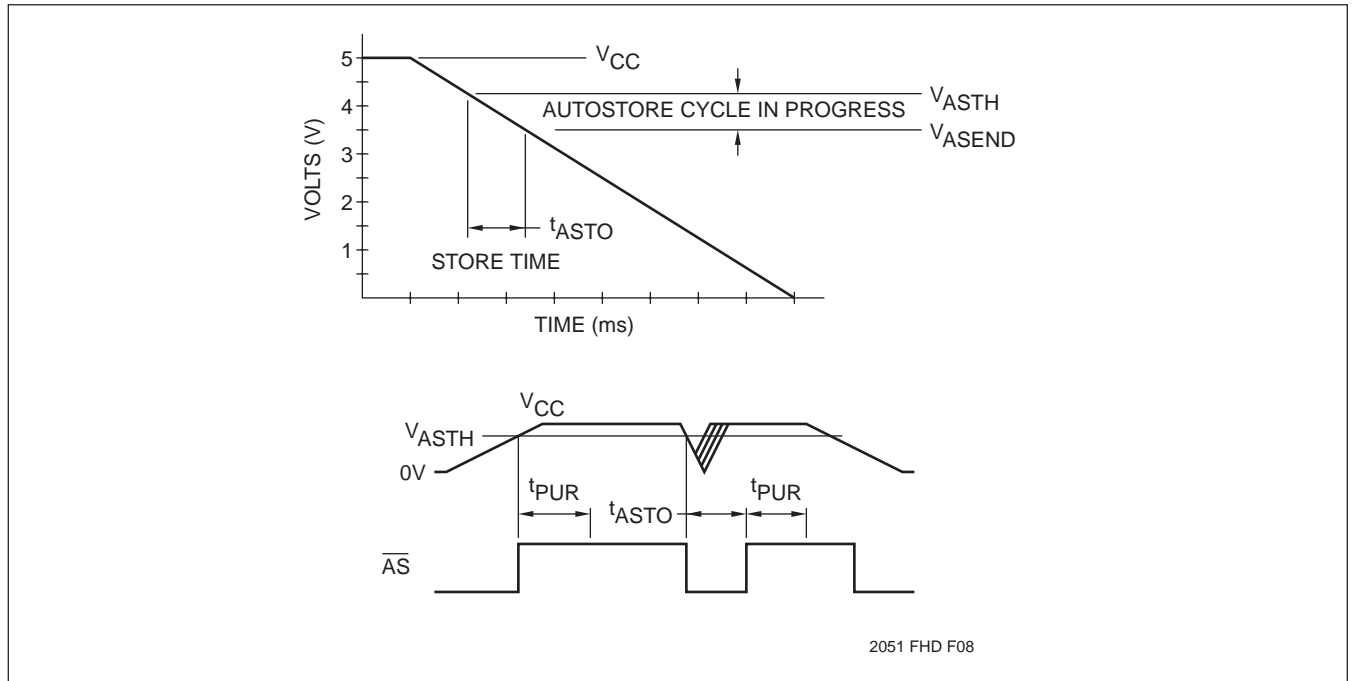
X25401

AUTOSTORE Cycle Limits

| Symbol | Parameter | Min. | Max. | Units |
|-------------|-----------------------------|------|------|-------|
| V_{ASTO} | AUTOSTORE Cycle Time | | 5 | ms |
| V_{ASTH} | AUTOSTORE Threshold Voltage | 4.0 | 4.3 | V |
| V_{ASEND} | AUTOSTORE Cycle End Voltage | 3.5 | | V |

2051 PGM T13

AUTOSTORE Cycle Timing Diagrams



2051 FHD F08

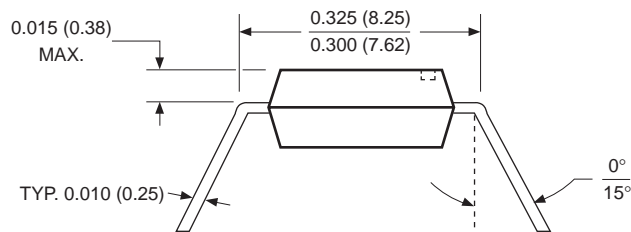
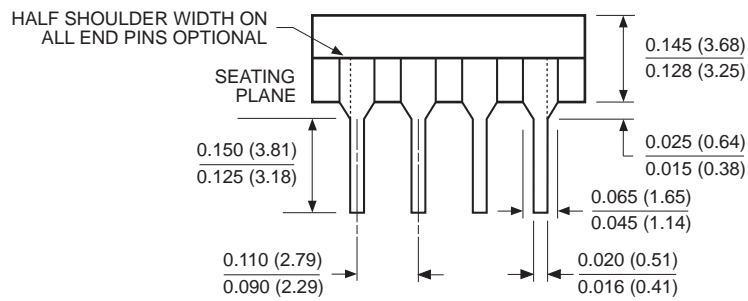
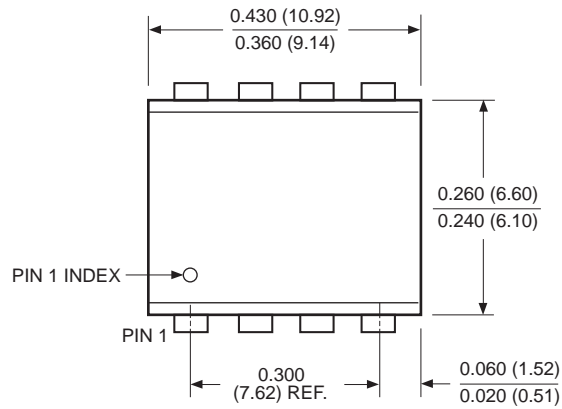
SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|----------|-----------------------------|-------------------------------|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

X25401

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

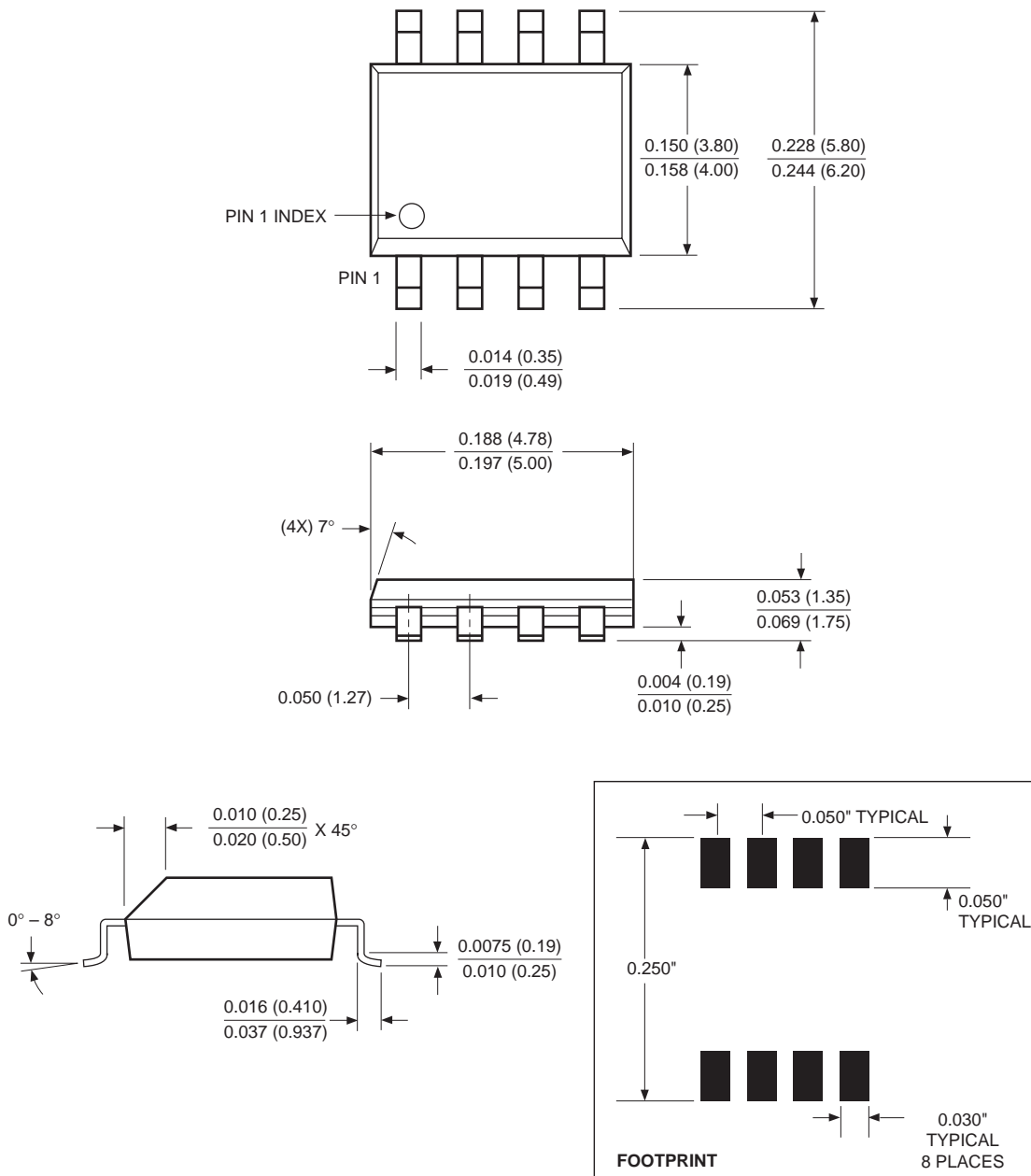
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F01

X25401

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

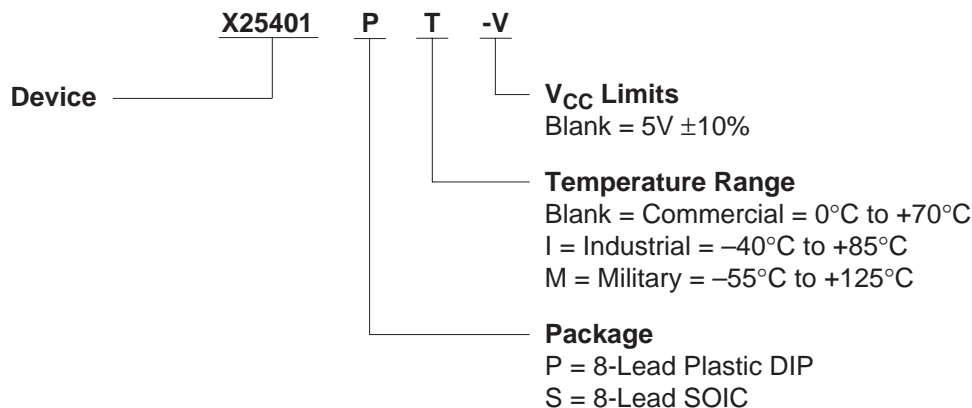


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

X25401

ORDERING INFORMATION



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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.