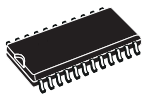
HCF40208B

4 x 4 MULTIPORT REGISTER

- ONE INPUT AND TWO OUTPUT BUSES
- UNLIMITED EXPANSION IN BIT AND WORD DIRECTION
- DATA LINES HAVE LATCHED INPUTS
- 3-STATE OUTPUTS
- SEPARATE CONTROL OF EACH BUS, ALLOWING SIMULTANEOUS INDEPENDENT READING AND ANY OF FOUR REGISTERS ON BUS A AND BUS B AND INDEPENDENT WRITING INTO ANY OF THE FOUR REGISTERS
- 40208B IS PIN-COMPATIBLE WITH INDUSTRY TYPE MC14580
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



SOP

ORDER CODES

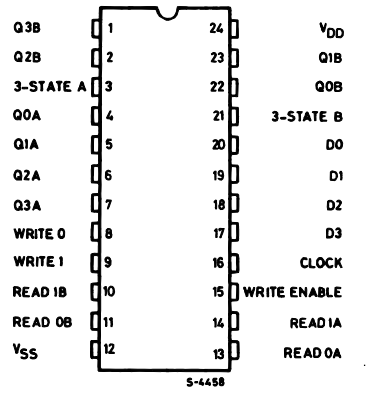
PACKAGE	TUBE	T & R
SOP	HCF40208BM1	HCF40208M013TR

DESCRIPTION

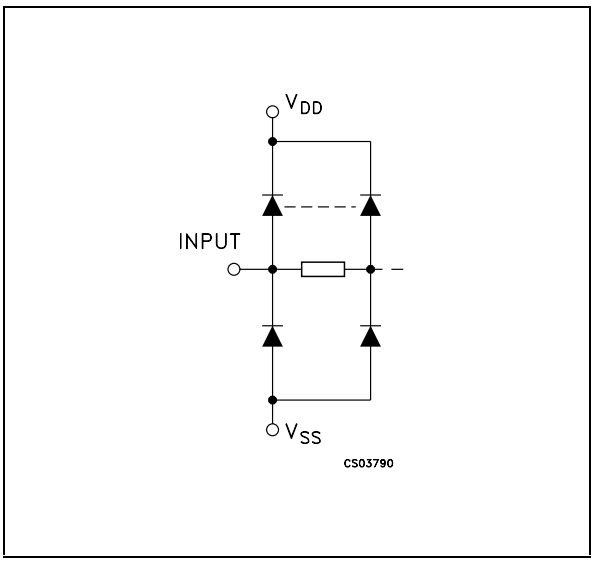
HCF40208B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in SOP packages.

HCF40208B is a 4 x 4 multiport register containing four 4-bit registers, a write address decoder, two separate read address decoders, and two 3-state output buses. When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high impedance state. The high impedance third state provides the outputs with the capability of being connected to the bus lines in a bus organized system without the need for interface or pull-up components. When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

PIN CONNECTION



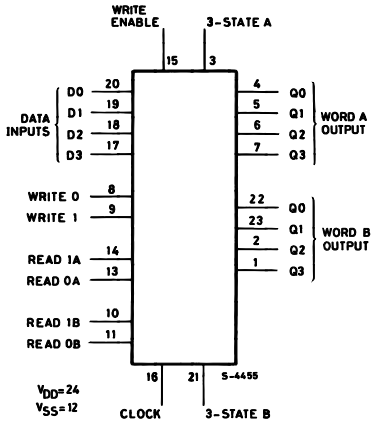
INPUT EQUIVALENT CIRCUIT



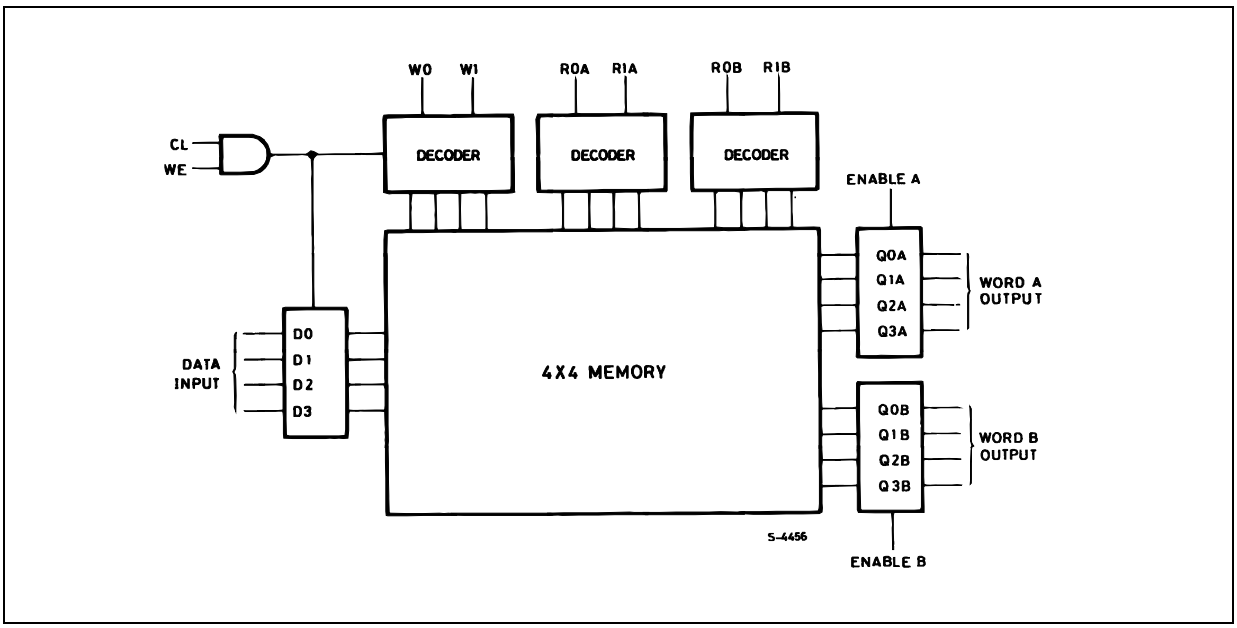
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
4, 5, 6, 7	Q0A to Q3A	Word A Output
22, 23, 2, 1	Q0B to Q3B	Word B Output
20, 19, 18, 17	D0 to D3	Data Inputs
16	CLOCK	Clock Input
15	WRITE ENABLE	Write Enable Input
21	3-STATE B	3 State Output
3	3-STATE A	3 State Output
8, 9	WRITE 0, WRITE 1	Write Address Inputs
10, 11	READ 0B, READ 1B	Read Address Inputs
13, 14	READ 0A, READ 1A	Read Address Inputs
12	V_{SS}	Negative Supply Voltage
24	V_{DD}	Positive Supply Voltage

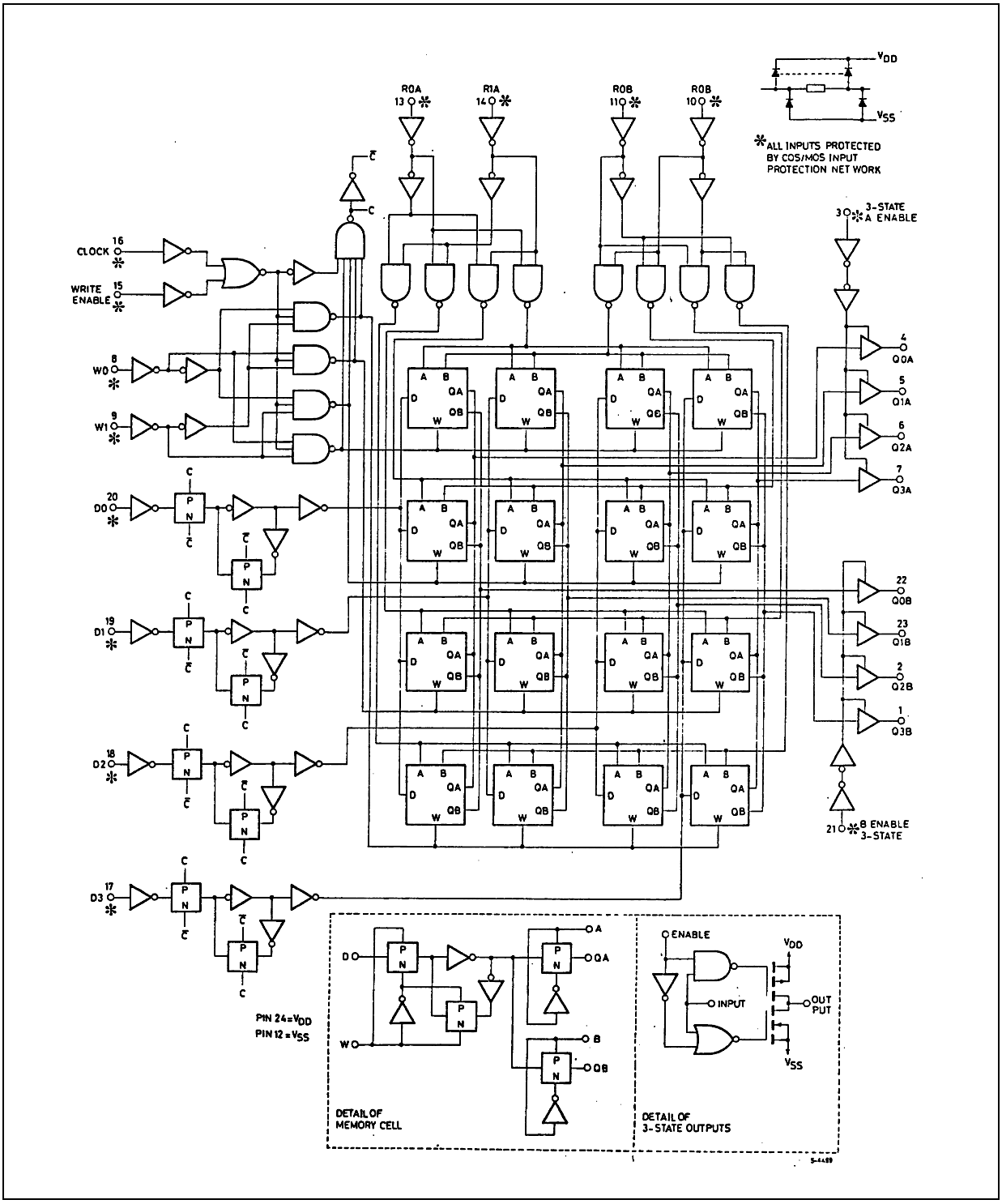
FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



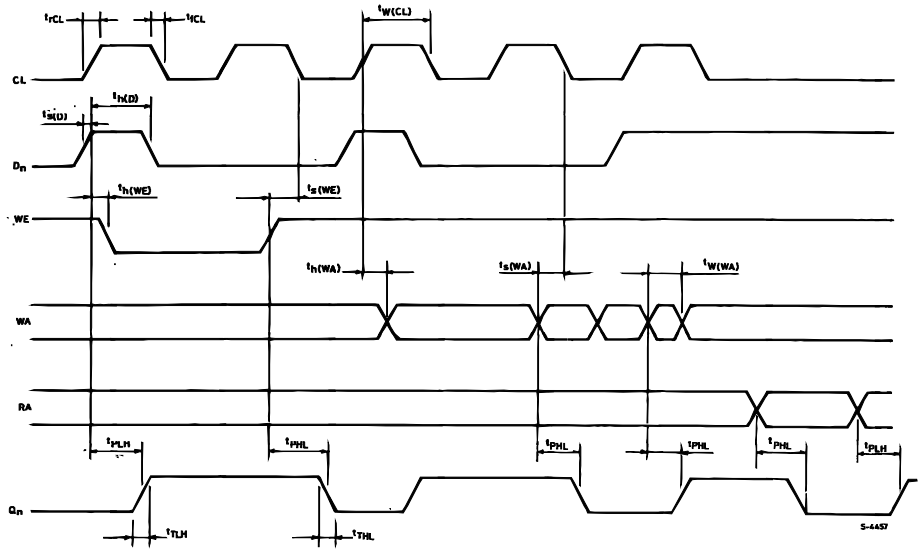
SCHEMATIC DIAGRAM



TRUTH TABLE

CLOCK	Write Enable	Write 1	Write 2	Read 1A	Read 0A	Read 1B	Read 0B	Enable A	Enable B	Dn	DnA	QnB
⎍	H	S1	S2	S1	S2	S1	S2	H	H	H	H	H
⎍	H	S1	S2	S1	S2	S1	S2	H	L	L	L	L
X	X	X	X	X	X	X	X	L	L	Z	Z	Z
⎍	H	L	L	L	H	H	L	H	H	Dn to word 0	Word 1 Out	Word 2 Out
⎍	L	L	L	L	H	H	L	H	H	Word 0 not altered	Word 1 Out	Word 2 Out
X	X	X	X	H	L	L	H	H	X	X	Word 2 Out	Word 1 Out
⎎	X	X	X	X	X	X	X	H	H	X	NC	NC

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

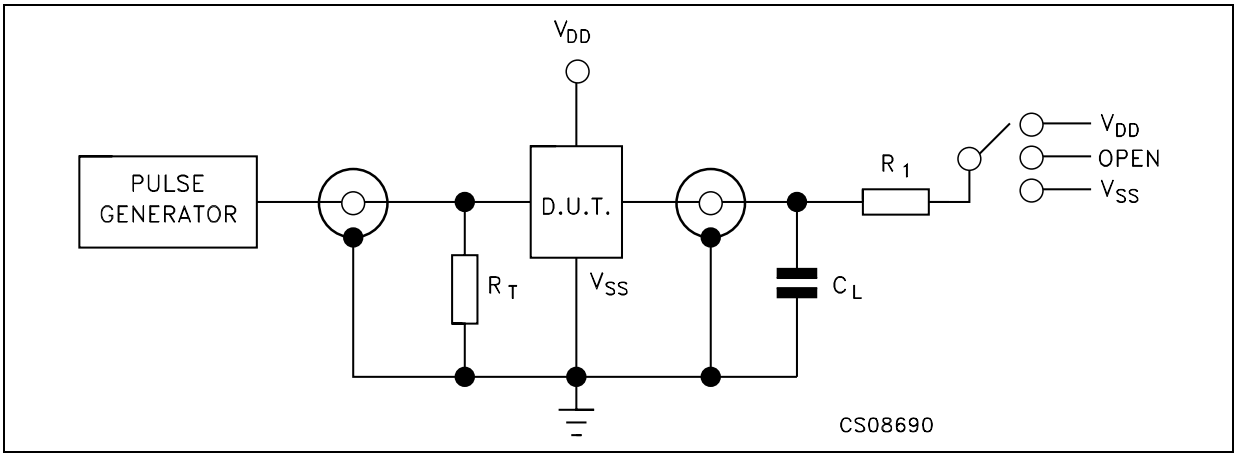
Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
I_{OZ}	3-State Output Leakage Current	0/18	Any Input		18		$\pm 10^{-4}$	±0.4		±12		±12	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time Clock or Write Enable to Q	5			360	720	ns
		10			140	280	
		15			100	200	
	Propagation Delay Time Read or Write Address to Q	5			300	600	ns
		10			120	240	
		15			85	170	
t_{PZH} t_{PHZ}	3-State Disable Delay Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{PZL} t_{PLZ}	3-State Display Delay Time	5			130	260	ns
		10			60	120	
		15			50	100	
t_{THL} t_{TLH}	Output Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{setup}	Setup Time Data to Clock $t_{s(D)}$	5		0	-95		ns
		10		0	-35		
		15		0	-20		
	Setup Time Write Enable to Clock $t_{s(WE)}$	5		250	125		ns
		10		100	50		
		15		70	35		
	Setup Time Write Address to Clock $t_{s(WA)}$	5		250	125		ns
		10		100	50		
		15		70	35		
t_r, t_s	Clock Rise and Fall Time	5				15	ns
		10				5	
		15				5	
t_{hold}	Hold Time Data to Clock $t_{s(D)}$	5		220	110		ns
		10		100	50		
		15		80	40		
	Hold Time Write Enable to Clock $t_{s(WE)}$	5		270	135		ns
		10		130	65		
		15		80	40		
	Hold Time Write Address to Clock $t_{s(WA)}$	5		330	165		ns
		10		140	70		
		15		90	45		
t_W	Clock Pulse Width Clock or Write Enable $t_{W(CL)}$	5		350	175		ns
		10		130	65		
		15		90	45		
t_W	Clock Pulse Width Write Address $t_{W(WA)}$	5		300	150		ns
		10		150	75		
		15		90	45		
f_{CL}	Maximum Clock Input Frequency	5		1.5	3		MHz
		10		3.5	7		
		15		4.5	9		

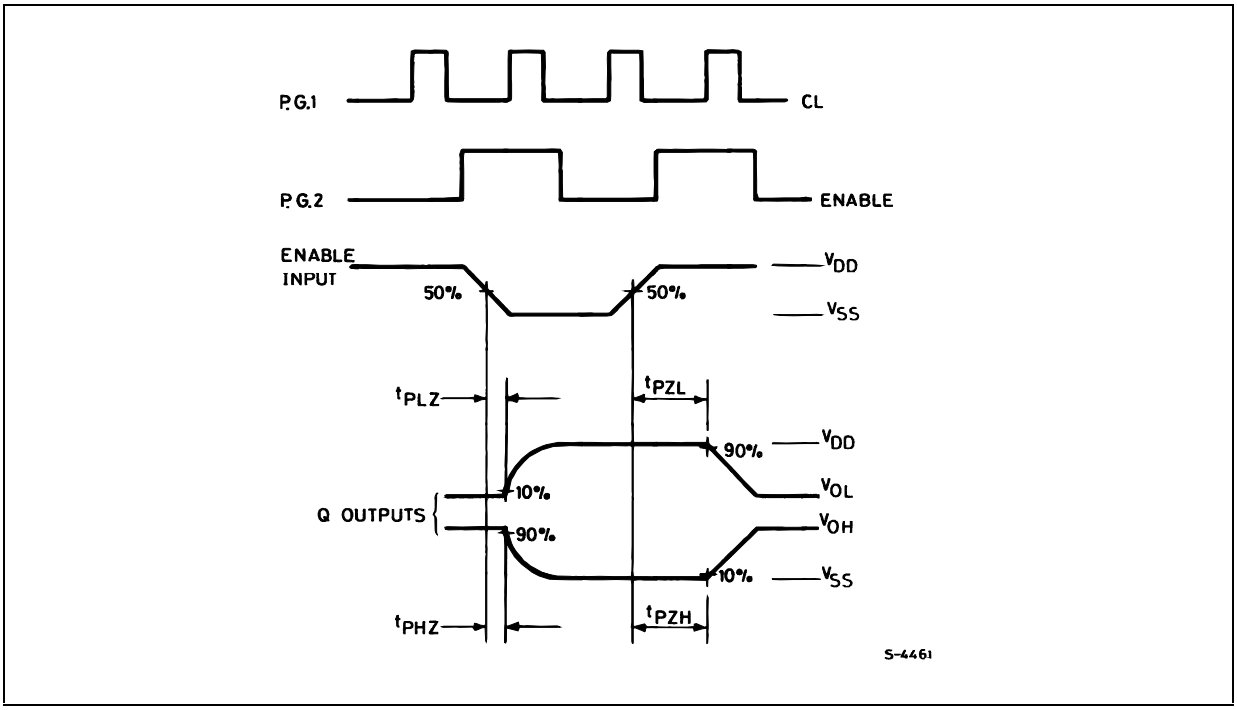
TEST CIRCUIT



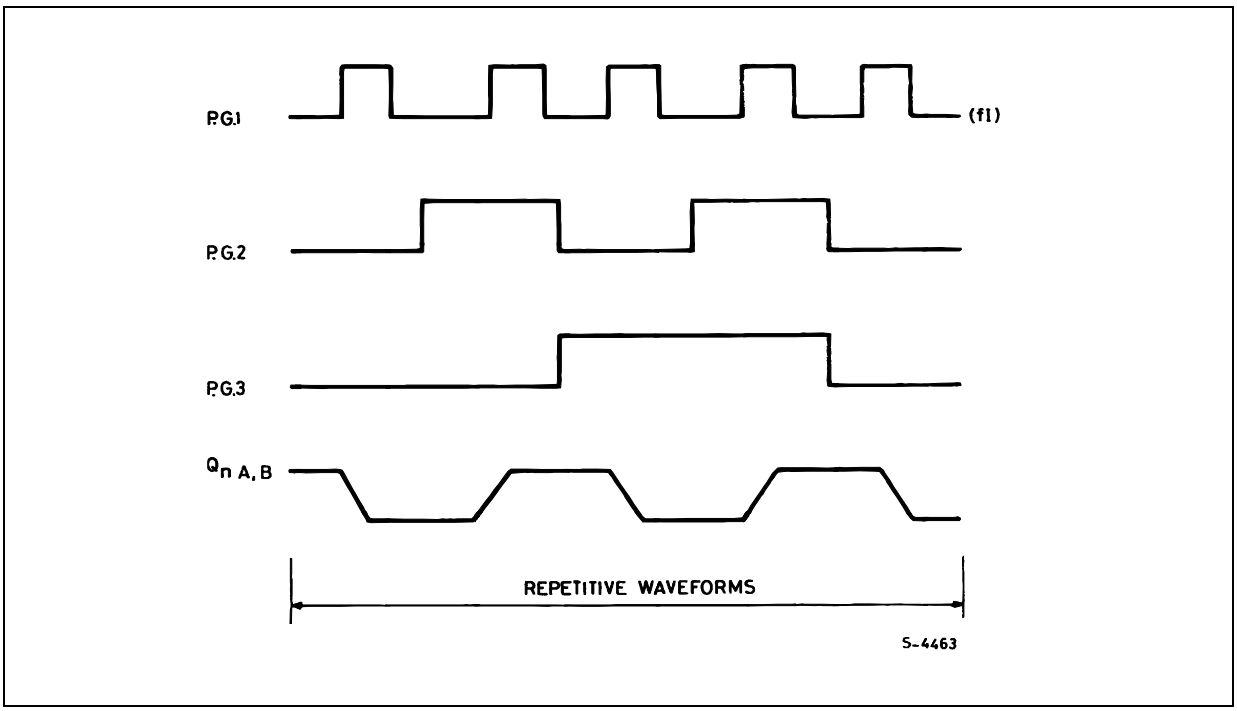
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{DD}
t_{PZH}, t_{PHZ}	V_{SS}

C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM : ENABLE AND DISABLE TIME

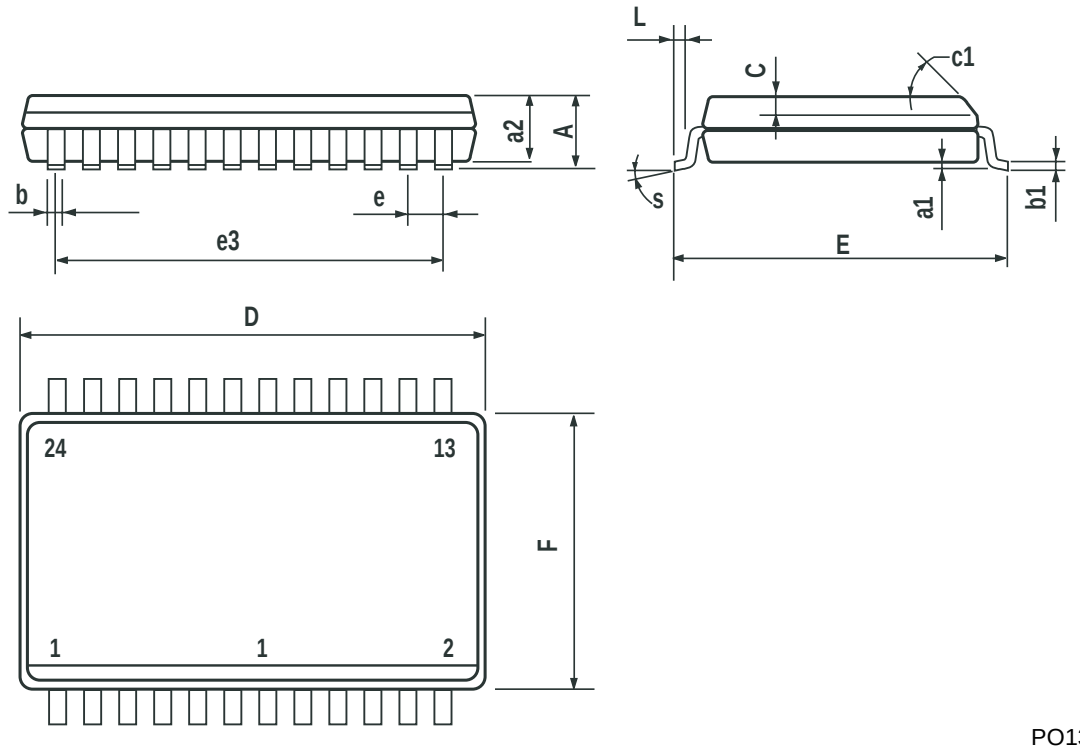


SWITCHING WAVEFORM



SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



PO13T