



## DUAL 4-INPUT NOR GATE

The HEF4002B provides the positive dual 4-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

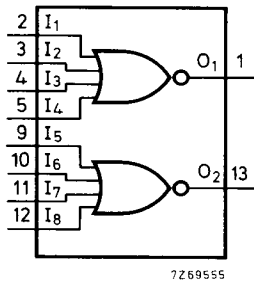


Fig. 1 Functional diagram.

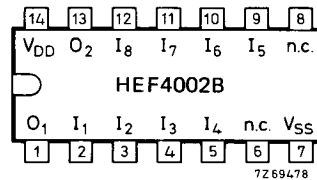


Fig. 2 Pinning diagram.

HEF4002BP : 14-lead DIL; plastic (SOT-27).  
 HEF4002BD: 14-lead DIL; ceramic (cerdip) (SOT-73).  
 HEF4002BT : 14-lead mini-pack; plastic  
 (SO-14; SOT-108A).

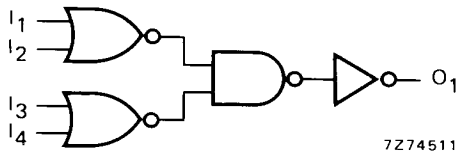


Fig. 3 Logic diagram (one gate).

FAMILY DATA

see Family Specifications

I<sub>DD</sub> LIMITS category GATES

## A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $C_L = 50 \text{ pF}$ ; input transition times  $\leq 20 \text{ ns}$

	$V_{DD}$ V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	$t_{PHL}; t_{PLH}$	60	120	ns	$33 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		25	50	ns	$14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		20	40	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{TLH}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	$V_{DD}$ V	typical formula for P ( $\mu\text{W}$ )	where
Dynamic power dissipation per package (P)	5	$1050 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	$f_i$ = input freq. (MHz)
	10	$4300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	$f_o$ = output freq. (MHz)
	15	$11700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	$C_L$ = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			$V_{DD}$ = supply voltage (V)