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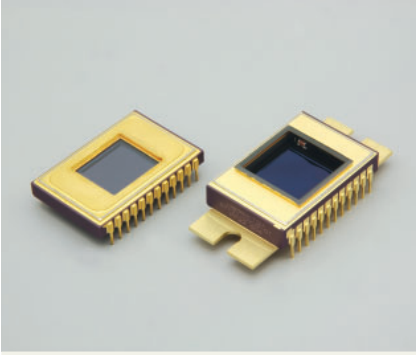
CCD area image sensors



S7170-0909 S7171-0909-01

512 × 512 pixels, back-thinned FFT-CCD

HAMAMATSU developed MPP (multi-pinned phase) mode back-thinned FFT-CCDs S7170-0909, S7171-0909-01 specifically designed for low-light-level detection in scientific applications. The S7170-0909, S7171-0909-01 have sensitivity from the UV to near-IR as well as having low dark current and wide dynamic range. Stability of the spectral response curve is also achieved for high precision measurements.
Either one-stage or two-stage thermoelectric cooler is built into the package (S7171-0909-01, S7172-0909). At room temperature operation, the device can be cooled down to -10 °C by one-stage cooler and -30 °C by two-stage cooler, respectively. In addition since both the CCD chip and the thermoelectric cooler are hermetically sealed, no dry air is required, thus allowing easy handling.

Features

- **512 × 512 pixel format**
- **Greater than 90% quantum efficiency at peak sensitivity wavelength**
- **Wide spectrum range**
- **Low readout noise**
- **Wide dynamic range**
- **MPP operation**
- **Non-cooled type: S7170-0909**
  One-stage TE-cooled type: S7171-0909-01

Applications

- **Scientific measuring instrument**
- **Semiconductor inspection**
- **UV imaging**
- **Bio-photon observation**

Selection guide

Type no.	Cooling	Number of total pixels	Number of effective pixels	Image size [mm (H) × mm (V)]	Suitable multichannel detector head
S7170-0909	Non-cooled	532 × 520	512 × 512	12.288 × 12.288	C7180
S7171-0909-01	One-stage TE-cooled				C7181

Note: Two-stage TE-cooled type (S7172-0909) is also available.

Structure

Parameter	S7170-0909	S7171-0909-01
Pixel size	24 (H) × 24 (V) µm	
Vertical clock phase	2 phases	
Horizontal clock phase	2 phases	
Output circuit	One-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outlines)	
Window	Sapphire*1	AR-coated sapphire

*1: Window-less type (ex. S7170-0909N) is available upon request.
(Temporary window is fixed by tape to protect the CCD chip and wire bonding.)

Absolute maximum ratings (Ta=25 °C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
Output transistor drain voltage	VOD	-0.5	-	+25	V
Reset drain voltage	VRD	-0.5	-	+18	V
Vertical input source voltage	VISV	-0.5	-	+18	V
Horizontal input source voltage	VISH	-0.5	-	+18	V
Vertical input gate voltage	VIG1V, VIG2V	-10	-	+15	V
Horizontal input gate voltage	VIG1H, VIG2H	-10	-	+15	V
Summing gate voltage	VSG	-10	-	+15	V
Output gate voltage	VOG	-10	-	+15	V
Reset gate voltage	VRG	-10	-	+15	V
Transfer gate voltage	VTG	-10	-	+15	V
Vertical shift register clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal shift register clock voltage	VP1H, VP2H	-10	-	+15	V

*2: Package temperature (S7170-0909), chip temperature (S7171-0909-01)

Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbo	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	18	20	22	V
Reset drain voltage		VRD	11.5	12	12.5	V
Output gate voltage		VOG	1	3	5	V
Substrate voltage		VSS	-	0	-	V
Test point	Vertical input source voltage	VISV	-	VRD	-	V
	Horizontal input source voltage	VISH	-	VRD	-	V
	Vertical input gate voltage	VIG1V, VIG2V	-9	-8	-	V
	Horizontal input gate voltage	VIG1H, VIG2H	-9	-8	-	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	
External load resistance		RL	20	22	24	kΩ

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	MHz
Vertical shift register capacitance	CP1V, CP2V	-	6400	-	pF
Horizontal shift register capacitance	CP1H, CP2H	-	120	-	pF
Summing gate capacitance	CSG	-	30	-	pF
Reset gate capacitance	CRG	-	30	-	pF
Transfer gate capacitance	CTG	-	70	-	pF
Charge transfer efficiency*3	CTE	0.99995	0.99999	-	-
DC output level	Vout	14	16	18	V
Output impedance	Zo	-	3	4	kΩ
Power consumption*4	P	-	13	14	mW

*3: Charge transfer efficiency per pixel, measured at half of the full well capacity
*4: Power consumption of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C unless otherwise noted)

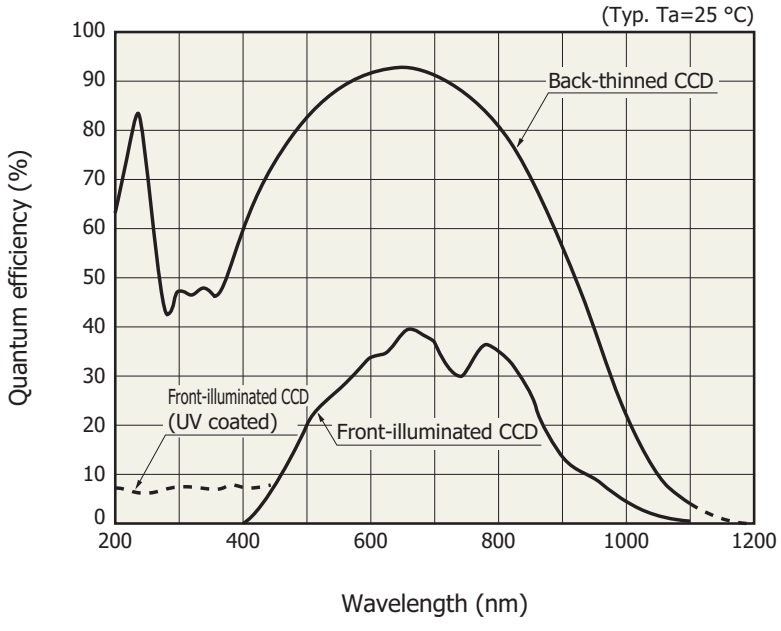
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × Sv	-	V
Full well capacity		Vertical	Fw	240	320	-	ke⁻
		Horizontal*5		300	600	-	
CCD node sensitivity			Sv	1.8	2.2	-	μV/e⁻
Dark current*6 (MPP mode)		25 °C	DS	-	100	1000	e⁻/pixel/s
		0 °C		-	10	100	
Readout noise*7			Nr	-	8	16	e⁻ rms
Dynamic range*8		Line binning	DR	37500	75000	-	-
		Area scanning		30000	40000	-	-
Photo response non-uniformity*9			PRNU	-	±3	±10	%
Spectral response range			λ	-	200 to 1100	-	nm
Blemish	Point defect*10	White spots	-	-	-	0	-
		Black spots		-	-	10	-
	Cluster defect*11			-	-	3	-
	Column defect*12			-	-	0	-

*5: The linearity is ±1.5%.
*6: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*7: Measured with a HAMAMATSU C4880 digital CCD camera with a CDS circuit (sensor temperature: -40 °C, operating frequency: 150 kHz)
*8: Dynamic range = Full well capacity / Readout noise
*9: Measured at half of the full well capacity, using LED light (peak emission wavelength: 560 nm)

$$\text{Photo Response Non-Uniformity (PRNU)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \ [\%]$$

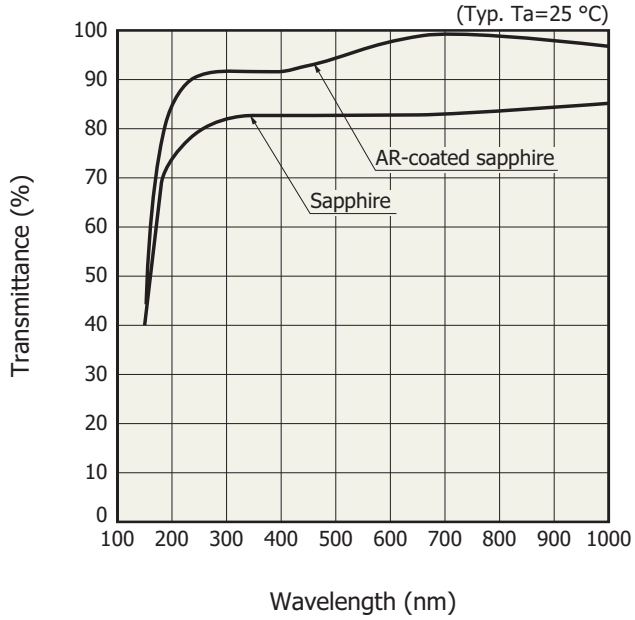
*10: White spots
Pixels whose dark current is higher than 1 ke⁻ after one-second integration at 0 °C
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output (measured with uniform light producing one-half of the saturation charge)
*11: 2 to 9 contiguous defective pixels
*12: 10 or more contiguous defective pixels

Spectral response (without window)*13



*13: Spectral response is decreased according to the spectral transmittance characteristic of window material.

Spectral transmittance characteristic of window material



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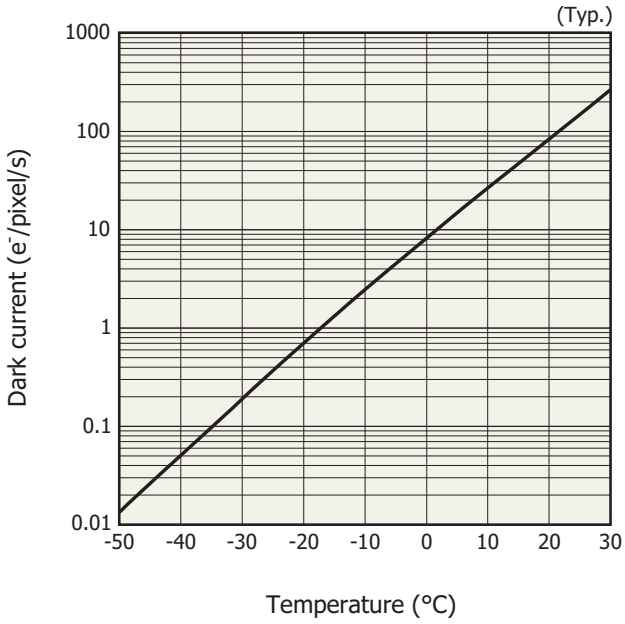
Window material

Type no.	Window material
S7170-0909	Sapphire*14 (option: windowless)
S7172-0909 (two-stage TE-cooled type)	
S7171-0909-01	AR-coated sapphire*14 (option: windowless)

*14: Hermetic sealing

Dark current vs. temperature



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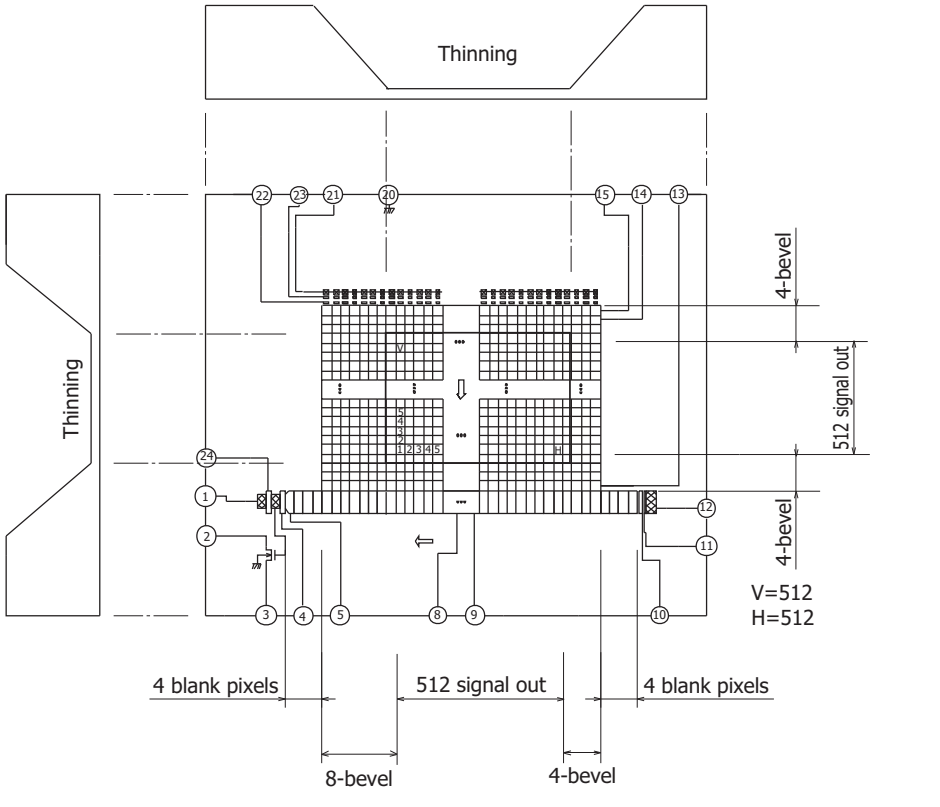
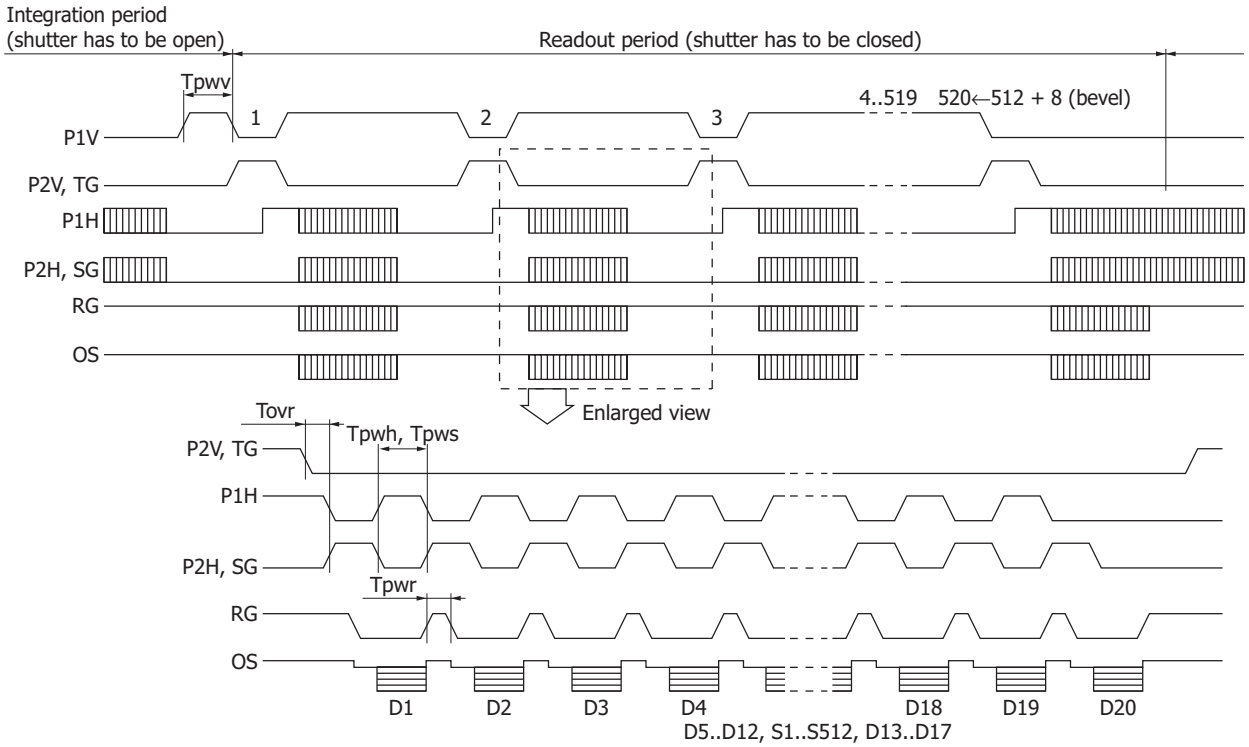
Device structure (conceptual drawing of top view)



Timing chart

Area scanning (large full well mode)

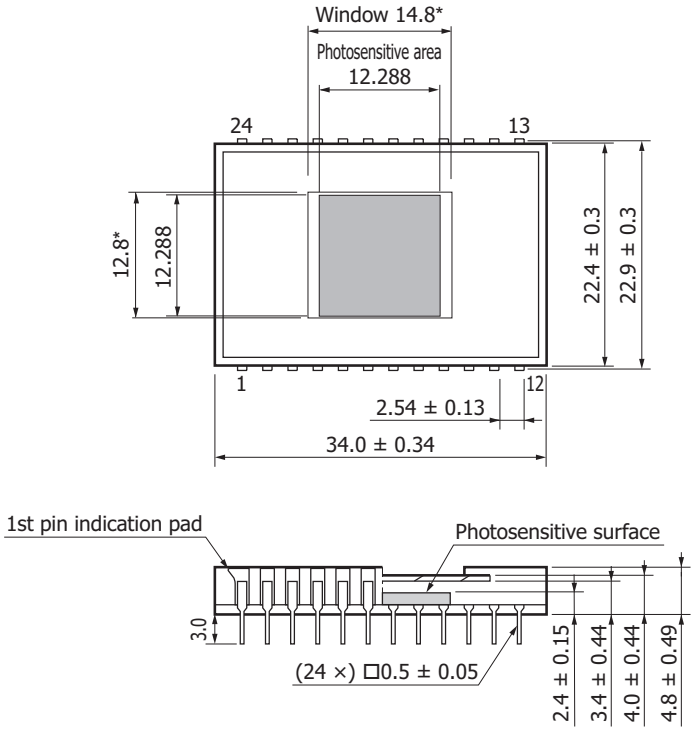


Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*15	Pulse width	Tpwv	6	8	-	µs
	Rise and fall times	Tprv, Tpfv	200	-	-	ns
P1H, P2H*15	Pulse width	Tpwh	500	2000	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	500	2000	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	100	-	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time	Tovr	3	-	-	µs

*15: Symmetrical clock pulses should be overlapped at 50% of maximum amplitude.

Dimensional outlines (unit: mm)

S7170-0909



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristic of window material" graph

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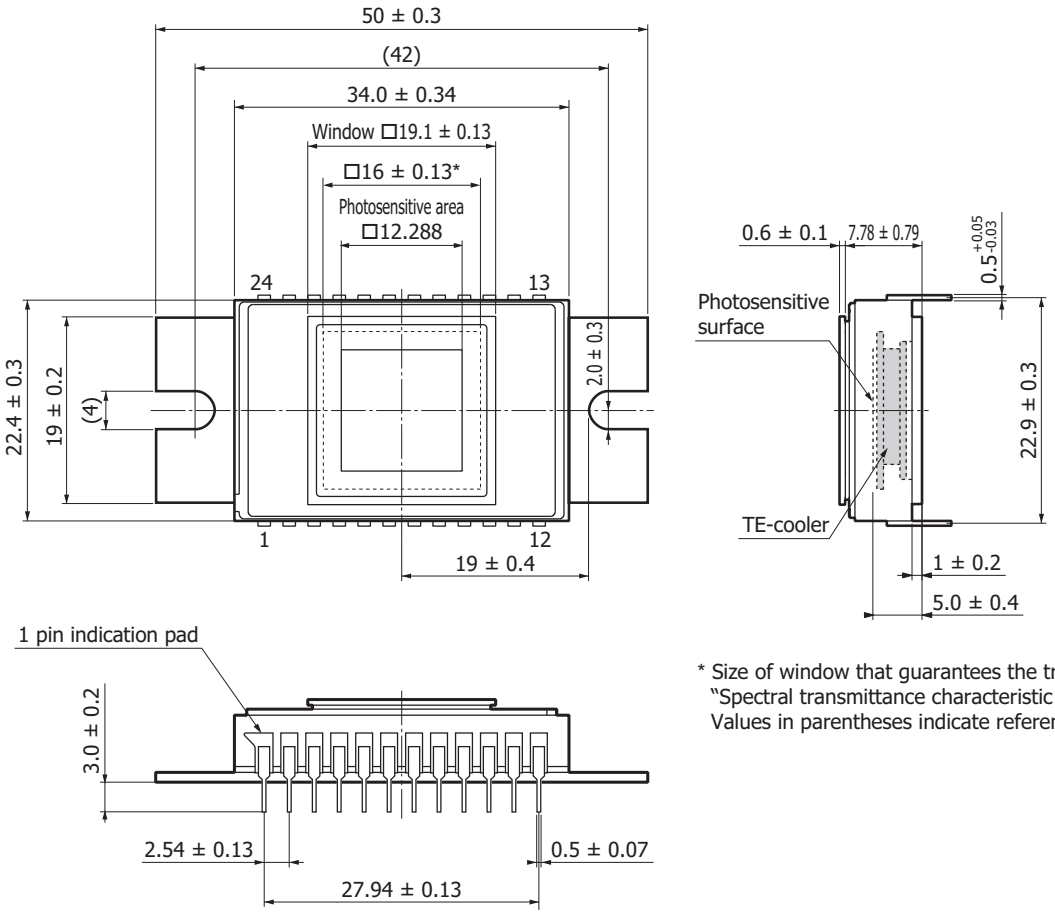
S7171-0909-01



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristic of window material" graph. Values in parentheses indicate reference value.

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Pin connections

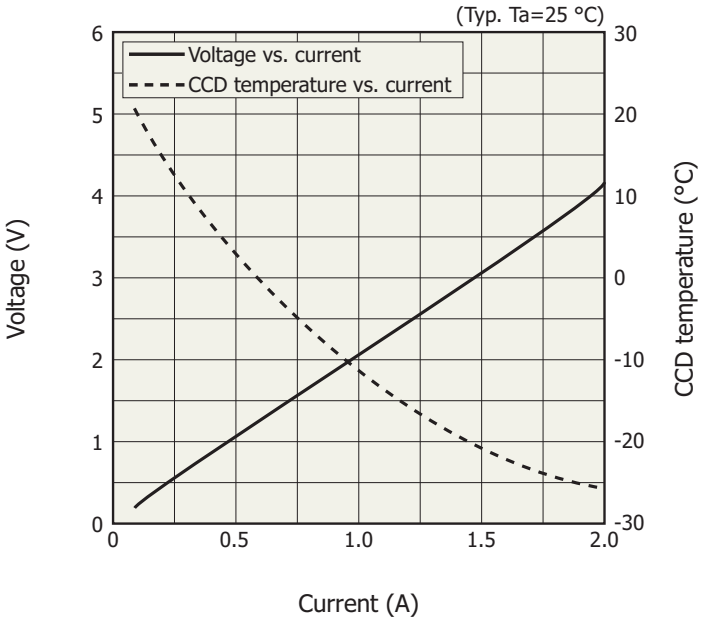
Pin no.	S7170-0909		S7171-0909-01		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	R_L=22 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+20 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same pulse as P2H
6	-		-		
7	-		-		
8	P2H	Horizontal shift register clock-2	P2H	Horizontal shift register clock-2	
9	P1H	Horizontal shift register clock-1	P1H	Horizontal shift register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG*16	Transfer gate	TG*16	Transfer gate	Same pulse as P2V
14	P2V	Vertical shift register clock-2	P2V	Vertical shift register clock-2	
15	P1V	Vertical shift register clock-1	P1V	Vertical shift register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-8 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-8 V
24	RG	Reset gate	RG	Reset gate	

*16: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Specifications of built-in TE-cooler (S7171-0909-01)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=25 °C	-	2.1	-	Ω
Maximum current*17	Imax	Tc*18=Th*19=25 °C	-	-	2.0	A
Maximum voltage	Vmax	Tc*18=Th*19=25 °C	-	-	4.2	V
Maximum heat absorption*20	Qmax		-	-	4.5	W
Maximum temperature of heat radiating side	-		-	-	70	°C

*17: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*18: Temperature of the cooling side of thermoelectric cooler
*19: Temperature of the heat radiating side of thermoelectric cooler
*20: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.



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Specifications of built-in temperature sensor (S7171-0909-01)

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: resistance at absolute temperature T1 [K]

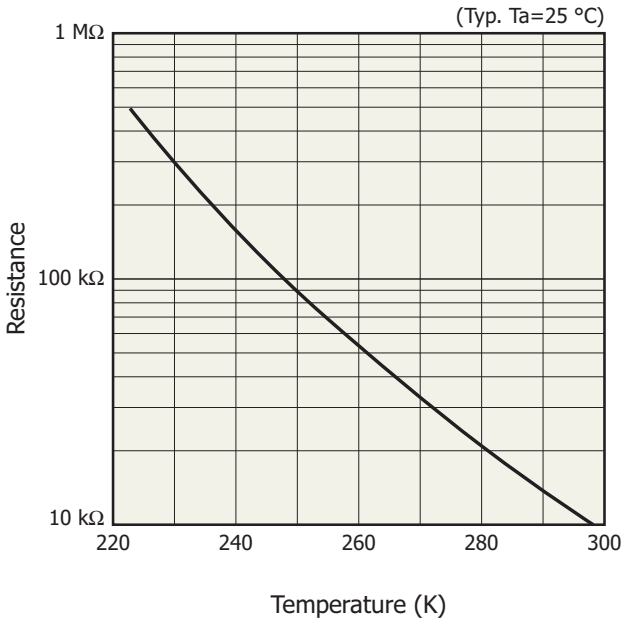
R_{T2}: resistance at absolute temperature T2 [K]

$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.

R_{298}=10 kΩ

$B_{298/323}$=3450 K



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Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

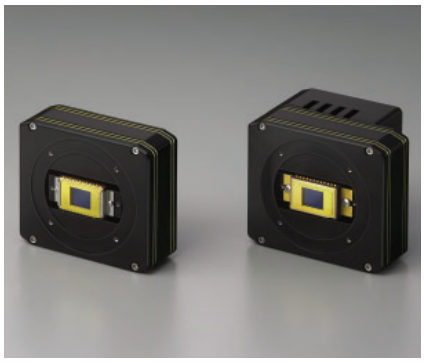
It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Element cooling/heating temperature gradient rate

When using an external cooler, the element cooling/heating temperature gradient rate should be set at less than 5 K/min.

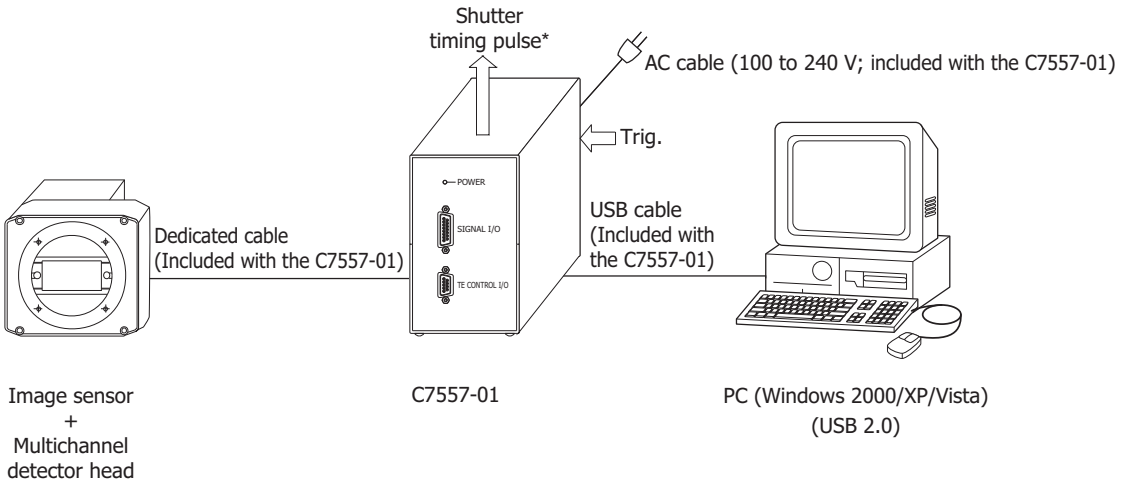
Multichannel detector heads (C7180, C7181)

Features



- **Designed for back-thinned CCD area image sensor**
  C7180: for non-cooled type (S7170-0909)
  C7181: for TE-cooled type (S7171-0909-01)
- **Choice of line binning operation/area scanning operation**
- **Built-in driver circuit**
- **Highly stable temperature controller (C7181)**
  Cooling temperature: fixed at Ts=-10 ± 0.05 °C
- **Operates with simple input signals**
- **High UV sensitivity and high quantum efficiency**
- **Compact configuration**

Connections to multichannel detector head and PC



* Shutter, etc. are not available.

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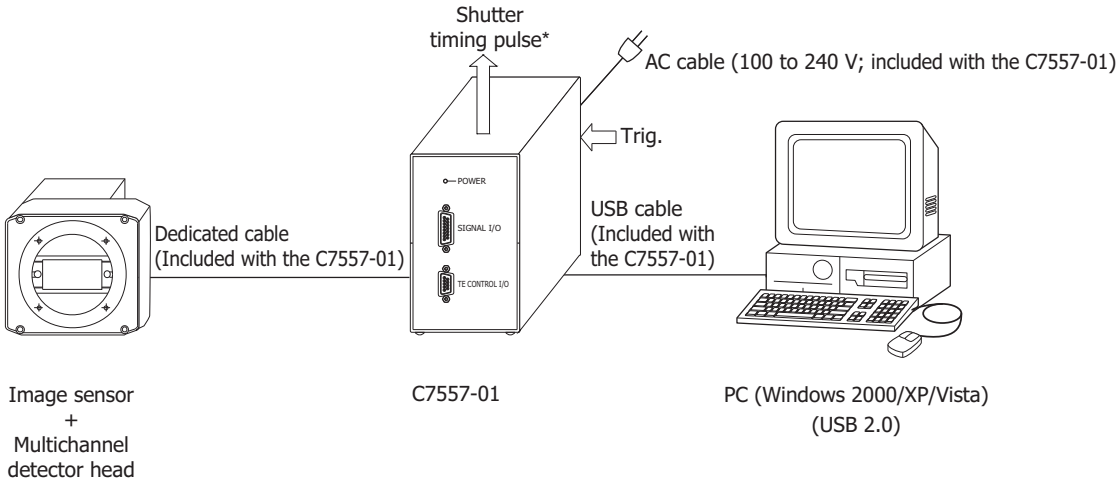
Multichannel detector head controller C7557-01

Features

- **For control of multichannel detector head and data acquisition**
- **Easy control and data acquisition using supplied software via USB interface**

Connection example



* Shutter, etc. are not available.

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