

**CMOS 8-bit Single Chip Microcomputer**

**Description**

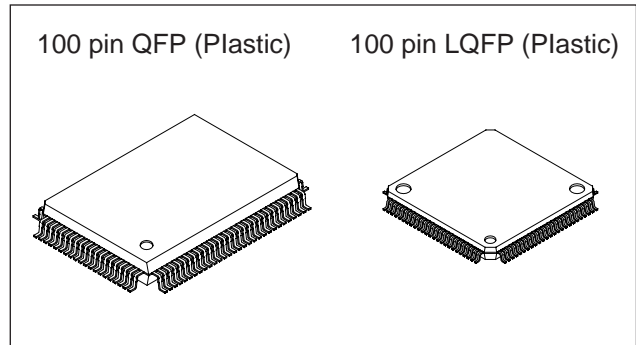
The CXP819P60M is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, 32kHz timer/event counter, remote control receiving circuit, general purpose prescaler, and external signal, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP819P60M provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.

This IC is the PROM-incorporated version of the CXP81960M with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

**Features**

- A wide instruction set (213 instructions) which cover various types of data
  - 16-bit operation/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
  - 250ns at 16MHz operation (4.5 to 5.5V)
  - 333ns at 12MHz operation (2.7 to 5.5V)
  - 122µs at 32kHz operation
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 2048 bytes
- Peripheral functions
  - A/D converter 8-bit, 12-channel, successive approximation system (Conversion time 20.0µs/16MHz)
  - Serial Interface Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel  
Incorporated 8-bit and 8-stage FIFO for data (1 to 8 bytes auto transfer) 1-channel
  - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
  - High precision timing pattern generator PPG 19-pin 32-stage programmable  
RTG 5-pin 2-channel
  - PWM/DA gate output PWM 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)  
DA gate pulse output 13-bit, 4-channel
  - FRC capture unit Incorporated 26-bit and 8-stage FIFO
  - PWM output 14-bit, 1-channel
  - Remote control receiving circuit 8-bit pulse measurement counter with on-chip, 6-stage FIFO
  - General purpose prescaler 7-bit (PG5 input frequency divided, FRC capture possible)
- Interruption 20 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin plastic QFP/LQFP

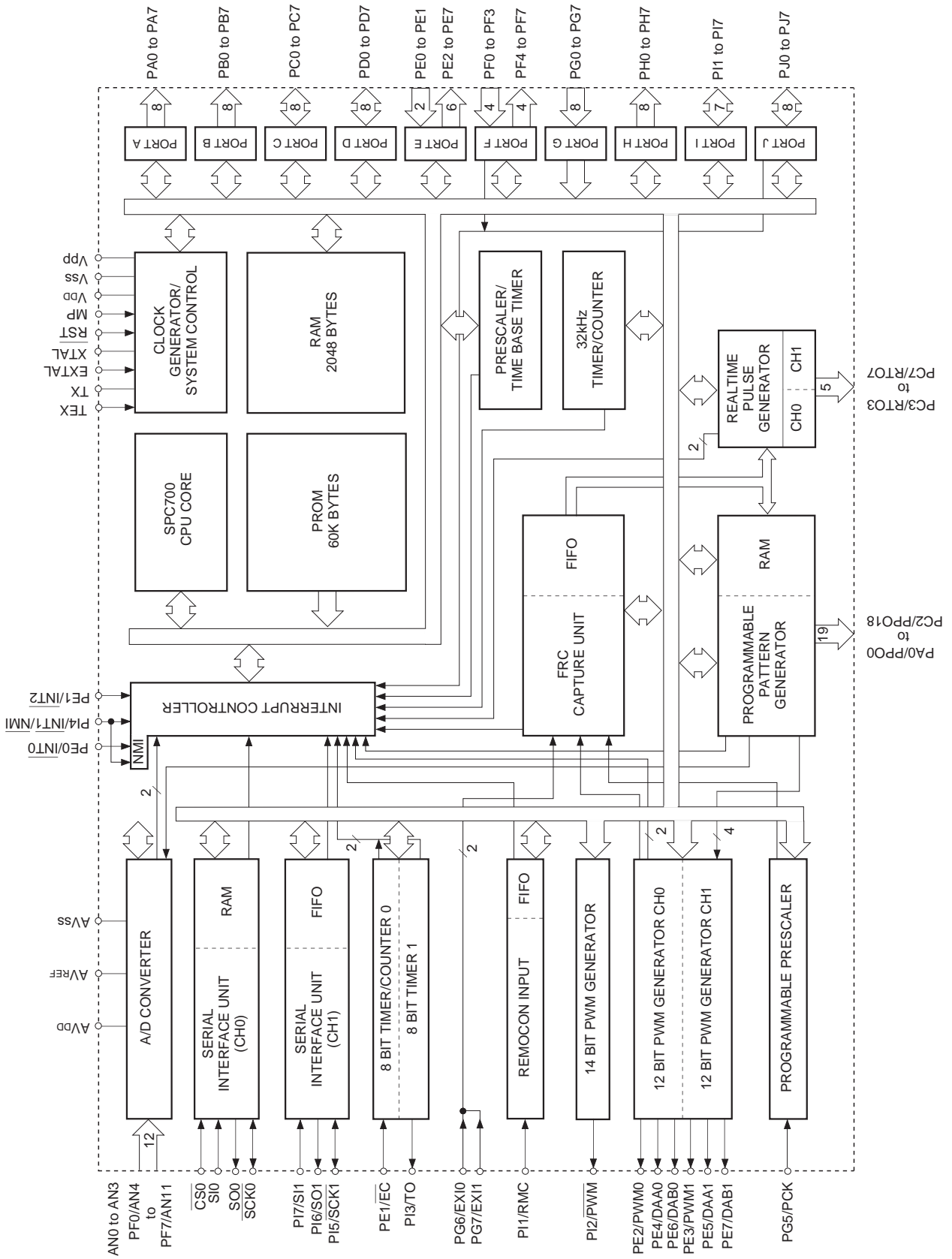


**Structure**

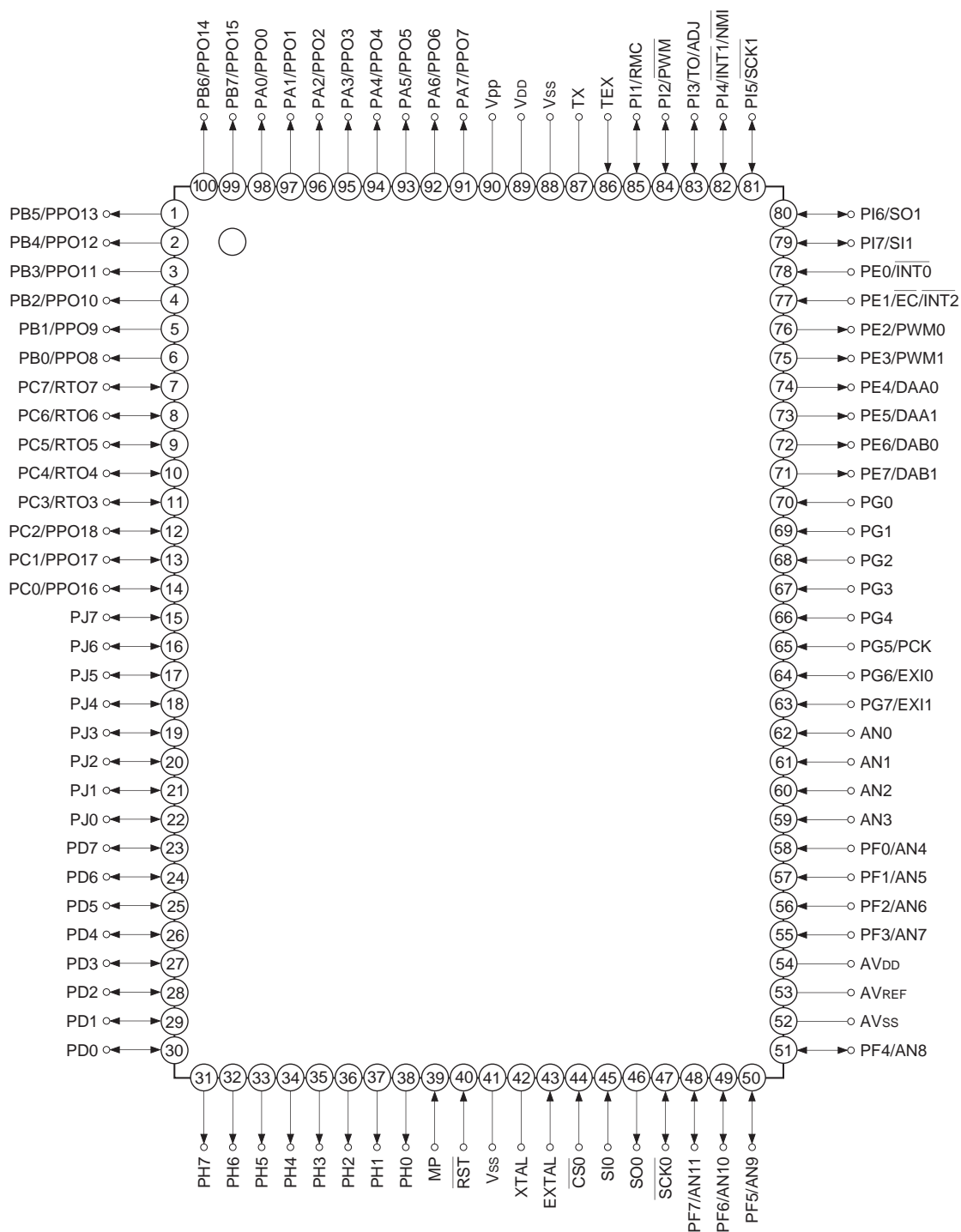
Silicon gate CMOS IC

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Block Diagram

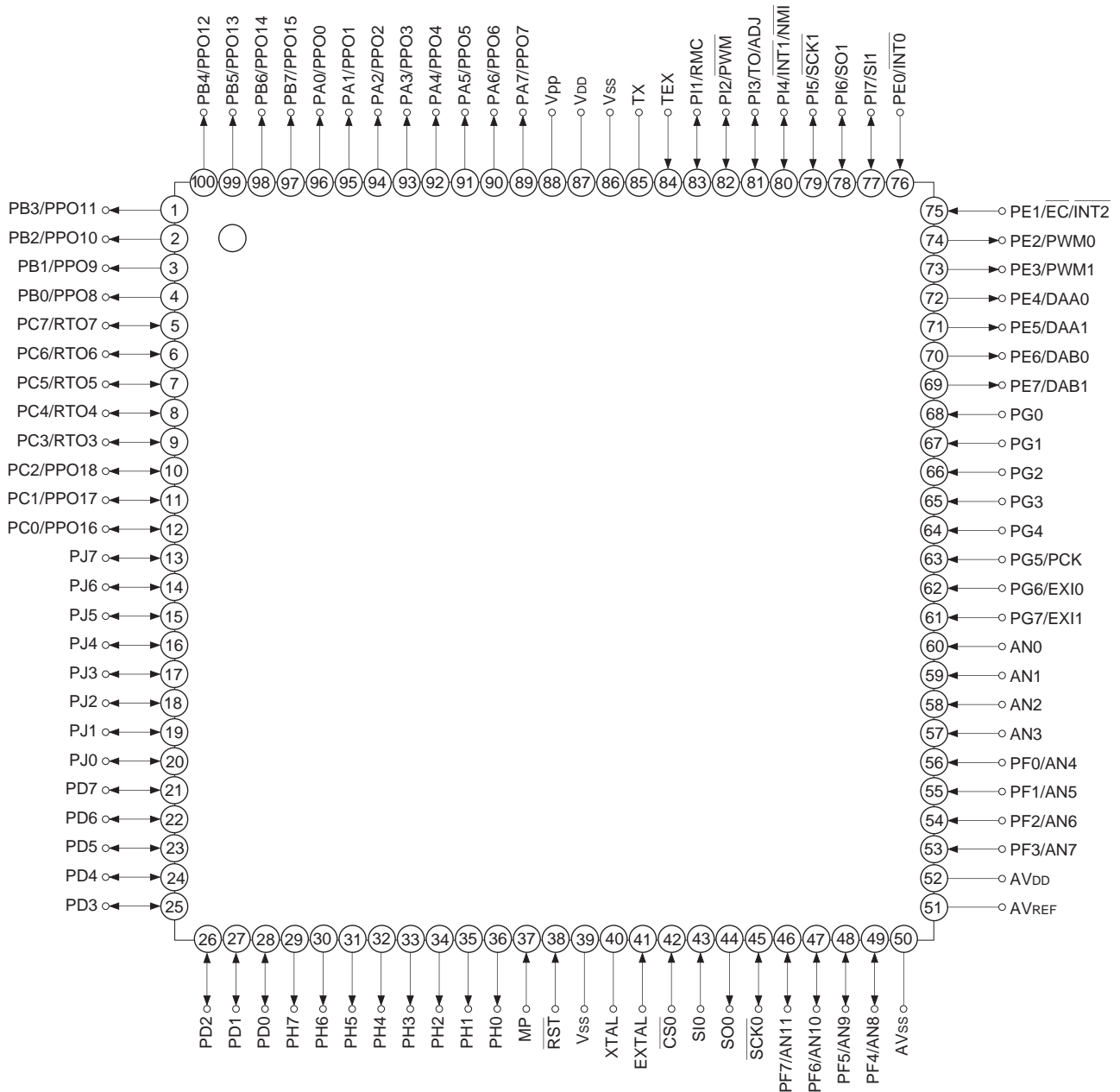


Pin Configuration 1 (Top View) 100-pin QFP package



- Note**
1. Vpp (Pin 90) is always connected to VDD.
  2. Vss (Pins 41 and 88) are both connected to GND.
  3. MP (Pin 39) is always connected to GND.

Pin Configuration 2 (Top View) 100-pin LQFP package



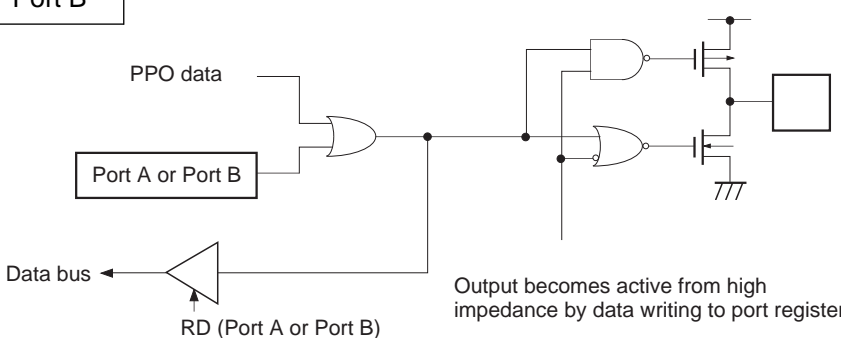
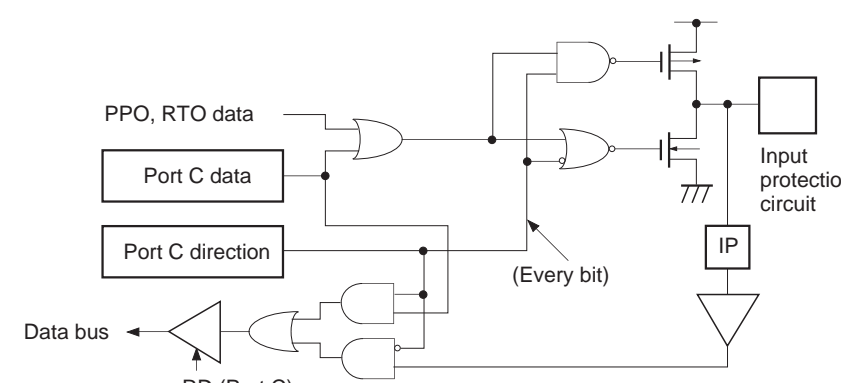
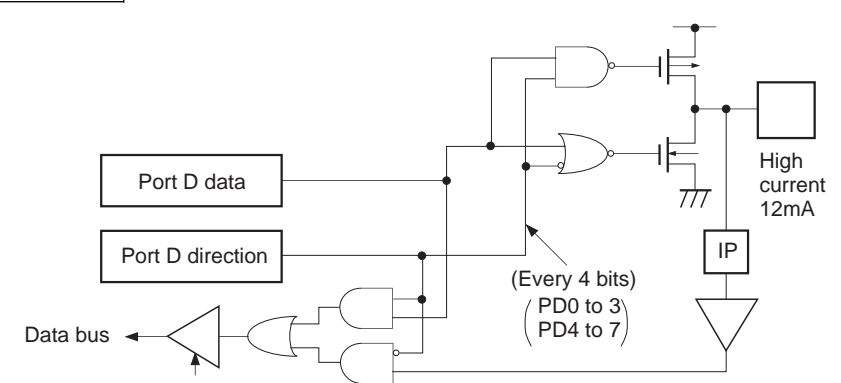
- Note** 1. Vpp (Pin 88) is always connected to VDD.  
 2. Vss (Pins 39 and 86) are both connected to GND.  
 3. MP (Pin 37) is always connected to GND.

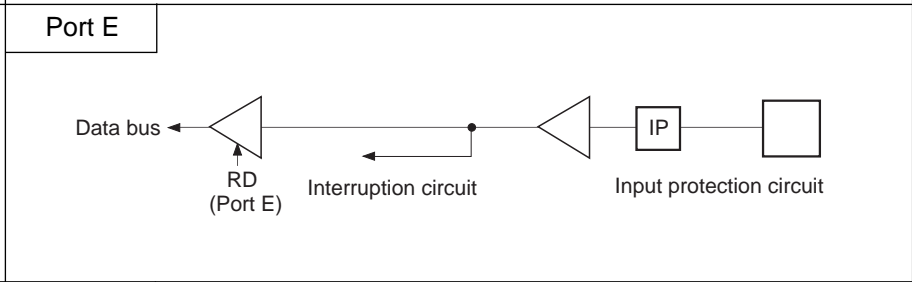
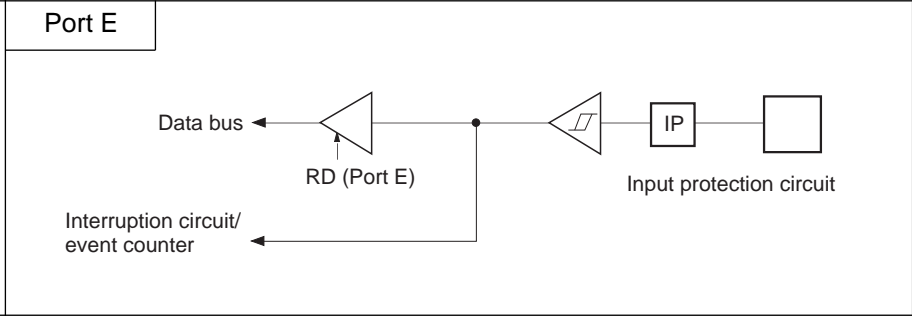
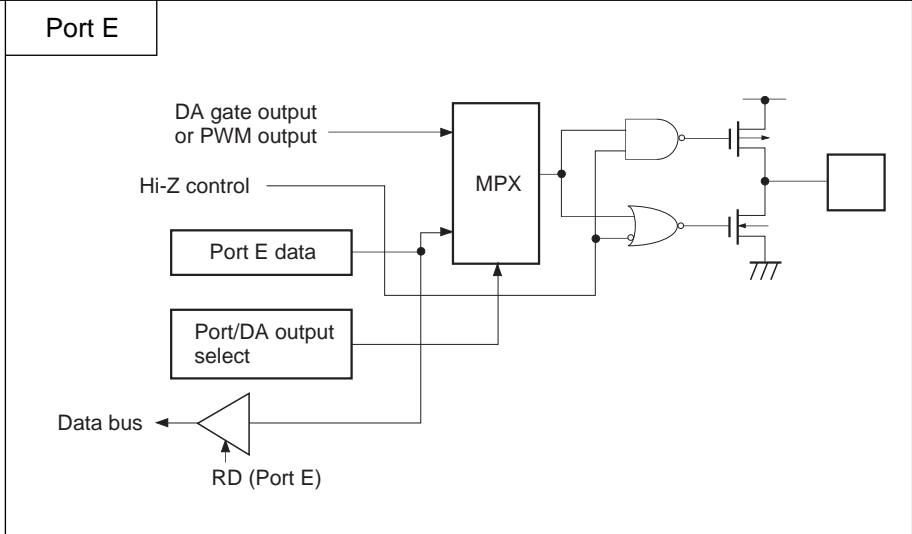
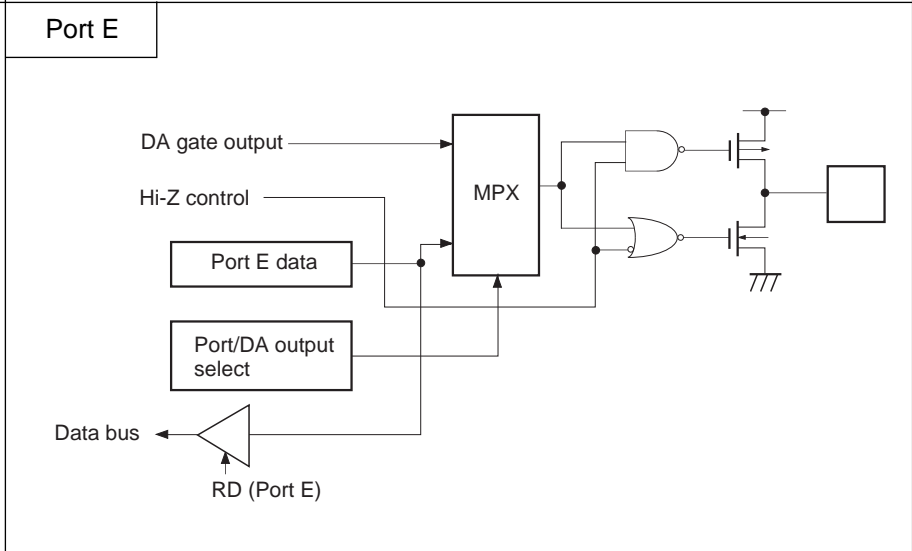
## Pin Description

| Symbol   | I/O                            | Description  |   |   |
|--|--------------------------------|--|---|---|
| PA0/PPO0<br>to<br>PA7/PPO7                         | Output/<br>Real time<br>output | (Port A)<br>8-bit output port. Data is<br>gated with PPO contents by<br>OR-gate and they are output.<br>(8 pins)   | Programmable pattern generator (PPG)<br>output.<br>Functions as high precision real time<br>pulse output port.<br>(19 pins) |   |
| PB0/PPO8<br>to<br>PB7/PPO15                        | Output/<br>Real time<br>output | (Port B)<br>8-bit output port. Data is<br>gated with PPO contents by<br>OR-gate and they are output.<br>(8 pins)   |   |   |
| PC0/PPO16<br>to<br>PC2/PPO18                       | I/O/<br>Real time<br>output    | (Port C)<br>8-bit I/O port, enables to<br>specify I/O by bit unit.<br>Data is gated with PPO or<br>RTO contents by OR-gate<br>and they are output.<br>(8 pins) |   |   |
| PC3/RTO3<br>to<br>PC7/RTO7                         | I/O/<br>Real time<br>output    |  | Real time pulse generator (RTG) output.<br>Functions as high precision real time<br>pulse output port. (5 pins)             |   |
| PD0 to PD7   | I/O                            | (Port D)<br>8-bit I/O port. Enable to specify I/O by 4-bit unit.<br>Enables to drive 12mA sink current.<br>(8 pins)  |   |   |
| PE0/ $\overline{\text{INT0}}$                      | Input/Input                    | (Port E)<br>8-bit port.<br>Lower 2 bits<br>are input pins<br>and upper 6<br>bits are output<br>pins.<br>(8 pins)   | Input pin to request external interruption.<br>Active when falling edge.  |   |
| PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$ | Input/Input/Input              |  | External event input<br>pin for timer/counter.  | Input pin to request<br>external interruption.<br>Active when falling edge. |
| PE2/PWM0   | Output/Output                  |  | Pulse width modulation (PWM) output pins.<br>(2 pins)   |   |
| PE3/PWM1   | Output/Output                  |  |   |   |
| PE4/DAA0   | Output/Output                  |  |   | DA gate pulse output pins.<br>(4 pins)                                      |
| PE5/DAA1   | Output/Output                  |  |   |   |
| PE6/DAB0   | Output/Output                  |  |   |   |
| PE7/DAB1   | Output/Output                  |  |   |   |
| AN0 to AN3   | Input                          | Analog input pins to A/D converter. (12 pins)  |   |   |
| PF0/AN4<br>to<br>PF3/AN7                           | Input/Input                    | (Port F)<br>Lower 4 bits are input port and upper 4 bits are output port.<br>Lower 4 bits also serve as standby release input pin.<br>(8 pins)                 |   |   |
| PF4/AN8<br>to<br>PF7/AN11                          | Output/Input                   |  |   |   |
| $\overline{\text{SCK0}}$                           | I/O                            | Serial clock (CH0) I/O pin.  |   |   |
| SO0  | Output                         | Serial data (CH0) output pin.  |   |   |
| SI0  | Input                          | Serial data (CH0) input pin.   |   |   |
| $\overline{\text{CS0}}$                            | Input                          | Serial chip select (CH0) input pin.  |   |   |

| Symbol           | I/O               | Description   |   |
|------------------|-------------------|---|---|
| PG0 to PG4       | Input             | (Port G)<br>8-bit input port.<br>(8 pins)   |   |
| PG5/PCK          |                   |   | 7 bit general purpose prescaler input pin.  |
| PG6/EXI0         |                   |   | External input pin to FRC capture unit.   |
| PG7/EXI1         |                   |   |   |
| PH0 to PH7       | Output            | (Port H)<br>8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output.<br>(8 pins)   |   |
| PI1/RMC          | I/O/Input         | (Port I)<br>7-bit I/O port.<br>I/O port can be specified by bit unit.<br>(7 pins)   | Remote control receiving circuit input pin.   |
| PI2/PWM          | I/O/Output        |   | 14-bit PWM output pin.  |
| PI3/TO/ADJ       | I/O/Output/Output |   | Timer/counter, 32kHz oscillation adjustment output pin.   |
| PI4/INT1/<br>NMI | I/O/Input/Input   |   | Input pin to request external interruption and non-maskable interruption. Active when falling edge.                           |
| PI5/SCK1         | I/O/I/O           |   | Serial clock (CH1) I/O pin.   |
| PI6/SO1          | I/O/Output        |   | Serial data (CH1) output pin.   |
| PI7/SI1          | I/O/Input         |   | Serial data (CH1) input pin.  |
| PJ0 to PJ7       | I/O               |   | (Port J)<br>8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit. |
| EXTAL            | Input             | Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin. |   |
| XTAL             | Output            |   |   |
| TEX              | Input             | Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)         |   |
| TX               | Output            |   |   |
| RST              | Input             | System reset pin of active "L" level.   |   |
| MP               | Input             | Microprocessor mode input pin. Always connect to GND.   |   |
| AVDD             |                   | Positive power supply pin of A/D converter.   |   |
| AVREF            | Input             | Reference voltage input pin of A/D converter.   |   |
| AVSS             |                   | GND pin of A/D converter.   |   |
| VDD              |                   | Positive power supply pin.  |   |
| Vpp              |                   | Positive power supply pin for built-in PROM writing. Please connect to VDD for normal operation.  |   |
| Vss              |                   | GND pin. Connect both Vss pins to GND.  |   |

Input/Output Circuit Formats for Pins

| Pin   | Circuit format  | When reset  |
|---|---|-------------|
| <p>PA0/PPO0 to PA7/PPO7</p> <p>PB0/PPO8 to PB7/PPO15</p> <p>16 pins</p> | <p>Port A</p> <p>Port B</p>  <p>Output becomes active from high impedance by data writing to port register.</p> | <p>Hi-Z</p> |
| <p>PC0/PPO16 to PC2/PPO18</p> <p>PC3/RTO3 to PC7/RTO7</p> <p>8 pins</p> | <p>Port C</p>  <p>(Every bit)</p>  | <p>Hi-Z</p> |
| <p>PD0 to PD7</p> <p>8 pins</p>   | <p>Port D</p>  <p>(Every 4 bits)<br/>(PD0 to 3)<br/>(PD4 to 7)</p>  | <p>Hi-Z</p> |

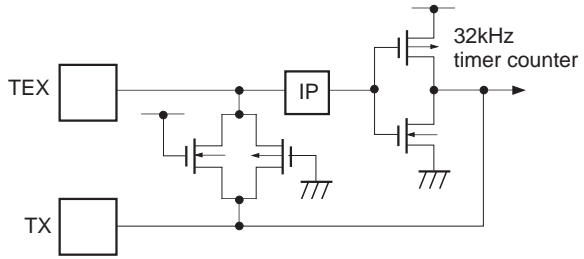
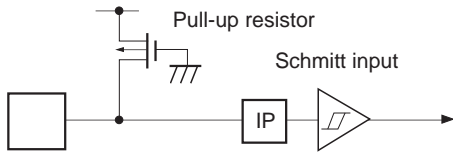
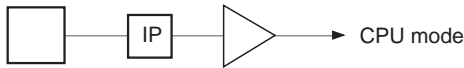
| Pin  | Circuit format  | When reset     |
|--|---|----------------|
| <p>PE0/<math>\overline{\text{INT0}}</math></p> <p>1 pin</p>                      | <p>Port E</p>  <p>Data bus</p> <p>RD (Port E)</p> <p>Interruption circuit</p> <p>Input protection circuit</p>   | <p>Hi-Z</p>    |
| <p>PE1/<math>\overline{\text{EC}}/\overline{\text{INT2}}</math></p> <p>1 pin</p> | <p>Port E</p>  <p>Data bus</p> <p>RD (Port E)</p> <p>Interruption circuit/<br/>event counter</p> <p>Input protection circuit</p>  | <p>Hi-Z</p>    |
| <p>PE2/PWM0<br/>PE3/PWM1<br/>PE4/DAA0<br/>PE5/DAA1</p> <p>4 pins</p>             | <p>Port E</p>  <p>DA gate output<br/>or PWM output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output<br/>select</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p> | <p>Hi-Z</p>    |
| <p>PE6/DAB0<br/>PE7/DAB1</p> <p>2 pins</p>                                       | <p>Port E</p>  <p>DA gate output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output<br/>select</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p>                  | <p>H level</p> |



| Pin                             | Circuit format                         | When reset |
|---------------------------------|--|------------|
| AN0 to AN3<br>4 pins            | <p>Input multiplexer</p>               | Hi-Z       |
| PF0/AN4 to PF3/AN7<br>4 pins    | <p>Port F</p> <p>Input multiplexer</p> | Hi-Z       |
| PF4/AN8 to PF7/AN11<br>4 pins   | <p>Port F</p>                          | Hi-Z       |
| PG0 to PG4<br>PG5/PCK<br>6 pins | <p>Port G</p> <p>Schmitt input</p>     | Hi-Z       |
| PG6/EXI0<br>PG7/EXI1<br>2 pins  | <p>Port G</p> <p>Schmitt input</p>     | Hi-Z       |
| PH0 to PH7<br>8 pins            | <p>Port H</p>                          | Hi-Z       |

| Pin   | Circuit format  | When reset  |
|---|---|-------------|
| <p>PI2/PWM<br/>PI3/TO/ADJ</p> <p>2 pins</p>               | <p>Port I</p> <p>( PI2 ... From 14-bit PWM<br/>PI3 ... From timer/counter,<br/>32kHz timer</p> <p>Port I function select</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>IP</p>   | <p>Hi-Z</p> |
| <p>PI1/RMC<br/>PI4/INT1/NMI<br/>PI7/SI1</p> <p>3 pins</p> | <p>Port I</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>( PI1 ... To remote control circuit<br/>PI4 ... To interruption circuit<br/>PI7 ... To serial CH1</p>   | <p>Hi-Z</p> |
| <p>PI5/SCK1<br/>PI6/SO1</p> <p>2 pins</p>                 | <p>Port I</p> <p>Port I function select</p> <p>From serial CH1</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>Note)<br/>(PI5 is schmitt input<br/>PI6 is inverter input)</p> <p>To serial CH1</p> <p>IP</p> | <p>Hi-Z</p> |

| Pin   | Circuit format   | When reset         |
|---|--|--------------------|
| <p>PJ0 to PJ7</p> <p>8 pins</p>                                 |  | <p>Hi-Z</p>        |
| <p><math>\overline{\text{CS0}}</math><br/>SIO</p> <p>2 pins</p> |  | <p>Hi-Z</p>        |
| <p>SO0</p> <p>1 pin</p>   |  | <p>Hi-Z</p>        |
| <p><math>\overline{\text{SCK0}}</math></p> <p>1 pin</p>         |  | <p>Hi-Z</p>        |
| <p>EXTAL<br/>XTAL</p> <p>2 pins</p>                             | <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul> | <p>Oscillation</p> |

| Pin  | Circuit format  | When reset         |
|--|---|--------------------|
| <p>TEX<br/>TX</p> <p>2 pins</p>                        |  <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.</li> </ul> | <p>Oscillation</p> |
| <p><math>\overline{\text{RST}}</math></p> <p>1 pin</p> |   | <p>L level</p>     |
| <p>MP</p> <p>1 pin</p>                                 |   | <p>Hi-Z</p>        |

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

| Item                            | Symbol            | Rating                                 | Unit | Remarks  |
|---------------------------------|-------------------|--|------|--|
| Supply voltage                  | V <sub>DD</sub>   | -0.3 to +7.0                           | V    |  |
|                                 | V <sub>pp</sub>   | -0.3 to +13                            | V    | On-chip PROM power supply                      |
|                                 | AV <sub>DD</sub>  | AV <sub>SS</sub> to +7.0* <sup>1</sup> | V    |  |
|                                 | AV <sub>SS</sub>  | -0.3 to +0.3                           | V    |  |
| Input voltage                   | V <sub>IN</sub>   | -0.3 to +7.0* <sup>2</sup>             | V    |  |
| Output voltage                  | V <sub>OUT</sub>  | -0.3 to +7.0* <sup>2</sup>             | V    |  |
| Medium withstand output voltage | V <sub>OUTP</sub> | -0.3 to +15.0                          | V    | PH pin   |
| High level output current       | I <sub>OH</sub>   | -5                                     | mA   |  |
| High level total output current | ΣI <sub>OH</sub>  | -50                                    | mA   | Total of output pins                           |
| Low level output current        | I <sub>OL</sub>   | 15                                     | mA   | Other than large current output pins: per pin  |
|                                 | I <sub>OLC</sub>  | 20                                     | mA   | Large current port pin* <sup>3</sup> : per pin |
| Low level total output current  | ΣI <sub>OL</sub>  | 130                                    | mA   | Total of output pins                           |
| Operating temperature           | T <sub>opr</sub>  | -10 to +75                             | °C   |  |
| Storage temperature             | T <sub>stg</sub>  | -55 to +150                            | °C   |  |
| Allowable power dissipation     | P <sub>D</sub>    | 600                                    | mW   | QFP package type                               |
|                                 |                   | 380                                    |      | LQFP package type                              |

\*<sup>1</sup> AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*<sup>2</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*<sup>3</sup> The large current operation transistors are the N-CH transistors of the PD and PH ports.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

| Item                     | Symbol            | Min.                  | Max.                  | Unit                              | Remarks  |
|--------------------------|-------------------|-----------------------|-----------------------|-----------------------------------|--|
| Supply voltage           | V <sub>DD</sub>   | 2.7                   | 5.5                   | V                                 | Guaranteed range during high speed mode (1/2 dividing clock) operation |
|                          |                   | 2.7                   | 5.5                   | V                                 | Guaranteed range during low speed mode (1/16 dividing clock) operation |
|                          |                   | 2.5                   | 5.5                   | V                                 | Guaranteed operation range by TEX clock                                |
|                          |                   | 2.0                   | 5.5                   | V                                 | Guaranteed data hold operation range during STOP                       |
| Analog power supply      | AV <sub>DD</sub>  | 3.0                   | 5.5                   | V                                 | *1   |
| High level input voltage | V <sub>IH</sub>   | 0.7V <sub>DD</sub>    | V <sub>DD</sub>       | V                                 | *2   |
|                          | V <sub>IHS</sub>  | 0.8V <sub>DD</sub>    | V <sub>DD</sub>       | V                                 | CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin             |
|                          |                   |                       | 5.5                   | V                                 | CMOS schmitt input*6   |
|                          | V <sub>IHEX</sub> | V <sub>DD</sub> - 0.4 | V <sub>DD</sub> + 0.3 | V                                 | EXTAL pin*4, *7 and TEX pin*5, *7                                      |
| V <sub>DD</sub> - 0.2    |                   | V <sub>DD</sub> + 0.2 | V                     | EXTAL pin*4, *8 and TEX pin*5, *8 |  |
| Low level input voltage  | V <sub>IL</sub>   | 0                     | 0.3V <sub>DD</sub>    | V                                 | *2, *7   |
|                          |                   | 0                     | 0.2V <sub>DD</sub>    | V                                 | *2, *8   |
|                          | V <sub>ILS</sub>  | 0                     | 0.2V <sub>DD</sub>    | V                                 | CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin             |
|                          | V <sub>ILEX</sub> | -0.3                  | 0.4                   | V                                 | EXTAL pin*4, *7 and TEX pin*5, *7                                      |
|                          |                   | -0.3                  | 0.2                   | V                                 | EXTAL pin*4, *8 and TEX pin*5, *8                                      |
| Operating temperature    | Topr              | -10                   | +75                   | °C                                |  |

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*2 Normal input port (each pin of PC, PD, PF0 to PF3, PG, PI and PJ), MP pin.

\*3 Each pin of  $\overline{\text{SCK0}}$ ,  $\overline{\text{RST}}$ , PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$ , PI1/RMC, PI4/ $\overline{\text{INT1}}$ / $\overline{\text{NMI}}$ , PI5/ $\overline{\text{SCK1}}$  and PI7/SI1.

\*4 It specifies only when the external clock is input.

\*5 It specifies only when the external event count clock is input.

\*6 Each pin of  $\overline{\text{CS0}}$ , SI0, and PG.

\*7 In case of 4.5 to 5.5V supply voltage (V<sub>DD</sub>).

\*8 In case of 2.7 to 3.3V supply voltage (V<sub>DD</sub>).

## Electrical Characteristics

DC Characteristics ( $V_{DD} = 4.5$  to  $5.5V$ )( $T_a = -10$  to  $+75^\circ C$ ,  $V_{SS} = 0V$ )

| Item   | Symbol   | Pins  | Conditions                                       | Min.                                 | Typ. | Max.     | Unit    |
|--|--|---|--|--------------------------------------|------|----------|---------|
| High level output voltage                                | $V_{OH}$   | PA to PD,<br>PE2 to PE7,<br>PF4 to PF7,<br>PH ( $V_{OL}$ only)                | $V_{DD} = 4.5V$ , $I_{OH} = -0.5mA$              | 4.0                                  |      |          | V       |
|  |  |   | $V_{DD} = 4.5V$ , $I_{OH} = -1.2mA$              | 3.5                                  |      |          | V       |
| Low level output voltage                                 | $V_{OL}$   | PH ( $V_{OL}$ only)<br>PI1 to PI7<br>PJ, SO0, SCK0                            | $V_{DD} = 4.5V$ , $I_{OL} = 1.8mA$               |                                      |      | 0.4      | V       |
|  |  |   | $V_{DD} = 4.5V$ , $I_{OL} = 3.6mA$               |                                      |      | 0.6      | V       |
|  |  | PD, PH  | $V_{DD} = 4.5V$ , $I_{OL} = 12.0mA$              |                                      |      | 1.5      | V       |
| Input current  | $I_{IHE}$  | EXTAL   | $V_{DD} = 5.5V$ , $V_{IH} = 5.5V$                | 0.5                                  |      | 40       | $\mu A$ |
|  | $I_{ILE}$  |   | $V_{DD} = 5.5V$ , $V_{IL} = 0.4V$                | -0.5                                 |      | -40      | $\mu A$ |
|  | $I_{IHT}$  | TEX   | $V_{DD} = 5.5V$ , $V_{IH} = 5.5V$                | 0.1                                  |      | 10       | $\mu A$ |
|  | $I_{ILT}$  |   | $V_{DD} = 5.5V$ ,<br>$V_{IL} = 0.4V$             | -0.1                                 |      | -10      | $\mu A$ |
|  | $I_{ILR}$  |   | $\overline{RST}$                                 | $V_{DD} = 5.5V$ ,<br>$V_{IL} = 0.4V$ | -1.5 |          | -400    |
| I/O leakage current                                      | $I_{IZ}$   | PA to PG,<br>PI, PJ, MP<br>AN0 to AN3,<br>$\overline{CS0}$ , SI0, SO0<br>SCK0 | $V_{DD} = 5.5V$ ,<br>$V_I = 0, 5.5V$             |                                      |      | $\pm 10$ | $\mu A$ |
| Open drain output leakage current (N-CH Tr OFF in state) | $I_{LOH}$  | PH  | $V_{DD} = 5.5V$<br>$V_{OH} = 12V$                |                                      |      | 50       | $\mu A$ |
| Supply current*1   | $I_{DD1}$  | $V_{DD}$  | 16MHz crystal oscillation ( $C_1 = C_2 = 15pF$ ) |                                      | 28   | 50       | mA      |
|  |  |   | $V_{DD} = 5V \pm 0.5V^{*2}$                      |                                      |      |          |         |
|  | $I_{DDS1}$   |   | SLEEP mode                                       |                                      | 1.7  | 8        | mA      |
|  |  |   | $V_{DD} = 5V \pm 0.5V$                           |                                      |      |          |         |
|  | $I_{DD2}$  |   | 32kHz crystal oscillation ( $C_1 = C_2 = 47pF$ ) |                                      | 0.6  | 1.8      | mA      |
|  |  |   | $V_{DD} = 2.75V \pm 0.25V$                       |                                      |      |          |         |
|  | $I_{DDS2}$   |   | SLEEP mode                                       |                                      | 7    | 30       | $\mu A$ |
| $V_{DD} = 2.75V \pm 0.25V$                               |  |   |  |                                      |      |          |         |
| $I_{DDS3}$   | STOP mode<br>(EXTAL and TEX pins oscillation stop) |   |  |                                      | 30   | $\mu A$  |         |
| $V_{DD} = 5V \pm 0.5V$                                   |  |   |  |                                      |      |          |         |
| Input capacity   | $C_{IN}$   | Other than $V_{DD}$ ,<br>$V_{SS}$ , $AV_{DD}$ , and<br>$AV_{SS}$              | Clock 1MHz<br>0V other than the measured pins    |                                      | 10   | 20       | pF      |

\*1 When entire output pins are open.

\*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

DC Characteristics ( $V_{DD} = 2.7$  to  $3.3V$ )

( $T_a = -10$  to  $+75^\circ C$ ,  $V_{SS} = 0V$ )

| Item                              | Symbol     | Pins  | Conditions  | Min. | Typ. | Max.     | Unit    |
|-----------------------------------|------------|---|---|------|------|----------|---------|
| High level output voltage         | $V_{OH}$   | PA to PD, PE2 to PE7, PF4 to PF7, PH ( $V_{OL}$ only), PI1 to PI7, PJ, SO0, $\overline{SCK0}$ | $V_{DD} = 2.7V$ , $I_{OH} = -0.12mA$  | 2.5  |      |          | V       |
|                                   |            |   | $V_{DD} = 2.7V$ , $I_{OH} = -0.45mA$  | 2.1  |      |          | V       |
| Low level output voltage          | $V_{OL}$   | PA to PD, PE2 to PE7, PF4 to PF7, PH ( $V_{OL}$ only), PI1 to PI7, PJ, SO0, $\overline{SCK0}$ | $V_{DD} = 2.7V$ , $I_{OL} = 1.0mA$  |      |      | 0.25     | V       |
|                                   |            |   | $V_{DD} = 2.7V$ , $I_{OL} = 1.4mA$  |      |      | 0.4      | V       |
|                                   |            |   | $V_{DD} = 2.7V$ , $I_{OL} = 4.5mA$  |      |      | 0.9      | V       |
| Input current                     | $I_{IHE}$  | EXTAL   | $V_{DD} = 3.3V$ , $V_{IH} = 3.3V$   | 0.3  |      | 20       | $\mu A$ |
|                                   | $I_{ILE}$  |   | $V_{DD} = 3.3V$ , $V_{IL} = 0.3V$   | -0.3 |      | -20      | $\mu A$ |
|                                   | $I_{IHT}$  | TEX   | $V_{DD} = 3.3V$ , $V_{IH} = 3.3V$   | 0.1  |      | 10       | $\mu A$ |
|                                   | $I_{ILT}$  |   | $V_{DD} = 3.3V$ , $V_{IL} = 0.3V$   | -0.1 |      | -10      | $\mu A$ |
|                                   | $I_{ILR}$  | $\overline{RST}$  | $V_{DD} = 3.3V$ , $V_{IL} = 0.3V$   | -0.9 |      | -200     | $\mu A$ |
| I/O leakage current               | $I_{IZ}$   | PA to PG, PI, PJ, MP, AN0 to AN3, $\overline{CS0}$ , SI0, SO0, $\overline{SCK0}$              | $V_{DD} = 3.3V$ , $V_I = 0, 3.3V$   |      |      | $\pm 10$ | $\mu A$ |
| Open drain output leakage current | $I_{LOH}$  | PH  | $V_{DD} = 3.3V$ , $V_{OH} = 12V$  |      |      | 50       | $\mu A$ |
| Supply current*1                  | $I_{DD1}$  | $V_{DD}$  | 12MHz crystal oscillation ( $C_1 = C_2 = 15pF$ )<br>$V_{DD} = 3.0V \pm 0.3V^{*2}$ |      | 10   | 30       | mA      |
|                                   | $I_{DDS1}$ |   | SLEEP mode<br>$V_{DD} = 3.0V \pm 0.3V$  |      | 0.7  | 2.5      | mA      |
|                                   | $I_{DDS3}$ |   | STOP mode (EXTAL and TEX pins oscillation stop)<br>$V_{DD} = 3.0V \pm 0.3V$       |      |      | 30       | $\mu A$ |
| Input capacity                    | $C_{IN}$   | Other than $V_{DD}$ , $V_{SS}$ , $AV_{DD}$ , and $AV_{SS}$                                    | Clock 1MHz<br>0V other than the measured pins                                     |      | 10   | 20       | pF      |

\*1 When entire output pins are open.

\*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).



AC Characteristics

(1) Clock timing

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

| Item  | Symbol                 | Pins                   | Conditions  | Min.                            | Max. | Unit          |     |
|---|------------------------|------------------------|---|---------------------------------|------|---------------|-----|
| System clock frequency                      | $f_c$                  | XTAL<br>EXTAL          | Fig. 1,<br>Fig. 2   | $V_{DD} = 4.5$ to $5.5\text{V}$ | 1    | 16            | MHz |
|   |                        |                        |   |                                 | 1    | 12            |     |
| System clock input pulse width              | $t_{XL}$ ,<br>$t_{XH}$ | XTAL<br>EXTAL          | Fig. 1,<br>Fig. 2 (External clock drive)                                  | $V_{DD} = 4.5$ to $5.5\text{V}$ | 28   |               | ns  |
|   |                        |                        |   |                                 | 37.5 |               |     |
| System clock input rise and fall times      | $t_{CR}$ ,<br>$t_{CF}$ | XTAL<br>EXTAL          | Fig. 1, Fig. 2<br>(External clock drive)                                  |                                 | 200  | ns            |     |
| Event count clock input pulse width         | $t_{EH}$ ,<br>$t_{EL}$ | $\overline{\text{EC}}$ | Fig. 3  | $t_{\text{sys}} \times 4^*$     |      | ns            |     |
| Event count clock input rise and fall times | $t_{ER}$ ,<br>$t_{EF}$ | $\overline{\text{EC}}$ | Fig. 3  |                                 | 20   | ns            |     |
| System clock frequency                      | $f_c$                  | TEX<br>TX              | Fig. 2 $V_{DD} = 2.5$ to $5.5\text{V}$<br>(32kHz clock applied condition) | 32.768                          |      | kHz           |     |
| Event count clock input pulse width         | $t_{TL}$ ,<br>$t_{TH}$ | TEX                    | Fig. 3  | 10                              |      | $\mu\text{s}$ |     |
| Event count clock input rise and fall times | $t_{TR}$ ,<br>$t_{TF}$ | TEX                    | Fig. 3  |                                 | 20   | ms            |     |

\*  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/f_c \text{ (Upper 2 bits = "00")}, 4000/f_c \text{ (Upper 2 bits = "01")}, 16000/f_c \text{ (Upper 2 bits = "11")}$$

Fig. 1. Clock timing

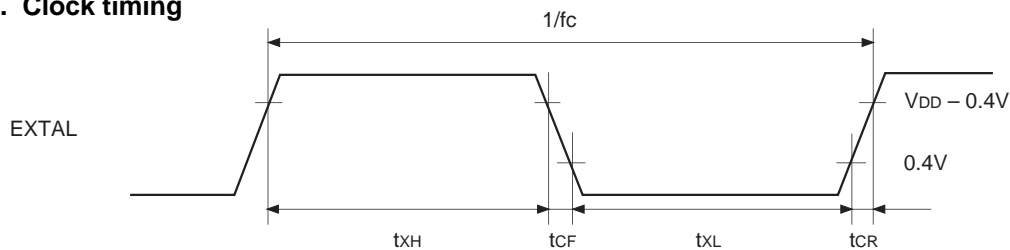


Fig. 2. Clock applied condition

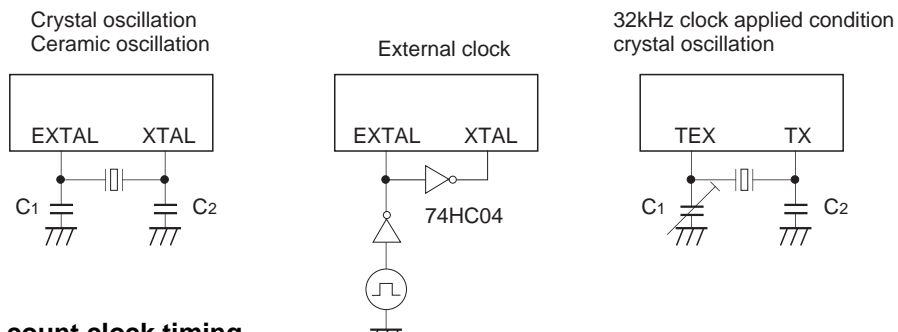
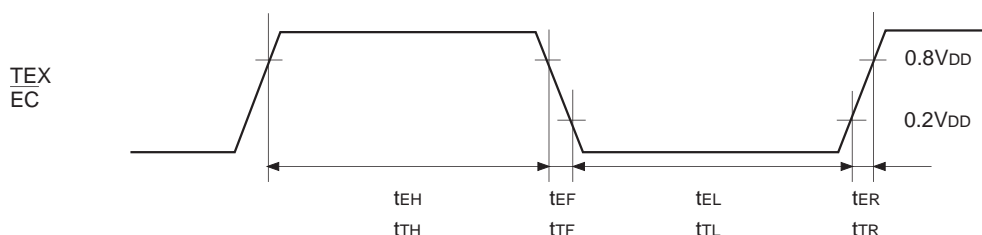


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

| Item   | Symbol               | Pin               | Condition  | Min.             | Max.             | Unit |
|--|----------------------|-------------------|--|------------------|------------------|------|
| $\overline{CS} \downarrow \rightarrow \overline{SCK}$<br>delay time        | $t_{DCSK}$           | $\overline{SCK0}$ | Chip select transfer mode<br>( $\overline{SCK}$ = output mode) |                  | $t_{sys} + 200$  | ns   |
| $\overline{CS} \uparrow \rightarrow \overline{SCK}$<br>floating delay time | $t_{DCSKF}$          | $\overline{SCK0}$ | Chip select transfer mode<br>( $\overline{SCK}$ = output mode) |                  | $t_{sys} + 200$  | ns   |
| $\overline{CS} \downarrow \rightarrow SO$<br>delay time                    | $t_{DCSO}$           | SO0               | Chip select transfer mode                                      |                  | $t_{sys} + 200$  | ns   |
| $\overline{CS} \downarrow \rightarrow SO$<br>floating delay time           | $t_{DCSOF}$          | SO0               | Chip select transfer mode                                      |                  | $t_{sys} + 200$  | ns   |
| $\overline{CS}$<br>high level width  | $t_{WHCS}$           | $\overline{CS0}$  | Chip select transfer mode                                      | $t_{sys} + 200$  |                  | ns   |
| $\overline{SCK}$<br>cycle time   | $t_{KCY}$            | $\overline{SCK0}$ | Input mode   | $2t_{sys} + 200$ |                  | ns   |
|  |                      |                   | Output mode  | $16000/fc$       |                  | ns   |
| $\overline{SCK}$<br>high and low level widths                              | $t_{KH}$<br>$t_{KL}$ | $\overline{SCK0}$ | Input mode   | $t_{sys} + 100$  |                  | ns   |
|  |                      |                   | Output mode  | $8000/fc - 100$  |                  | ns   |
| SI input setup time<br>(against $\overline{SCK} \uparrow$ )                | $t_{SIK}$            | SI0               | $\overline{SCK}$ input mode                                    | $-t_{sys} + 100$ |                  | ns   |
|  |                      |                   | $\overline{SCK}$ output mode                                   | 200              |                  | ns   |
| SI input hold time<br>(against $\overline{SCK} \uparrow$ )                 | $t_{KSI}$            | SI0               | $\overline{SCK}$ input mode                                    | $2t_{sys} + 100$ |                  | ns   |
|  |                      |                   | $\overline{SCK}$ output mode                                   | 100              |                  | ns   |
| $\overline{SCK} \downarrow \rightarrow SO$ delay time                      | $t_{KSO}$            | SO0               | $\overline{SCK}$ input mode                                    |                  | $2t_{sys} + 200$ | ns   |
|  |                      |                   | $\overline{SCK}$ output mode                                   |                  | 100              | ns   |

**Note 1)**  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys}$  [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)**  $\overline{CS}$ ,  $\overline{SCK}$ , SI and SO means each pin of  $\overline{CS} \rightarrow \overline{CS0}$ ,  $\overline{SCK} \rightarrow \overline{SCK0}$ , SI  $\rightarrow$  SI0, and SO  $\rightarrow$  SO0 respectively.

**Note 3)** The load of  $\overline{SCK}$  output mode and SO output delay time is 50pF + 1TTL.

## Serial transfer (CH0)

(Ta = -10 to +75°C, V<sub>DD</sub> = 2.7 to 3.3V, V<sub>SS</sub> = 0V)

| Item   | Symbol                             | Pin                      | Condition   | Min.                    | Max.                    | Unit |
|--|------------------------------------|--------------------------|---|-------------------------|-------------------------|------|
| $\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}}$<br>delay time        | t <sub>DCSK</sub>                  | $\overline{\text{SCK0}}$ | Chip select transfer mode<br>( $\overline{\text{SCK}}$ = output mode) |                         | t <sub>sys</sub> + 250  | ns   |
| $\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}}$<br>floating delay time | t <sub>DCSKF</sub>                 | $\overline{\text{SCK0}}$ | Chip select transfer mode<br>( $\overline{\text{SCK}}$ = output mode) |                         | t <sub>sys</sub> + 200  | ns   |
| $\overline{\text{CS}} \downarrow \rightarrow \text{SO}$<br>delay time                    | t <sub>DCSO</sub>                  | SO0                      | Chip select transfer mode   |                         | t <sub>sys</sub> + 250  | ns   |
| $\overline{\text{CS}} \downarrow \rightarrow \text{SO}$<br>floating delay time           | t <sub>DCSOF</sub>                 | SO0                      | Chip select transfer mode   |                         | t <sub>sys</sub> + 200  | ns   |
| $\overline{\text{CS}}$<br>high level width   | t <sub>WHCS</sub>                  | $\overline{\text{CS0}}$  | Chip select transfer mode   | t <sub>sys</sub> + 200  |                         | ns   |
| $\overline{\text{SCK}}$<br>cycle time  | t <sub>KCY</sub>                   | $\overline{\text{SCK0}}$ | Input mode  | 2t <sub>sys</sub> + 200 |                         | ns   |
|  |                                    |                          | Output mode   | 16000/fc                |                         | ns   |
| $\overline{\text{SCK}}$<br>high and low level widths                                     | t <sub>KH</sub><br>t <sub>KL</sub> | $\overline{\text{SCK0}}$ | Input mode  | t <sub>sys</sub> + 100  |                         | ns   |
|  |                                    |                          | Output mode   | 8000/fc - 150           |                         | ns   |
| SI input setup time<br>(against $\overline{\text{SCK}} \uparrow$ )                       | t <sub>SIK</sub>                   | SI0                      | $\overline{\text{SCK}}$ input mode                                    | -t <sub>sys</sub> + 100 |                         | ns   |
|  |                                    |                          | $\overline{\text{SCK}}$ output mode                                   | 200                     |                         | ns   |
| SI input hold time<br>(against $\overline{\text{SCK}} \uparrow$ )                        | t <sub>KSI</sub>                   | SI0                      | $\overline{\text{SCK}}$ input mode                                    | 2t <sub>sys</sub> + 100 |                         | ns   |
|  |                                    |                          | $\overline{\text{SCK}}$ output mode                                   | 100                     |                         | ns   |
| $\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time                      | t <sub>KSO</sub>                   | SO0                      | $\overline{\text{SCK}}$ input mode                                    |                         | 2t <sub>sys</sub> + 250 | ns   |
|  |                                    |                          | $\overline{\text{SCK}}$ output mode                                   |                         | 125                     | ns   |

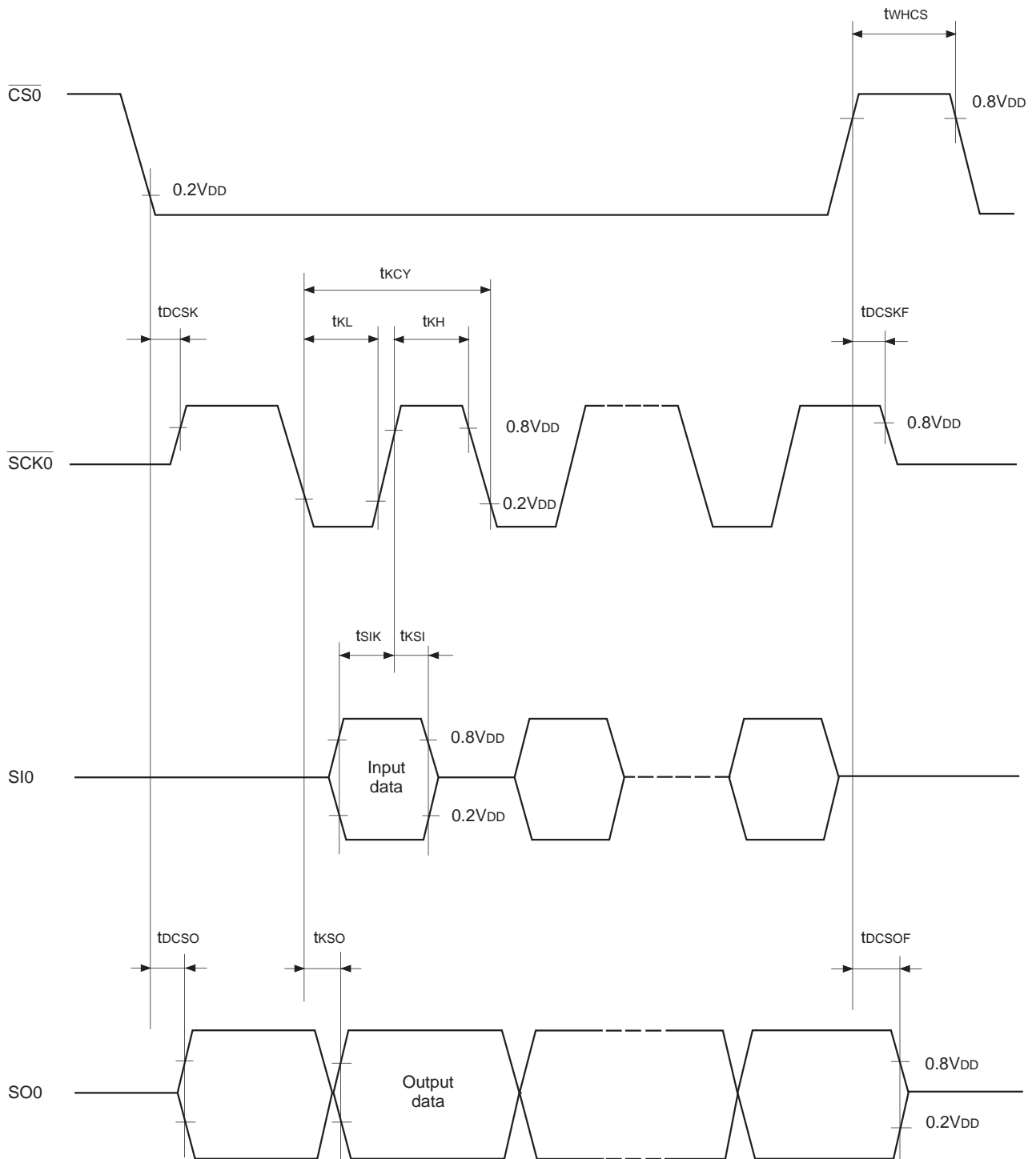
**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)**  $\overline{\text{CS}}$ ,  $\overline{\text{SCK}}$ , SI and SO means each pin of  $\overline{\text{CS}} \rightarrow \overline{\text{CS0}}$ ,  $\overline{\text{SCK}} \rightarrow \overline{\text{SCK0}}$ , SI  $\rightarrow$  SI0, and SO  $\rightarrow$  SO0 respectively.

**Note 3)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



## Serial transfer (CH1)

(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V)

| Item  | Symbol                             | Pin                      | Condition                            | Min.                    | Max.                   | Unit |
|---|------------------------------------|--------------------------|--------------------------------------|-------------------------|------------------------|------|
| $\overline{\text{SCK1}}$ cycle time                       | $t_{\text{KCY}}$                   | $\overline{\text{SCK1}}$ | Input mode                           | $2t_{\text{sys}} + 200$ |                        | ns   |
|   |                                    |                          | Output mode                          | $8000/f_c$              |                        | ns   |
| $\overline{\text{SCK1}}$ high and low level widths        | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SCK1}}$ | Input mode                           | $t_{\text{sys}} + 100$  |                        | ns   |
|   |                                    |                          | Output mode                          | $4000/f_c - 100$        |                        | ns   |
| SI1 input setup time (against $\overline{\text{SCK1}}$ ↑) | $t_{\text{SIK}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | 100                     |                        | ns   |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode | 200                     |                        | ns   |
| SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)  | $t_{\text{KSI}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | $t_{\text{sys}} + 200$  |                        | ns   |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode | 100                     |                        | ns   |
| $\overline{\text{SCK1}}$ ↓ → SO1 delay time               | $t_{\text{KSO}}$                   | SO1                      | $\overline{\text{SCK1}}$ input mode  |                         | $t_{\text{sys}} + 200$ | ns   |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode |                         | 100                    | ns   |

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

$t_{\text{sys}}$  [ns] = 2000/ $f_c$  (Upper 2 bits = "00"), 4000/ $f_c$  (Upper 2 bits = "01"), 16000/ $f_c$  (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is 50pF + 1TTL.

## Serial transfer (CH1)

(Ta = -10 to +75°C, V<sub>DD</sub> = 2.7 to 3.3V, V<sub>SS</sub> = 0V)

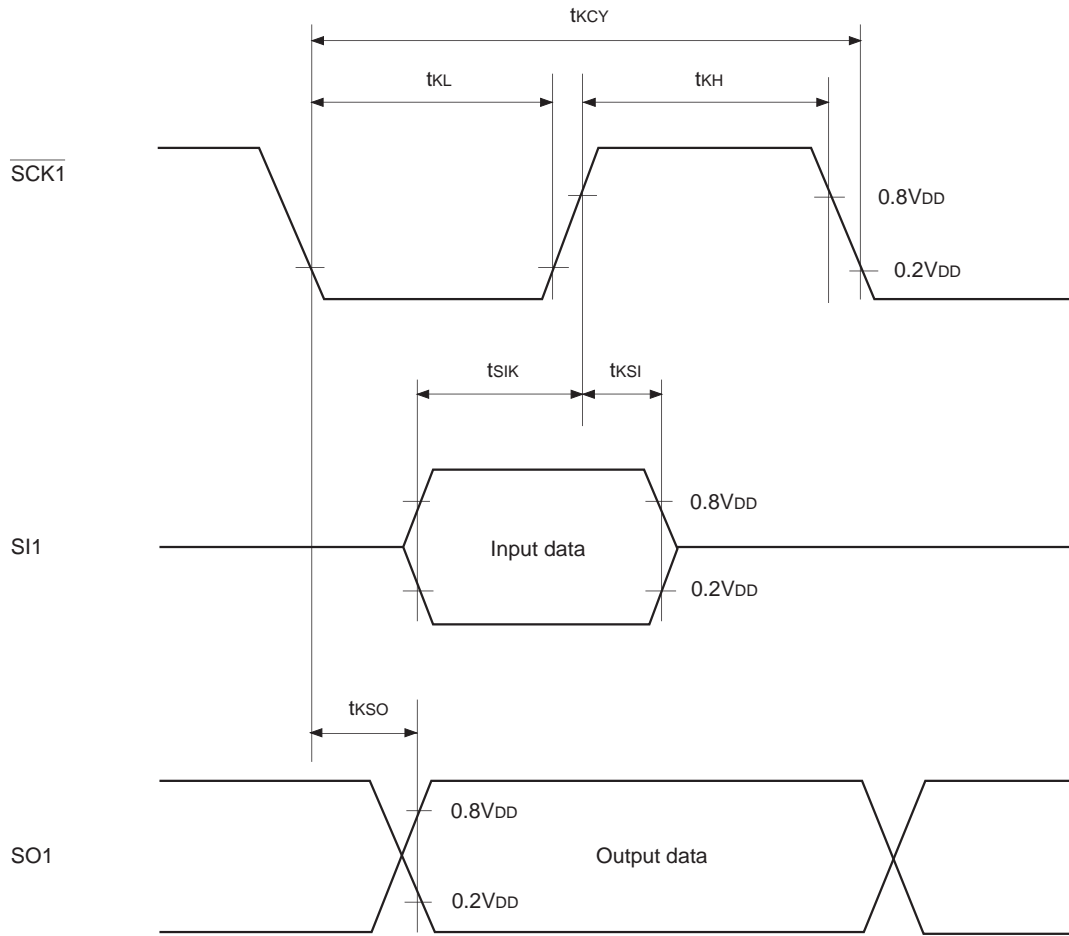
| Item  | Symbol                             | Pin                      | Condition                            | Min.                    | Max.                   | Unit |
|---|------------------------------------|--------------------------|--------------------------------------|-------------------------|------------------------|------|
| $\overline{\text{SCK1}}$ cycle time                       | $t_{\text{KCY}}$                   | $\overline{\text{SCK1}}$ | Input mode                           | $2t_{\text{sys}} + 200$ |                        | ns   |
|   |                                    |                          | Output mode                          | $8000/f_c$              |                        | ns   |
| $\overline{\text{SCK1}}$ high and low level widths        | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SCK1}}$ | Input mode                           | $t_{\text{sys}} + 100$  |                        | ns   |
|   |                                    |                          | Output mode                          | $4000/f_c - 150$        |                        | ns   |
| SI1 input setup time (against $\overline{\text{SCK1}}$ ↑) | $t_{\text{SIK}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | 100                     |                        | ns   |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode | 200                     |                        | ns   |
| SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)  | $t_{\text{KSI}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | $t_{\text{sys}} + 200$  |                        | ns   |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode | 100                     |                        | ns   |
| $\overline{\text{SCK1}}$ ↓ → SO1 delay time               | $t_{\text{KSO}}$                   | SO1                      | $\overline{\text{SCK1}}$ input mode  |                         | $t_{\text{sys}} + 250$ | ns   |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode |                         | 125                    | ns   |

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

$t_{\text{sys}}$  [ns] = 2000/ $f_c$  (Upper 2 bits = "00"), 4000/ $f_c$  (Upper 2 bits = "01"), 16000/ $f_c$  (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing

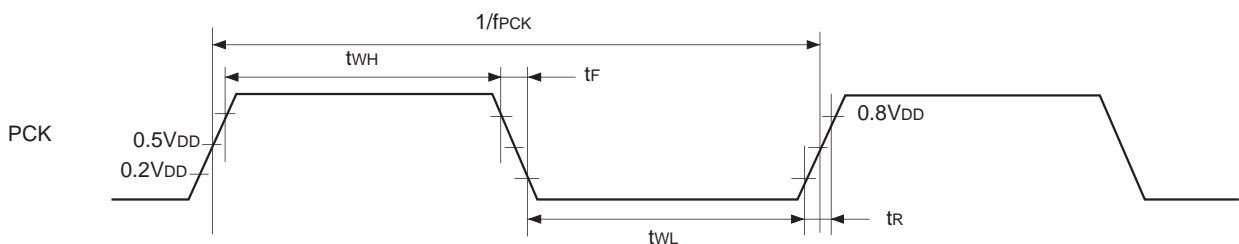


(3) General purpose prescaler

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

| Item                                     | Symbol           | Pin | Condition | Min. | Typ. | Max. | Unit |
|--|------------------|-----|-----------|------|------|------|------|
| External clock input frequency           | $f_{PCK}$        | PCK |           |      |      | 12   | MHz  |
| External clock input pulse width         | $t_{WH}, t_{WL}$ | PCK |           | 33   |      |      | ns   |
| External clock input rise and fall times | $t_R, t_F$       | PCK |           |      |      | 200  | ns   |

Fig. 6. General purpose prescaler timing



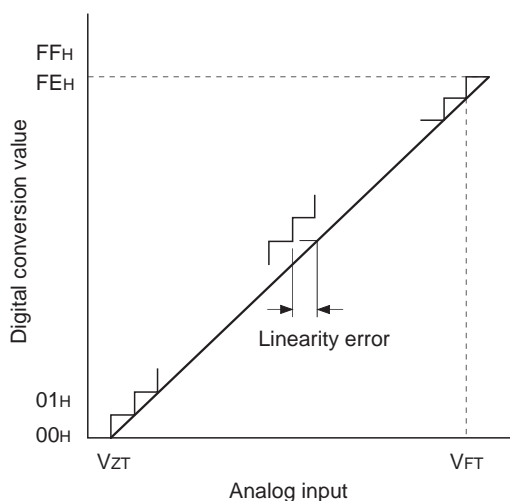
**(4) A/D converter characteristics** ( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

| Item                    | Symbol     | Pins        | Conditions  | Min.            | Typ. | Max.      | Unit          |
|-------------------------|------------|-------------|---|-----------------|------|-----------|---------------|
| Resolution              |            |             |   |                 |      | 8         | Bits          |
| Linearity error         |            |             | $T_a = 25^\circ\text{C}$<br>$V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$<br>$V_{SS} = AV_{SS} = 0\text{V}$ |                 |      | $\pm 1$   | LSB           |
| Absolute error          |            |             |   |                 |      | $\pm 2$   | LSB           |
| Conversion time         | $t_{CONV}$ |             |   | $160/f_{ADC}^*$ |      |           | $\mu\text{s}$ |
| Sampling time           | $t_{SAMP}$ |             |   | $12/f_{ADC}^*$  |      |           | $\mu\text{s}$ |
| Reference input voltage | $V_{REF}$  | $AV_{REF}$  | $V_{DD} = AV_{DD} = 4.5$ to $5.5\text{V}$   | $AV_{DD} - 0.5$ |      | $AV_{DD}$ | V             |
| Analog input voltage    | $V_{IAN}$  | AN0 to AN11 |   | 0               |      |           | V             |
| AVREF current           | $I_{REF}$  | AVREF       | Operating mode  |                 | 0.6  | 1.0       | mA            |
|                         | $I_{REFS}$ |             | SLEEP mode<br>STOP mode<br>32kHz operating mode   |                 |      | 10        | $\mu\text{A}$ |

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 2.7$  to  $3.3\text{V}$ ,  $AV_{REF} = 2.7$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

| Item                    | Symbol     | Pins        | Conditions  | Min.            | Typ. | Max.      | Unit          |
|-------------------------|------------|-------------|---|-----------------|------|-----------|---------------|
| Resolution              |            |             |   |                 |      | 8         | Bits          |
| Linearity error         |            |             | $T_a = 25^\circ\text{C}$<br>$V_{DD} = AV_{DD} = AV_{REF} = 3.0\text{V}$<br>$V_{SS} = AV_{SS} = 0\text{V}$ |                 |      | $\pm 1$   | LSB           |
| Absolute error          |            |             |   |                 |      | $\pm 2$   | LSB           |
| Conversion time         | $t_{CONV}$ |             |   | $160/f_{ADC}^*$ |      |           | $\mu\text{s}$ |
| Sampling time           | $t_{SAMP}$ |             |   | $12/f_{ADC}^*$  |      |           | $\mu\text{s}$ |
| Reference input voltage | $V_{REF}$  | $AV_{REF}$  | $V_{DD} = AV_{DD} = 2.7$ to $3.3\text{V}$   | $AV_{DD} - 0.3$ |      | $AV_{DD}$ | V             |
| Analog input voltage    | $V_{IAN}$  | AN0 to AN11 |   | 0               |      |           | V             |
| AVREF current           | $I_{REF}$  | AVREF       | Operating mode  |                 | 0.3  | 0.7       | mA            |
|                         | $I_{REFS}$ |             | SLEEP mode<br>STOP mode<br>32kHz operating mode   |                 |      | 10        | $\mu\text{A}$ |

**Fig. 7. Definitions of A/D converter terms**



\* The value of  $f_{ADC}$  is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).  
 When PS2 is selected,  $f_{ADC} = f_c/2$   
 When PS1 is selected,  $f_{ADC} = f_c$

(5) Interruption, reset input

(Ta = -10 to +75°C, VDD = 2.7 to 5.5V, VSS = 0V)

| Item  | Symbol                             | Pins  | Conditions | Min.  | Max. | Unit |
|---|------------------------------------|---|------------|-------|------|------|
| External interruption high and low level widths | t <sub>IH</sub><br>t <sub>IL</sub> | $\overline{\text{INT0}}$<br>$\overline{\text{INT1}}$<br>$\overline{\text{INT2}}$<br>NMI<br>PJ0 to PJ7 |            | 1     |      | μs   |
| Reset input low level width                     | t <sub>RSL</sub>                   | $\overline{\text{RST}}$   |            | 32/fc |      | μs   |

Fig. 8. Interruption input timing

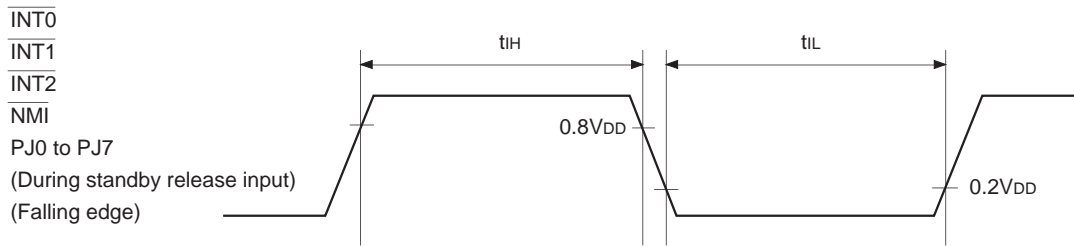
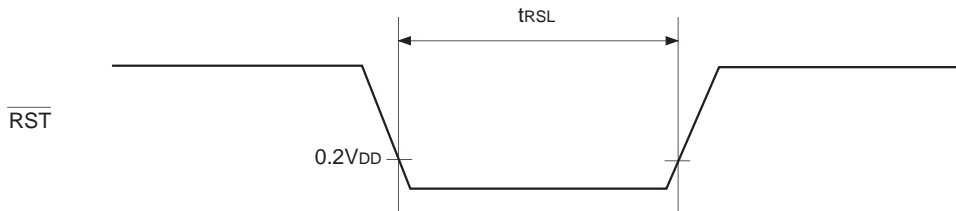


Fig. 9. Reset input timing



(6) Others

(Ta = -10 to +75°C, VDD = 2.7 to 5.5V, VSS = 0V)

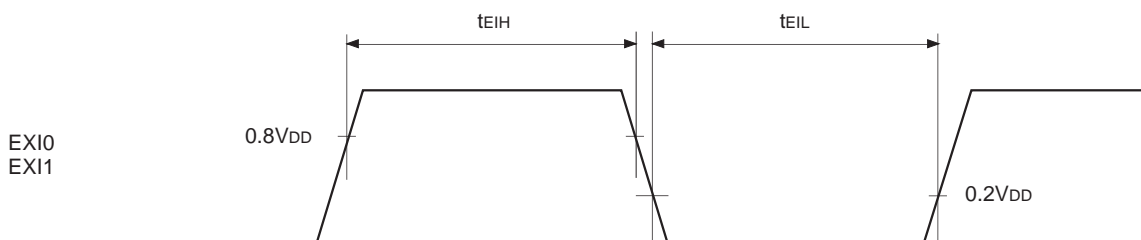
| Item                                | Symbol                               | Pins         | Conditions                 | Min.  | Max. | Unit |
|-------------------------------------|--------------------------------------|--------------|----------------------------|---|------|------|
| EXI input high and low level widths | t <sub>EIH</sub><br>t <sub>EIL</sub> | EXI0<br>EXI1 | t <sub>sys</sub> = 2000/fc | t <sub>FRC</sub> × 8 + 200 + t <sub>sys</sub> |      | ns   |

**Note** t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

t<sub>FRC</sub> = 1000/fc [ns]

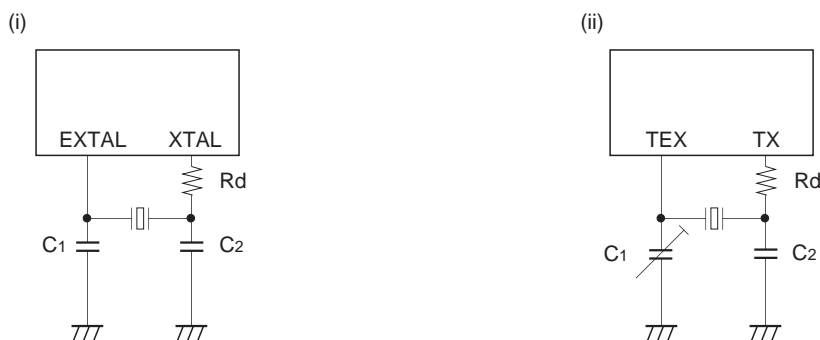
Fig. 10. Other timings





Supplement

Fig. 11. Recommended oscillation circuit

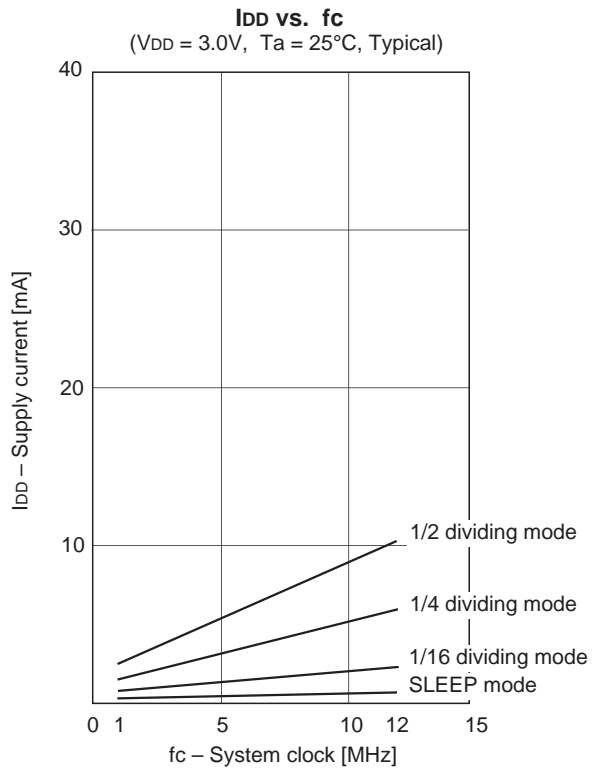
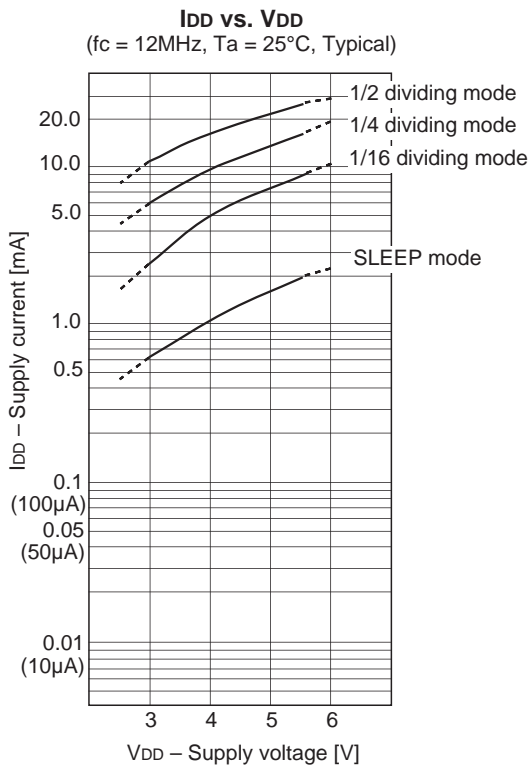
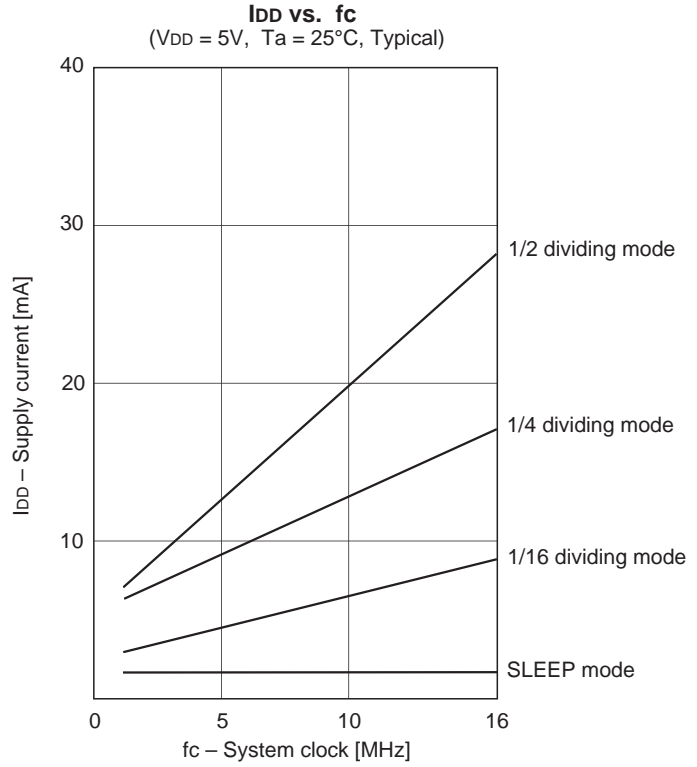
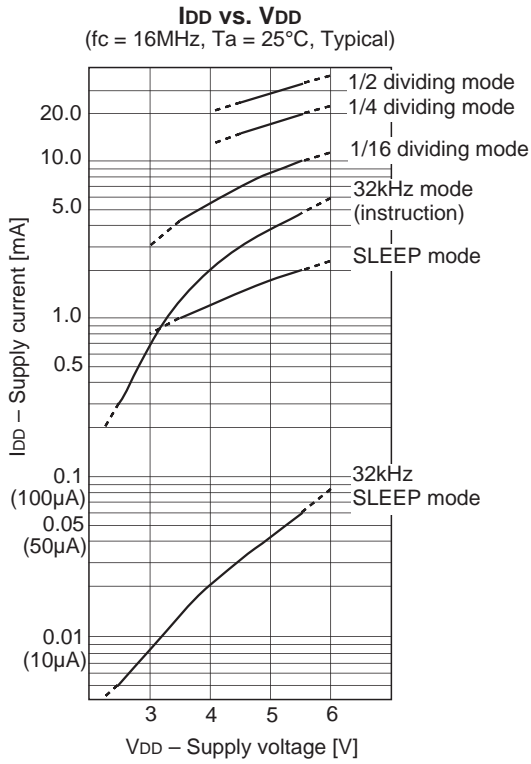


| Manufacturer           | Model        | fc (MHz)  | C1 (pF) | C2 (pF) | Rd ( $\Omega$ ) | Circuit example |
|------------------------|--------------|-----------|---------|---------|-----------------|-----------------|
| RIVER ELETEC CO., LTD. | HC-49/U03    | 8.00      | 10      | 10      | 0               | (i)             |
|                        |              | 10.00     | 5       | 5       |                 |                 |
|                        |              | 12.00     |         |         |                 |                 |
|                        |              | 16.00     |         |         |                 |                 |
| KINSEKI LTD.           | HC-49/U (-S) | 8.00      | 16 (12) | 16 (12) | 0               | (i)             |
|                        |              | 10.00     | 16 (12) | 16 (12) |                 |                 |
|                        |              | 12.00     | 12      | 12      |                 |                 |
|                        |              | 16.00     | 12      | 12      |                 |                 |
|                        | P3           | 32.768kHz | 30      | 18      | 470K            | (ii)            |

Products List

| Option item                    | Mask product             | CXP819P60MQ-4-□□□   | CXP819P60MR-4-□□□    |
|--------------------------------|--------------------------|---------------------|----------------------|
| Package                        | 100-pin plastic QFP/LQFP | 100-pin plastic QFP | 100-pin plastic LQFP |
| ROM capacity                   | 52K bytes/60K bytes      | PROM 60K bytes      | PROM 60K bytes       |
| Pull-up resistor for reset pin | Existent/Non-existent    | Existent            | Existent             |

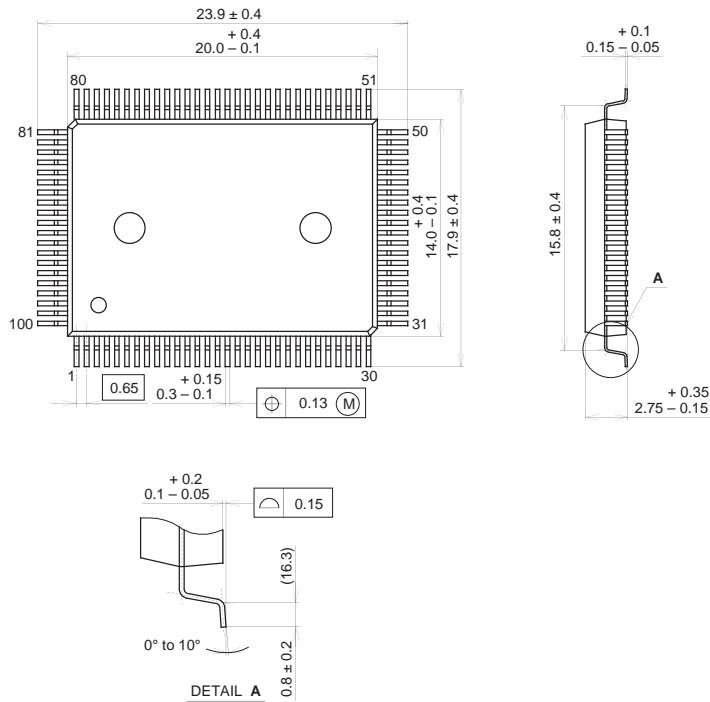
Characteristics Curve



Package Outline

Unit : mm

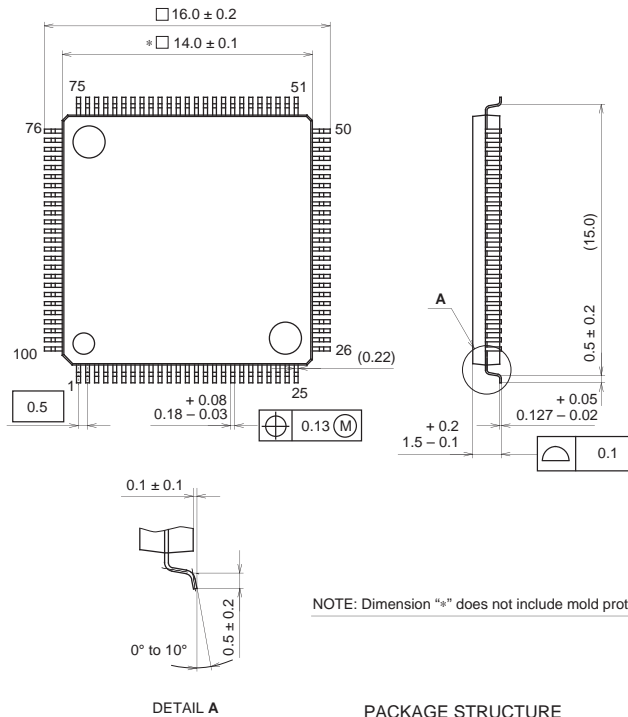
100PIN QFP (PLASTIC)



|            |               |
|------------|---------------|
| SONY CODE  | QFP-100P-L01  |
| EIAJ CODE  | QFP100-P-1420 |
| JEDEC CODE |               |

| PACKAGE STRUCTURE |                 |
|-------------------|-----------------|
| PACKAGE MATERIAL  | EPOXY RESIN     |
| LEAD TREATMENT    | SOLDER PLATING  |
| LEAD MATERIAL     | 42/COPPER ALLOY |
| PACKAGE MASS      | 1.7g            |

100PIN LQFP (PLASTIC)



|            |                |
|------------|----------------|
| SONY CODE  | LQFP-100P-L01  |
| EIAJ CODE  | LQFP100-P-1414 |
| JEDEC CODE |                |

| PACKAGE STRUCTURE |                |
|-------------------|----------------|
| PACKAGE MATERIAL  | EPOXY RESIN    |
| LEAD TREATMENT    | SOLDER PLATING |
| LEAD MATERIAL     | 42 ALLOY       |
| PACKAGE MASS      | 0.8g           |