TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87PM41NG
TMP87PM41FG
TMP87PM41UG

TOSHIBA CORPORATION

Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87PM41N	P-SDIP64-750-1.78	TMP87PM41NG	SDIP64-P-750-1.78	—
TMP87PM41F	P-QFP64-1420-1.00A	TMP87PM41FG	QFP64-P-1420-1.00A	—
TMP87PM41U	P-LQFP64-1010-0.50D	TMP87PM41UG	LQFP64-P-1010-0.50D	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

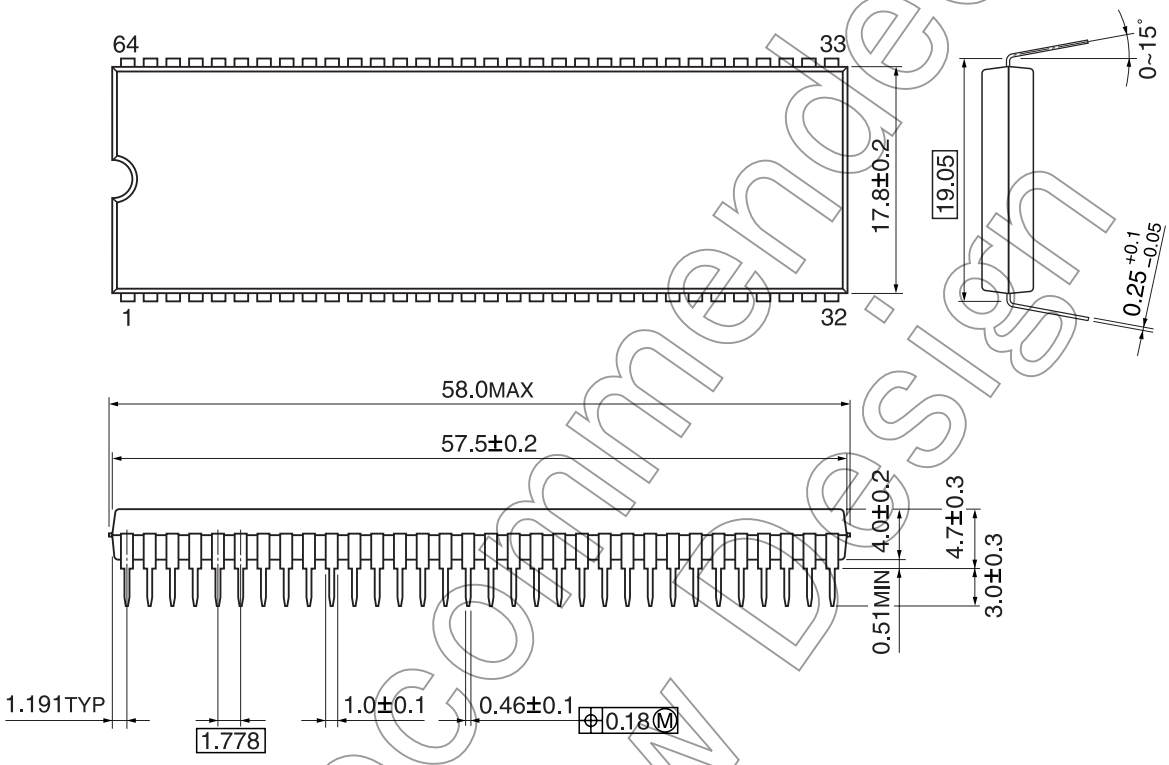
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

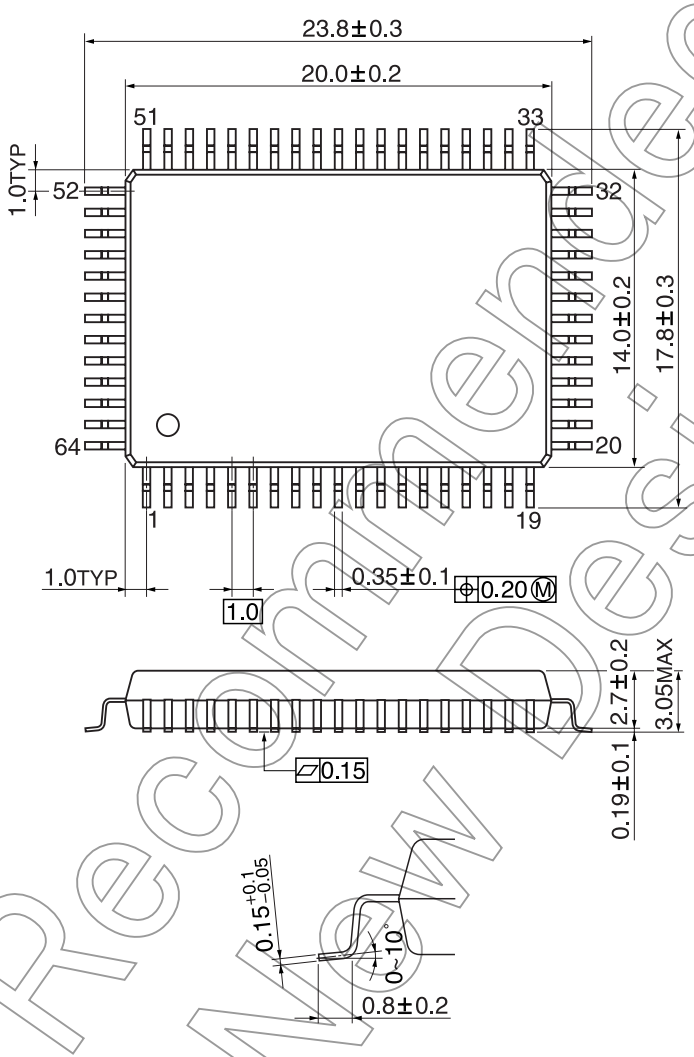
SDIP64-P-750-1.78

Unit: mm



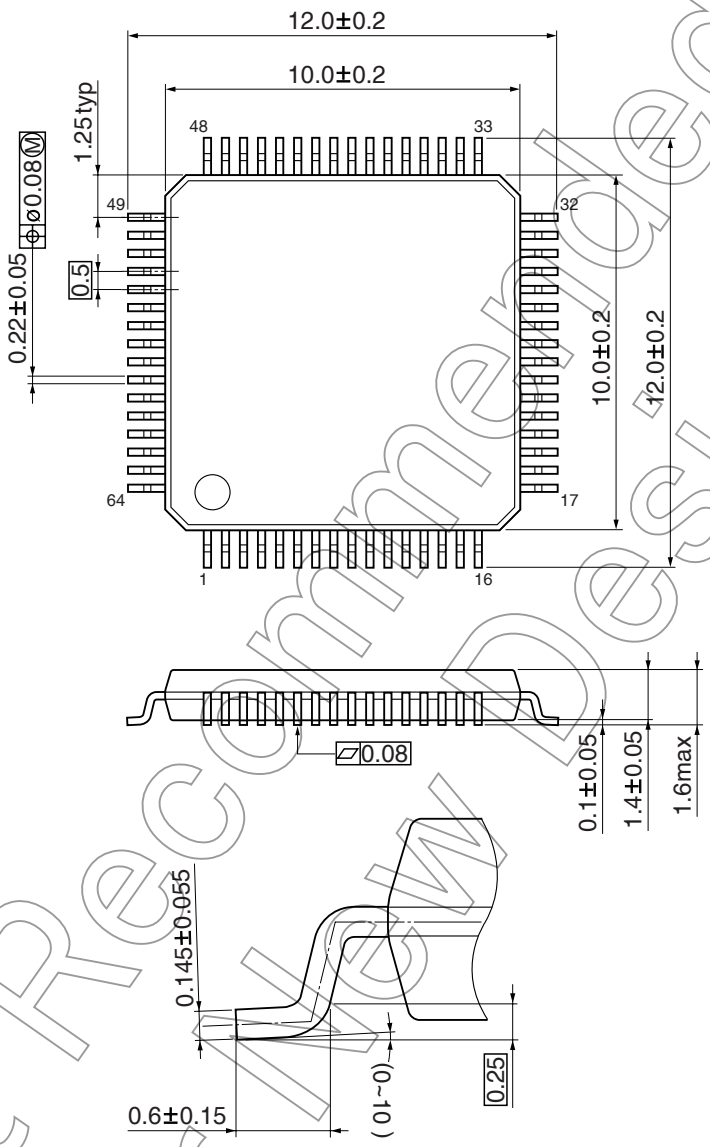
QFP64-P-1420-1.00A

Unit: mm



LQFP64-P-1010-0.50D

Unit: mm



CMOS 8-BIT MICROCONTROLLER

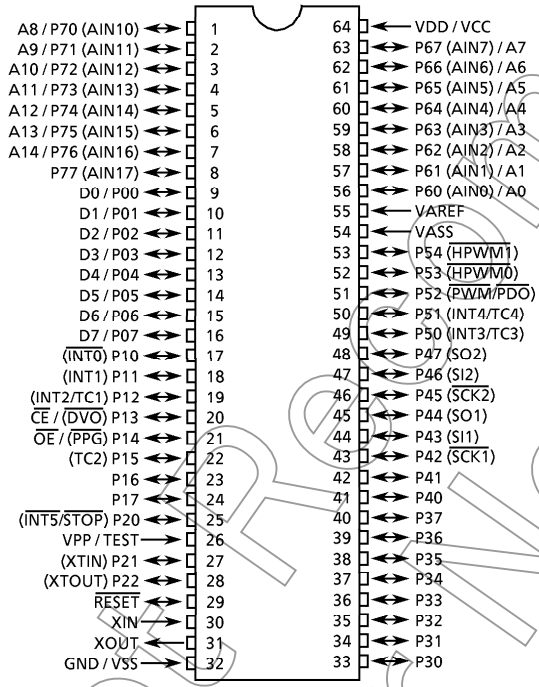
TMP87PM41N, TMP87PM41F, TMP87PM41U

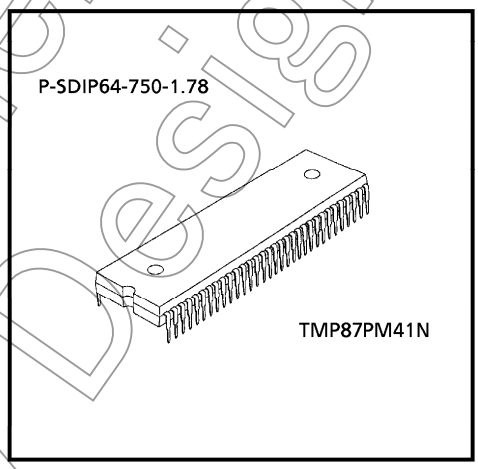
The 87PM41 is a One-Time PROM microcontroller with low-power 256K bits (32K bytes) electrically programmable read only memory for the 87C841/CC41/CH41/CK41/CM41 system evaluation. The 87PM41 is pin compatible with the 87C841/CC41/CH41/CK41/M41. The operations possible with the 87C841/CC41/CH41/CK41/M41 can be performed by writing programs to PROM. The 87PM41 can write and verify in the same way as the TC57256AD using an adaptor socket BM1136/BM1137/BM1121 and an EPROM programmer.

PART No.	OTP	RAM	PACKAGE	ADAPTOR SOKET
TMP87PM41N	32K × 8-bit	1K × 8-bit	P-SDIP64-750-1.78	BM1136
TMP87PM41F			P-QFP64-1420A-1.00A	BM1137
TMP87PM41U			P-LQFP64-1010-0.50D	BM11121

PIN ASSIGNMENTS (TOP VIEW)

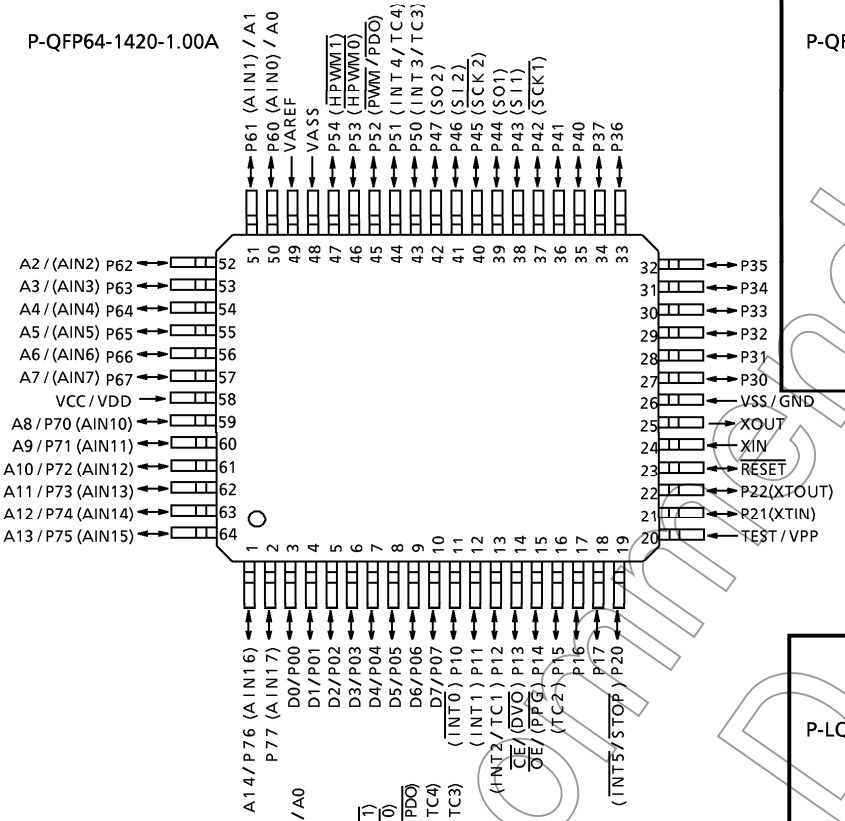
P-SDIP64-750-1.78



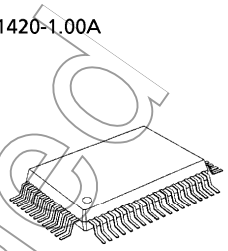


PIN ASSIGNMENTS (TOP VIEW)

P-QFP64-1420-1.00A

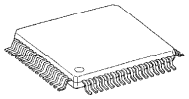


P-QFP64-1420-1.00A



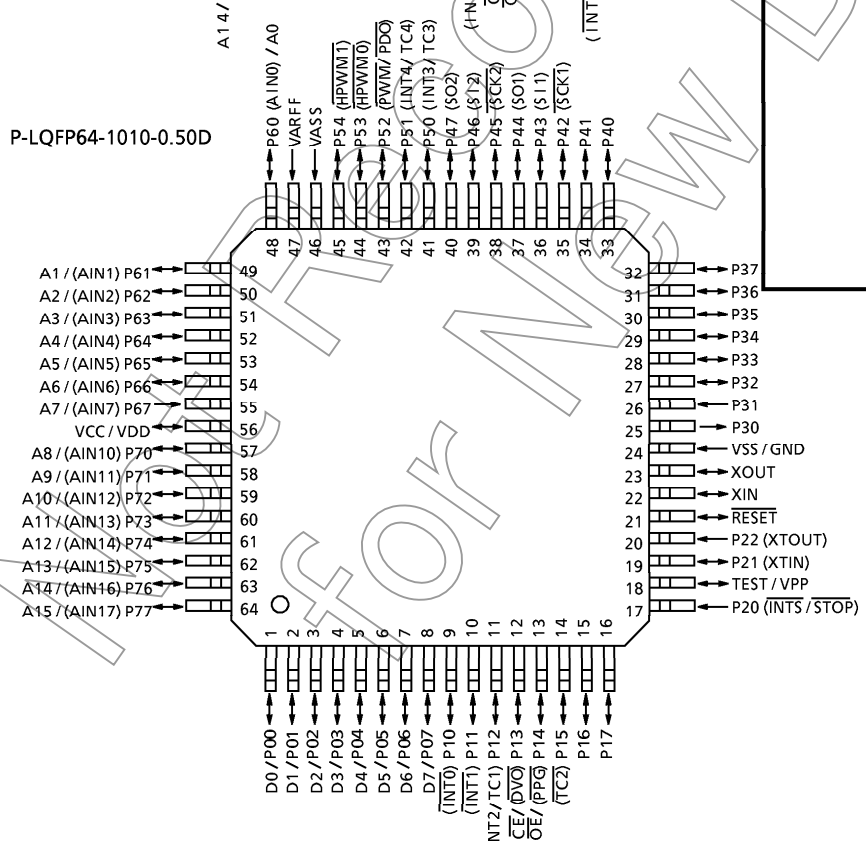
TMP87PM41F

P-LQFP64-1010-0.50D



TMP87PM41U

P-LQFP64-1010-0.50D



PIN FUNCTION

The 87PM41 has two modes: MCU and PROM.

(1) MCU mode

In this mode, the 87PM41 is pin compatible with the 87C841/CC41/CH41/CK41/CM41 (fix the TEST pin at low level).

(2) PROM mode

PIN NAME (PROM mode)	INPUT/OUTPUT	FUNCTIONS	PIN NAME (MCU mode)
A14 to A8	Input	PROM address inputs	P76 to P70
A7 to A0			P67 to P60
D7 to D0	I/O	PROM data input/outputs	P07 to P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
VPP	Power supply	+ 12.5 V / 5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
GND		0 V	VSS
P37 to P30	I/O	Pull-up with resistance for input processing	
P47 to P40			
P54 to P50			
P11		PROM mode setting pin. Be fixed at high level.	
P21			
P77			
P17 to P15		PROM mode setting pin. Be fixed at low level.	
P12, P10			
P22, P20			
$\overline{RESET}$			
XIN	Input	Connect an 8 MHz oscillator to stabilize the internal state.	
XOUT	Output		
VAREF	Power Supply	0 V (GND)	
VASS			

OPERATIONAL DESCRIPTION

The following explains the 87PM41 hardware configuration and operation. The configuration and functions of the 87PM41 are the same as those of the 87C841/CC41/CH41/CK41/CM41, except in that a one-time PROM is used instead of an on-chip mask ROM.

The 87PM41 is placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. OPERATING MODE

The 87PM41 has two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST / VPP pin at low level.

In the MCU mode, operation is the same as with the 87C841/CC41/CH41/CK41/CM41 (the TEST / VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The 87PM41 has a 32 K × 8-bit (addresses 8000_H to $FFFF_H$ in the MCU mode, addresses 0000_H to $7FFF_H$ in the PROM mode) of program memory (OTP).

To use the 87PM41 as the system evaluation for the 87C841/CC41/CH41/CK41/CM41 the program should be written to the program memory area as shown the Figure 1-1.

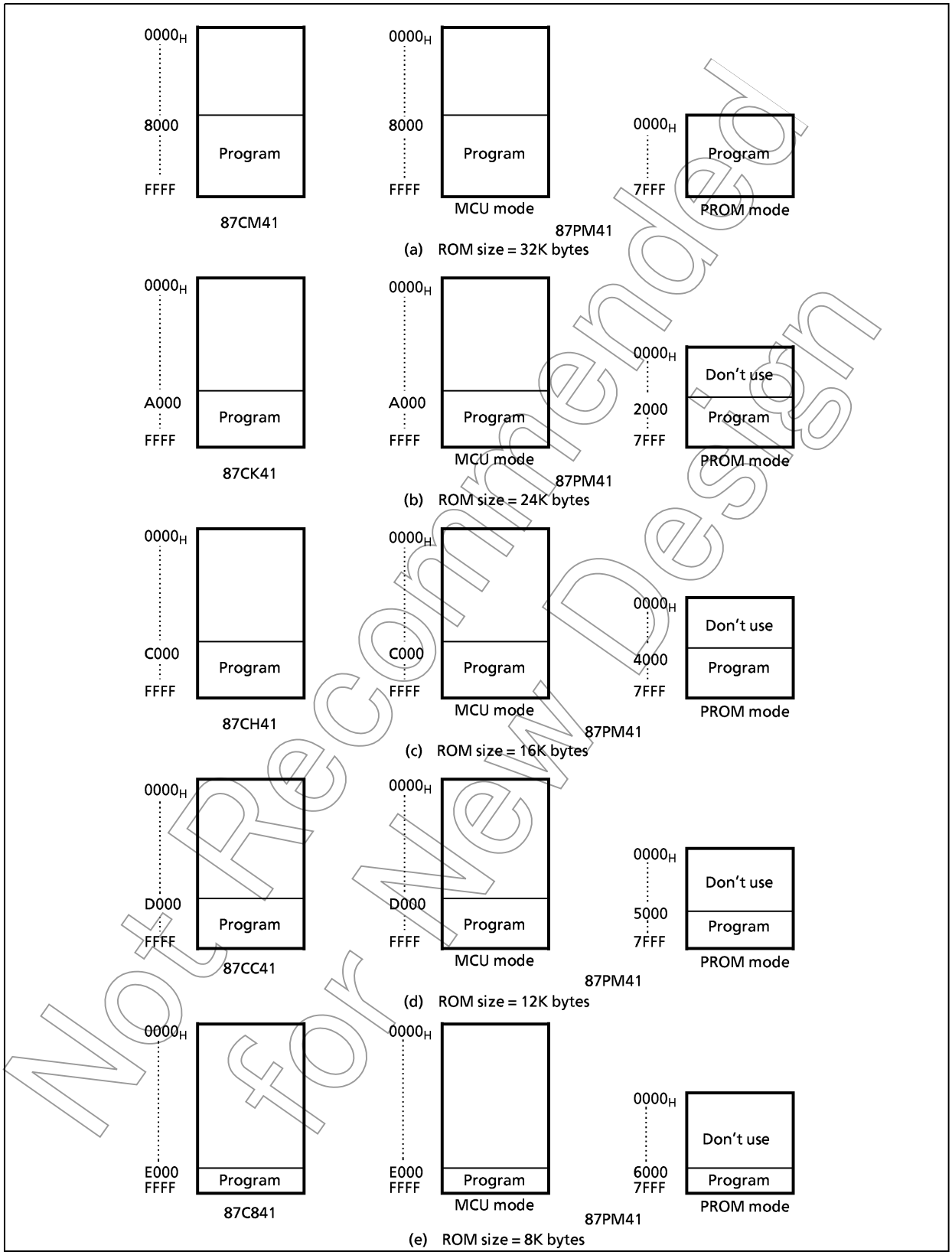


Figure 1-1. Program Memory Area

Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

1.1.2 Data Memory

The 87PM41 has an on-chip 1K × 8-bit data memory (static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the 87PM41 are the same as those of the 87C841/CC41/CH41/CK41/CM41 except that the TEST pin has is no built-in pull-down resistance.

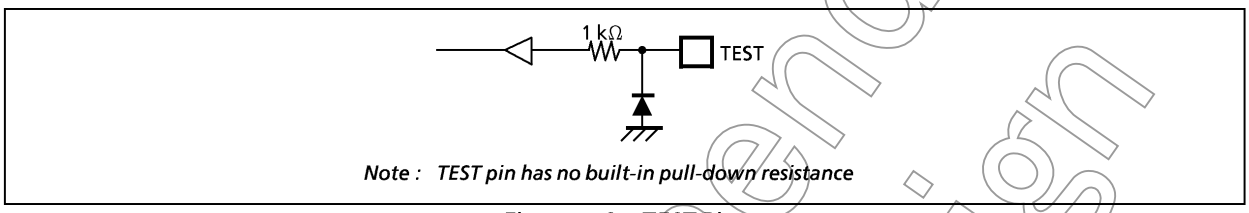


Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuitries of 87PM41 I/O ports the are the same as the code A type I/O circuitries of the 87C841/CC41/CH41/CK41/CM41.

1.2 PROM Mode

The PROM mode is activated by setting the TEST, $\overline{RESET}$ pin and the ports P17 to P10, P22 to P20 and P77 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer. The high-speed programming mode can be used for program operation.
The 87PM41 is not supported an *electric signature* mode, so the ROM type must be set to TC57256AD.
Set the adaptor socket switch to "P".

Note : Please set the high-speed programming mode according to each manual of PROM.

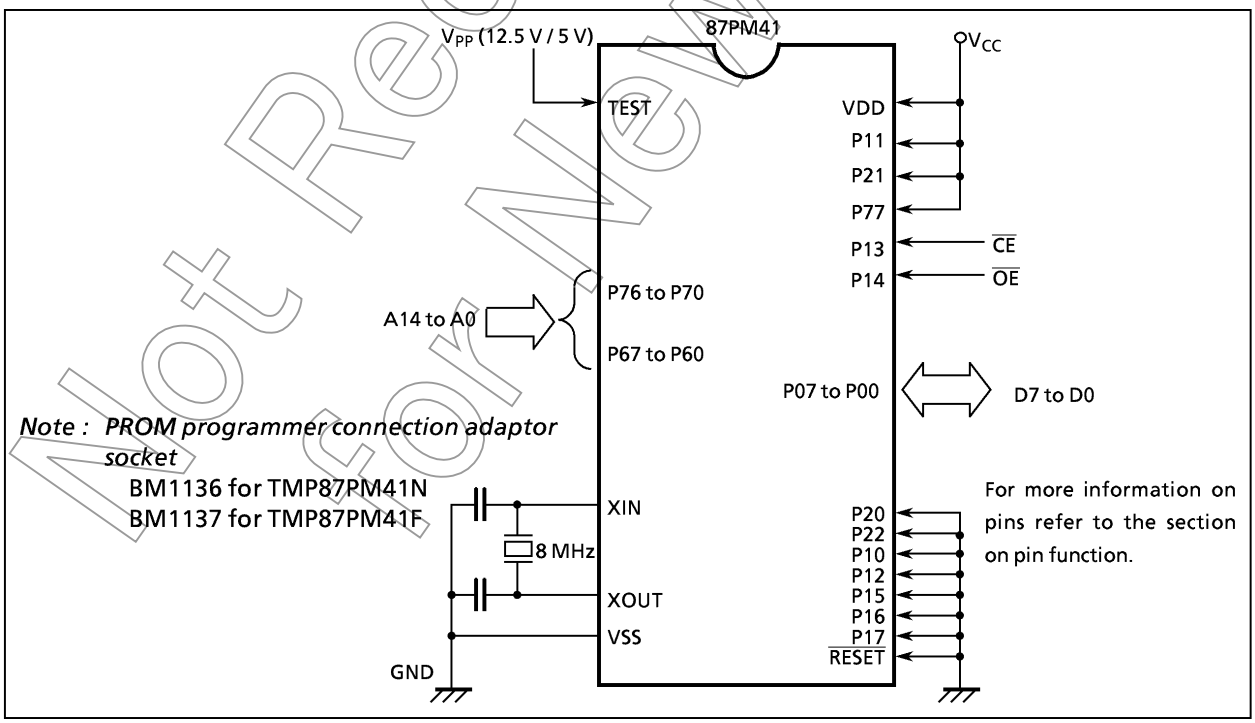


Figure 1-3. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed Programming Mode-I)

The high-speed programming mode is achieved by applying the program voltage (+ 12.5 V) to the VPP pin when Vcc = 6 V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 1 ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (number of programmed times × 1 ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

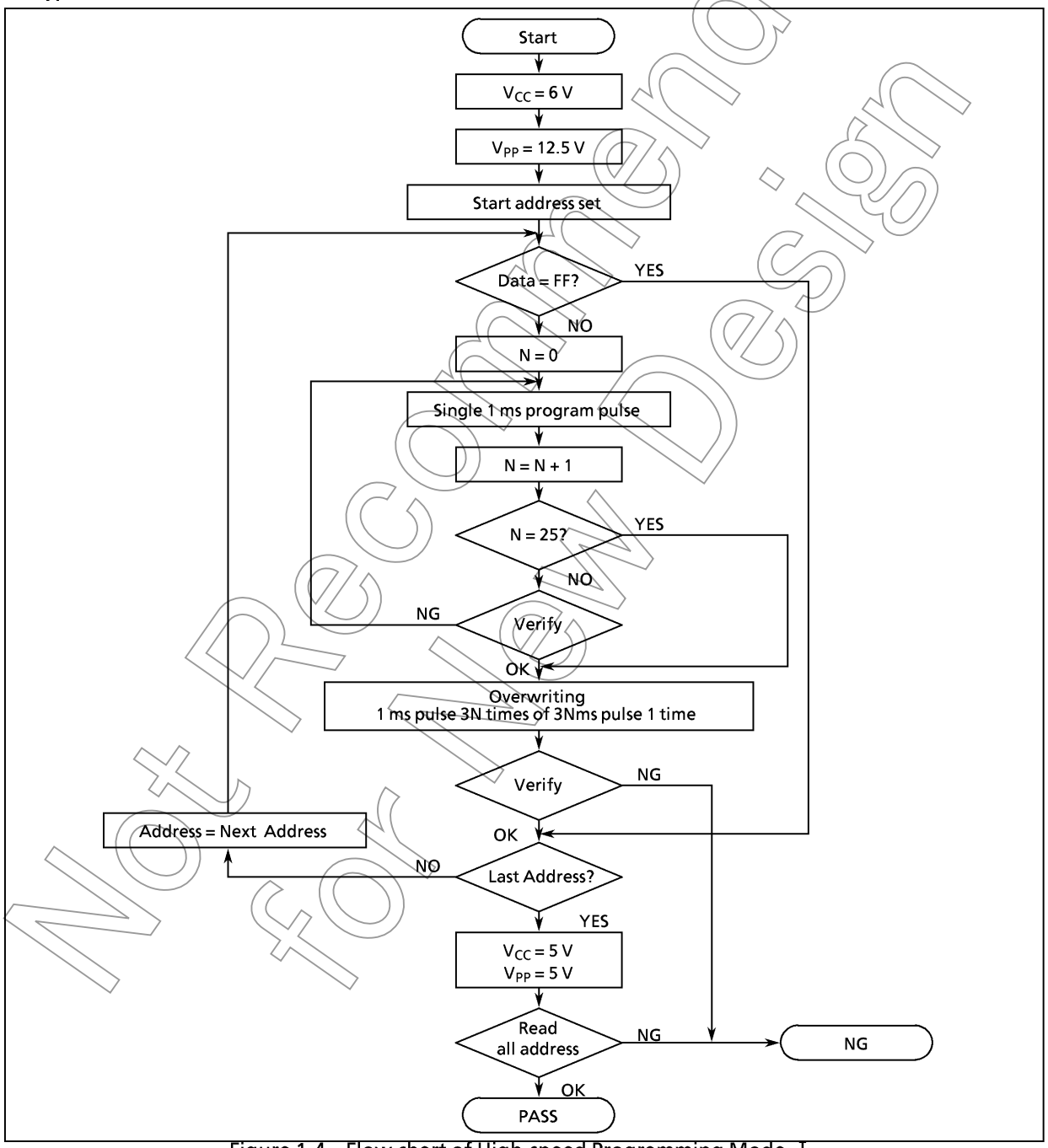


Figure 1-4. Flow chart of High-speed Programming Mode- I

1.2.2 Programming Flowchart (High-speed Programming Mode-II)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the Vpp pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 0.1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

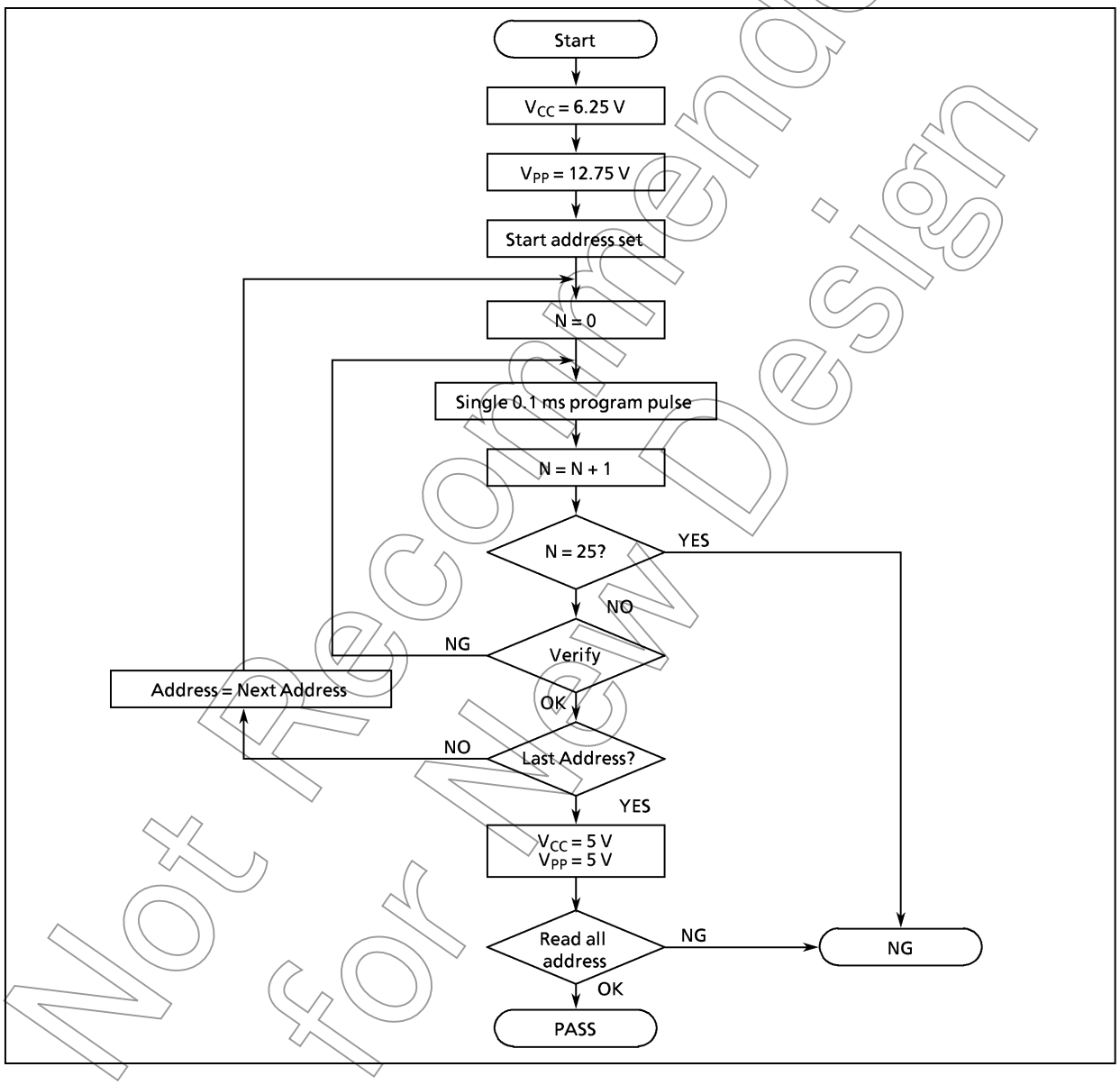


Figure 1-5. Flowchart of High-speed Programming Mode - II

1.2.3 Writing Method for General-purpose PROM Program

(1) Adapters
BM1136 : TMP87PM41N
BM1137 : TMP87PM41F
BM11121 : TMP87PM41U

(2) Adapter setting
Switch (SW1) is set to side N.

(3) PROM programmer specifying
i) PROM type is specified to TC57256D.
Writing voltage : 12.5 V (high-speed program mode-Ⅰ)
Writing voltage : 12.75 V (high-speed program mode-Ⅱ)

ii) Data transfer (copy) (note 1)
In the TMP87PM41, EPROM is within the addresses 0000_H to $7FFF_H$. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.
ROM capacity of 16KB : transferred addresses $C000_H$ to $FFFF_H$ to addresses 4000 to $7FFF_H$

iii) Writing address is specified. (note 1)
Start address : 0000_H
End address : $7FFF_H$

(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1 : The specifying method is referred to the PROM programmer description. Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

Note 2 : When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.

Note 3 : The TMP87PP23 does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12V ± 0.5V to the address pin 9 (A9). The signature must not be used.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Program Voltage	V_{PP}	TEST/VPP	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	Σ I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7	120	mA
	Σ I_{OUT2}	Port P3	120	
Power Dissipation [Topr = 70 °C]	PD	TMP87PM41N	600	mW
		TMP87PM41F, TMP87PM41U	350	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note : Clock frequency fc : Supply voltage range is specified in NORMAL1/2 mode and IDLE1/2 mode.

D.C. CHARACTERISTICS

(V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Low Current	I_{IL}	Push pull ports	V_{DD} = 5.5 V, V_{IN} = 0.4 V	–	–	– 2	mA
Input Resistance	R_{IN2}	$\overline{RESET}$		90	220	510	kΩ
Output Leakage Current	I_{LO}	Sink open drain ports Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
Output High Voltage	V_{OH1}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output Low current	I_{OL3}	P3	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	10	16	mA
Supply Current in IDLE 1, 2 modes			fc = 8 MHz fs = 32.768 kHz	–	4.5	6	mA
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V / 0.2 V fs = 32.768 kHz	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	μA

Note 1 : Typical values show those at Topr = 25 °C, V_{DD} = 5 V.
Note 2 : Input Current I_{IN1},I_{IN3} ; The current through resistor is not included, when the input resistor (pull-upor pull-down) is contained.
Note 3 : IDD except I_{REF}.

A/D CONVERSION CHARACTERISTICS

(Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.			UNIT
					ADCDR1	ADCDR2		
						ACK = 0	ACK = 1	
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	2.7	–	V_{DD}			V
	V_{ASS}		V_{SS}	–	1.5			
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}			V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V V_{ASS} = 0.0 V	–	0.5	1.0			mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V OR V_{DD} = 2.7 V, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	± 3	± 2	LSB
Zero Point Error			–	–	± 1	± 3	± 2	
Full Scale Error			–	–	± 1	± 3	± 2	
Total Error			–	–	± 2	± 6	± 4	

Note 1 : $\triangle V_{AREF} = V_{AREF} - V_{ASS}$
Note 2 : ADCDR1 ; 8 bit – A/D conversion result (1LSB = $\triangle V_{AREF}$ / 256)
ADCDR2 ; 10 bit – A/D conversion result (1LSB = $\triangle V_{AREF}$ / 1024)

A.C. CHARACTERISTICS

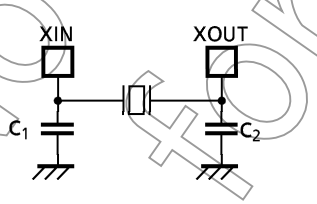
(V_{SS} = 0 V, V_{DD} = 2.7 / 4.5 to 5.5 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	62.5	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

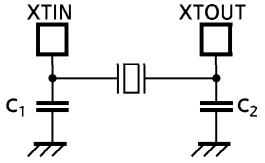
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0 V, V_{DD} = 2.7 / 4.5 to 5.5 V, Topr = – 40 to 85 °C)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

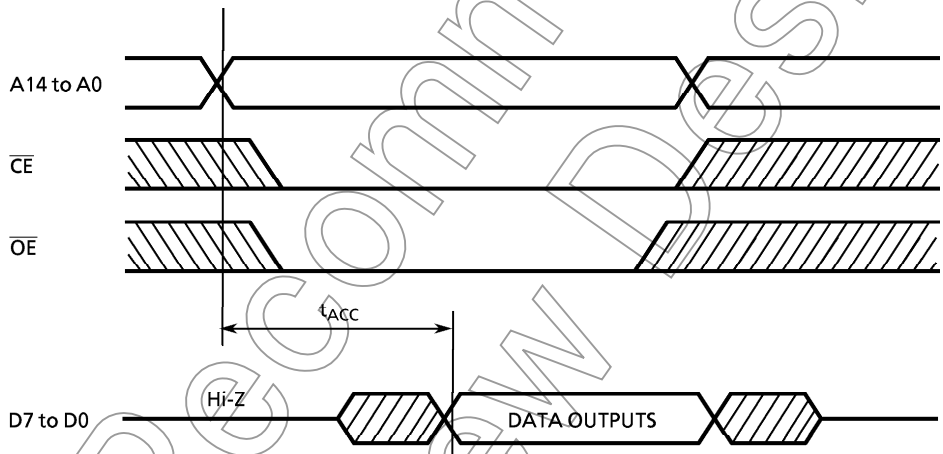
Note : When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.

D.C./A.C. CHARACTERISTICS (PROM mode) (V_{SS} = 0 V)

(1) Read Operation

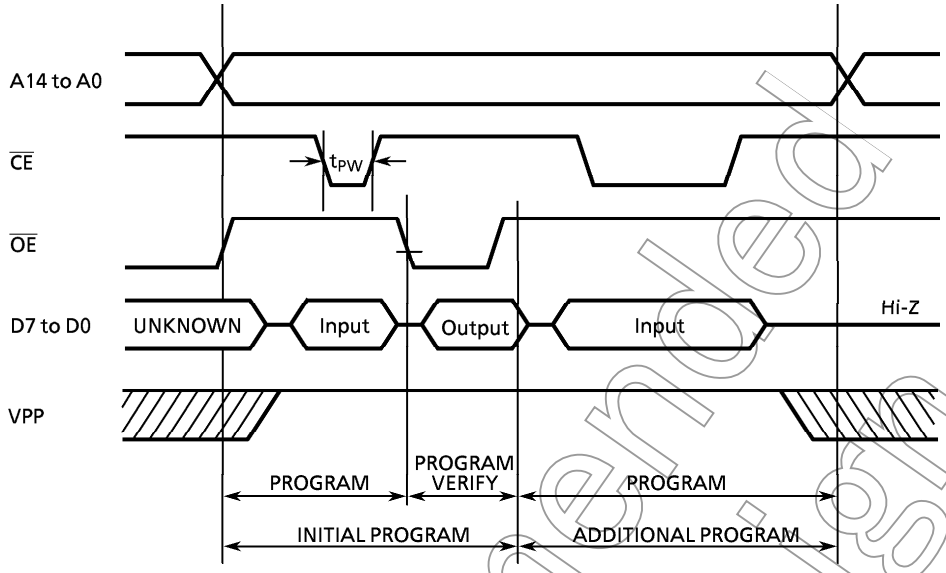
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Power Supply Voltage	V_{CC}		4.75	–	6.5	V
Program Power Supply Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	1.5tcyc + 300	–	ns

Note : tcyc = 500 ns at 8 MHz



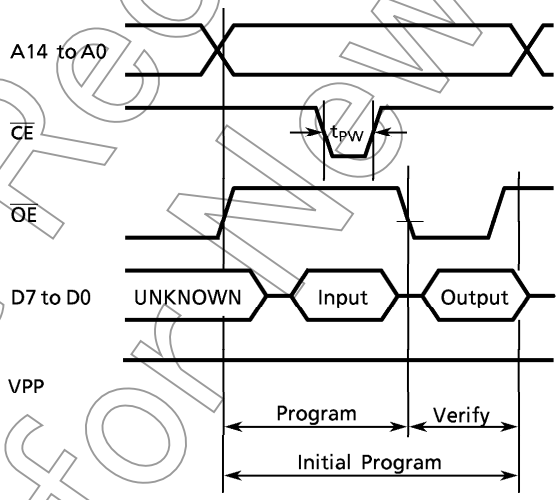
(2) Program Operation (High speed write mode-Ⅰ) (Topr = 25 ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Power Supply Voltage	V_{CC}		5.75	–	6.5	V
Program Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V V_{PP} = 12.5 V ± 0.5 V	0.95	1.0	1.05	ms



(3) Program Operation (High speed write mode - II) (Topr = 25 ± 5 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		6.00	6.25	6.50	V
Program Supply Voltage	V_{PP}		12.50	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V	0.095	0.1	0.105	ms



Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{pp} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.