EPSON

SED157A Series

Dot Matrix LCD Driver

- Support up to 65×224 Display
- Built-in Power Supply Circuit for LCD

■ OVERVIEW

The SED157A Series is a single-chip dot matrix liquid crystal display driver that can be connected directly to a microprocessor bus. Eight-bit parallel or serial display data transmitted from the microprocessor is stored in the internal display data RAM, and the chip generates liquid crystal drive signals, independently of the microprocessor.

It has a on-chip 65 × 256-bit display data RAM, and there is a one-to-one correspondence between the dot pixel on the liquid crystal panel pixels and internal RAM bit. This feature ensures implementation of highly free display.

The SED157A Series incorporate 65 common output circuits and 224 segment output circuits. A single chip can drive a 65 × 224 dot display (capable of displaying 14 columns × 4 rows with 16 × 16-dot kanji font). Further, display capacity can be extended by designing two chips in a master/display configuration.

The SED157A Series can read and write RAM data with the minimum current consumption because it does not require any external operation clock. Also it incorporates a LCD power supply featuring a very low current consumption, a LCD drive power voltage regulator resistor and a display clock CR oscillator circuit. This allows the display system of a high-performance for handy equipment to be realized at the minimum power consumption and minimum component configuration.

■ FEATURES

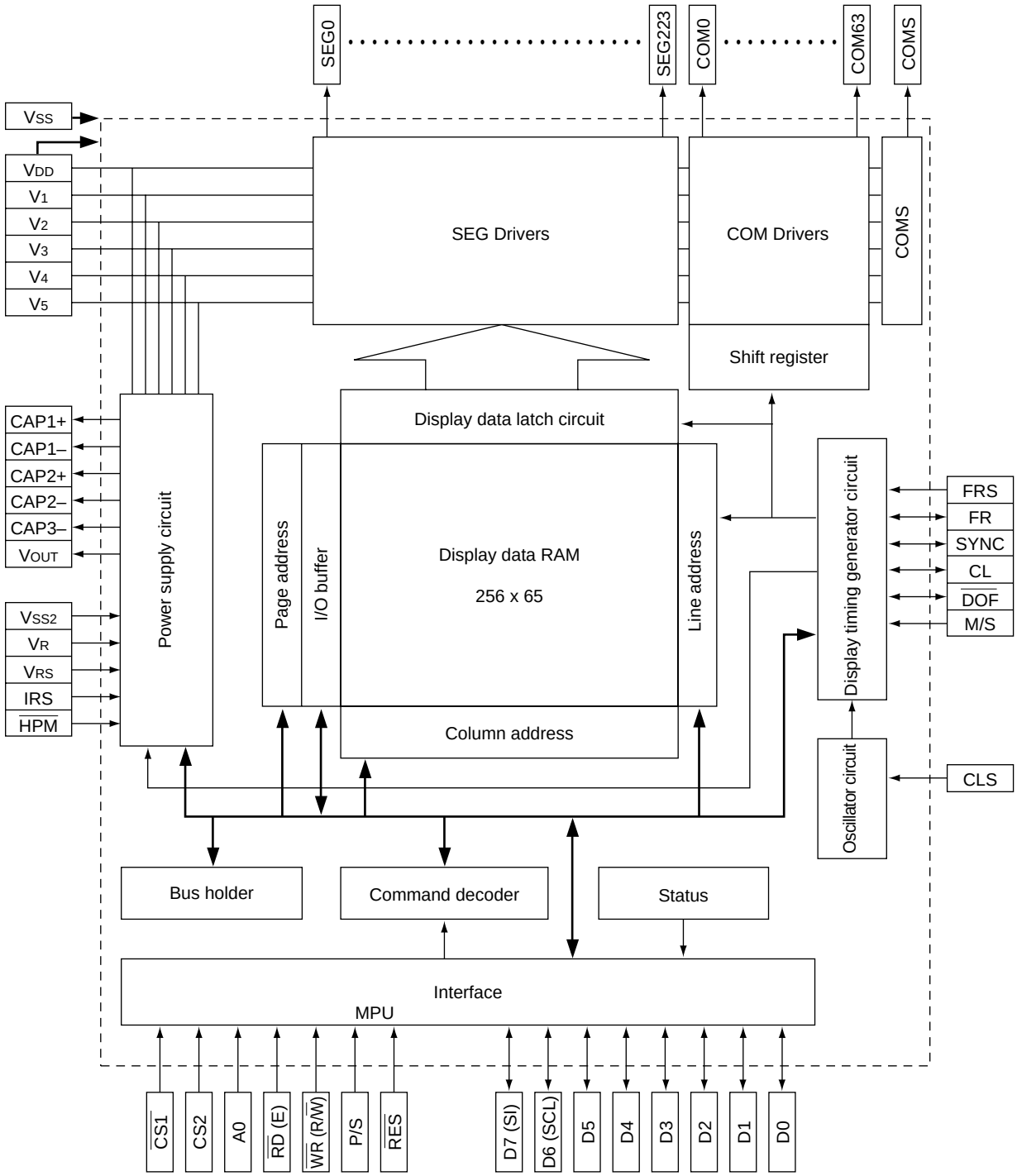
- Direct display of RAM data using the display data RAM
  RAM bit data "1" ..... goes on.
  "0" ..... goes off (at display normal rotation).
- RAM capacity
  65 × 256 = 16,640 bits
- Liquid crystal drive circuit
  65 circuits for the common output and 224 circuits for the segment output
- High-speed 8-bit MPU interface (Both the 80 and 68 series MUPs can directly be connected.)/serial interface enabled
- Abundant command functions
  Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Status Read, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V5 Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, Common Output State Selection, and Built-in Oscillator Circuit ON
- Built-in static drive circuit for indicators (One set, blinking speed variable)

- Built-in power supply circuit for low power supply liquid crystal drive
  Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- 3% high accuracy alternating current voltage adjusting circuit (Temperature gradient: –0.05%/°C)
  Built-in V_5 voltage adjusting resistor, built-in V_1 to V_4 voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Ultra-low power consumption
- Power supplies
  Logic power supply: $V_{DD} – V_{SS}$ = 1.8 to 5.5 V
  Boosting reference power supply: $V_{DD} – V_{SS}$ = 1.8 to 6.0 V
  Liquid crystal drive power supply: $V_5 – V_{DD}$ = –4.5 to –18.0 V
- Wide operating temperature range –40 to 85°C
- CMOS process
- Shipping form Bare chip, TCP
- No light-resistant and radiation-resistant design are provided.

Series specification

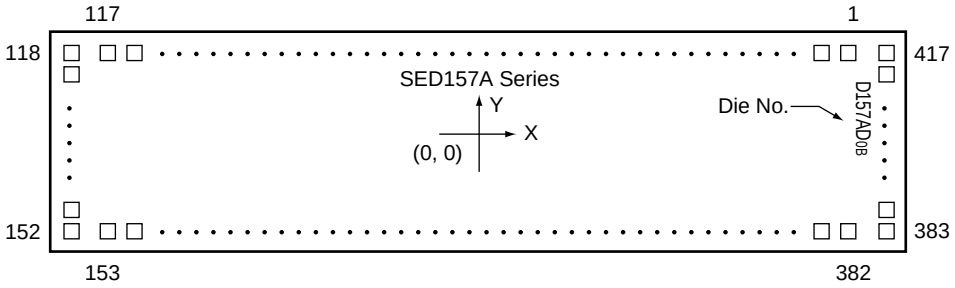
Product name	Duty	Bias	SEG Dr	COM Dr	V_{REG} temperature gradient	Shipping form
SED157AD0B	1/65	1/9, 1/7	224	65	–0.05%/°C	Bare chip
SED157AT0*	1/65	1/9, 1/7	224	65	–0.05%/°C	TCP

■ BLOCK DIAGRAM



■ PIN ASSIGNMENT

● Chip Specification



Item		Size X		Size Y	Unit
Chip size		16.65	×	2.90	mm
Chip thickness		0.625			mm
Bump pitch		69 (Min.)			µm
Bump size	PAD No.1 to 117	85	×	85	µm
	PAD No.118	85	×	73	µm
	PAD No.119 to 151	85	×	47	µm
	PAD No.152	85	×	73	µm
	PAD No.153	73	×	85	µm
	PAD No.154 to 381	47	×	85	µm
	PAD No.382	73	×	85	µm
	PAD No.383	86	×	73	µm
	PAD No.384 to 416	85	×	47	µm
	PAD No.417	85	×	73	µm
Bump height		17 (Typ.)			µm

■ PIN DESCRIPTION

● Power Supply Pin

Pin name	I/O	Description	Number of pins
V_{DD}	Power supply	Commonly used with the MPU power supply pin V_{CC}.	12
V_{SS}	Power supply	0 V pin connected to the system ground (GND)	9
V_{SS2}	Power supply	Boosting circuit reference power supply for liquid crystal drive	5
V_{RS}	Power supply	External input pin for liquid crystal power supply voltage adjusting circuit They are set to OPEN	2
V_1, V_2 V_3, V_4 V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied. The potential needs to be specified based on V_{DD} to establish the relationship of dimensions shown below: $V_{DD} (=V_0) \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ Master operation When the power supply is ON, the following voltages are applied to V_1 ~ V_4 from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command. V_1 1/9•V_5 1/7•V_5 V_2 2/9•V_5 2/7•V_5 V_3 7/9•V_5 5/7•V_5 V_4 8/9•V_5 6/7•V_5	10

● LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
CAP1–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
CAP2+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.	2
CAP2–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.	2
CAP3–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
V_{OUT}	O	Boosting output pin. Connects a capacitor between the pin and V_{SS2}.	2
V_R	I	Voltage adjusting pin. Applies voltage between V_{DD} and V_5 using a split resistor. Valid only when the V_5 voltage adjusting built-in resistor is not used (IRS="L") Do not use VR when the V_5 voltage adjusting built-in resistor is used (IRS="H")	1

● **System Bus Connecting Pins**

Pin name	I/O	Description	Number of pins
D7 to D0 (SI) (SCL)	I/O	An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), D7: Serial data entry pin (SI) D6: Serial clock input pin (SCL) In this case, D0 to D5 are set to high impedance. When Chip Select is in the non-active state, D0 to D7 are set to high impedance.	8
A0	I	Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands. A0="H": Indicates that D0 to D7 are display data. A0="L": Indicates that D0 to D7 are control data.	1
$\overline{RES}$	I	Initialized by setting $\overline{RES}$ to "L". Reset operation is performed at the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	Chip Select signal. When $\overline{CS1}$="L" and CS2="H", this signal becomes active and the input/output of data/commands is enabled.	2
$\overline{RD}$ (E)	I	• When the 80 series MPU is connected, active "L" is set. Pin that connects the $\overline{RD}$ signal of the 80 series MPU. When this signal is "L", the SED157A series data bus is set in the output state. • When the 68 series MPU is connected, active "H" is set. 68 series MPU enable clock input pin	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When the 80 series MPU is connected, active "L" is set. Pin that connects the $\overline{WR}$ signal of the 80 series MPU. The data bus signal is latched on the leading edge of the $\overline{WR}$ signal. • When the 68 series MPU is connected, Read/write control signal input pin R/$\overline{W}$="H": Read operation R/$\overline{W}$="L": Write operation	1
FRS	O	Output pin for static drive Used together with the SYNC pin	1
C86	I	MPU interface switching pin C86="H": 68 series MPU interface C86="L": 80 series MPU interface	1
P/S	I	Switching pin for parallel data entry/serial data entry P/S="H": Parallel data entry P/S="L": Serial data entry According to the P/S state, the following table is given. When P/S="L", D0 to D5 are set to high impedance. D0 to D5 can be "H", "L", or "OPEN". $\overline{RD}$(E) and $\overline{WR}$ (R/W) are fixed to "H" or "L". For the serial data entry, RAM display data cannot be read.	1

P/S	Data/ command	Data	Read/write	Serial clock
"H"	A0	D0 to D7	$\overline{RD}$, $\overline{WR}$	
"L"	A0	SI (D7)	Write-only	SCL (D6)

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks.
CLS=“H”: Built-in oscillator circuit valid
CLS=“L”: Built-in oscillator circuit invalid (external input)
When CLS=“L”, display clocks are input from the CL pin.
When the SED157A series is used for the master/slave configuration, each of the CLS pins is set to the same level together.
<table>
<tr><th>Display clock</th><th>Master</th><th>Slave</th></tr>
<tr><td>Built-in oscillator circuit used
External input</td><td>“H”
“L”</td><td>“H”
“L”</td></tr>
</table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>Pin that selects the master/slave operation for the SED157A series.
The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation.
M/S=“H”: Master operation
M/S=“L” : Slave operation
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>SYNC</th><th>FRS</th><th>DOF</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Valid
Invalid</td><td>Valid
Valid</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Invalid
Invalid</td><td>Invalid
Invalid</td><td>Input
Input</td><td>Input
Input</td><td>Input
Input</td><td>Output
Output</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock I/O pin
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Output
Input</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Input
Input</td></tr>
</table>When the SED157A series is used for the master/slave configuration, each CL pin is connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>Liquid crystal alternating current signal I/O pin
M/S=“H”: Output
M/S=“L”: Input
When the SED157A series is used for the master/slave configuration, each FR pin is connected.</td><td>1</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Liquid crystal synchronizing current signal I/O pin
M/S=“H”: Output
M/S=“L”: Input
When the SED157A series is used for the master/slave configuration, each SYNC pin is connected.</td><td>2</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>Liquid crystal display blanking control pin
M/S=“H”: Output
M/S=“L”: Input
When the SED157A series is used for the master/slave configuration, each $\overline{DOF}$ pin is connected.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>V_5 voltage adjusting resistor selection pin
IRS=“H”: Built-in resistor used
IRS=“L”: Built-in resistor not used. The V_5 voltage is adjusted by the V_R pin and stand-alone split resistor.
Valid only at master operation. The pin is fixed to “H” or “L” at slave operation.</td><td>1</td></tr>
<tr><td>$\overline{HPM}$</td><td>I</td><td>Power supply control pin of the power supply circuit for liquid crystal drive
$\overline{HPM}$=“H”: Normal mode
$\overline{HPM}$=“L”: High power supply mode
Valid only at master operation. The pin is fixed to “H” or “L” at slave operation.</td><td>1</td></tr>
</table>

● Liquid Crystal Drive Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>SEG0
to
SEG223</td><td>O</td><td>Output pins for the LCD segment drive. Contents of the display RAM and FR signal are combined to select a desired level among V_{DD}, V_2, V_3 and V_5.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Display normal operation</th><th>Display reversal</th></tr>
<tr><td>H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>224</td></tr>
<tr><td>COM0
to
COM63</td><td></td><td>Output pins for the LCD common drive. Scan data and FR signal are combined to select a desired level among V_{DD}, V_1, V_4 and V_5.
<table>
<tr><th>Scanning data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_5</td></tr>
<tr><td>H</td><td>L</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td>64</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator dedicated COM output pin
Set to OPEN when not used
When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.</td><td>2</td></tr>
</table>

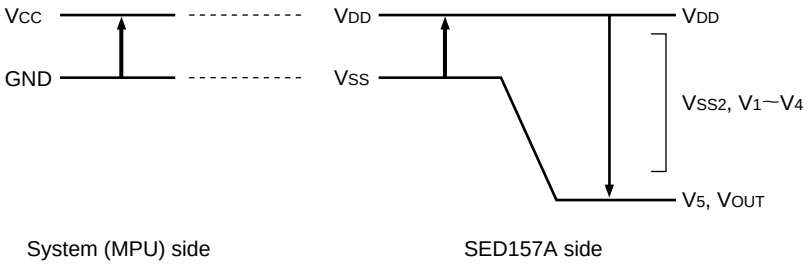
● Test Pin

Pin name	I/O	Description	Number of pins
TEST1 to 4, 10 to 13	I/O	IC chip test pin. Fix the pin to “H”.	8
TEST5 to 9, 14 to 16	I/O	IC chip test pin. Take into consideration so that the capacity of lines cannot be exhausted by setting the pin to OPEN.	13

■ ABSOLUTE MAXIMUM RATINGS

V_{SS}=0 V unless specified otherwise

Item		Symbol	Specification value			Unit
Power supply voltage		V_{DD}	–0.3	to	+7.0	V
Power supply voltage (2) (Based on V_{DD})		V_{SS2}	–7.0	to	+0.3	
	At triple boosting		–6.0	to	+0.3	
	At quadruple boosting		–4.5	to	+0.3	
Power supply voltage (3) (Based on V_{DD})		V_5, V_{OUT}	–22.0	to	+0.3	
Power supply voltage (4) (Based on V_{DD})		V_1, V_2, V_3, V_4	V_5	to	+0.3	
Input voltage		V_{IN}	–0.3	to	V_{DD}+0.3	
Output voltage		V_{OUT}	–0.3	to	V_{DD}+0.3	
Operating temperature		T_{OPR}	–40	to	+85	°C
Storage temperature	TCP	T_{STR}	–55	to	+100	
	Bare chip		–55	to	+125	



Notes: 1. The values of the V_{SS2}, V_1 to V_5, and V_{OUT} voltages are based on V_{DD}=0 V.
2. The V_1, V_2, V_3, and V_4 voltages must always satisfy the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Insure that voltage levels V_{SS2} and V_{OUT} are always such that the relationship of $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$ is maintained.
4. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

■ DC Characteristics

V_{SS}=0 V, V_{DD}=3.0 V ± 10%, and Ta=–40 to 85°C

Item		Symbol	Condition		Specification value Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)	Recommended operation	V_{DD}			2.7	—	3.3	V	V_{DD}
	Operable	V_{DD}			1.8	—	5.5		V_{DD}
Operating voltage (2)	Recommended operation	V_{SS2}	(Based on V_{DD})		–3.3	—	–2.7		V_{SS2}
	Operable	V_{SS2}	(Based on V_{DD})		–6.0	—	–1.8		V_{SS2}
Operating voltage (3)	Operable	V_5	(Based on V_{DD})		–18.0	—	–4.5		V_5
	Operable	V_1, V_2	(Based on V_{DD})		0.4×V_5	—	V_{DD}		V_1, V_2
	Operable	V_3, V_4	(Based on V_{DD})		V_5	—	0.6×V_5		V_3, V_4
High level input voltage		V_{IHC}			0.8×V_{DD}	—	V_{DD}		
Low level input voltage		V_{ILC}			V_{SS}	—	0.2×V_{DD}		
High level output voltage		V_{OHC}	I_{OH}=–0.5mA		0.8×V_{DD}	—	V_{DD}		
Low level output voltage		V_{OLC}	I_{OL}=0.5mA		V_{SS}	—	0.2×V_{DD}		
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}		–1.0	—	1.0	µA	
Output leak current		I_{LO}			–3.0	—	3.0		
Liquid crystal driver On resistance		R_{ON}	Ta=25°C	V_5=–14.0V	—	2.0	3.5	KΩ	SEGn
			(Based on V_{DD})	V_5=–8.0V	—	3.2	5.4		COMn
Static current consumption		I_{SSQ}			—	0.01	5	µA	V_{SS}, V_{SS2}
Output leak current		I_{5Q}	V_5=–18.0V (Based on V_{DD})		—	0.01	15		V_5
Input pin capacity		C_I	Ta=25°C, f=1MHz		—	5.0	8.0	pF	
Oscillating frequency	Built-in oscillation	f_{OSC}	Ta=25°C		18	22	26	kHz	
	External input	f_{CL}			4.5	5.5	6.5		CL

Item		Symbol	Condition		Specification value Min.	Typ.	Max.	Unit	Applicable pin
Built-in power supply circuit	Input voltage	V_{SS2}	At triple boosting (Based on V_{DD})		–6.0	—	–1.8	V	V_{SS2}
		V_{SS2}	At quadruple boosting (Based on V_{DD})		–5.0	—	–1.8		V_{SS2}
	Boosting output voltage	V_{OUT}	(Based on V_{DD})		–20.0	—	—		V_{OUT}
	Voltage adjusting circuit operating voltage	V_{OUT}	(Based on V_{DD})		–20.0	—	–6.0		V_{OUT}
	V/F circuit operating voltage	V_5	(Based on V_{DD})		–18.0	—	–4.5		V_5
	Reference voltage	V_{REG0}	Ta=25°C,	–0.05%/°C	–2.04	–2.10	–2.16		

Dynamic current consumption value (1) During display operation and built-in power supply OFF
Current values dissipated by the whole IC when the external power supply is used

Display All White Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
Dynamic current consumption	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	25	42	µA	
		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	25	42		

Display Checker Pattern Ta=25°C

Item	Symbo	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
Dynamic current consumption	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	38	64	µA	
		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	38	64		

Dynamic current consumption value (2) During display operation and built-in power supply ON
Current values dissipated by the whole IC containing the built-in power supply circuit

Display Checker Pattern Ta=25°C

Item	Symbo	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
Dynamic current consumption	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	92	154	µA	
		V_5–V_{DD}=–11.0V	High power mode	—	242	405		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	129	216		
		V_5–V_{DD}=–11.0V	High power mode	—	310	518		

Display Checker Pattern Ta=25°C

Item	Symbo	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
Dynamic current consumption	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	132	221	µA	
		V_5–V_{DD}=–11.0V	High power mode	—	280	468		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	167	279		
		V_5–V_{DD}=–11.0V	High power mode	—	350	585		

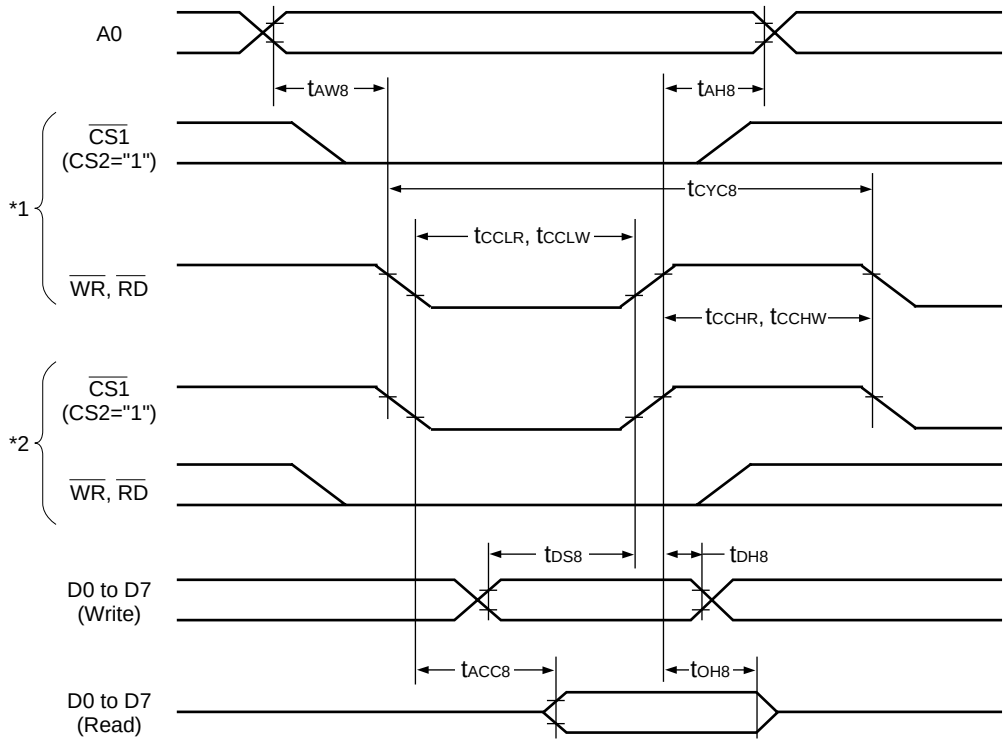
Current consumption at power save V_{SS}=0V and V_{DD}= 3.0 V ±10%

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}		—	0.01	5	µA	
Stand-by state	I_{DDS2}		—	4	8		

■ TIMING CHARACTERISTICS

● System bus read/write characteristics 1 (80 series MPU)



[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		333	—	
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	—	
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	
Data setup time	D0 to D7	t_{DS8}		30	—	
Data hold time		t_{DH8}		10	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	70	
Output disable time		t_{OH8}		5	50	

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

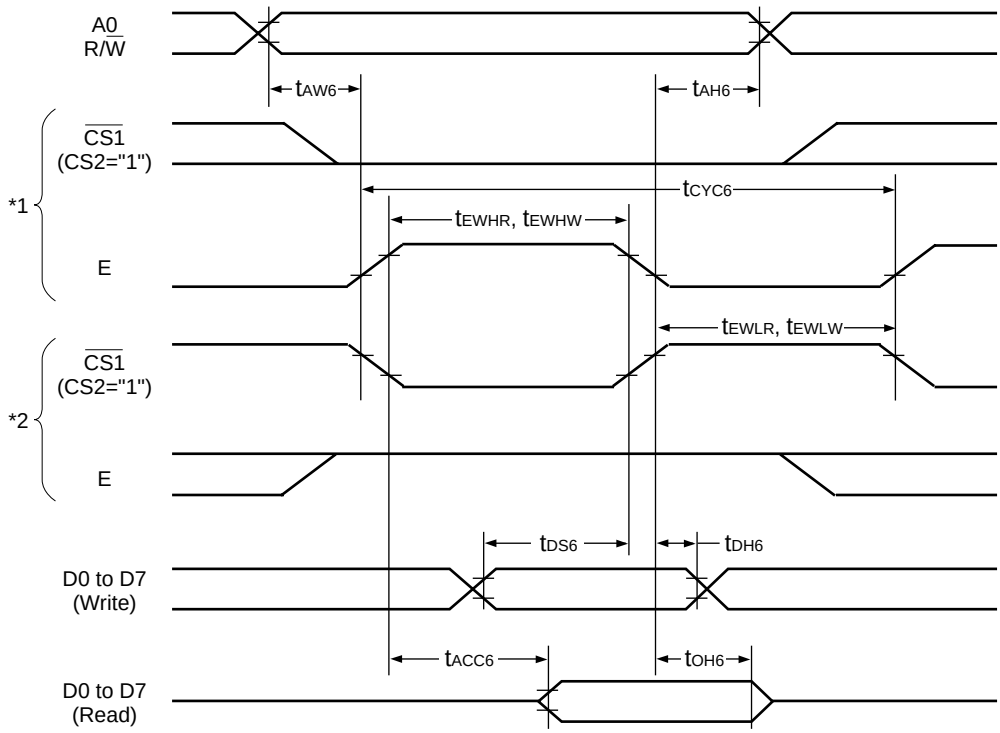
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		500	—	
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	
Data setup time	D0 to D7	t_{DS8}		40	—	
Data hold time		t_{DH8}		15	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	140	
Output disable time		t_{OH8}		10	100	

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		1000	—	
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	—	
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	—	
Data setup time	D0 to D7	t_{DS8}		80	—	
Data hold time		t_{DH8}		30	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	280	
Output disable time		t_{OH8}		10	200	

Notes: 1. This is the case of accessing by $\overline{WR}$ and $\overline{RD}$ when $\overline{CS1}$ = “L”.
2. This is the case of accessing by $\overline{CS1}$ when $\overline{WR}$ and $\overline{RD}$ = “L”.
3. The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t_r+t_f) ≤ (t_{CYC8}–t_{CCLW}–t_{CCHW}) or (t_r+t_f) ≤ (t_{CYC8}–t_{CCLR}–t_{CCHR}).
4. All timings are specified based on the 20 and 80% of V_{DD}.
5. t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS1}$ is at “L” (CS2= “H”) level and $\overline{WR}$, $\overline{RD}$ are at the “L” level.

● **System bus read/write characteristics 2 (68 series MPU)**



[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		333	—	
Data setup time		D0 to D7	t_{DS6}		30	—	
Data hold time			t_{DH6}		10	—	
Access time			t_{ACC6}	CL=100pF	—	70	
Output disable time			t_{OH6}		10	50	
Enable H pulse width	Read	E	t_{EWHR}		70	—	
	Write		t_{EWHW}		30	—	
Enable L pulse width	Read	E	t_{EWLR}		30	—	
	Write		t_{EWLW}		30	—	

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

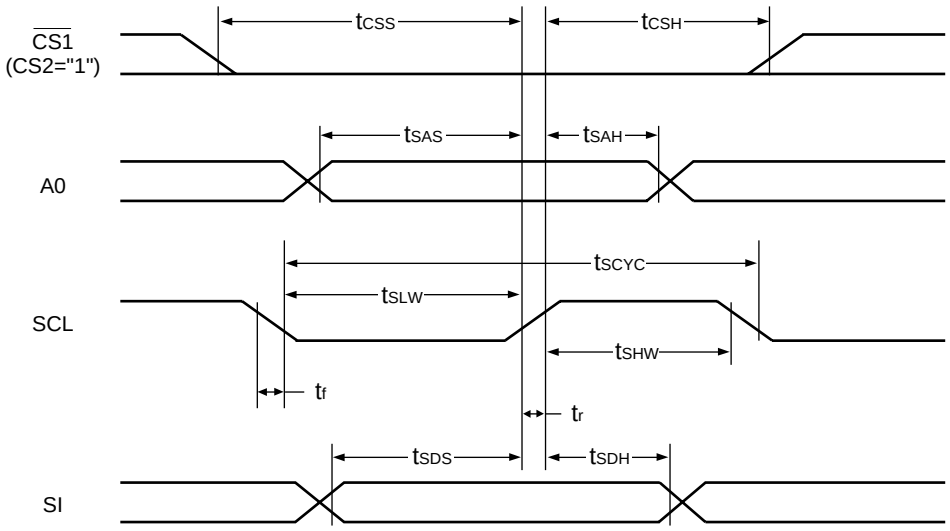
Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		500	—	
Data setup time		D0 to D7	t_{DS6}		40	—	
Data hold time			t_{DH6}		15	—	
Access time			t_{ACC6}	CL=100pF	—	140	
Output disable time			t_{OH6}		10	100	
Enable H pulse width	Read	E	t_{EWHR}		120	—	
	Write		t_{EWHW}		60	—	
Enable L pulse width	Read	E	t_{EWLR}		60	—	
	Write		t_{EWLW}		60	—	

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		1000	—	
Data setup time		D0 to D7	t_{DS6}		80	—	
Data hold time			t_{DH6}		30	—	
Access time			t_{ACC6}	CL=100pF	—	280	
Output disable time			t_{OH6}		10	200	
Enable H pulse width	Read	E	t_{EWHR}		240	—	
	Write		t_{EWHW}		120	—	
Enable L pulse width	Read	E	t_{EWLR}		120	—	
	Write		t_{EWLW}		120	—	

Notes: 1. This is the case of accessing by E when $\overline{CS1}$ = “L”.
2. This is the case of accessing by $\overline{CS1}$ when E = “H”.
3. The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t_r+t_f) ≤ (t_{CYC6}–t_{EWLW}–t_{EWHW}) or (t_r+t_f) ≤ (t_{CYC6}–t_{EWLR}–t_{EWHR}).
4. All timings are specified based on the 20 and 80% of V_{DD}.
5. t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS1}$ is at “L” (CS2 = “H”) level and E is at the “H” level.

● **Serial interface**



[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		200	—	ns
SCL “H” pulse width		t_{SHW}		75	—	
SCL “L” pulse width		t_{SLW}		75	—	
Address setup time	A0	t_{SAS}		50	—	
Address hold time		t_{SAH}		100	—	
Data setup time	SI	t_{SDS}		50	—	
Data hold time		t_{SDH}		50	—	
CS-SCL time	CS	t_{CSS}		100	—	
		t_{CSH}		100	—	

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

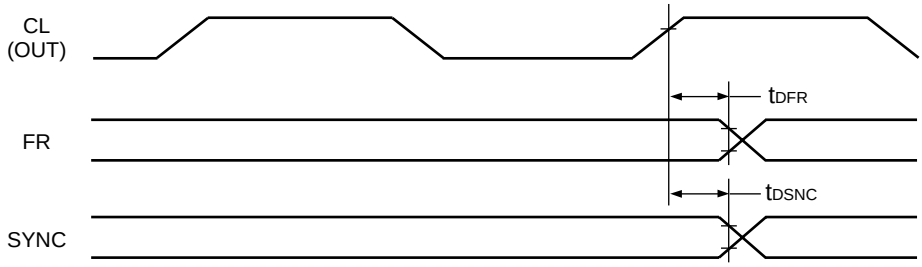
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		250	—	ns
SCL “H” pulse width		t_{SHW}		100	—	
SCL “L” pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	
Data hold time		t_{SDH}		100	—	
CS-SCL time	CS	t_{CSS}		150	—	
		t_{CSH}		150	—	

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		400	—	ns
SCL “H” pulse width		t_{SHW}		150	—	
SCL “L” pulse width		t_{SLW}		150	—	
Address setup time	A0	t_{SAS}		250	—	
Address hold time		t_{SAH}		250	—	
Data setup time	SI	t_{SDS}		150	—	
Data hold time		t_{SDH}		150	—	
CS-SCL time	CS	t_{CSS}		250	—	
		t_{CSH}		250	—	

Notes: 1. The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns.
2. All timings are specified based on the 20 and 80% of V_{DD}.

● **Display control output timing**



[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	10	40	ns
SYNC delay time	SYNC	t_{DSNC}	C_L=50pF	—	10	40	ns

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

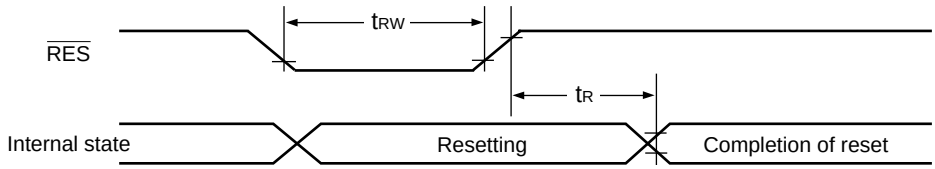
Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	20	80	ns
SYNC delay time	SYNC	t_{DSNC}	C_L=50pF	—	20	80	ns

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	50	200	ns
SYNC delay time	SYNC	t_{DSNC}	C_L=50pF	—	50	200	ns

Notes: 1. Valid only when the master mode is selected.
2. All timings are specified based on the 20 and 80% of V_{DD}.
3. Pay attention not to cause delays of the timing signals C_L, FR and SYNC to the salve side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.

● **Reset input timing**



[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	0.5	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		0.5	—	—	

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		1	—	—	

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		1.5	—	—	

Note: All timings are specified based on the 20 and 80% of V_{DD}.

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