[Channel Lab]
Suwon P.O BOX 416,
Maetan-3dong, Youngtong-gu, Suwon-si,
Gyeonggi-do, Korea 442-742
T: 82-31-279-7640

S5H1420

[Channel Decoder for DVB-S/DSS]

DATA SHEET

Samsung Electronics Co, Ltd.

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Note: This documentation is preliminary and is subject to change. Samsung Electronics Co, Ltd. reserves the right to do any kind of modification in this data sheet regarding hardware or software implementations without notice.

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1. INTRODUCTION

1.1 Overview

The S5H1420 is a single chip channel decoder IC for DBS (Digital Broadcasting System for Satellite) receiver. It consists of a multi-standard QPSK/BPSK demodulator and FEC (Forward Error Correction) decoder compliant with DVB-S and DSS standard. For multi-antenna control it provides DiSEqC1.x and 2.0 standards.

1.2 Features

- Compliant to DVB-S and DSS standard.
- Single chip decoder (ADC/QPSK/FEC).
- Flexible Interface (I^2C, MPEG2).
- DiSEqC 1.x or 2.0 specification support.
- Satellite dish control.
- DC offset cancellation.
- Automatic gain control
- Nyquist filter: 0.35 for DVB-S, 0.2 for DSS.
- Fully digital synchronization.
  Symbol timing recovery range up to ± 50000 ppm.
  Carrier recovery range up to ±12.5% of symbol rate.
- Carrier offset cancellation up to ±1/2sampling frequency
- Modulation rate from 1 to 87Mbps(1 ~ 50 Msps)
- QPSK demodulation quality estimation
- Viterbi decoding quality estimation.
  Viterbi Input and output BER measurement.
  Support depuncturing code rate from 1/2 to 7/8.
- Convolutional deinterleaver and Reed-Solomon decoder
- Automatic byte and frame synchronization
- Automatic spectral inversion ambiguity resolution.
- I^2C repeater for RF part
- Power down control
- Low power CMOS technology
- 3.3V Single power using diode for 2.5V
- Compact size package: 64LQFP-1010

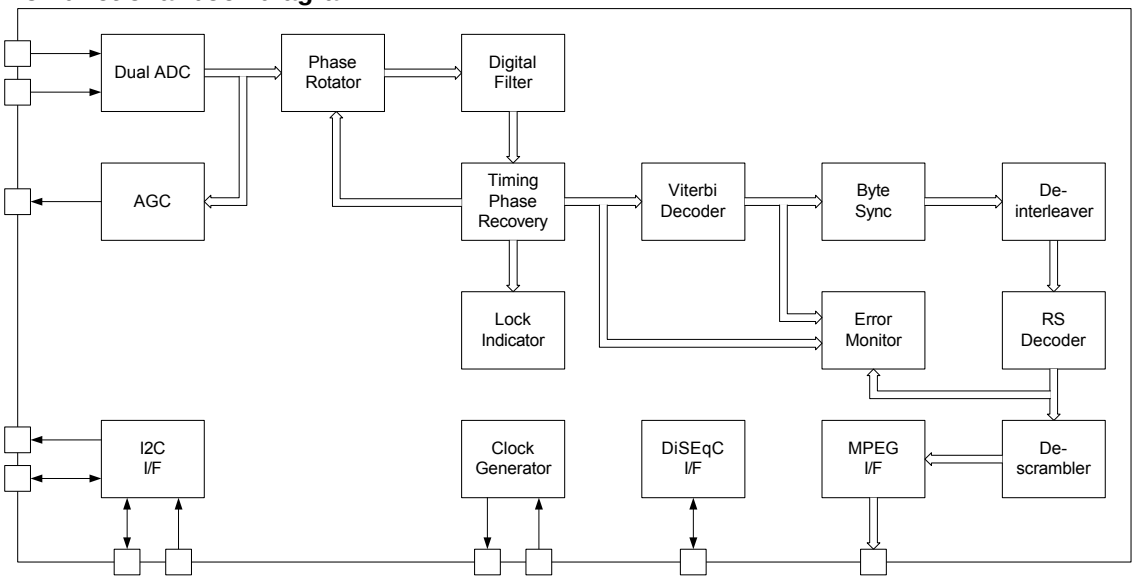
1.3 Applications

DVB-S Receiver and STB
Digital satellite TV
PCI satellite Card

1.4 Ordering information

Type Number	Package	Description
1. S5H1420X01	64 LQFP-1010	Plastic Low Profile Quad Flat Package; 64 leads (lead length 1.0mm) Body 10x10x1.0 mm

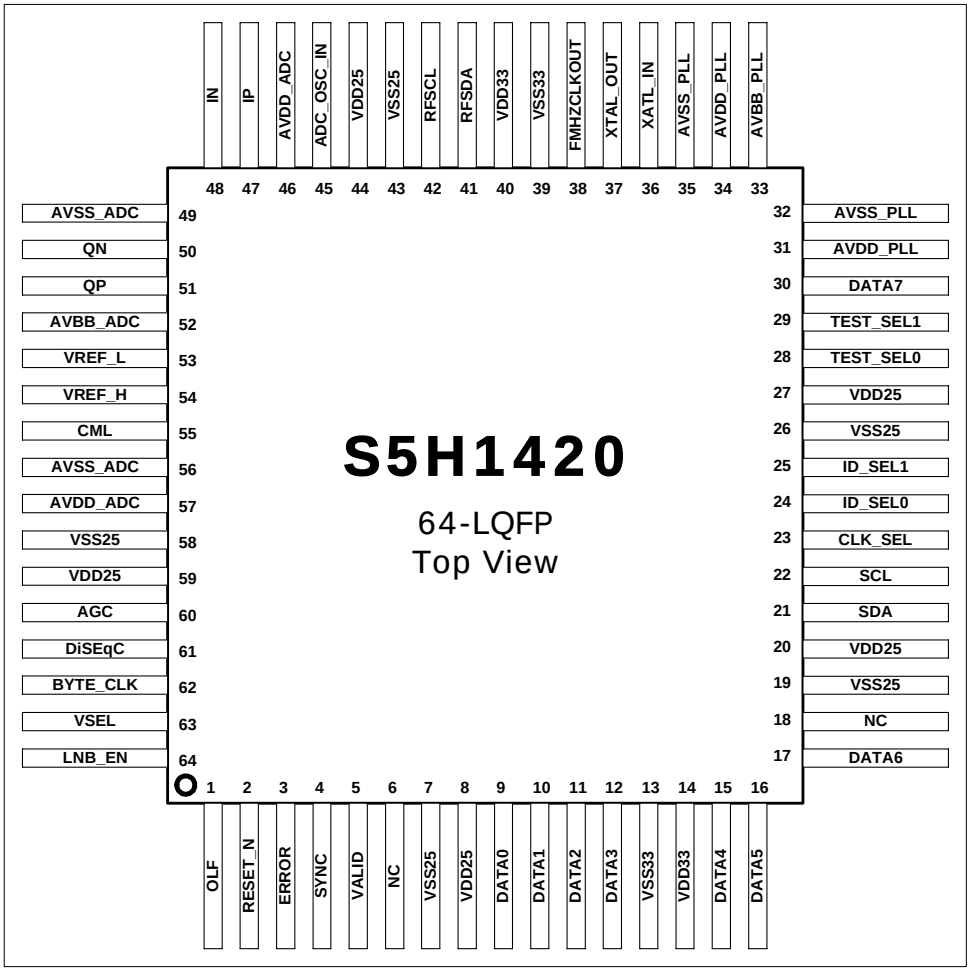
1.5 Functional bock diagram



2. PIN INFORMATION

2.1 Pin Assignment

Figure1: Pin-out for 64-pin LQFP



2.2 Pin descriptions

Pin Name	I/O Cell Type	Pin Number	Description
OLF	Input	1	LNB Over Load Flag
RESET_N	Schmitt Trigger	2	H/W Reset (Active Low)
ERROR	Error_out	3	Error indicator output
SYNC	Sync_out	4	Synchronization output
VALID	Valid_out	5	Valid data period
NC	NC	6	NC
DATA	Output [7]	30	MPEG2 Stream Serial Data
DATA	Output [7:0]	[:]	MPEG2 Stream Parallel Data [Pin 30,17,16,15,12,11,10,9]
SDA	I/O-open drain(5V)	21	Serial Data from host
SCL	Input(5V)	22	Serial Clock from host
CLK_SEL	Input	23	Master Clock Select
ID_SEL0	Input	24	I2C Address Select[T0]
ID_SEL1	Input	24	I2C Address Select[T1]
TEST_SEL0	Input	28	Test Mode Select[T2]
TEST_SEL1	Input	29	Test Mode Select[T3]
NC	NC	18	No connection
XTAL_IN	Oscillator Input	36	Crystal Oscillator Input
XTAL_OUT	Oscillator Output	37	Crystal Oscillator Output
FMHZCLKOUT	Output	38	Reference Clock Output
RFSDA	I/O-open drain (5V)	41	RF Module Control SDA
RFSCL	n-ch-open drain (5V)	42	RF Module Control SCL
ADC_OSC_IN	Oscillator Input	45	Oscillator Input
AVDD_ADC	Digital Power	46	ADC Total Power
IP	Inphase Positive	47	ADC Analog Input
IN	Inphase Negative	48	ADC Analog Input
QN	Quadrature Negative	50	ADC Analog Input
QP	Quadrature Positive	51	ADC Analog Input
VREF_L	Analog Reference	53	ADC Bottom Reference Voltage
VREF_H	Analog Reference	54	ADC Top Reference Voltage
CML	Analog Reference	55	Common Mode Level Voltage
AGC	n-ch Open Drain(5V)	60	Gain Control Output
DISEQC	Bidirectional (5V)	61	Antenna Select
BYTE_CLOCK	Output (3.3V)	62	Data Transfer clock
VSEL	Output	63	LNB Voltage Select Flag
LNB_EN	Output	64	LNB Enable Flag
RF Interface & ADC Power Supply (24)			
ADC	AVDD_ADC	46, 57	
	AVSS_ADC	56, 49	
	AVBB_ADC	52	
PLL	AVDD_PLL	31	
	AVSS_PLL	32	
	AVBB_PLL	33	
	AVDD_PLL	34	
	AVSS_PLL	35	
IO	VSS33	13, 39	
	VDD33	14, 40	
Logic	VSS25	7, 19, 26, 43, 58	
	VDD25	8, 20, 27, 44, 59	

3. FUNCTIONAL DESCRIPTION

3.1 Signal processing

3.1.1 I and Q inputs

The dual ADC can get differential (IP/IN, QP/QN) or single inputs (IP, QP), I/Q signals from the tuner are fed to the IP and QP inputs through a DC coupling capacitor and IN and QN must be set DC voltage as CML (typical: 1/2VDD). The reference voltage of high [VREF-H] and low [VREF-L] should be supplied from external generator for application flexibility.

3.1.2 PRE-AGC

The power of I/Q signal is compared to a programmable threshold value, and the difference is integrated. This signal is then converted into a Pulse Width Modulation (PWM) signal to drive the AGC output and it will be low pass filtered by a simple RC analog filter to control the gain command of any amplifier before the A/D converter. The PWM output operates at f_{clk}/ (1, 4, 8 and 16) in order to decrease the radiated noise and to simplify the filter design, and is a 5 V tolerant open drain stage.
The PRE-AGC Controls are in Address 0x07 and the PRE-AGC integrator register is in Address 0x15.

3.1.3 Root raised cosine and rate conversion filter

The Root raised cosine (RRC) and rate conversion filter performs anti-aliasing filtering, root raised cosine shaping, rate conversion, timing synchronization and tracking with the timing loop.
Two roll-off factors are available: 0.35 (DVB-S) and 0.20 (DSS).

3.1.4 Offset cancellation

This device suppresses the residual I/Q DC component in the QPSK system control register in Addresses 0x05 and 0x06.

3.1.5 POST-AGC

The POST-AGC shall be able to adjust the gain of the incoming I/Q sample from the RRC and rate conversion filter and implement the closed loop that sets the gain adjustment. The reset value (0x8000) of the POST-AGC integrator register can allow an initial settling time of less than 50k master clock periods.
The POST-AGC Controls are in Address 0x08 and the POST-AGC integrator register is in Address 0x16.

3.2 Timing recovery

3.2.1 Timing control

The timing loop is programmed with the expected symbol frequency.
We have δ parameter, which determine one or two sampling method. It can be expressed as:

$$(1+\alpha)\cdot fsym > \frac{f_{clk}}{2} \text{ for } \delta = 1.$$

In contrast,

$$(1+\alpha)\cdot fsym < \frac{f_{clk}}{2} \text{ for } \delta = 2.$$

Where α is roll-off factor: 0.35 for DVB-S, 0.2 for DSS.
Thus

Timing NCO frequency word register setting is:

$$\text{NCO frequency word} = \frac{f_{sym}}{f_{clk}} \cdot 2^{24} \cdot \delta$$

3.2.2 Loop equation

The timing loop may be considered as a second order loop. The loop equation may be calculated using the following formula:

$$\varepsilon = 1 << ((P_g + 8) - I_g)$$

$$\omega = \Phi_t \cdot (1 << I_g)$$

Where, P_g is propagational gain, I_g is integral gain and Φ_t is timing factor.

$$\Phi_t = 5.0 \times \frac{\frac{1}{2^{24}}}{\frac{f_{sym}}{f_{clk}}}$$

And we can choose Loop Bandwidth (*BL*), as follows:

$$BL = \omega \times \frac{1}{2} \times \xi \times (1 + \frac{1}{4\xi^2})$$

Where ξ is the reference level of the ε and ω.

$$\xi = \frac{\omega \times \varepsilon}{2}$$

3.2.3 Timing lock indicator

The timing detector need to a lot of symbols for stabilization in order to lock after tuning frequency change of RF and it takes a 1-bit input signal, and uses the presence or absence of locking information to either count up or count down respectively.

The counter operates up to reaches its maximum value when the lock signal goes active. Two cases can cause the lock signal to go to unlocked state; one is assertion of the active-low reset and the other the counter go zero again. User can monitor the MSB 8 bits of TLL (timing lock loop) counter in Address 0x1a and the TLL lock flag in Address 0x14.

3.3 Carrier recovery

The tracking range of the derotator is ± f_{clk} /2 (± $f_{sampling}$/2).

This algorithm is used with QPSK reception, over a small range of capture phases and with a channel noise value over 3.0 dB.

3.3.1 Loop equation

Like the timing loop, the carrier loop is a second-order system where two parameters, ε and ω.

$$\varepsilon = 1 << ((P_g + 8) - I_g)$$

$$\omega = \Phi_p \cdot (1 << I_g)$$

Where, P_g is propagational gain, I_g is integral gain and Φ_p is phase factor.

$$\Phi_p = 75.4 \times \frac{\frac{1}{2^{24}}}{\frac{f_{sym}}{f_{clk}}}$$

Also, we can choose Loop Bandwidth (*BL*), as follows:

$$BL = \omega \times \frac{1}{2} \times \xi \times (1 + \frac{1}{4\xi^2})$$

Where ξ is the reference level of the ε and ω.

$$\xi = \frac{\omega \times \varepsilon}{2}$$

3.3.2 Carrier lock detector

The carrier lock detector operates the same as the timing lock detector in the Phase locked loop (PLL). User can monitor the MSB 8 bits of PLL lock counter in Address 0x19 and the PLL lock flag in Address 0x14.

3.3.3 Derotator frequency

The derotator frequency can be either measured (read operation) or forced (write operation).

$$f_{derot} = \frac{f_{sym} \times 2^{24}}{f_{clk}}$$

3.3.4 Automatic frequency detector

The automatic frequency detector (AFD) can evaluate the carrier frequency offset quickly, and may be coupled to the carrier recovery loop.
The digital loop filter of PLL has two paths, proportional and integral, with programmable gain respectively. The integral path contains an accumulator whose contents can be analyzed as a averaged carrier frequency offset.
The phase error signal goes into two paths, the respective gains are applied, the “I” path is integrated, and the two are added together. A Kicker of AFD can help PLL to achieve lock fast. The Kicker finds the phase error signal for large transitions, inserts a large value, into the “I” path. Therefore, PLL can trace the large frequency offset.

3.3.5 False lock

A false lock occurs when phase lock has been detected in the QPSK, but the correct central frequency has not yet been reached. This situation occurs in QPSK for frequency offset points that are multiples of $f_{sym}/4$, where f_{sym} is the QPSK symbol rate, and also at other offsets dictated by the discrete nature of the carrier recovery loop. Therefore, the carrier recovery loop must be handled to take care of a false lock condition.

3.4 Forward Error Correction

3.4.1 FEC modes

Since the S5H1420 is a multi-standard decoder, several combinations are possible, at different levels:
- the demodulator may accept either QPSK or BPSK signals - the only impact is on the carrier algorithm choice. The algorithm choice also affects the carrier lock detector and the noise evaluation.
- there are two primary options concerning the FEC operation - between DVB-S, DSS and Reserved Mode.
- there are two options concerning the FEC feeding. The first is IQ flow, which is the usual case in QPSK modes DVB-S or DSS. The second mode is I-only flow, used for BPSK.

The FEC Mode Register is in Address Hex 22.
In Modes DVB-S and DSS, data is fed to the Soft Decisions.

3.4.2 Soft decisions

The adaptive equalizer output is converted into 4-bit sign-magnitude format by the soft decision block, for use by the Viterbi decoder. The MSB corresponds to the sliced bit value. The 3 LSBs of the soft decisions represent the confidence of the sliced bit value, where 111 are high confidence, and 000 is low confidence. A programmable set of thresholds can be used in generating the three LSBs and, consequently, in optimizing the Viterbi decoder performance as a function of code rate.

3.4.3 Viterbi decoder and synchronization

The convolutional codes are generated by the polynomial G_x = 171 octets and G_y = 133 octets in modes DVB-S or DSS. The Viterbi decoder computes for each symbol the metrics of the four possible paths, proportional to the square of the Euclidian distance between the received I and Q and the theoretical symbol value.
The puncture rate and phase are estimated on the error rate basis. Several rates are allowed and may be enabled/disabled through register programming:

■1/2, 2/3, 3/4, 5/6, 7/8 for DVB-S
■1/2, 2/3, 6/7 for DSS
For each enabled rate, the current error rate is compared to a programmable threshold.
If it is greater than this threshold, another phase (or another rate) is tried until the right rate is obtained.
A programmable hysterics is added to avoid losing the phase during short-term perturbation. The rate may also be imposed by external software, and the phase is incremented only upon request by the microprocessor. The error rate may be read at any time in order to use an algorithm other than that implemented.
The Viterbi decoder produces an absolute decoding. The decoder is controlled via several Viterbi Threshold Registers (Registers 29, 2A, 2B, 2C, 2D and 2E). For each Viterbi Threshold Register, bits 7 to 0 represent a normalization rate threshold – the average number of normalization occurring during sync periods. The sync period is controlled via Viterbi Sync Register (Register 2F). The puncture Rate and Viterbi initial configuration is in Address 30, 31. The automatic rate research is only done through the enabled rates (see the corresponding bit set in the Puncture register). In DSS, it is recommended that you disable puncture rates 3/4, 5/6 and 7/8 in order to save time in the synchronization process.
The Viterbi decoder sync search can control using the Puncture register.

3.4.4 Synchronization

In DVB-S, the packet length after inner decoding is 204. The sync word is the first byte of each packet. Its value is Hex 47, but this value is complemented every 8 packets. In DSS, the packet length is 147 and the sync word is Hex 1D.
An Up/Down Sync counter counts whenever a sync word is recognized with the correct timing and counts down during each missing sync word.
This counter is bounded by a programmable maximum - when this value is reached, the SYNC_FLAG bit (“locked”) is set in the SYNC02 register. When the event counter counts down to until 0, this flag is reset.

3.4.5 Error monitoring

A 16-bit counter, ERRCNT, allows the counting of errors at different levels. ERRCNT is fed either by:
■ the input QPSK bit errors (that are corrected by the Viterbi decoder), or,
■ the bit, or,
■ the byte error (it will be corrected by the Reed-Solomon decoder)
■ the packet error (It is uncorrectable and lead to a pulse at the ERROR output)

The content of ERRCNT may be transferred to the read only registers ERR_CNT_L (LSB) and ERR-CNT_H (MSB). Two functional modes are proposed, depending on a control register bit:
1. ERR_DISP = 0. The uncorrectable block flag ERROR that error count is not incremented.
2. ERR_DISP = 1. The uncorrectable block flag ERROR that error is counted as 27 erroneous bits (It has nine erroneous bytes with three corrupted bits per byte).

3.4.6 Convolutional deinterleaver

In DVB-S, the Convolutional deinterleaver is 17×12. The periodicity of 204 bytes per sync byte is retained. In DSS, the Convolutional deinterleaver is 146×13, and there is also a periodicity of 147 bytes per sync byte. The deinterleaver may be bypassed.

3.4.7 Reed-Solomon decoder and descrambler

The input blocks are 204-byte long with 16 parity bytes in DVB-S. The sync byte is the first byte of the block. Up to 8 byte errors may be fixed.
The code generator polynomial is:
$g(\chi) = (\chi - \alpha^0)(\chi - \alpha^1)(...)(\chi - \alpha^{15})$
Over the Galois Field generated by:
$$\alpha^8 + \alpha^4 + \alpha^3 + \alpha^2 + 1 = 0$$
Energy dispersal descrambler and output energy dispersal descrambler generator:
$$\chi^{15} + \chi^{14} + 1$$
The polynomial is initialized every eight blocks with the sequence 100101010000000.
The sync words are unscrambled and the scrambler is reset every 8 packets.

The output interface may be forced into high impedance mode by setting MPEG_OEN =0 in the Address 39. Doing this affects the DATA [7:0], BYTE_CLOCK, SYNC, VALID and ERROR pins. The output stream is either parallel (byte stream) or serial (bit stream) depending on bit 1 of Address 39.

3.4.8 Spectrum Inverse of Code Rate 5/6

In case of Code Rate 5/6, because of its character, regardless of condition of spectrum it can be locked. Rest of the code rates except 5/6, if Viterbi is locked, byte becomes sync but in case of code rate 5/6, even if Viterbi is locked there are chances byte does not become sync. Therefore, in case of Code Rate 5/6, it should be processed using S/W.

Processing procedure is like below.
1. When the rest is locked except byte sync, code rate check 5/6.
- Code rate monitoring : Addr [**0x32**], Bit position[**0-2**]
2. When Code Rate is 5/6, Check inverse spectrum status.
- Spectrum inverse monitoring : Addr [**0x32**], Bit poisition[**3**]
3. Inverse inversion spectrum.
- Spectrum inverse setting : Addr [**0x31**], Bit poisition[**3**], Set 1
  Addr [**0x31**], Bit poisition[4], Set 1 or 0

3.4.9.1 Parallel output interface

A schematic diagram of the parallel output interface is shown in Figure 4. The parallel output format is compliant with the DVB-S common interface protocol.
When the byte sync is not found (SYNC_FLAG = 0 in the SYNC02 register), VALID (corresponding to the MiVAL signal of the DVB-S common interface standard) remains at a low level.
BYTE_CLOCK has a duty cycle between 40 and 60%. The VALID signal is generated depending on bit 2 of Address 39. The BYTE_CLOCK, SYNC, VALID and ERROR signal polarity is controlled depending on contents in the Register 38.

3.4.9.2 Serial output interface

The serial output interface is shown in Figure5. The serial bit stream is available on D7, where MSB is first to reconstruct the original order. If MPEG_DOUT = 1, then the parity bits are output (Register 39). If MPEG_DOUT =0, the data is null during the parity time slots.
SYNC is only high during the first bit of each packet, instead of during the first byte in Parallel mode.
ERROR has the same function as in parallel mode.
BYTE_CLOCK is the serial bit clock; it is same the master clock, fclk. All of the outputs are synchronous of the same master clock edge. D7, SYNC, VALID and ERROR may be properly sampled externally by the rising edge of BYTE_CLOCK.
The first bit detected in a valid packet may be decoded if it is found on the appropriate edge of BYTE_CLOCK, where SYNC = 1, ERROR = 0, VALID = 1. The following bits only require the assertion of VALID (while VALID = 1,). Outputs D0 to D6 remain at low level in serial mode.

Figure4 : Parallel output interface

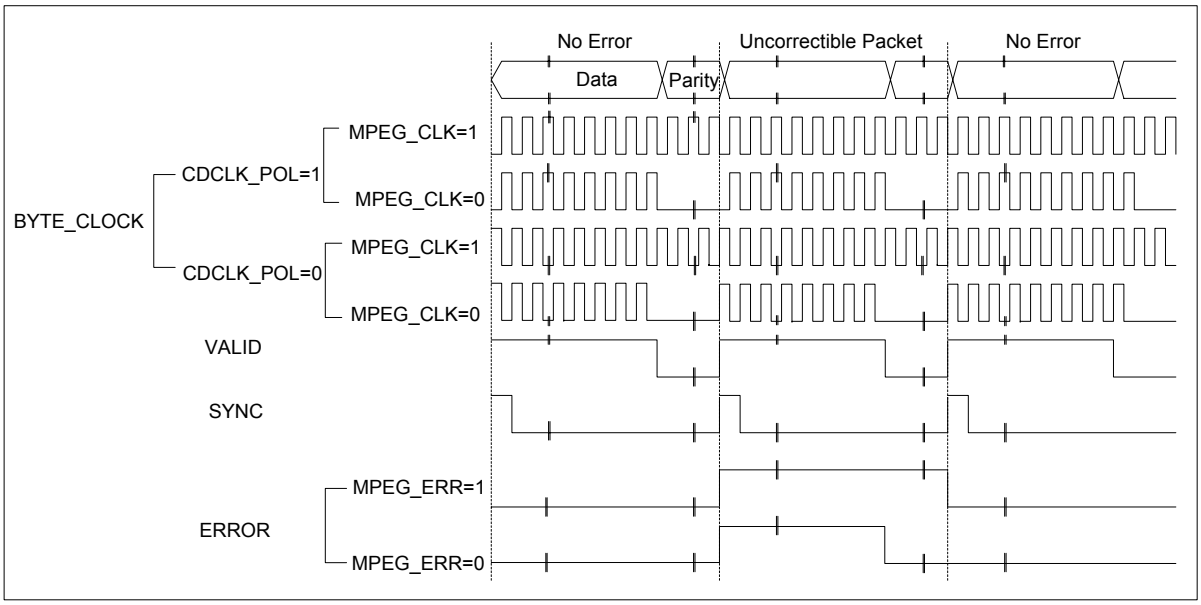


Figure5 : Serial output interface

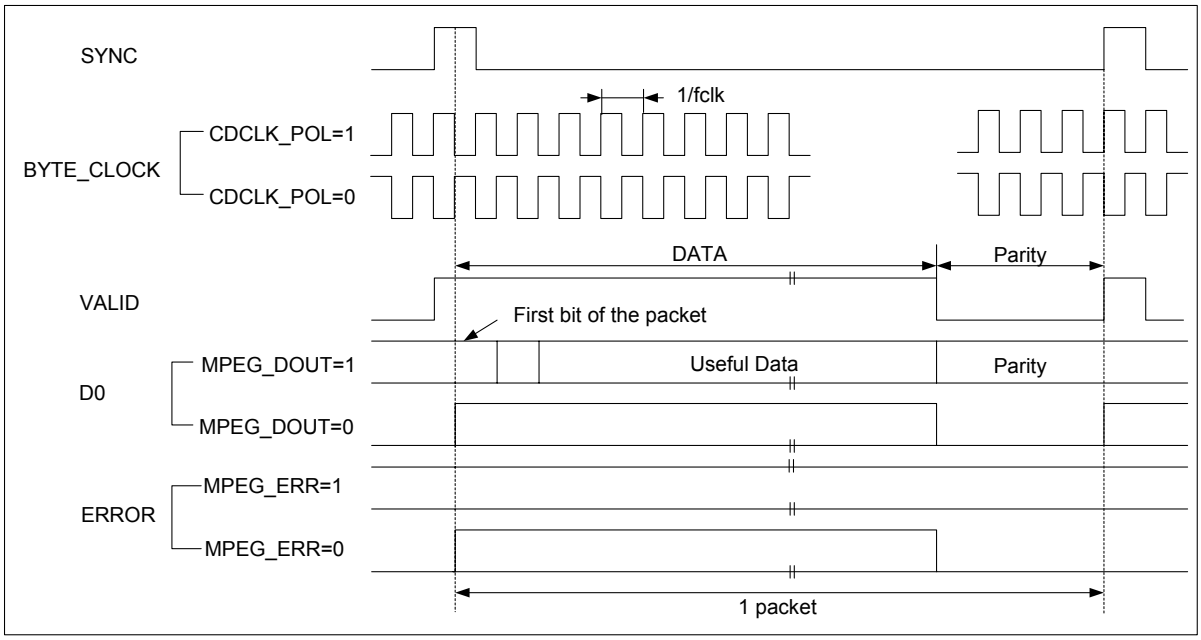


Table 0

	Bit1 of 0x39	Bit4 of 0x02	MPEG Data	MPEG Clock
	SER_PAR	SER_SEL_MODE		
Parallel	0	1	DATA [7:0]	BYTE_CLK
Serial	1	1	DATA[7]	BYTE_CLK

3.4.9.3 MPEG Clock Control

- Through Register Setting, S5H1420 can control MPEG CLOCK to MCU.

STB MCU	60MHz		81MHz	
Symbol Rate	Symbol Rate >= 25	Symbol Rate < 25	Symbol Rate >= 25	Symbol Rate < 25
S5H1420 Master Clock	59MHz	88MHz	80MHz	88MHz
Sampling	1	2	1	2

- Control register, 3-bit, uses Address 0x22 (MPEG_CLK_INTL [2:0])
- If Control registers changes, Some blocks will be reset automatically.
- In case, Auto reset does not work, these blocks' reset can be done manually.
- MPEC IF Clock is made by Control Register and the Rules are as follows

- Tmp = (fMCLK/fSR)*(1/(2*CR)), fMCLK : System Clock Frequency,fSR : Symbol Rate, CR : Code Rate

Control Register (0x22)	MPEG Clock(Parallel)	MPEG Clock (Serial)	Range	Divide	MCLK=88 MHz MPEG Clock (MHz)	
					Serial	Parallel
0	$F_{MCLK}/8$	F_{MCLK}	1<Tmp≤2	1	88	11
1	$F_{MCLK}/16$	$F_{MCLK}/2$	2<Tmp≤5	2	44	5.5
2	$F_{MCLK}/32$	$F_{MCLK}/4$	5<Tmp≤9	3	22	2.75
3	$F_{MCLK}/64$	$F_{MCLK}/8$	9<Tmp≤13	4	11	1.375
4	$F_{MCLK}/96$	$F_{MCLK}/12$	13<Tmp≤17	5	7.3333	0.9166625
5	$F_{MCLK}/128$	$F_{MCLK}/16$	17<Tmp≤25	6	5.5	0.6875
6	$F_{MCLK}/192$	$F_{MCLK}/24$	25<Tmp≤33	7	3.6666	0.458325
7	$F_{MCLK}/256$	$F_{MCLK}/32$	33<Tmp	8	2.75	0.34375

Example1) System Clock Frequency = 88MHZ, Symbol Rate : 44MSps

Code Rate	Tmp Value	Setting Control Register Value
1/2	2	1
2/3	1.5	0
3/4	1.333	0
5/6	1.2	0
6/7	1.166	0
7/8	1.142	0

3.5 Front end interfaces

3.5.1 I²C interface

The standard I²C protocol is used whereby the first byte is Hex A0 for a write operation, or Hex A1 for a read operation.

3.5.2 Write operation

The byte sequence is as follows:

- the first byte gives the device Address plus the direction bit (R/W = 0).
- the second byte contains the internal Address of the first register to be accessed.
- the next byte is written in the internal register. Following bytes (if any) are written in successive internal registers.
- the transfer lasts until stop conditions are encountered.
- the S5H1420 acknowledges every byte transfer.

3.5.3 Read operation

The Address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device Address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial Address. Figure 2 shows the I²C Normal Mode Write and Read Registers.

Figure 2: I²C Read and Write operations in Mode

Write register 0 to 3 with AA, BB, CC, and DD

Start	Device Address Write D0	ACK	Register Address 00	ACK	DataAA	ACK	DataBB	ACK	DataCC	ACK	DataDD	ACK	Stop

Read register 2 and 3

Start	Device Address Write D0	ACK	Register Address 02	ACK	Stop		
Start	Device Address Read D1	ACK	Data Read CC	ACK	Data Read DD	$\overline{\text{ACK}}$	Stop

3.5.4 Identification register

The Identification Register (at Address Hex 00) gives the release number of the circuit.
The content of this register at reset is presently (Hex02)

3.5.5 Sampling frequency

The S5H1420 converts the analog inputs into digital 6 bit I and Q flow. The sampling frequency is f_{clk} which is derived from an external reference described in Section 3.5.6 'Clock generation'. The maximum value of fclk is 90 MHz.
The sampling causes the repetition of the input spectrum at each integer multiple of f_{clk} One has to ensure that no frequency component is folded in the useful signal bandwidth of f_{sym} (1+ α)/2 where f_{sym} is the symbol frequency, and α is the roll-off value.

3.5.6 Clock generation

An integrated PLL is the circuit synchronizing an output signal (generated by a VCO with a reference signal in frequency as well as in phase. In this application, it includes the following basic blocks. The phase frequency detector to detect the phase difference between the reference frequency and the output frequency (after division) and to control the charge pumps voltage. Register setting can program the desired frequency.

$f_{out} = (m \times f_{in}) / (p \times s)$
f_{in}: input frequency, m=M+8, p=P+2, s=2^S
M: Register 03, P: Register 04 [5:0], S: Register 04[7:6]

3.5.7 I²C bus repeater

In low symbol rate applications, signal pollution generated by the SDA/SCL lines of the I²C bus may dramatically worsen tuner phase noise. In order to avoid this problem, the S5H1420 offers an I2C bus repeater so that the RFSDA and RFSCL are active only when necessary. Both RFSDA and RFSCL pins are set high at reset. When the microprocessor writes a 1 into register bit I2C_RPT, the next I²C message on SDA and SCL is repeated on the RFSDA and RFSCL pins respectively, until stop conditions are detected.

To write to the tuner, the external microprocessor must, for each tuner message, perform the following:
■ Program 1 in I2C_RPT.
■ Send the message to the tuner.
Any size of byte transfers is allowed, regardless of the Address, until the stop conditions are detected. Transfers are fully bi-directional. The I2C_RPT bit is automatically reset at the stop condition. The I²C repeater register in Address Hex 02 controls configuration.

3.5.9 DiSEqC interface

This interface allows for the simplification of real time processing of the dialog from microprocessor to LNB. It includes register set (8 bytes) that is filled by the microprocessor via the I²C bus, and then transmitted by modulating to 22 kHz clock. The S5H1420 support DiSEqC2.0 for bi-directional interface between microprocessor to LNB and can change the tone frequency by register setting.

< Transmission >

The S5H1420 have three modes for DiSEqC Interface.
■ Continuous Mode: The S5H1420 generates continuous tone signal until the mode changes.
■ Tone Burst Mode: For the “Modulated Tone Burst”, only one byte (with value Hex FF) and parity bit 1 is sent. As a result, the output signal is 9 bursts of 0.5ms, separated by 8 intervals of 1ms.
For the “Unmodulated Tone Burst” only one byte (with value Hex 00) is sent. The parity bit is still 1, and as a result, the signal is a continuous train of 12.5ms.
■ DiSEqC Mode: DiSEqC is a command-based protocol used to control multiple LNBs in a cascaded network configuration. The S5H1420 complies with DiSEqC2.0. Figure illustrates a typical application of the DiSEqC mode.

< Receive >

The S5H1420 receives the data from LNBs using DiSEqC pin. In order to receive the data from LNBs should set the register RCV_EN to 1. The received data is stored to register set.
Two control signals are available on the I²C bus:
DiS_RDY (Transfer Ready/Finish) and DiS_LENGTH (Message Length).
A typical byte transfer loop, as seen from the microprocessor, may be the following:
While (there is data to transfer)
1 Read the DiS_RDY signals
2 If DiS_RDY =0, Write byte to transfer in the register set.
3 Set the DiS_LENGTH.
4 Set the DiS_RDY =1.
Note, for the above transfer loop, the following:
■ At the beginning, the register set is empty (DiS_RDY =0). This is the idle state.
■ As soon as set the DiS_RDY =1, the transfer will begin.
■ After the last transmitted byte, the interface will go into the idle state.

Figure3: Schematic showing Bit Transmission

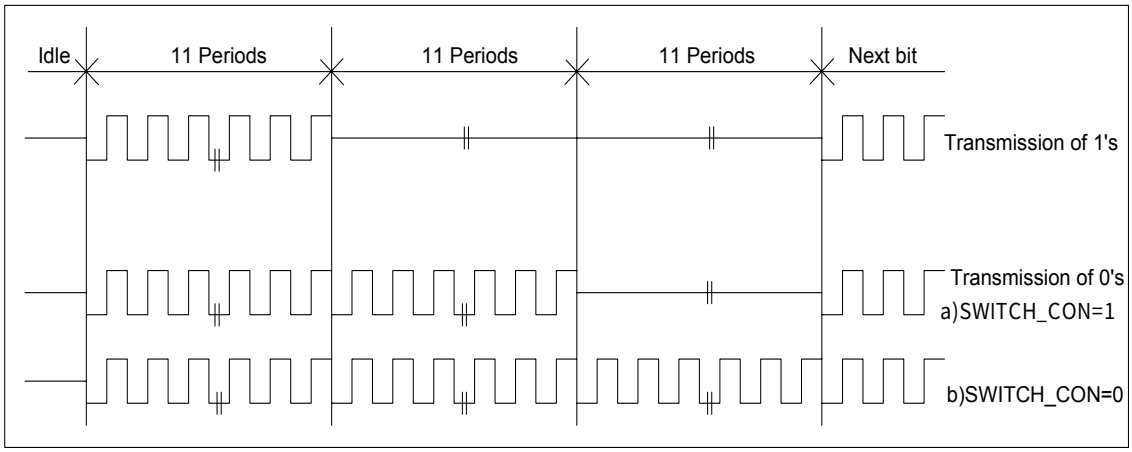


Table1

LNB_CON	SWITCH_CON	Register set	Output
00	X	Empty	Continuous tone
01	0	DATA=00	Unmodulated tone burst
	1	DATA=FFor00	Module tone burst
10	x	Note 1	DiSEpC signal
11	x	xx	Reserved

Note: 1 Byte to transfer in DiSEqC mode.
2 In Mode LNB_CON (1:0) =10, the DiSEqC pin return to high 2 mode once the transmission is completed.

4. REGISTER LIST

구분	Add	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ID	0x00	ID01	S5H1420_ID							
SYSTEM	0x01	CON_0				0	SOFT_RST	0	0	DSS_DVB
	0x02	CON_1		0	0	SER_SEL	0	0	PWR_DN	I2C_RPT
PLL	0x03	PLL01	M							
	0x04	PLL02	S		P					
QPSK	0X05	QPSK01	KICK_EN	0	1	DC_EN	1	1	MODE	Q_START
	0X06	QPSK02	1	1	0	1	DUMP_ACC	DC_WIN		
	0x07	Pre01	INV_PULSE	0	1	PRE_TH				
	0x08	Post01	0	0	POST_TH					
	0x09	Loop01	WT_TNCO	WT_PNCO	1	1	0	0	0	0
	0x0A	Loop02	LOOP_OUT	KICK_VAL			KICK_MUL			
	0x0B	Loop03	IGA_PLF				PGA_PLF			
	0x0C	Loop04	IGT_PLF				PGT_PLF			
	0x0D	Loop05	IG_TLF				PG_TLF			
	0x0E	Pnco01	PNCO0[31:24]							
	0x0F	Pnco02	PNCO1[23:16]							
	0X10	Pnco03	PNCO2[15:08]							
	0X11	Tnco01	TNCO0[31:24]							
	0X12	Tnco02	TNCO1[23:16]							
	0X13	Tnco03	TNCO2[15:08]							
	0x14	Monitor01					Reserved		TLOCK	PLOCK
	0x15	Monitor02	PRE_LEVEL							
	0x16	Monitor03	POST_LEVEL							
	0x17	Monitor04	DC_I_LEVEL							
	0x18	Monitor05	DC_Q_LEVEL							
	0x19	Monitor06	Reserved							
	0x1A	Monitor07	Reserved							
	0x1F	Monitor12		QPSK_OUT						DC_FREEZE
FEC	0x22	FEC01		0	0	0	0	MPEG_CLK_INTL		
	0x23	Soft01	Reserved							
	0x24	Soft02	Reserved							
	0x25	Soft03	Reserved							
	0x26	Soft04	Reserved							
	0x27	Soft05	Reserved							
	0x28	Soft06	Reserved							
	0x29	Vit01	Reserved							
	0X2A	Vit02	Reserved							
	0X2B	Vit03	Reserved							
	0X2C	Vit04	Reserved							
	0X2D	Vit05	Reserved							
	0X2E	Vit06	Reserved							
	0X2F	Vit07	Reserved							
	0X30	Vit08	0	0	VIT_SR78	VIT_SR67	VIT_SR56	VIT_SR34	VIT_SR23	VIT_SR12
	0X31	Vit09				PARM_FIX	INV_SPEC	VIT_FR		
	0x32	Vit10					VIT_SPEC_STS	VIT_CR		
	0x33	Vit11								
	0x34	Vit12								
	0x35	Sync01	SYNC_MISS_TH				SYNC_HIT_TH			
	0x36	Sync02			BYTE_SYNC	Reserved				VIT_SYNC
	0X37	Rs01								
	0X38	Mpeg01					ERR_POL	SYNC_POL	VALID_POL	CDCLK_POL
	0X39	Mpeg02		1	1	1	CLK_CONT	1	SER_PAR	DSS_SYNC
	0X3A	DiS01	TONE_FREQ							
	0X3B	DiS02	RCV_EN	DIS_LENGTH			DIS_RDY	SWITCH_CON	LNB_CON	
	0X3C	DIS03						OLF_N	LNB_DN	V18_13V
	0X3D	DiS04	LNB_MESGE0							
	0X3E	DiS05	LNB_MESGE1							
	0X3F	DiS06	LNB_MESGE2							
	0X40	DiS07	LNB_MESGE3							
	0X41	DiS08	LNB_MESGE4							
	0X42	DiS09	LNB_MESGE5							
	0X43	DiS10	LNB_MESGE6							
	0X44	DiS11	LNB_MESGE7							
	0x45	Rf01		SLAVE_ADDR						
	0X46	Err01				ALARM _MODE	ERR_CNT_PRD		ERR_SRC	
	0x47	Err02	ERR_CNT_L							
	0x48	Err03	ERR_CNT_H							
	0x49	Err04	PARITY_ERR							

ID control register (Address: 0x00)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x00	ID01 (0x03)	S5H1420_ID	[7:0]	R	Revision ID

System control registers (Address: 0x01-0x02)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x01	CON_0 (0x00)		[4]	R/W	Set to "0"
		SOFT_RST	[3]	R/W	System soft reset mode (active high) [1] Enable [0] Disable
			[2]	R/W	Set to "0"
			[1]	R/W	Set to "0"
		DSS_ DVB	[0]	R/W	DSS/DVB mode selection [1] DSS [0] DVB
0x02	CON_1 (0x00)		[6]	R/W	Set to "0"
			[5]	R/W	Set to "0"
		SER_SEL	[4]	R/W	Set to "1"
			[3]	R/W	Set to "0"
			[2]	R/W	Set to "0"
		PWR_DN	[1]	R/W	Power down mode [1] Power down enable [0] Power down disable
		I2C_RPT	[0]	R/W	I2C repeater control [1] I2C repeater enable, [0] I2C repeater disable. Note: The master should be set this bit to "1" in order to interface with the tuner. When the master is not communicated with the tuner, this bit should be set to "0"

PLL control registers (Address: 0x03-0x04)

Addr.	RegName	Signal name	Width	Property	Description
0x03	PLL01 (0x50)	M	[7:0]	R/W	PLL programming information $F_{out} = ((M+8)\times F_{in})/((P+2)\times 2^{S})$ F_{in} = 4 MHz
0x04	PLL02 (0x40)	P	[5:0]	R/W	
		S	[7:6]	R/W	

QPSK control registers (Address: 0x05 – 0x06)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x05	QPSK01 (0xBC)	KICK_EN	[7]	R/W	[1] PLL Kicker enable [0] Disable
			[6]	R/W	Set to "0"
			[5]	R/W	Set to "1"
		DC_EN	[4]	R/W	DC offset remove [1] Enable [0] Disable
			[3]	R/W	Set to "1"
			[2]	R/W	Set to "1"
		MODE	[1]	R/W	QPSK operation mode [1] 1 sampling/1 symbol [0] 2 sampling/1 symbol
		Q_START	[0]	R/W	QPSK start signal [1] Start [0] Idle
0x06	QPSK02 (0xC1)		[7]	R/W	Set to "1"
			[6]	R/W	Set to "1"
			[5]	R/W	Set to "0"
			[4]	R/W	Set to "0"
		DUMP_ACC	[3]	R/W	Dump phase loop filter & timing loop filter accumulator [0 and then 1] The read operation enabled, when user set DUMP_ACC "0" and then "1".
		DC_WIN	[2:0]	R/W	Window position from MSB removing DC offset. Unsigned integer (0 ≤ DC_WIN≤ 7)

AGC control registers (Address: 0x07 – 0x08)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x07	Pre01 (0x30)	INV_PULSE	[7]	R/W	PWM signal is reversed [1] PWM signal active low [0] PWM signal active high
			[6]	R/W	Set to "0"
			[5]	R/W	Set to "1"
		PRE_TH	[4:0]	R/W	PRE-AGC threshold
0x08	Post01 (0x10)		[7:6]	R/W	Set to "0"
		POST_TH	[5:0]	R/W	POST-AGC threshold

Loop filter control registers (Address: 0x09 – 0x0D)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x09	Loop01 (0x30)	WT_TNCO	[7]	R/W	Write TNCO center frequency [0 and then 1] The write operation enabled, when user set WT_TNCO "0" and then "1"
		WT_PNCO	[6]	R/W	Write PNCO center frequency [0 and then 1] The write operation enabled, when user set WT_PNCO "0" and then "1"
			[5]	R/W	Set to "1"
			[4]	R/W	Set to "1"
			[3]	R/W	Set to "0"
			[2]	R/W	Set to "0"
			[1]	R/W	Set to "0"
			[0]	R/W	Set to "0"
0x0A	Loop02 (0x65)	LOOP_OUT	[7]	R/W	Loop filter monitoring selection [1] Loop filter accumulator + NCO [0] Loop filter accumulator
		KICK_VAL	[6:4]	R/W	The value that gets injected into the accumulator when a "kick" is needed.
		KICK_MUL	[3:0]	R/W	The number of bits KICK_VAL is up-shifted (2^N) before it is injected into the accumulator.
0x0B	Loop03 (0x78)	PGA_PLF	[3:0]	R/W	Phase loop, proportional gain (2^{PGA_PLF}) in the acquisition mode (default +8 added)
		IGA_PLF	[7:4]	R/W	Phase loop, integral gain (2^{IGA_PLF}) in the acquisition mode
0x0C	Loop04 (0x28)	PGT_PLF	[3:0]	R/W	Phase loop, proportional gain in the tracking mode (default +8 added)
		IGT_PLF	[7:4]	R/W	Integral gain in the tracking mode
0x0D	Loop05 (0x17)	PG_TLF	[3:0]	R/W	Timing loop, proportional gain (default +8 added)
		IG_TLF	[7:4]	R/W	Timing loop, integral gain

NCO control registers (Address: 0x0E – 0x13)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x0E	Pnco01 (0x00)	PNCO1 [31:24]	[7:0]	R/W	LOOP_OUT [1] Read PLF accumulator + PNCO LOOP_OUT [0] Read PLF accumulator
0x0F	Pnco02 (0x00)	PNCO2 [23:16]	[7:0]	R/W	
0x10	Pnco03 (0x00)	PNCO3 [15:08]	[7:0]	R/W	
0x11	Tnco01 (0x00)	TNCO1 [31:24]	[7:0]	R/W	LOOP_OUT [1] Read TLF accumulator + TNCO LOOP_OUT [0] Read TLF accumulator
0x12	Tnco02 (0x00)	TNCO2 [23:16]	[7:0]	R/W	
0x13	Tnco03 (0x00)	TNCO3 [15:08]	[7:0]	R/W	

QPSK monitoring registers (Address: 0x14 – 0x1F)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x14	Monitor01 (0x00)		[7:4]	R	Reserved
			[3:2]	R	Reserved
		TLOCK	[1]	R	Timing loop lock (Symbol sync) [1] Timing loop has locked [0] Timing loop has not locked
		PLOCK	[0]	R	Phase loop lock (Carrier sync) [1] Phase loop has locked [0] Phase loop has not locked
0x15	Monitor02 (0x00)	PRE_LEVEL	[7:0]	R	PRE-AGC gain level
0x16	Monitor03 (0x00)	POST_LEVEL	[7:0]	R	POST-AGC gain level
0x17	Monitor04 (0x00)	DC_I_LEVEL	[7:0]	R	DC offset of I samples
0x18	Monitor05 (0x00)	DC_Q_LEVEL	[7:0]	R	DC offset of Q samples
0x19	Monitor06 (0x00)		[7:0]	R	Reserved
0x1A	Monitor07 (0x00)		[7:0]	R	Reserved
		(0x1B ~ 0x1E)			Reserved
0x1F	Monitor12 (0x00)		[7]		Reserved
		QPSK_OUT	[6:1]	R	QPSK output monitoring
		DC_FREEZE	[0]	R/W	[1] Do not update DC_OFFSET
		(0x20 ~ 0x21)			Reserved

FEC control registers (Address: 0x22)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x22	FEC01 (0x01)		[6]	R/W	Set to "0"
			[5]	R/W	Set to "0"
			[4]	R/W	Set to "0"
			[3]	R/W	Set to "0"
		MPEG_CLK_INTL	[2:0]	R/W	Tmp=(FMClk/FSR)×(1/(2×CR)) FMClk: System Clock Frequency FSR: Symbol Rate, CR: Code Rate 0: 1<Tmp≤ 2 4: 13<Tmp≤ 17 1: 2<Tmp≤ 5 5: 17<Tmp≤ 25 2: 5<Tmp≤ 9 6: 25<Tmp≤ 33 3: 9<Tmp≤ 13 7: 33<Tmp

Viterbi control registers (Address: 0x30 – 0x31)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x30	Vit08 (0xFF)		[7]	R/W	Set to "0"
			[6]	R/W	Set to "0"
		VIT_SR78	[5]	R/W	[1] Include code rate 7/8 in sync search [0] Disable
		VIT_SR67	[4]	R/W	[1] Include code rate 6/7 in sync search [0] Disable
		VIT_SR56	[3]	R/W	[1] Include code rate 5/6 in sync search [0] Disable
		VIT_SR34	[2]	R/W	[1] Include code rate 3/4 in sync search [0] Disable
		VIT_SR23	[1]	R/W	[1] Include code rate 2/3 in sync search [0] Disable
		VIT_SR12	[0]	R/W	[1] Include code rate 1/2 in sync search [0] Disable
0x31	VIT9 (0x00)	PARM_FIX	[4]	R/W	Parameter fix mode [1] Known parameter [0] Unknown parameter
		VIT_INV_SPEC	[3]	R/W	Initial spectrum information [1] Inv spectrum [0] Not inv spectrum
		VIT_FR	[2:0]	R/W	Start synchronization search at code rate as follows: [0] R=1/2 [1] R=2/3 [2] R=3/4 [3] R=5/6 [4] R=6/7 [5] R=7/8

Viterbi status registers (Address: 0x32)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x32	VIT10 (0x00)	VIT_SPEC_STS	[3]	R	Spectrum information monitoring [1] Inv spectrum [0] Not inv spectrum
		VIT_CR	[2:0]	R	Viterbi decoder current code rate [0] R=1/2 [1] R=2/3 [2] R=3/4 [3] R=5/6 [4] R=6/7 [5] R=7/8

SYNC control register (Address: 0x35)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x35	Sync01 (0x33)	SYNC_MISS_TH	[7:4]	R/W	Sync byte detector's miss threshold
		SYNC_HIT_TH	[3:0]	R/W	Sync byte detector's hit threshold *Note: This value should be greater than 2

SYNC status register (Address: 0x36)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x36	Sync02 (0x00)	BYTE_SYNC	[5]	R	[1] Acquire byte sync [0] Not acquire byte sync
			[4:1]	R	Reserved
		VIT_SYNC	[0]	R	[1] Viterbi decoder is in sync [0] Viterbi decoder is out of sync

MPEG control registers (Address: 0x38~0x39)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x38	Mpeg01 (0x00)	ERR_POL	[3]	R/W	Packet error polarity [1] Active low [0] Active high
		SYNC_POL	[2]	R/W	Sync polarity [1] Active low [0] Active high
		VALID_POL	[1]	R/W	Data valid polarity [1] Active low [0] Active high
		CDCLK_POL	[0]	R/W	CDCLK polarity [1] Falling edge event [0] Rising edge event
0x39	Mpeg02 (0x3D)		[6]	R/W	Set to "1"
			[5]	R/W	Set to "1"
			[4]	R/W	Set to "1"
		CLK_CONT	[3]	R/W	Clock continuous mode [1] Continuous clock, [0] Clock is enable during payload data transfer
			[2]	R/W	Set to "1"
		SER_PAR	[1]	R/W	Serial / Parallel mode [1] Serial mode, [0] Parallel mode
		DSS_SYNC	[0]	R/W	DSS sync mode [1] Output sync, [0] No output sync

DiSEqC control registers (Address: 0x3A~ 0x3C)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x3A	DiS01 (0x01)	TONE_FREQ	[7:0]	R/W	Tone frequency ratio *Note: $f_{tone} = f_{clk} / (TONE\_FREQ \times 32)$
0x3B	DiS02 (0x00)	RCV_EN	[7]	R/W	DiSEqC receive enable mode [1] Receive enable [0] Receive disable
		DIS_LENGTH	[6:4]	R/W	Message length
		DIS_RDY	[3]	R/W	Data Transfer ready / finish [1] Ready [0] Finish *Note: The Microprocessor set to "1" only when this bit is "0". When this bit is "1", the slaver is not yet received message. The slaver is starting to receive the signal at the rising edge detection
		SWICH_CON	[2]	R/W	Satellite switch in tone burst mode [1] Satellite B [0] Satellite A
		LNB_CON	[1:0]	R/W	LNB control mode [0] Continuous mode [1] Tone burst mode [2] DiSEqC mode [3] Reserved

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x3C	DiS03 (0x04)	OLF_N	[2]	R/W	[1] Disable [0] OLF (active low)
		LNB_DN	[1]	R/W	[1] LNB down [0] Disable (active high)
		18V_13V	[0]	R/W	13V/18V select register [1] 18V [0] 13V

DiSEqC message registers (Address: 0x3D~0x44)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x3D	DiS04 (0x00)	LNB_MESGE0	[7:0]	R/W	LNB message contents *MSB sent first on each byte
0x3E	DiS05 (0x3E)	LNB_MESGE1	[7:0]	R/W	
0x3F	DiS06 (0x00)	LNB_MESGE2	[7:0]	R/W	
0x40	DiS07 (0x00)	LNB_MESGE3	[7:0]	R/W	
0x41	DiS08 (0x00)	LNB_MESGE4	[7:0]	R/W	
0x42	DiS09 (0x00)	LNB_MESGE5	[7:0]	R/W	
0x43	DiS10 (0x00)	LNB_MESGE6	[7:0]	R/W	
0x44	DiS11 (0x00)	LNB_MESGE7	[7:0]	R/W	

RF slave register (Address: 0x45)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x45	Rf01 (0x61)	SLAVE_ADDR	[6:0]	R/W	RF tuner slave Address (SOC VERSION)

Error control register (Address: 0x46)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x46	Err01 (0x00)		[4]	R/W	Set to "1"
			[3:2]	R/W	Set to "1"
		ERR_SRC	[1:0]	R/W	Error monitoring source [0] QPSK bit errors [1] Viterbi bit errors [2] Viterbi byte errors [3] Packet errors

Error monitoring registers (Address: 0x47-0x49)

Addr.	RegName (Reset val)	Signal name	Width	Property	Description
0x47	Err02 (0x00)	ERR_CNT_L	[7:0]	R	Error counter value register (LSB 8 bits)
0x48	Err03 (0x00)	ERR_CNT_H	[7:0]	R	Error counter value register (MSB 8 bits)
0x49	Err04 (0x00)	PARITY_ERR	[7:0]	R	Error flag for DiSEqC receive data

5. ELECTERICAL CHARACTERISTICS

5.1 Absolute maximum ratings

Symbol	Parameter	Range	Unit
V_{CC}	DC Supply Voltage	-0.3 to 4.6	V
V_{IN}	3.3V Input Voltage	-0.3 to V_{DD}+0.3	V
I_{IN}	DC 3.3V Input Current	+/- 10	mA
T_{stg}	Storage Temperature	-40 to +125	ºC
Topr	Operation Temperature	0 to +70	ºC

5.2 Recommended operating conditions

Symbol	Parameter	Range	Unit
V_{CC}	DC Supply Voltage	3.0 to 3.6	V
T_J	Junction Temperature	MAX 125	ºC
T_R	Thermal Resistance	45	ºC /W
V_{IN}	DC Input	0 to V_{CC}	V
V_{OUT}	Output Voltage	0 to V_{CC}	
T_{LT}	Lead Temperature (soldering 10 sec)	300	ºC

5.3 DC electrical characteristics

(V_{DD} = 3.3+/-10%, Ta = -40(C~ -85(C, unless otherwise specified)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
VCC33	I/O Supply Voltage		3.0	3.3	3.6	V
VCC25	Internal Supply Voltage		2.2	2.5	2.7	V
Vih	Input Voltage Low	All In out			0.7 VDD	
		Rst_n, S_clk	-	-	2.1	V
Vil	Input Voltage High	All Input	0.3VDD	-	-	V
		Rst_n, S_clk	0.8	-	-	
Iih	High Level Input Current	VIN = VDD	- 10	-	+ 10	uA
I_{il}	Low Level Input Current	V_{IN} = V_{SS}	-10	-	+10	uA
V_{ol}	Output Low Voltage	I_{OL} = 8mA	-	-	0.4	V
V_{oh}	Output High Voltage	I_{OH} = -6mA	2.4	-	V_{DD}	V
I_{oz}	3-State Output Leakage Current	V_{OH} = V_{SS} or V_{DD}	-10	-	+10	uA
I_{cc}	Dynamic Supply Current	F_{in} = 4.0MHz, V_{DD} = 3.6V	-	-	TBD	mA

5.4 A/D converter

(V_{cc25} = 2.5+/-5%, Ta = -40(C~ -85(C, unless otherwise specified)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
VREF-H	Reference Voltage High Input	VREF-H Value	1.5	1.6	1.7	V
VREF-L	Reference Voltage Low Input	VREF-L Value	0.8	0.9	1.0	V
Ain	Analog Input (IP/IN/QP/QN)	(VREF-H)-(VREF-L)	0.5	0.7	0.9	VPP
CML	Common Mode Level	CML Output	-	1.25	-	V
I_{DD} 45M	Average $V_{DD\_2.5V}$ Current	$V_{DD=2.6V}$ = 59MHz	-	-	200	mA
I_{DD} 45M	Average $V_{DD\_2.5V}$ Current	$V_{DD=2.6V}$ = 88MHz	-	-	240	mA
INE	Integral Linearity Error	F_{IN}=30MHz, F_S=90MHz	-	-	±1.0	dB
DLE	Differential Linearity Error	F_{IN}=30MHz, F_S=90MHz	-	-	±2.0	dB
OFF	Offset Error Voltage	F_{IN}=30MHz, F_S=90MHz	-	±1.0	-	dB
GAIN	Gain Error Voltage	F_{IN}=30MHz, F_S=90MHz	-	±2.0	-	dB
SNDR	Signal to Noise & Distortion Ratio	F_{IN}=30MHz, F_S=90MHz	-32	-30	-28	dB
FIN	Analog Input Bandwidth		-	-	30	MHz
FS	Sampling Frequency		-	-	90	MHz

5.5 Timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO}	Internal VCO frequency	300		400	MHz
f_{CLK_IN}	CLK_IN OR XTAL frequency	4		30	MHz
PARALLEL OUTPUT D[7:0], D/P, CLK_OUT, STR_OUT, ERROR OUTPUT CHARACTERITICS					
Bit RS=1 in RS CONTROL REGISTER(Address33). Refer to Figure 6					
t_{CLK_duty}	CLK_OUT duty cycle	40	50	60	%
t_{CKSU}	D[7:0], D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge	2*Tm(1)			ns
t_{CKH}	D[7:0], D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge	2*Tm(1)			ns
Bit RS=0 in RS CONTROL REGISTER(Address33). Refer to Figure 7					
t_{CKSU}	D[7:0], D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge	2*Tm(1)			ns
t_{CKH}	D[7:0], D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge	2*Tm(1)			ns
SERIAL OUTPUT D[7:0], D/P, CLK_OUT, STR_OUT, ERROR OUTPUT CHARACTERITICS					
Bit RS=1 in RS CONTROL REGISTER(Address33). f_{CLK}= 90MHz. Refer to Figure 8					
t_{CKSU}	D[7:0], D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge	3.5			ns
t_{CKH}	D[7:0], D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge	2			ns
Bit RS=0 in RS CONTROL REGISTER(Address33). f_{CLK} = 90MHz. Refer to Figure 9					
t_{CKSU}	D[7:0], D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge	3.5			ns
t_{CKH}	D[7:0], D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge	2			ns

Figure 6

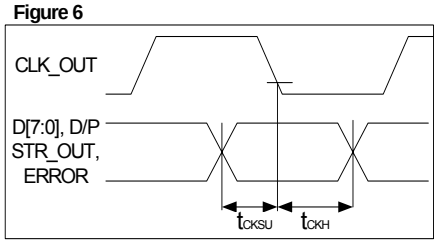


Figure 7

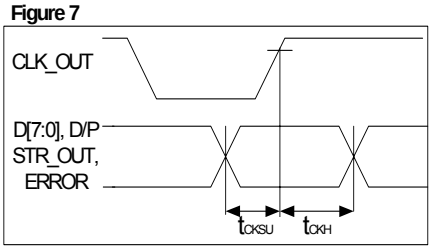


Figure 8

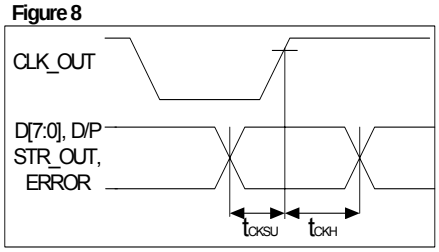
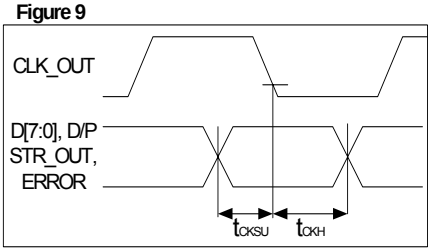


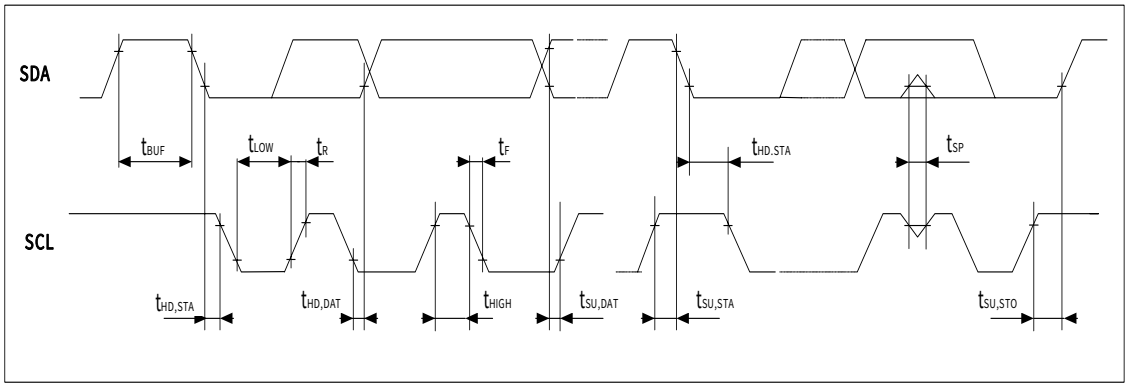
Figure 9



5.6 I²C bus characteristics

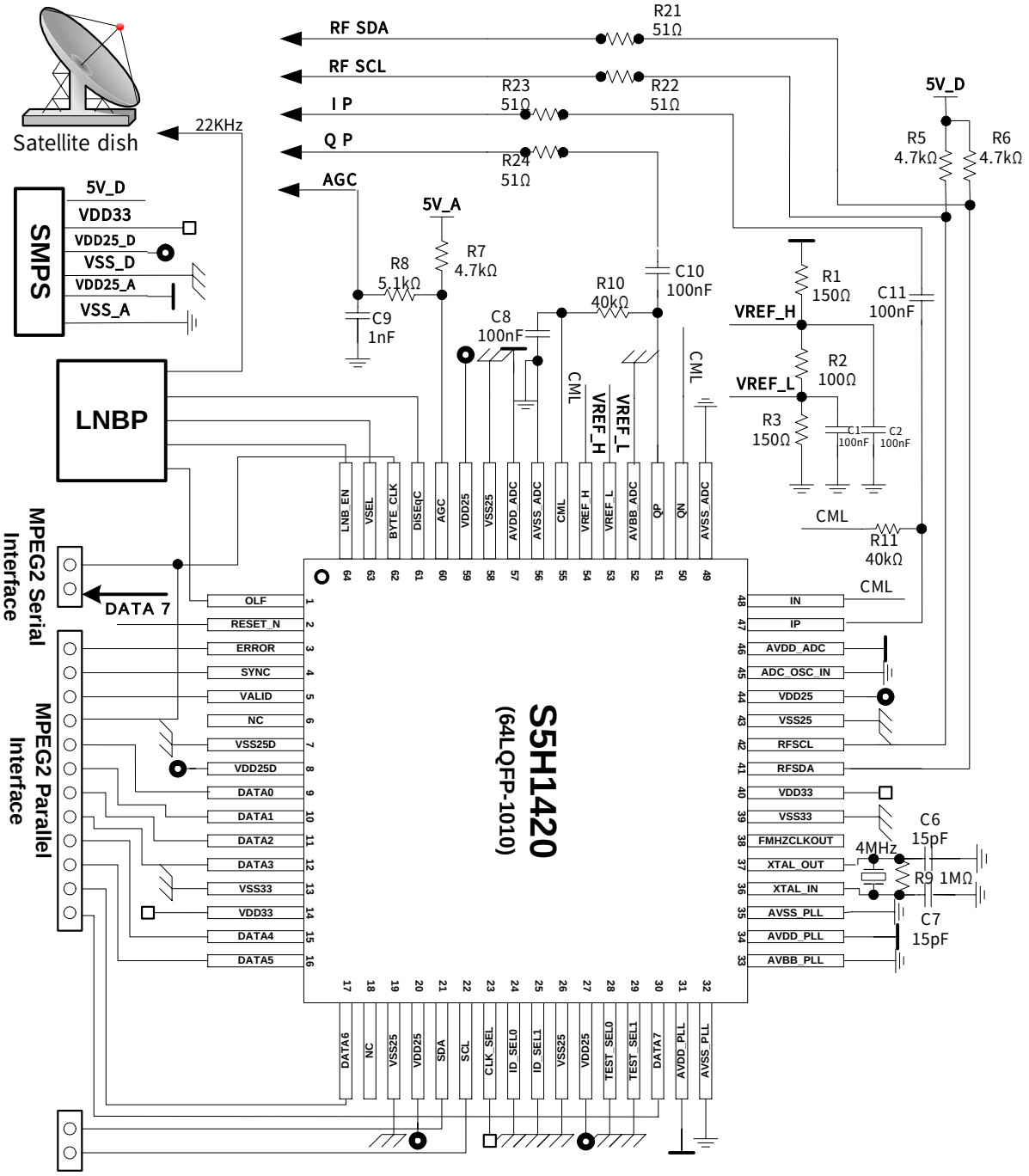
Symbol	Parameter	Test Condition s	Min	Typ	Max	Unit
V_{IL}	Low Level input Voltage	Pull up to 5V ±10%	- 0.5		0.8	V
V_{IH}	High Level input Voltage		2.0		5.5	V
V_{OH}	High Level output Voltage	Pull up to 5V ±10%			5.5	V
V_{OL}	Low Level output Voltage				0.4	V
I_{LK}	Input Leakage Current	VIN = 0V to 5V	-10		10	uA
C_{IN}	Input Capacitance	0		3.5		pF
I_{OL}	Output Sink Current	VOL = 0.5V		10		mA
f_{SCLN}	SCL Clock Frequency	Normal Mode	0		f_{M_CLK} /40	_
f_{SCLS}		Standby Mode	0		f_{M_CLK} /10	_
t_{BUF}	Bus Free Time between a STOP and START Condition		1.3			us
$t_{HD,STA}$	Hold Time(repeated)START Condition. After this period, the first clock pulse is generated		0.6			us
t_{LOW}	Low Period of the SCL Clock		1.3			us
t_{HIGH}	High Period of the SCL Clock		0.6			us
$t_{SU,STA}$	Setup Time for a repeated START Condition		0.6			us
$t_{SU,STO}$	Setup Time for STOP Condition		0.6			us
$t_{SU,DAT}$	Data Setup Time		100			ns
t_R, t_F	Rise and Fall Time of both SDA and SCL signals				300	ns
C_B	Capacitive Load for each Bus Line				400	pF

I²C bus timing diagram

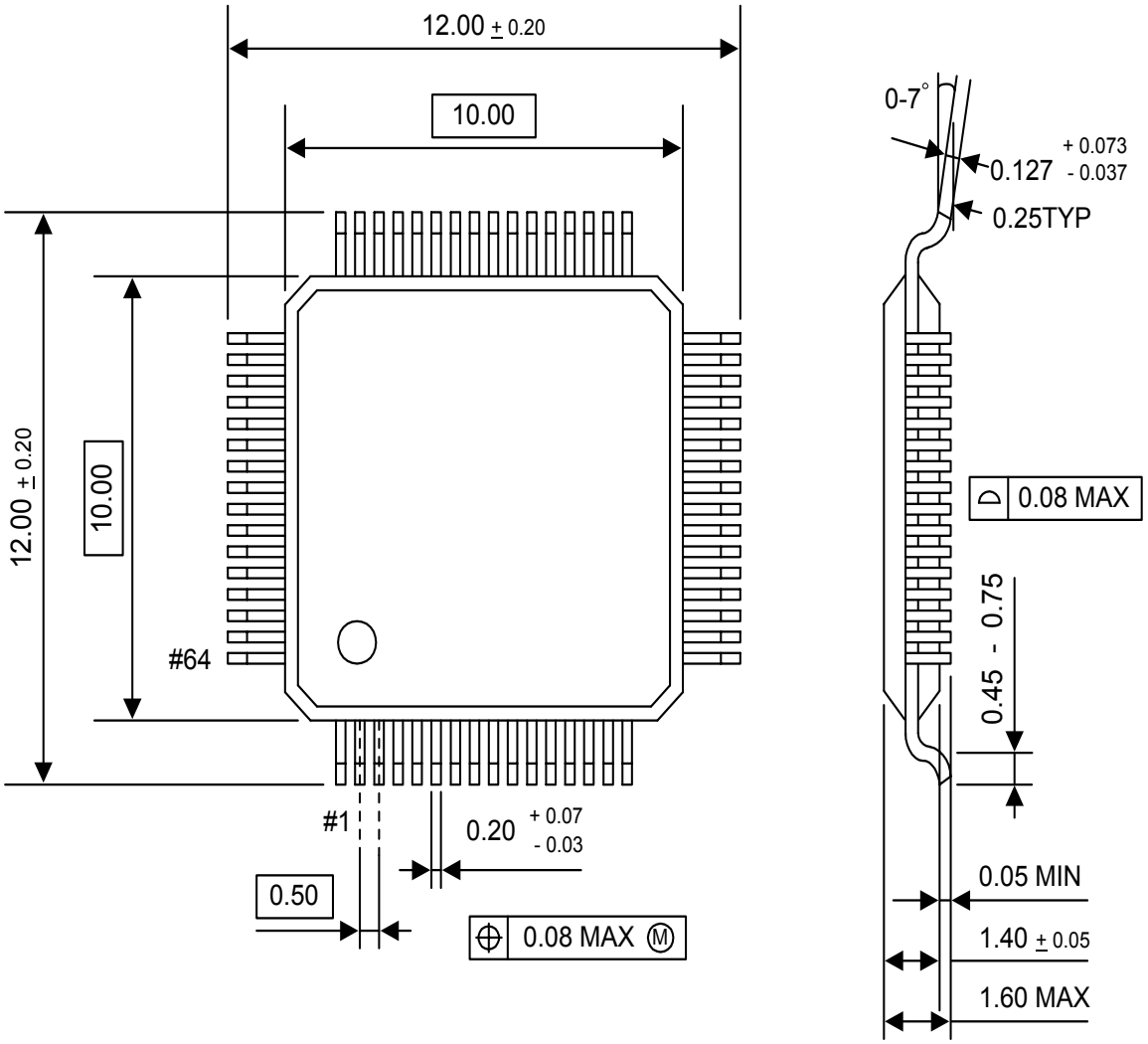


6. APPLICATION EXAMPLES

Application example (with DVB-S I/Q Tuner)



7. Package Dimension



NOTE: Dimensions are in millimeters.

8. Data sheet update history

- 2004-01-05 : Release version : 4.5

Add chapter : 3.4.8 Spectrum Inverse of Code Rate 5/6 (Page 10).
Add chapter : 3.4.9.3 MPEG Clock Control (Page 12).
Change register map : Hide unnecessary register Field to user (Page 16).

- 2004-01-10 : Release version : 4.5.1
Update chapter : 3.2.2 Loop equation (Page 7).
Update chapter : 3.3.1 Loop equation (Page 7).
Update chapter : 3.4.9.2 Serial output interface (Page 10).
Update chapter : 3.4.9.3 MPEG Clock Control (Page 12).

Samsung Electronics Co, Ltd.
www.samsung.com
T : 82-31-279-7640
Suwon P.O.BOX 416 Maetan-3dong, YoungTong-gu, Suwon-si, Gyeonggi-do, Korea 442-742