CML Semiconductor Products

PRODUCT INFORMATION

FX203 Selcall Tone Codec with Microprocessor Interface

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Provisional Issue

Features/Applications

- **Single-Chip Selcall Codec**
- **CCIR, EEA or ZVEI/SZVEI Versions**
- **On-Chip General Purpose Timer**
- **Separate General Purpose 4-bit Input/2-bit Output Port**
- **Mobile or Handheld Selcall**
- **4-bit Microprocessor I/O Data Port**
- **Powersave Facility**
- **Uses Low-Cost 4MHz Xtal**
- **Low-Power 5V CMOS Process**

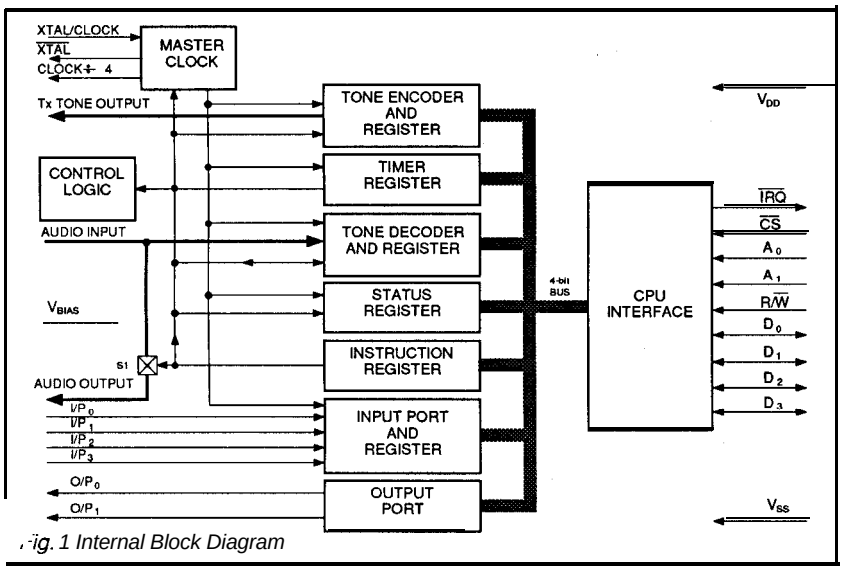


Fig. 1 Internal Block Diagram

FX203

Brief Description

The FX203 is a single-chip 'N' tone Selective Call encoder-decoder peripheral intended for use with a host microprocessor. The device is available in 3 toneset formats, CCIR, EEA or ZVEI/SZVEI.

A 4-bit data I/O bus, 2-bit address, $\overline{CS}$, R/W and $\overline{IRQ}$ lines are provided for connection to the microprocessor.

Separate general purpose 4-bit input and 2-bit output ports are available to allow external circuitry access to the microprocessor via this device. Functions such as 'PTT,' 'Rx Squelch,' 'Alert Bleeps' and 'Lamp Drivers' could operate through this facility.

An on-chip general purpose timer is provided for such functions as Rx and Tx tone period timing. Time periods of between 1 Oms and 140ms in 1 Oms steps may be programmed via the microprocessor interface.

The FX203 reference oscillator utilizes a low-cost 4.0 MHz Xtal or externally derived clock. The divide by 4 (1 .O MHz) output may be used to drive the clock circuitry of other devices such as the FX365 CTCSS Encoder/ Decoder, FXO04 Voice Band Inverter, or the FX214 VSB Audio Scrambler.

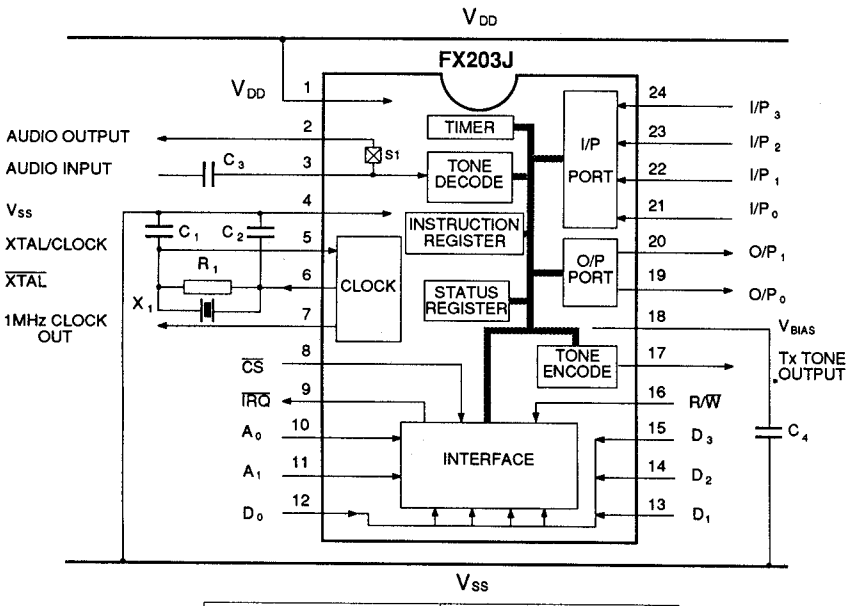
The FX203 requires a single 5-volt supply and utilizes 'chip enable'/'powersave' facilities for reduced current consumption in the Standby mode.

Pin Number		Function
DIL FX203*J	Quad FX203*LG FX203*LS	
1	1	**V_{DD} :** Positive supply rail. A single +5-volt power supply is required.
2	2	**Audio Output :** The received audio output, selected by the Audio Output Enable bit, D_1, in the Instruction Register. This output could be the result of a squelch function.
3	3	**Audio Input :** The audio input to the Tone Decoder and audio output switching. The composite (voice and tone) received audio requires to be coupled to this pin via capacitor C_3. See Figures 1 and 2.
4	4	**V_{SS} :** Negative supply rail (GND).
5	5	**Xtal/Clock :** The input to the clock oscillator inverter. A 4.0 MHz Xtal or externally derived clock should be connected here. See Figure 2.
6	6	**$\overline{Xtal}$:** The output of the 4.0 MHz clock oscillator. See Figure 2.
7	7	**Clock ÷ 4 :** A 1.0 MHz ($X_1 \div 4$) clock is available at this output for external use. Note the output impedance and source current limits.
8	8	**$\overline{CS}$:** The chip select input. A logic '0' on this pin will select the FX203. See Figure 3, Timing diagram.
9	9	**$\overline{IRQ}$:** The Interrupt logic output. An active interrupt is set as a logic '0'. This pin can be wire OR'd to external circuitry. An external pullup resistor may be required on this output. Conditions that cause Interrupt Requests are: (1) Rx Ready (tone decoded) – $\overline{IRQ}$ and Status bit D_0 (2) Timer Cycle expired – $\overline{IRQ}$ and Status bit D_1 (3) Input Port data change – $\overline{IRQ}$ and Status bit D_2
10 11	10 11	**A_0 :** **A_1 :** Register address pins. These inputs, with the R/$\overline{W}$ input, select the internal register to be addressed via the CPU Interface ($D_0 - D_3$) using the logic states as detailed below. Register information is detailed on pages 4 and 5.
12 13 14 15	12 13 14 15	**D_0 :** **D_1 :** **D_2 :** **D_3 :** The 4-bit microprocessor interface for communication with the internal registers as directed by the A_0, A_1 and R/$\overline{W}$ inputs.
16	16	**R/$\overline{W}$:** The Read/Write logic input, which with the A_0 and A_1 address inputs determine the Microprocessor/ Register communication. Read = logic'1', Write = logic '0'.
17	17	**Tx Tone Output :** The transmitted tone output of the Tone Encoder. Tone 'F' (Notone) will cause this output to go to V_{BIAS}. When not enabled this output is high impedance.
18	18	**V_{BIAS} :** The output of the on-chip bias circuitry, held at $V_{DD}/2$. When the Encoder is not enabled this pin will be at V_{SS}. This pin requires to be decoupled to V_{SS} with a capacitor, C_4.
19 20	19 20	**O/P_0 :** **O/P_1 :** The 2-bit logic output port whose state is controlled by the Instruction Register (D_2, D_3).
21 22 23 24	21 22 23 24	**I/P_0 :** **I/P_1 :** The 4-bit logic input port. See page 5. **I/P_2 :** These pins each have an internal 1MΩ pullup resistor. **I/P_3 :**

*** C, E, Z tonesets**

	R/$\overline{W}$	A_1	A_0	Register
	0	0	0	Tone Encode
Write	0	0	1	Instruction
	0	1	0	Timer
	1	0	0	Tone Decode
Read	1	0	1	Status
	1	1	0	Input Port

External Components



Component	Value	Component	Value
R_1	1MΩ	C_3	0.1µF
C_1	33pF	C_4	1.0µF
C_2	33pF	X_1	4.0MHz

Tolerances: R = ± 10%. C = ± 20%.

Fig.2 External Component Connections

General and Operational Notes

Power-up Arrangements

It is recommended that the following sequence be employed to set all internal registers to a start-up state upon power-up.

Write – Hex. '0' to Timer Register for a period greater than Power-Up Reset Time (TS).

The following actions clear the Status Register and reset all interrupts.

Read – Status Register.

Read – Tone Decode Register.

Read – Input Port Register.

Write – To Output Port as required.

The data in the Decoder Register is not valid until after the first active Decoder interrupt has been received.

Operation

Operation of the FX203 is Full Duplex.

The receive mode is achieved by writing any Timer setting except Hex. '0.'

The Tone Decode Register must be read before the expected arrival of the next tone, as register contents are overwritten.

Data written to the device via the CPU Interface is acted upon at the end of the Data Set-up Time (t_{DSW}), when the $\overline{CS}$ input goes high (logic '1').

The Timer may be written to at any time. The Timer is reset when data is written to it. The new Timer period starts when the $\overline{CS}$ input goes high (logic '1').

Layout

All external components (as recommended in Figure 2) should be kept close to the package.

Tracks should be kept short, particularly the Audio and V_{BIAS} inputs.

Xtal/clock and digital tracks should be kept well away from analogue circuitry. Analogue inputs and outputs should be screened wherever possible and the high level Tx Tone Output kept separate from other analogue inputs and outputs.

A "ground plane" connected to V_{SS} will assist in eliminating external pick-up.

Internal Register States

The following descriptions show the condition of each of the 6 registers used by the FX203 to communicate with both microprocessor and radio systems. Table 1 details the hexadecimal 4-bit data words used in these registers. Timing information for the CPU Interface is given in Figure 3.

Instruction Register — Write Only — $R/\overline{W} = 0$ $A_1 = 0$ $A_0 = 1$

The Instruction Register addresses the functions of the FX203

Bit No	Logic	Function		
D_0	1	**Tx Enable :**	–	Enables the Transmitter circuitry.
	0		–	Disables the Transmitter circuitry.
D_1	1	**Audio Output Enable :**	–	Switches the Audio Input to the Audio Output.
	0		–	Disables the Audio Output switch (S1).
D_2	1 or 0	**Output Port O/P_0 :**	–	The logic state of this line.
D_3	1 or 0	**Output Port O/P_1 :**	–	The logic state of this line.

Tone Encode Register — Write Only — $R/\overline{W} = 0$ $A_1 = 0$ $A_0 = 0$

D_0 D_1 D_2 D_3

LSB **MSB**

The 4-bit Hex. word written to this register will produce the required tone (Table 1) at the TX Tone Output

Tone Decode Register — Read Only — $R/\overline{W} = 1$ $A_1 = 0$ $A_0 = 0$

D_0 D_1 D_2 D_3

LSB **MSB**

The 4-bit Hex. word in this register will indicate the frequency (Table 1) of the received tone

Timer Register — Write Only — $R/\overline{W} = 0$ $A_1 = 1$ $A_0 = 0$

D_0 D_1 D_2 D_3

LSB **MSB**

The 4-bit Hex. word written to this register will automatically reset the timer and start a timing cycle as shown

Hex Code		Function/Tone Period
0	–	Disable Receiver, Transmitter and Timer
		Reset and start tone period of:
1	–	10ms
2	–	20ms
3	–	30ms
4	–	40ms
5	–	50ms
6	–	60ms
7	–	70ms
8	–	80ms
9	–	90ms
A	–	100ms
B	–	110ms
C	–	120ms
D	–	130ms
E	–	140ms
F	–	Disable Timer operation only

Internal Register States

Status Register	Read Only	$R/\overline{W} = 1$ $A_1 = 0$ $A_0 = 1$

The Status Register indicates the source of any interrupt

Bit No	Condition
	A logic '1' in the Status Register indicates that the bit is **Set** The Interrupt line ($\overline{IRQ}$) is a logic '0' when active
D_0	**Rx Ready :** D_0 and an interrupt are **Set** when the Tone Decoder has decoded a received tone and latched the 4-bit Hex. word into the Tone Decode Register. This register requires to be read before the next tone is decoded or that information will be overwritten. D_0 and the interrupt are **Cleared** by reading the Status Register followed by reading the Tone Decode Register.
D_1	**Timer :** D_1 and an interrupt are **Set** when the intervals programmed by the Timer Register have expired. D_1 and the interrupt are **Cleared** after reading the Status Register.
D_2	**Input Port ($I/P_0 - I/P_3$) :** D_2 and an interrupt are **Set** when the data state at the Input Port changes. D_2 and the interrupt are **Cleared** by reading the Status Register followed by reading the Input Port register.
D_3	This bit is unallocated. Set at a logic '0.'

Input Port	Read Only	$R/\overline{W} = 1$ $A_1 = 1$ $A_0 = 0$

D_0 D_1 D_2 D_3

LSB **MSB**

By reading this register the microprocessor can monitor the state of the 4 logic input pins ($I/P_0 - I/P_3$).This facility allows external systems to communicate with the microprocessor via this device

The FX203 caters for CCIR, EEA and ZVEI/Suppressed ZVEI sequential tone system frequencies in three tone sets, "C," "E" and "Z" respectively, as shown in Table 1.
See the 'Specifications' pages for overall FX203 Tone performance characteristics.

Hex. Input/Output	D_3	D_2	D_1	D_0	'C' Tone Set f_0 (Hz)	'E' Tone Set f_0 (Hz)	'Z' Tone Set f_0 (Hz)
0	0	0	0	0	1981	1981	2400
1	0	0	0	1	1124	1124	1060
2	0	0	1	0	1197	1197	1160
3	0	0	1	1	1275	1275	1270
4	0	1	0	0	1358	1358	1400
5	0	1	0	1	1446	1446	1530
6	0	1	1	0	1540	1540	1670
7	0	1	1	1	1640	1640	1830
8	1	0	0	0	1747	1747	2000
9	1	0	0	1	1860	1860	2200
A	1	0	1	0	2400	1055	2800
B	1	0	1	1	930	930	810
C	1	1	0	0	2247	2247	970
D	1	1	0	1	991	991	885
E	1	1	1	0	2110	2110	2600
F	1	1	1	1	Notone	Notone	Notone

Table 1 Tone Frequency Programming Codes

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	FX203J	-30°C to +85°C (ceramic)
	FX203LG/LS	-30°C to +70°C (plastic)
Storage temperature range:	FX203J	-55°C to +125°C (ceramic)
	FX203LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
Voo = 5.0V, T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0 MHz. Audio level 0dB ref: = 775mV rms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current –					
Rx on, Tx and Timer Disabled			1.25		mA
Rx on, Tx Enabled, Timer Running	1		3.0		mA
Interface Levels					
CPU Data Port ($D_0 - D_3$) In/Out	8				
Logic '1'		3.5			V
Logic '0				1.5	V
Output Logic '1' Source Current	9			120	µA
Output Logic '0' Sink Current	10			360	µA
Three State Output Leakage Current		–		4.0	µA
Input Port ($I/P_0 - I/P_3$) & (R/W, A,,, A_1,$\overline{CS}$)					
Logic '1'		3.5			V
Logic '0		–		1.5	V
output Port ($O/P_0 - O/P_1$), ($\overline{IRQ}$)	2				
Logic '1'		4.0			V
Logic '0		–		1.0	V
Impedances					
Input Port		0.1	1.0		MΩ
output Port		–	15.0	50.0	kΩ
Audio Input	11	0.1	1.0	–	MΩ
Audio Switch S1 'ON'	11	–	2.0	5.0	kΩ
Audio Switch S1 'OFF'	11	1.0	10.0		MΩ
Tx Tone Output (Enabled)	14	–	1.0		kΩ
Tx Tone Output (Disabled)		1.0	10.0		MΩ
Clock + 4 Output		–	3.0	10.0	kΩ
$\overline{IRQ}$ Output (Logic '1')		–	25.0	100.0	kΩ
$\overline{IRQ}$ Output (Logic '0')		–	150.0	500.0	Ω
Encoder					
Tone Output Level	1	-1.0	0	+1.o	dB
Tone Frequency Accuracy 'C		-4.0	*fo*	+4.0	Hz
Tone Frequency Accuracy 'E		-0.3	*fo*	+0.3	%
Tone Frequency Accuracy 'Z		-0.3	*fo*	+0.3	%
Tone Output Risetime	3	–	2.0		ms
Total Harmonic Distortion				5.5	%

Characteristics		See Note	Min.	Typ.	Max.	Unit
Decoder						
Signal Input Range		4	-26.0	–	+7.0	dB
Decode Bandwidth –						
Probability > 0.995	'C'	5	±1.0	–		%
Probability > 0.995	'E'	5	±1.0	–		%
Probability > 0.995	'Z	5	±2.0	–		%
Not Decode Bandwidth –						
Probability < 0.03	'C	6	–		±3.0	%
Probability < 0.03	'E	6	–		±3.0	%
Probability < 0.03	'Z'	6	–		±4.5	%
Noise Response Rate	'C'	7,12	–	1.0		Digits
Noise Response Rate	'E	7,12	–	1.0		Digits
Noise Response Rate	'Z	7,13	–	1.0		Digits
Decode Response Time						
Notone to Tone		5	20	25	T_P	ms
Tone to Notone			33		58	ms
Timing – (Figure 3)						
Address Set Up Time	t_{AS}		50			ns
Read/Write Set Up lime	t_{RWS}		50			ns
Address Hold Time	t_{AH}		0			ns
Read/Write Recovery Time	t_{RWR}		0			ns
Chip Select Access Time	t_{ACS}				250	ns
Output Hold Time (Read)	t_{OHR}		0		100	ns
Data Set Up Time (Write)	t_{DSW}		150			ns
Data Hold Time (Write)	t_{DHW}		20			ns
Power Up Reset Time	TS		3.0			ms

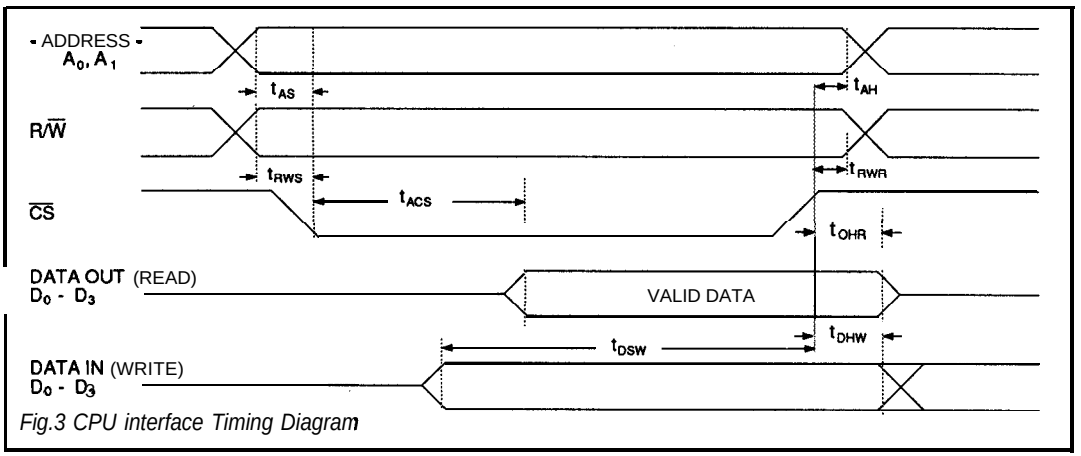


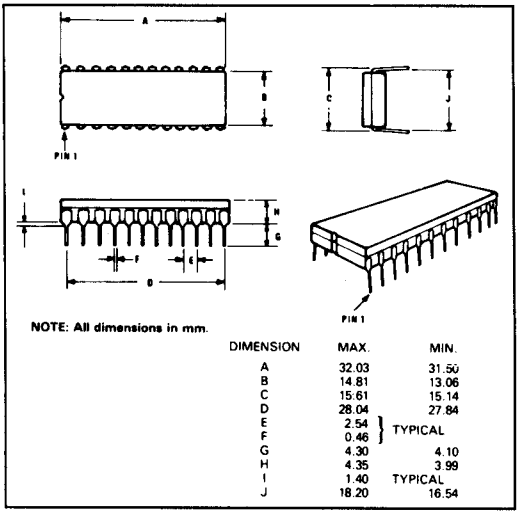
Fig.3 CPU interface Timing Diagram

Notes
1. No Tx Tone load.
2. Sink/Source currents $0.1 mA.
3. To 90% of nominal output, (from 'F tone' to 'not-F tone').
4. Sine or Square, a.c. coupled input.
5. With minimum tone period (Tp) for the tone set, S/N ratio 0dB.
6. Under all conditions of input amplitude and S/N ratio, with maximum Tp specified for the tone set.
7. Gaussian Noise Input 6kHz band limited with a maximum input level corresponding to l-digit code falsing rate. (random to random single characters).
6. With each data line loaded as: C = 50pf and R=10kΩ.
9. $V_{OUT} = 4.6V$
10. $V_{OUT} = 0.4V$
11. External'connections on the Audio Output may alter these values.
12. Single digit response in a 40.0-hour period.
13. Single digit response in a 1 .O-hour period.
14. An emiter follower output with an internal 10kΩ pulldown resistor.

Package Outline

The FX203J, the cerdip package is shown in Figure 4. The 'LG' version is shown in Figure 5 and the 'LS' version in Figure 6.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

Fig. 4 **FX203*J** *24-pin DIL Package*



NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	32.03	31.50
B	14.81	13.06
C	15.61	15.14
D	28.04	27.84
E	2.54	TYPICAL
F	0.46	
G	4.30	4.10
H	4.35	3.99
I	1.40	TYPICAL
J	18.20	16.54

Ordering Information

* Insert the required system toneset

CCIR	*EEA*	*ZVEI/SZVEI*
* (C)	(E)	(Z)

FX203(*)J – Figure 4
24-pin cerdip DIL

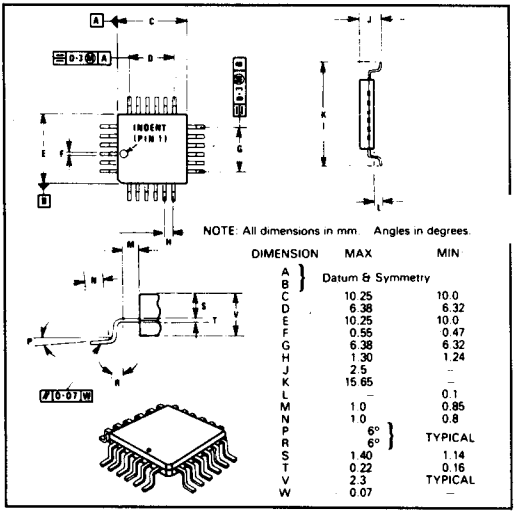
FX203(*)LG – Figure 5
24-pin quad plastic encapsulated bent and cropped

FX203(*)LS – Figure 6
24-lead plastic leaded chip carrier

Handling Precautions

The FX203 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

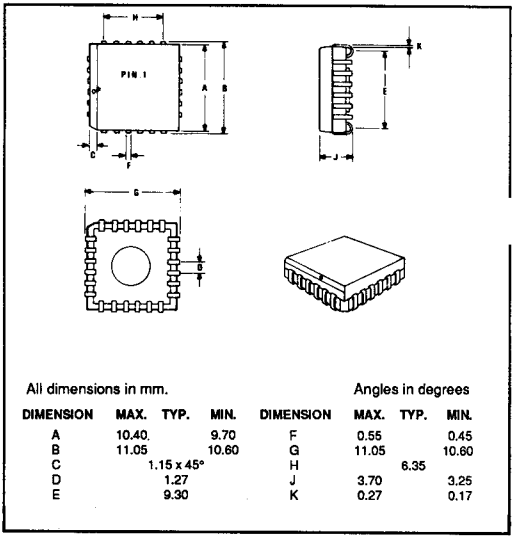
Fig. 5 **FX203*LG** *24-pin Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A, B, C	Datum & Symmetry	
D	10.25	10.0
E	6.38	6.32
F	10.25	10.0
G	0.55	0.47
H	6.38	6.32
J	1.30	1.24
K	2.5	–
L	15.65	–
M	–	0.1
N	1.0	0.85
P	1.0	0.8
R	6°	TYPICAL
S	6°	TYPICAL
T	1.40	1.14
V	0.22	0.16
W	2.3	TYPICAL
	0.07	–

Fig. 6 **FX203*LS** *24-pin Package*



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.	DIMENSION	MAX.	TYP.	MIN.
A	10.40		9.70	F	0.55		0.45
B	11.05		10.60	G	11.05		10.60
C	1.15 x 45°			H		6.35	
D	1.27			J	3.70		3.25
E	9.30			K	0.27		0.17