



T-52-33-47

UM6845E/EA/EB

CRT Controller

Features

- Single +5 volt (±5%) power supply
- Alphanumeric and limited graphics capabilities
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- External light pen capability
- Addressing capability up to 16K-character Video Display RAM
- No DMA required
- Pin-compatible with MC6845R
- Row/column or straight-binary addressing for Video Display RAM
- Video Display RAM configurable as part of microprocessor memory field or as independent slave to UM6845
- Internal status register
- 3.7 MHz character clock
- Transparent address mode

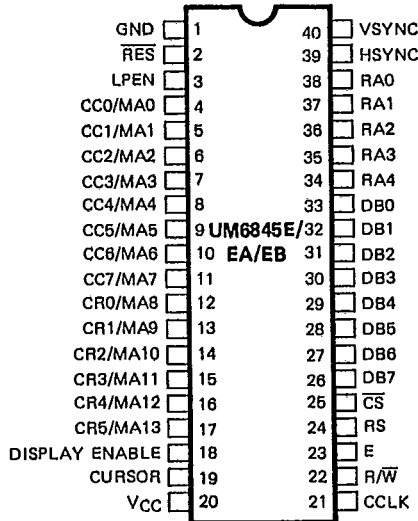


General Description

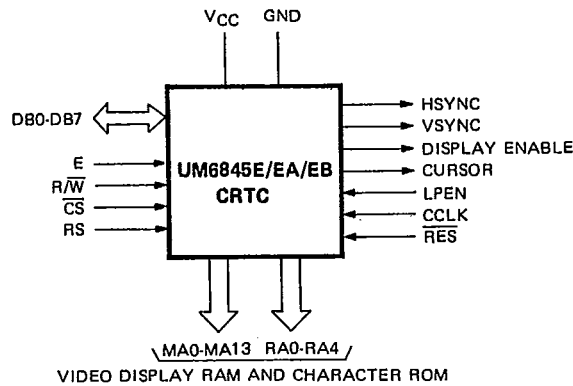
The UM6845E/EA/EB is a CRT Controller intended to provide capability for interfacing 8 or 16-bit microprocessors to CRT or TV-type raster scan displays. It's unique feature

is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of features.

Pin Configuration



Block Diagram





UM6845E/EA/EB

Absolute Maximum Ratings*

Supply Voltage, V_{CC} -0.3V to +7.0V
 Input/Output Voltage, V_{IN} -0.3V to +7.0V
 Operating Temperature, T_{OP} 0°C to 70°C
 Storage Temperature, T_{STG} -55°C to 150°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

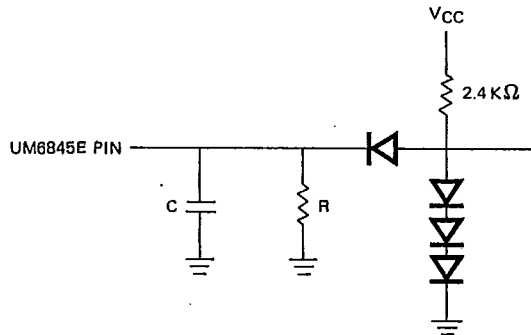
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

D. C. Electrical Characteristics

($V_{CC} = 5.0V \pm 5\%$, $T_A = 0 - 70^\circ C$, unless otherwise noted)

Symbol	Characteristics	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
I_{IN}	Input Leakage ($\phi 2$, R/W, RES, CS, RS, LPEN, CCLK)	-		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) $V_{IN} = 0.4$ to $2.4V$	-10.0		+10.0	μA
V_{OH}	Output High Voltage $I_{LOAD} = -205\mu A$ (DB0-DB7) $I_{LOAD} = -100\mu A$ (all others)	2.4		-	V
V_{OL}	Output Low Voltage $I_{LOAD} = 1.6mA$	-		0.4	V
P_D	Power Dissipation	-	325	650	mW
C_{IN}	Input Capacitance $\phi 2$, R/W, RES, CS, RS, LPEN, CCLK DB0-DB7	-		10.0 12.5	pF pF
C_{OUT}	Output Capacitance	-		10.0	pF

Test Load



R = $11K\Omega$ FOR DB0-DB7
 R = $24K\Omega$ FOR ALL OTHER OUTPUTS
 C = 130 pF TOTAL FOR DB0-DB7
 C = 30 pF ALL OTHER OUTPUTS

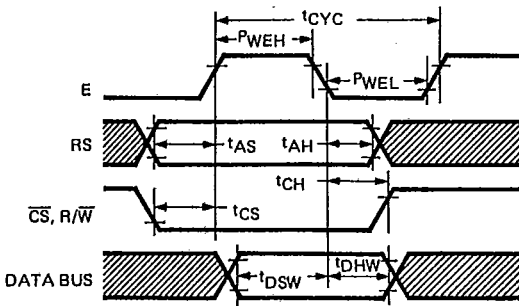
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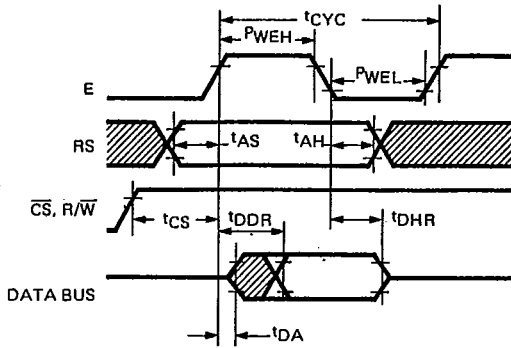
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MPU Bus Interface Characteristics

WRITE CYCLE



READ CYCLE



Write Timing Characteristics ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0 - 70^\circ C$, unless otherwise noted)

Symbol	Characteristics	UM6845E		UM6845EA		UM6845EB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Cycle Time	1.0	—	0.5	—	0.33	—	μs
PWEH	E Pulse Width, High	440	—	200	—	150	—	ns
PWEL	E Pulse Width, Low	420	—	190	—	140	—	ns
tAS	Address Set-Up Time	80	—	40	—	30	—	ns
tAH	Address Hold Time	0	—	0	—	0	—	ns
tCS	R/W, \overline{CS} Set-Up Time	80	—	40	—	30	—	ns
tCH	R/W, \overline{CS} Hold Time	0	—	0	—	0	—	ns
tDSW	Data Bus Set-Up Time	165	—	60	—	60	—	ns
tDHW	Data Bus Hold Time	10	—	10	—	10	—	ns

(t_r and $t_f = 10$ to 30 ns)

Read Timing Characteristics ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0 - 70^\circ C$, unless otherwise noted)

Symbol	Characteristics	UM6845E		UM6845EA		UM6845EB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Cycle Time	1.0	—	0.5	—	0.33	—	μs
PWEH	ϕ_2 Pulse Width, High	440	—	200	—	150	—	ns
PWEL	ϕ_2 Pulse Width, Low	420	—	190	—	140	—	ns
tAS	Address Set-Up Time	80	—	40	—	30	—	ns
tAH	Address Hold Time	0	—	0	—	0	—	ns
tCS	R/W, CS Set-Up Time	80	—	40	—	30	—	ns
tDDR	Read Access Time (Valid Data)	—	290	—	150	—	100	ns
tDHR	Read Hold Time	10	—	10	—	10	60	ns
tDA	Data Bus Active Time (Invalid Data)	20	60	20	60	20	60	ns
tTAD	MA0-MA13 Switching Delay (Refer to Figure Trans. Addressing)	100 typ.	160	100 typ.	160	90 typ.	130	ns

(t_r and $t_f = 10$ to 30 ns)

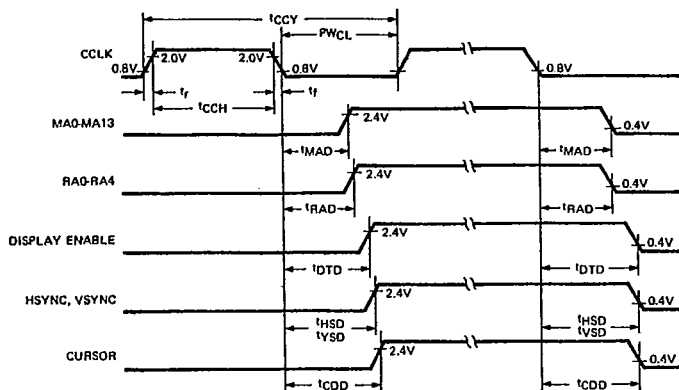




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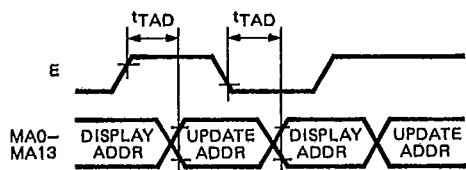
Memory and Video Interface Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

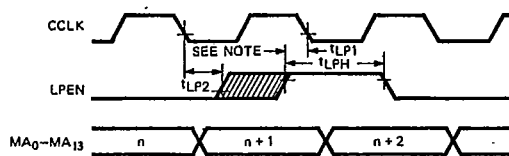


Symbol	Parameter	Min.	Typ.	Max.	Units
t _{CCH}	Minimum Clock Pulse Width, High	130			ns
t _{CCV}	Clock Frequency			3.7	MHz
t _r , t _f	Rise and Fall Time for Clock Input			20	ns
t _{MAD}	Memory Address Delay Time		100	160	ns
t _{RAD}	Raster Address Delay Time		100	160	ns
t _{DTD}	Display Timing Delay Time		160	250	ns
t _{HSD}	Horizontal Sync Delay Time		160	250	ns
t _{VSD}	Vertical Sync Delay Time		160	250	ns
t _{CDD}	Cursor Display Timing Delay Time		160	250	ns

Transparent Addressing (φ1/φ2 Interleaving)



Light Pen Strobe Timing



Note: "Safe" time position for LPEN positive edge to cause address n + 2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristics	UM6845E		UM6845EA		UM6845EB		Unit
		Min.	max.	Min.	Max.	Min.	Max.	
t _{LPH}	LPEN Strobe Width	100	—	100	—	100	—	ns
t _{LP1}	LPEN to CCLK Delay	—	120	—	120	—	120	ns
t _{LP2}	CCLK to LPEN Delay	—	0	—	0	—	0	ns

t_r and t_f = 20 ns (max.)

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UM6845E/EA/EB

MPU Interface Signal Description

E (Enable)

The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the UM6845E/EA/EB. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the UM6845E/EA/EB to be easily interfaced to non-6500-compatible microprocessors.

R/W (Read/Write)

The R/W signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/W pin allows the processor to read the data supplied by the UM6845E/EA/EB; a low on the R/W pin allows a write to the UM6845E/EA/EB.

CS (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The UM6845E/EA/EB is selected when CS is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writing into the Address Register and reads from the Status Register. The Address Register contains the identity of the register accessed when RS is high.

DB0-DB7 (Data Bus)

The DB0-DB7 pins are the eight data lines used for transfer of data between the processor and the UM6845E/EA/EB. These lines are bi-directional and are normally high-impedance except during read/write cycles when the chip is selected.

Video Interface Signal Description

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the UM6845E/EA/EB is generating active display information. The number of horizontally displayed characters and the number of vertically displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE

signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

RES

The RES signal is an active-low input used to initialize all internal scan counter circuits. When RES is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. RES must stay low for at least one CCLK period. All scan timing is initiated when RES goes high. In this way, RES can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0-MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-13:

- Binary
Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially numbered addresses for video display memory operations.
- Row/Column
In this mode, MA0-7 functions as the column addresses C0-7, and MA8-13, as row addresses R0-R5. In this case, the software may handle addresses in terms of row and column locations, but additional address compression circuits are needed to convert C0-7 and R0-5 into a memory-efficient binary scheme.





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RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the UM6845E/EA/EB is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the UM6845E/EA/EB with only a small amount of external circuitry.

Description of Internal Registers

Figure 1 illustrates the format of a typical video display and shows the functions of the various UM6845E/EA/EB internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct UM6845E/EA/EB data transfers to and from the system MPU. It contains the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

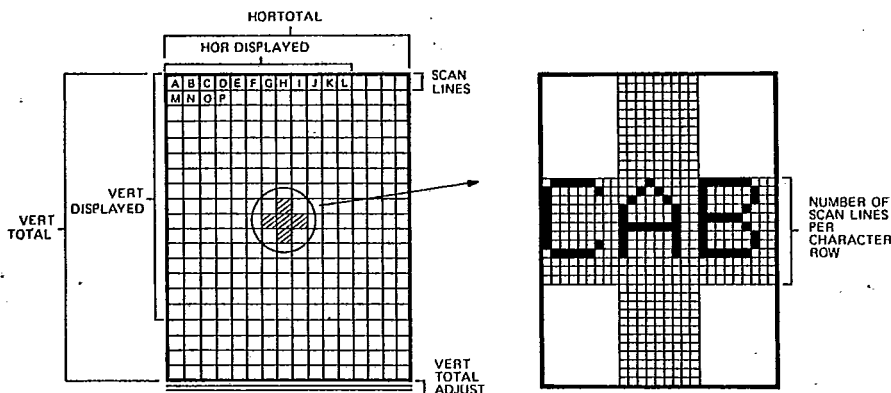
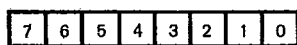


Figure 1. Video Display Format

Status Register

This 3-bit register is used to monitor the status of the CRT, as follows:



- 7
 - 6
 - 5
 - 4 NOT USED
 - 3
 - 2
 - 1
 - 0
- VERTICAL BLANKING
 "0": Scan is not currently in vertical blanking portion of its timing
 "1": Scan currently is in its vertical blanking time.
- LPEN REGISTER FULL
 "0": This bit goes to "0" whenever either register R16 or R17 is read by the MPU.
 "1": This bit goes to "1" whenever a LPEN strobe occurs.
- UPDATE READY
 "0": This bit goes to "0" when register R31 has been either read or written by the MPU.
 "1": This bit goes to "1" when an Update Strobe occurs.

Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Display (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

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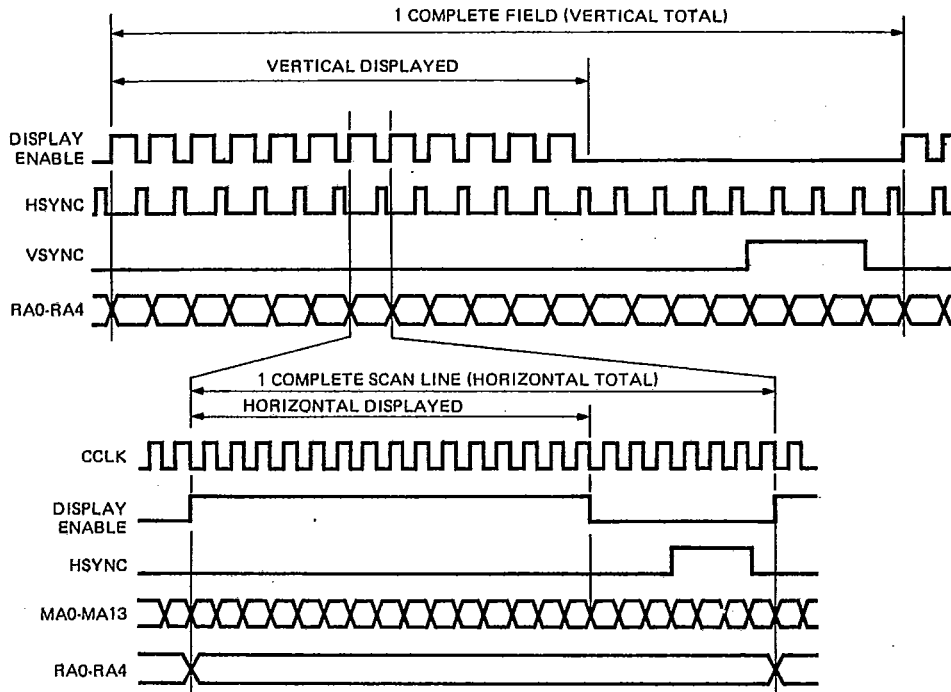
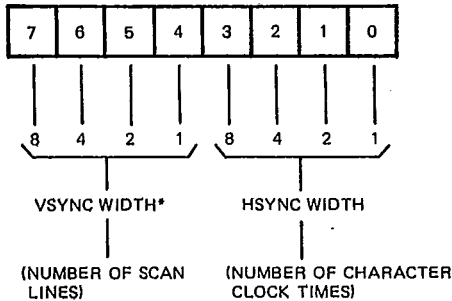


Figure 2. Vertical and Horizontal Timing



Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the UM6845E/EA/EB to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then RES may be used to provide absolute synchronization.

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time for the VSYNC pulse and thus is used to position the displayed text in the vertical direction

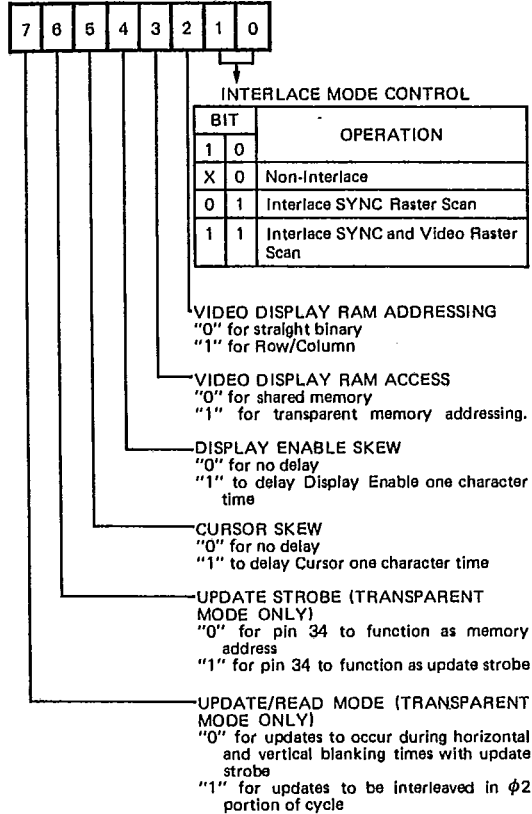
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Mode Control (R8)

This register is used to select the operating modes of the UM6845E/EA/EB and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing, minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R 10 are used to select the cursor mode, as follows:

BIT		Cursor Mode
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16 x field period
1	1	Blink at 32 x field period

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underlined. Registers R14 and R15 are used to control

the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register containing the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the UM6845E/EA/EB as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register containing the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register containing the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, on the next negative-going edge of CCLK the contents of the internal scan counter are stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register containing the memory address at which the next read or update will occur (for transparent address mode only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

Description of Operation

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this



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Straight Binary Addressing Sequence

TOTAL = 90												
DISPLAY = 80												
TOTAL = 34 DISPLAY = 24	0	1	2	77	78	79	80	81	...	89
	80	81	82	167	168	169	160	161	...	169
	160	161	162	237	238	239	240	241	...	249

	1760	1761	1762	1837	1838	1839	1840	1841	...	1849
	1840	1841	1842	1917	1918	1919	1920	1921	...	1929
	1920	1921	1922	1997	1998	1999	2000	2001	...	2009
	2000	2001	2002	2077	2078	2079	2080	2081	...	2089

	2640	2641	2642	2217	2218	2219	2220	2221	...	2229

Row/Column Addressing Sequence

TOTAL = 90													
DISPLAY = 80													
COLUMN ADDRESS (MA0-MA7)													
TOTAL = 34 DISPLAY = 24 ROW ADDRESS (MA8-MA13)	0	1	2	77	78	79	80	81	...	89	
	1	256	257	258	333	334	335	336	337	...	345
	2	512	513	514	589	590	591	592	593	...	601

	21
	22	5632	5633	5634	5709	5710	5711	5712	5713	...	5721
	23	5888	5889	5890	5965	5966	5967	5968	5969	...	5977
	24	6144	6145	6146	6221	6222	6223	6224	6225	...	6233
	25	6400	6401	6402	6477	6478	6479	6480	6481	...	6489

	33	8448	8449	8450	8525	8526	8527	8528	8529	...	8537

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

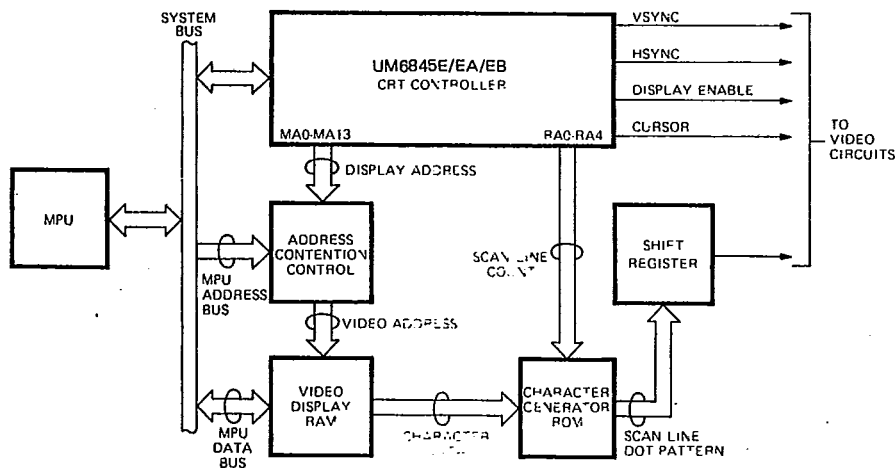


Figure 5. Shared Memory System Configuration



2. Transparent Memory Addressing.

For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the

UM6845E/EA/EB. All MPU accesses are made via the UM6845E/EA/EB and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

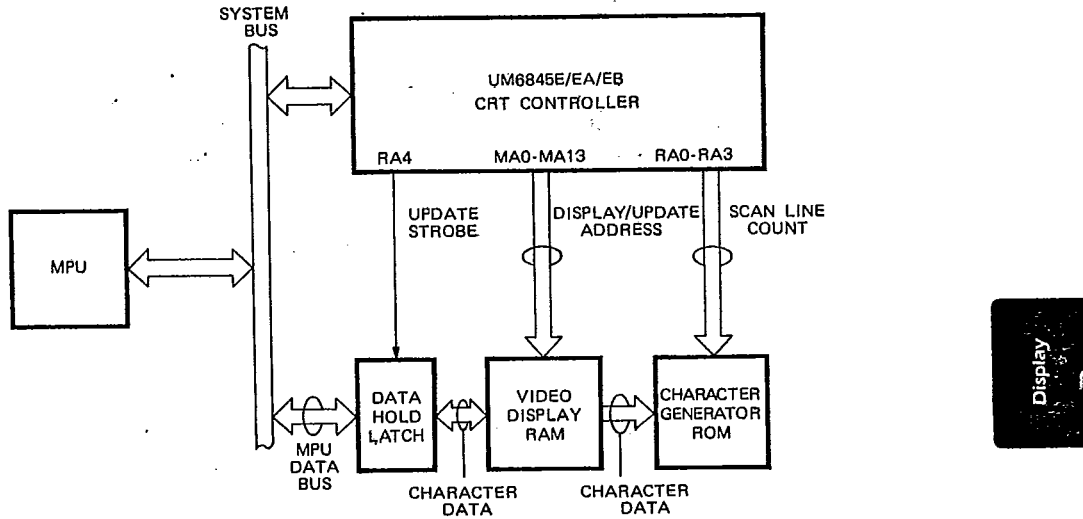


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates only).

Memory Contention Schemes for Shared Memory Addressing

From the Figure 5 it is clear that both the UM6845E/EA/EB and the system MPU must be capable of addressing the video display memory. The UM6845E/EA/EB repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual contention requirement are apparent:

■ MPU Priority

In this technique, the address lines to the video display memory are normally driven by the UM6845E/EA/EB unless the MPU needs access, in which case the MPU addresses immediately over-ride those from the UM6845E/EA/EB and the MPU has immediate access.

■ $\phi 1/\phi 2$ Memory Interleaving

This method gives both the UM6845E/EA/EB and the MPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when E is low), the UM6845E/EA/EB address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the UM6845E/EA/EB and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

■ Vertical Blanking

With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.



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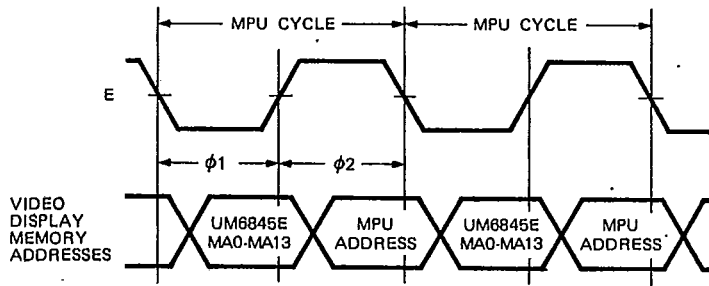


Figure 7. $\phi 1/\phi 2$ Interleaving

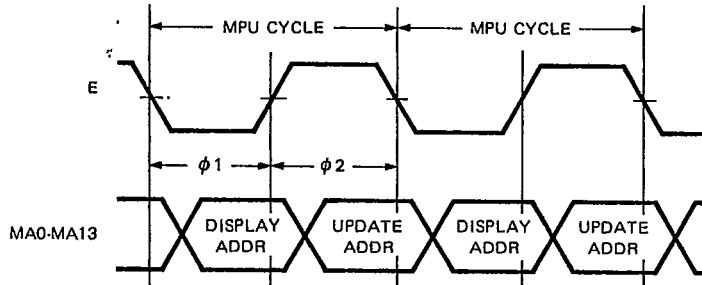


Figure 8. $\phi 1/\phi 2$ Transparent Interleaving

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the UM6845E/EA/EB. In effect, the contention is handled by the UM6845E/EA/EB. As a result, the schemes for accessing MPU memory are different:

■ **$\phi 1/\phi 2$ Interleaving**

This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi 2$ address is generated from the Update Address Register (Registers R18 and R19) in the UM6845E/EA/EB. Thus, the MPU must first load the address to be accessed into R18/R19. This address is then always gated

onto the MA lines during $\phi 2$. Figure 8 shows the timing.

■ **Horizontal/Vertical Blanking**

In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blanking times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STR) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

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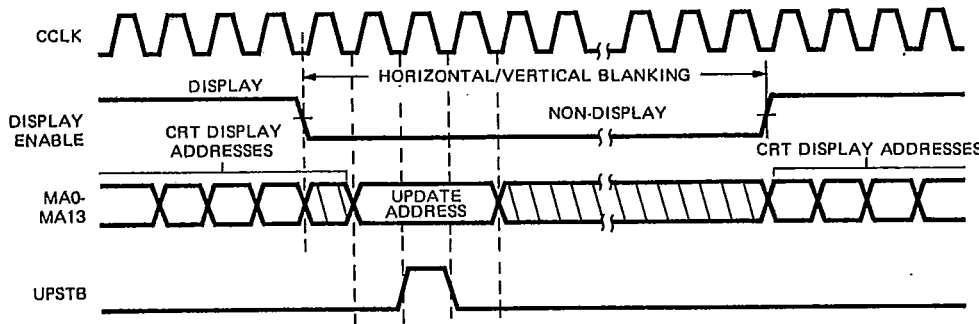


Figure 9. Retrace Update Timings

Interlaced Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode

In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlaced Sync Mode

This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in device operation: in alternate fields, the position of the VSYNC signal is delayed by 1/2 of a scan line time. This is illustrated in Figure 11, and is the only deviance of UM6845E/EA/EB operation in this mode.

c) Interlaced Sync and Video Mode

This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlaced-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

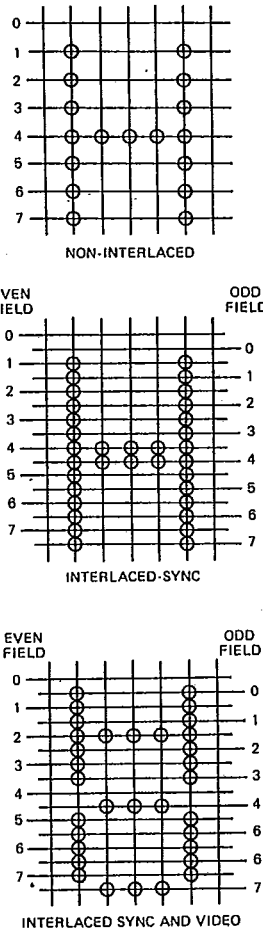


Figure 10. Comparison of Display Modes



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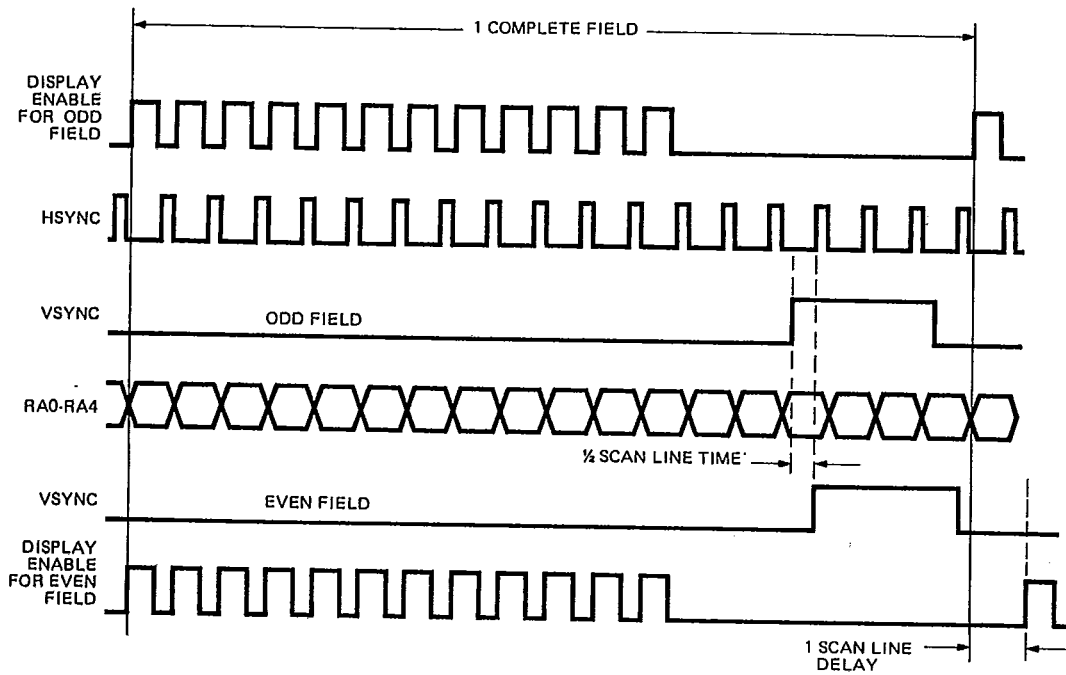


Figure 11. Interlaced Sync Mode and Interlaced Sync & Video Mode Timing

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effects of the delays.

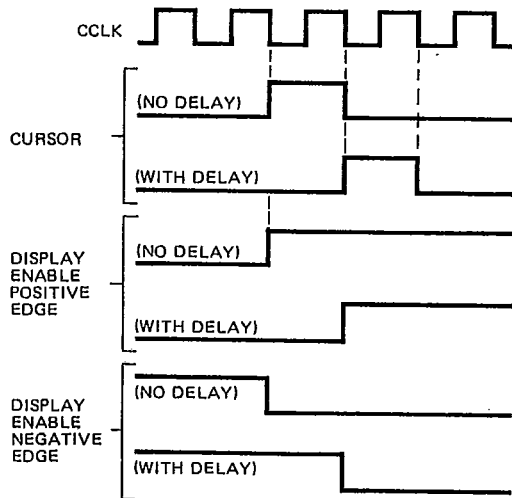


Figure 12. Cursor and Display Enable Skew

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UM6845E/EA/EB

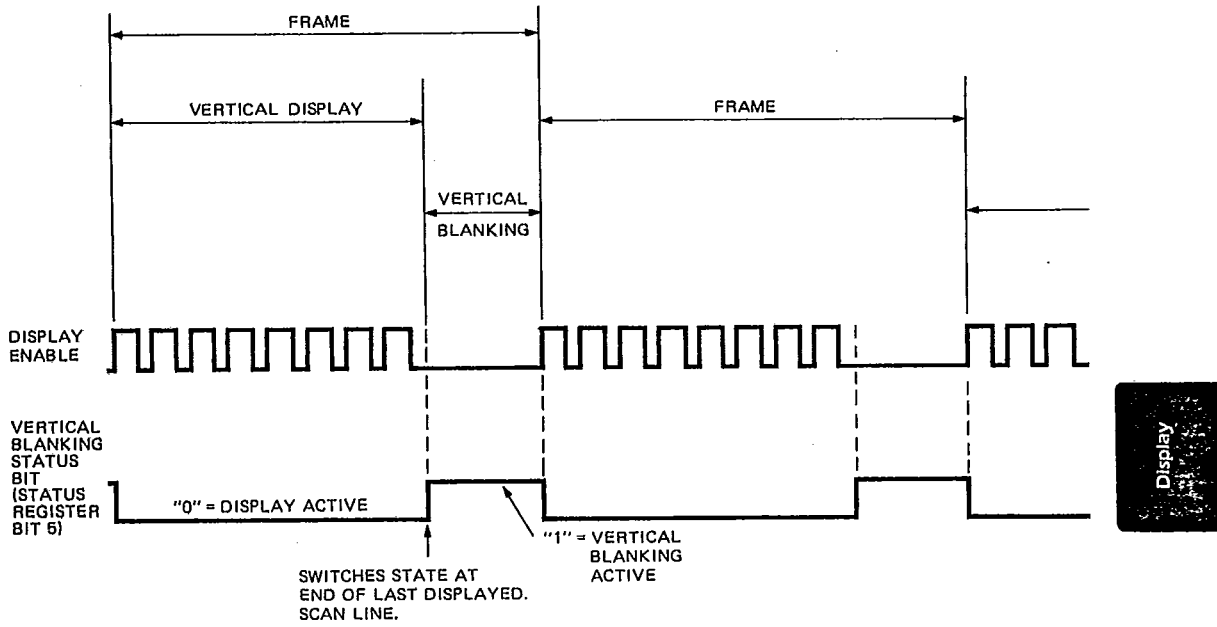


Figure 13. Operation of Vertical Blanking Status Bit



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UM6845E/EA/EB

CRTC Register Comparison Table

NON-INTERLACED

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R/RA/RB HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-1	Interlace	Interlace	Interlace	Interlace
Mode Select B2	—	—	—	Row/Column or Binary Addr.
B3	—	—	—	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	—	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	—	Display Enable Skew	Cursor Skew
B6	(Cursor Skew *1)	—	Cursor Skew	RA4/
B7	(Cursor Skew *1)	—	Cursor Skew	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write Only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write Only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes

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UM6845E/EA/EB

CRTC Register Comparison Table (Continued)

INTERLACED SYNC

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R/RA/RB HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even

INTERLACED SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R6 Vdisp	Total	Total/2	Total	Total
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even
lcCLK	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz



Ordering Information

Part Number	CPU Clock Rate	Package
UM6845E	1 MHz	40L DIP
UM6845EA	2 MHz	40L DIP
UM6845EB	3 MHz	40L DIP