

Integrated Power MOSFET with PNP Low $V_{CE(sat)}$ Switching Transistor

This integrated device represents a new level of safety and board-space reduction by combining the 20V P-Channel FET with a PNP Silicon Low $V_{CE(sat)}$ switching transistor. This newly integrated product provides higher efficiency and accuracy for battery powered portable electronics.

Features

- Low $R_{DS(on)}$ (MOSFET) and Low $V_{CE(sat)}$ (Transistor)
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive (MOSFET)
- Performance DFN Package
- This is a Halogen-Free Device

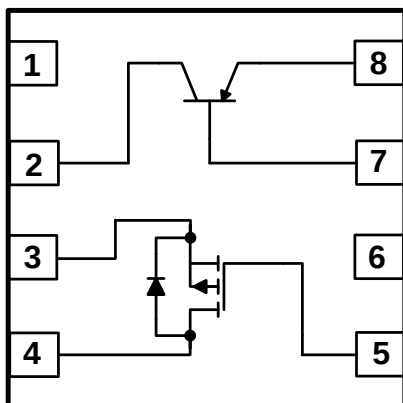
Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

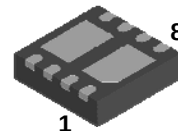
Ordering Information

Device	Marking	Package
SUM202MN	SUM202	DFN8

Simple Schematic



DFN-8



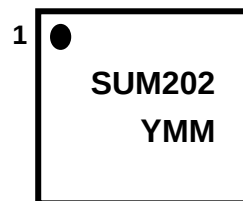
MOSFET

BV_{DSS}	$R_{DS(on)}$ Typ.	I_D Max
-20V	48m Ω @ $V_{GS} = -4.5V$	-5.3A
	65m Ω @ $V_{GS} = -2.5V$	

PNP BJT

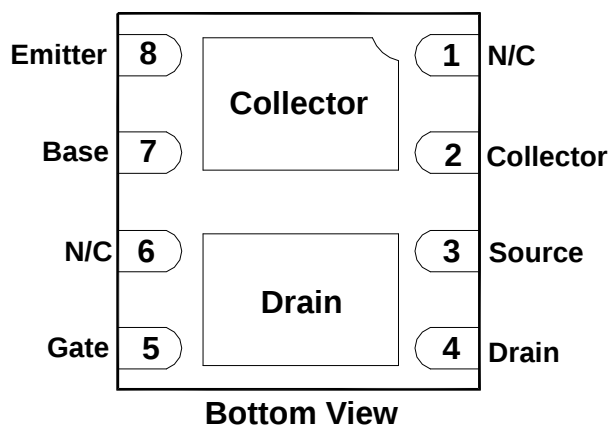
BV_{CEO}	BV_{EBO}	I_C Max
-12V	-5V	-5A

Marking Diagram



Column 1 : Device Code
Column 2 : Date Code (year, month)

PIN Connection



Absolute maximum ratings for P-Ch MOSFET

(Ta=25°C)

Characteristic	Symbol		Rating		Unit
			5sec	Steady State	
Drain-source voltage	V _{DSS}		-20		V
Gate-source voltage	V _{GSS}		±12		V
Drain current (DC) ^(Note.1)	I _D	T _A =25℃	-5.3	-3.9	A
		T _A =85℃	-3.8	-2.8	A
Drain current (Pulsed)	I _{DP}		±20		A
Continuous Source current	I _S		-5.3	-3.9	A
Total Power dissipation ^(Note.1)	P _D	T _A =25℃	2.5	1.3	W
		T _A =85℃	1.3	0.7	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}		-55 ~ 150		℃

Absolute maximum ratings for PNP Transistor

(Ta=25°C)

Characteristic	Symbol	Rating	Unit
Collector-Base voltage	V_{CBO}	-15	V
Collector-Emitter voltage	V_{CEO}	-12	V
Emitter-Base voltage	V_{EBO}	-5	V
Collector current – continuous	I_C	-5	A
Peak Collector current	I_{CM}	-15	A

Thermal Characteristics for P-Ch MOSFET

Characteristic	Symbol	Condition	Typ.	Max.	Unit
Junction to Ambient (Note.5)	$R_{TH(J-A)}$	$t \leq 5 \text{ sec}$	40	50	°C/W
		Steady State	80	95	
Junction to Foot (Drain)	$R_{TH(J-F)}$	Steady State	15	20	°C/W

Thermal Characteristics for PNP Transistor

Characteristic	Symbol	Max.	Unit
Total Device Dissipation	P_D (Note.2)	635	mW
Thermal Resistance, Junction to Ambient	$R_{TH(J-A)}$ (Note.2)	200	°C/W
Total Device Dissipation	P_D (Note.3)	1.35	W
Thermal Resistance, Junction to Ambient	$R_{TH(J-A)}$ (Note.3)	90	°C/W
Thermal Resistance, Junction to Lead #1	$R_{TH(J-L)}$	15	°C/W
Total Device Dissipation (Single Pulse < 10 sec)	$P_{D\text{single}}$ (Note.3&4)	2.75	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 ~ 150	°C

1. Surface Mounted on FR4 Board using 1in square pad size (Cu area =1.27 in square [1 oz] including traces)

2. FR-4 @ 100 mm², 1 oz copper traces.3. FR-4 @ 500 mm², 1 oz copper traces.

4. Thermal response.

Electrical Characteristics for P-Ch MOSFET

(Ta=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Drain-source breakdown voltage	BV_{DSS}	$I_D = -250\mu A, V_{GS} = 0$	-20	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D = -250\mu A, V_{DS} = V_{GS}$	-0.6		-1.2	V
Drain-source cut-off current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$	-	-	-1	μA
Gate leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$	-	-	± 100	nA
On-State Drain Current (Note.6)	$I_{D(ON)}$	$V_{DS} \leq -5.0V, V_{GS} = -4.5V$	-20	-	-	A
Drain-source on-resistance (Note.6)	$R_{DS(ON)}$	$V_{GS} = -3.6V, I_D = -1.0A$	-	50	60	m Ω
		$V_{GS} = -2.5V, I_D = -1.0A$	-	70	83	
Forward transfer conductance (Note.6)	g_{fs}	$V_{DS} = -10V, I_D = -3.9A$	-	12	-	S
Diode Forward Voltage (Note.6)	V_{SD}	$I_S = -2.1A, V_{GS} = 0V$	-	-0.8	-1.2	V
Dynamic (Note.7)						
Input capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -5V,$ $f = 1MHz$	-	710	-	pF
Output capacitance	C_{oss}		-	400	-	
Reverse transfer capacitance	C_{rss}		-	140	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -10V, I_D = -1.0A$ $R_G = 6\Omega, R_D = 10\Omega$ $V_{GS} = -4.5V$	-	14	30	ns
Rise time	t_r		-	22	55	
Turn-off delay time	$t_{d(off)}$		-	42	100	
Fall time	t_f		-	35	70	
Total gate charge	Q_g	$V_{DD} = -10V, V_{GS} = -4.5V$ $I_D = -3.9A$	-	9.7	22	nC
Gate-source charge	Q_{gs}		-	1.2	-	
Gate-drain charge	Q_{gd}		-	3.6	-	

5. Surface Mounted on FR4 Board using 1 inch square pad size (Cu area =1.27 inch square [1 oz] including traces).

6. Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

7. Guaranteed by design, not subject to production testing.

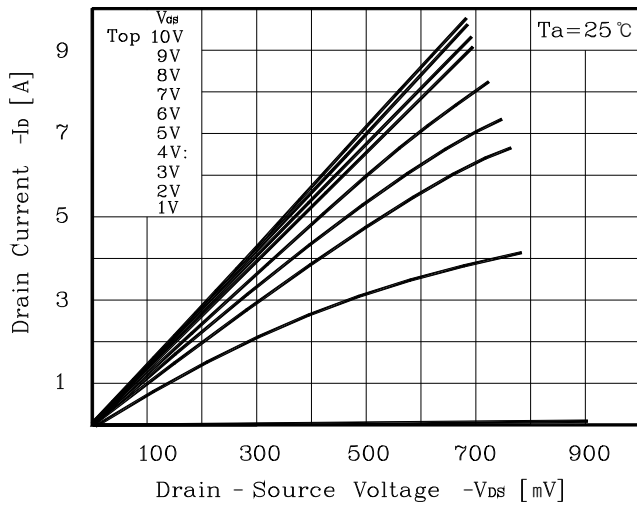
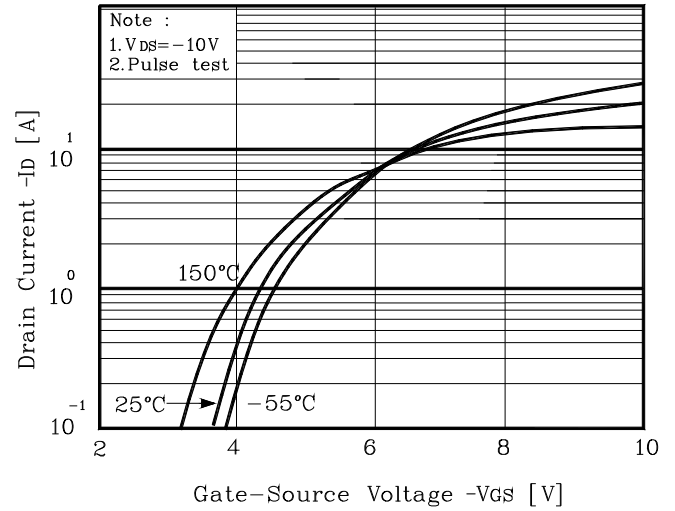
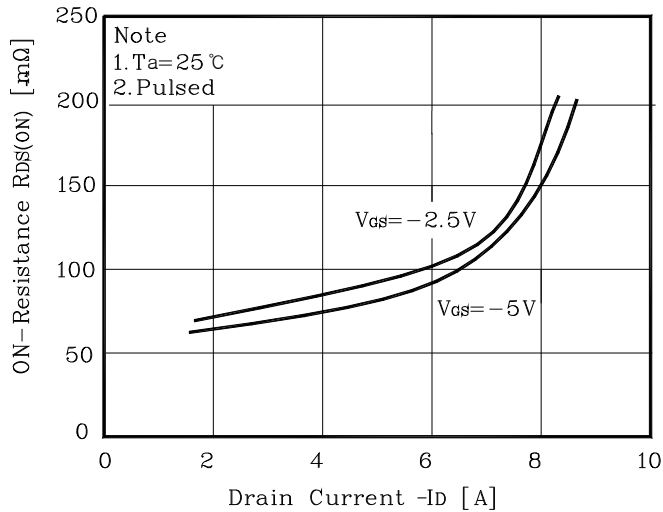
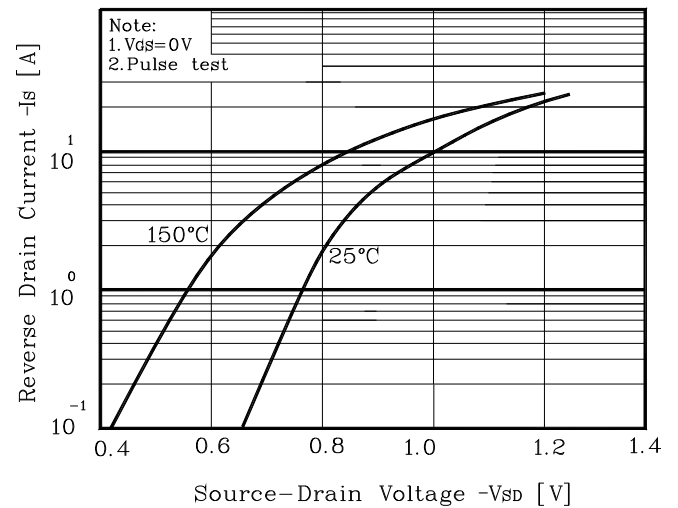
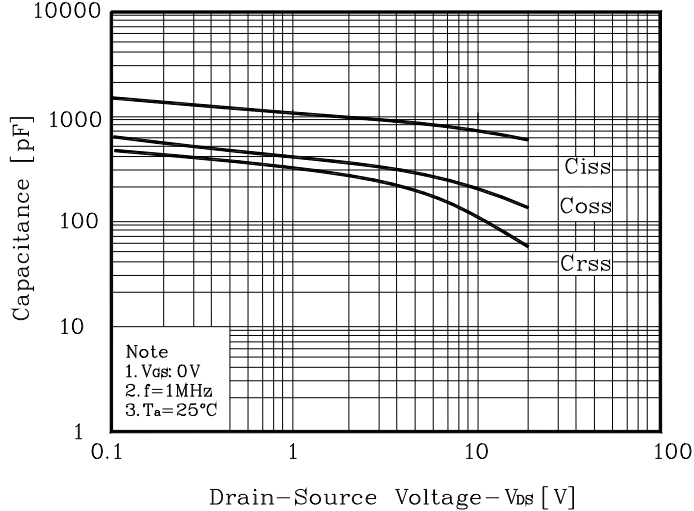
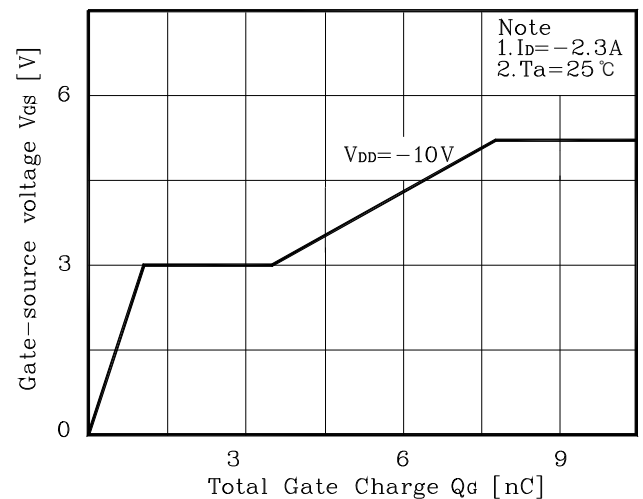
Electrical Characteristics for PNP Transistor

(Ta=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics						
Collector-Base breakdown voltage	BV_{CBO}	$I_C = -50\mu A, I_E = 0$	-15	-	-	V
Collector-Emitter breakdown voltage	BV_{CEO}	$I_C = -1mA, I_B = 0$	-12	-	-	V
Emitter-Base breakdown voltage	BV_{EBO}	$I_E = -50\mu A, I_C = 0$	-5	-	-	V
Collector cut-off current	I_{CBO}	$V_{CB} = -15V, I_E = 0$	-	-	-1	μA
Emitter cut-off current	I_{EBO}	$V_{EB} = -5V, I_C = 0$	-	-	-1	μA
On Characteristics						
DC current gain (Note.8)	h_{FE}^*	$V_{CE} = -2V, I_C = -500mA$	160	-	320	-
Base-Emitter on voltage (Note.8)	$V_{BE(on)}$	$V_{CE} = -2V, I_C = -500mA$	-	-	-1	V
Collector-Emitter saturation voltage (Note.8)	$V_{CE(sat)}$	$I_C = -3A, I_B = -150mA$	-	-0.2	-0.5	V
Transition frequency	f_T	$V_{CB} = -5V, I_C = -500mA$	-	150	-	MHz
Collector output capacitance	C_{ob}	$V_{CB} = -10V, I_E = 0, f = 1MHz$	-	-	50	pF

8. Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Electrical Characteristic Curves (P-Channel MOSFET)

Fig. 1 $I_D - V_{DS}$ Fig. 2 $I_D - V_{GS}$ Fig. 3 $R_{DS(on)} - I_D$ Fig. 4 $I_S - V_{SD}$ Fig. 5 Capacitance - V_{DS} Fig. 6 $V_{GS} - Q_G$ 

Electrical Characteristics (P-Channel MOSFET)

Fig. 7 $V_{DSS} - T_J$

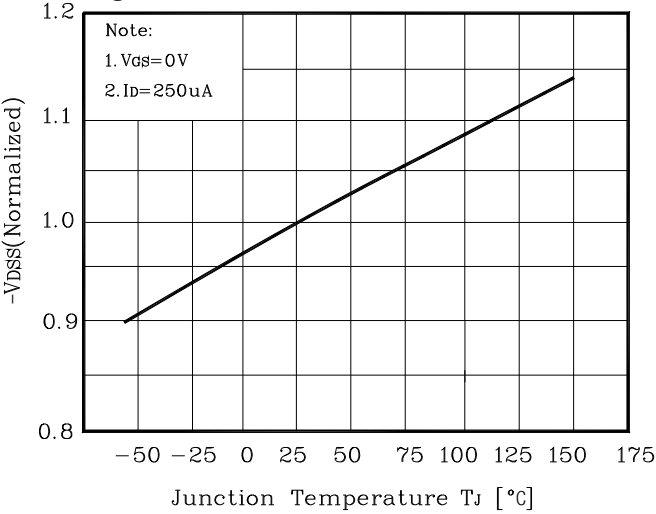


Fig. 8 $R_{DS(on)} - T_J$

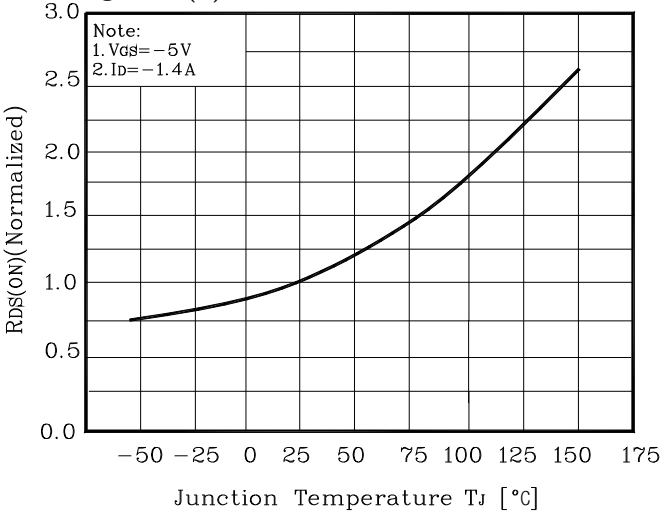
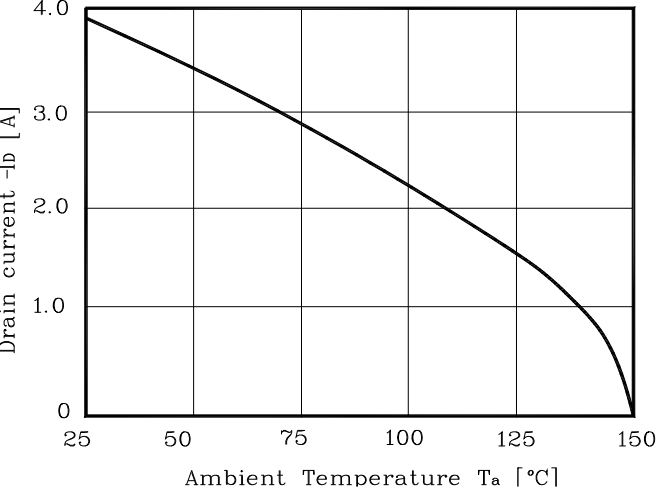


Fig. 9 $I_D - T_a$



Electrical Characteristic Curves (PNP BJT)

Fig. 1 $P_c - T_a$

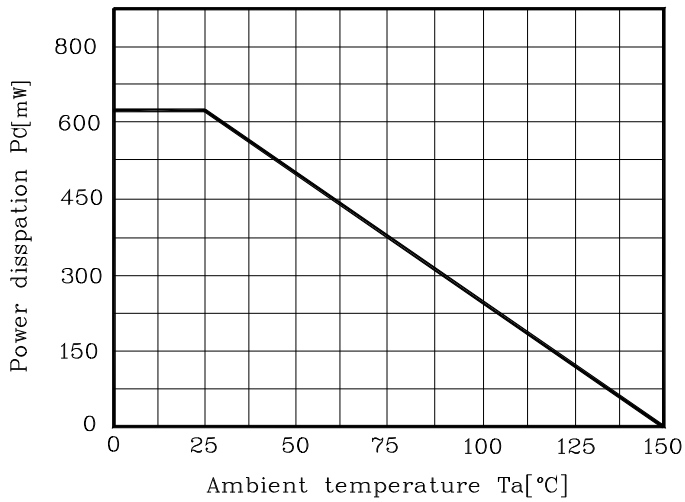


Fig. 2 $I_c - V_{BE}$

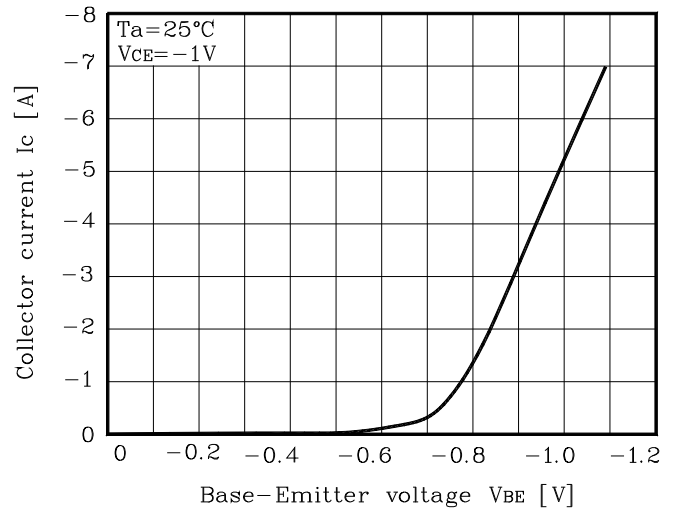


Fig. 3 $h_{FE} - I_c$

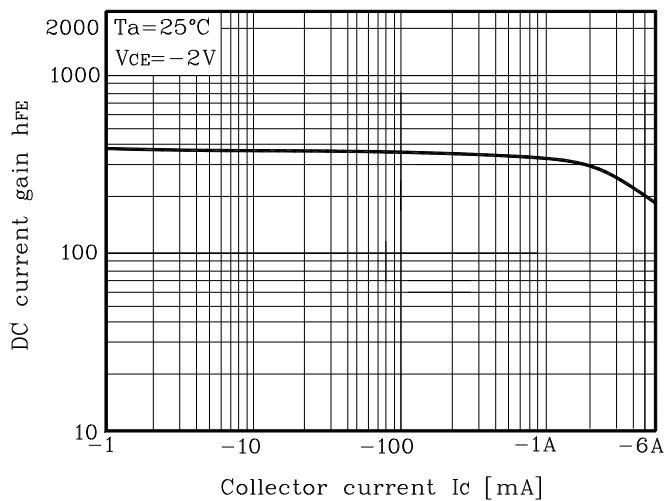
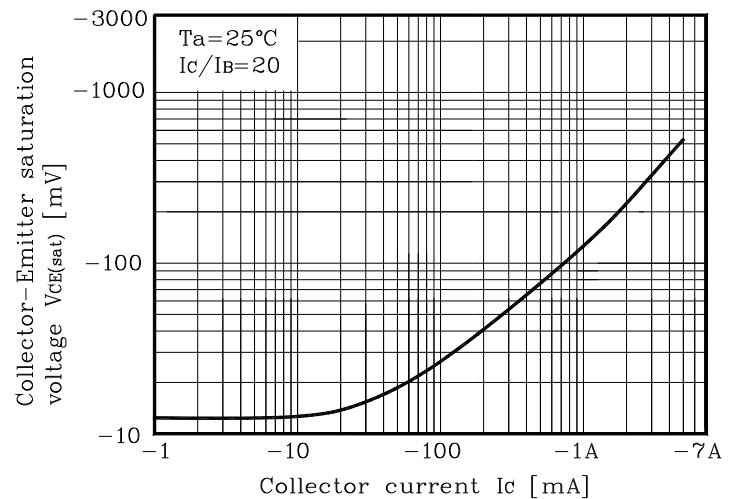
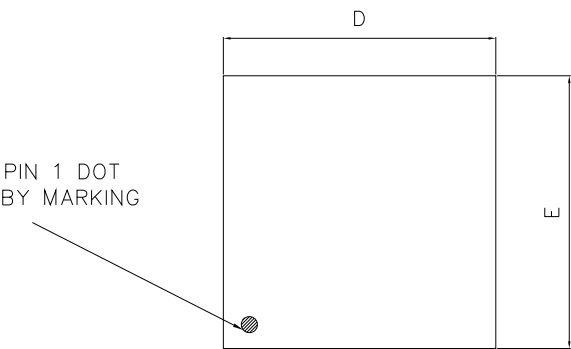


Fig. 4 $V_{CE(sat)} - I_c$

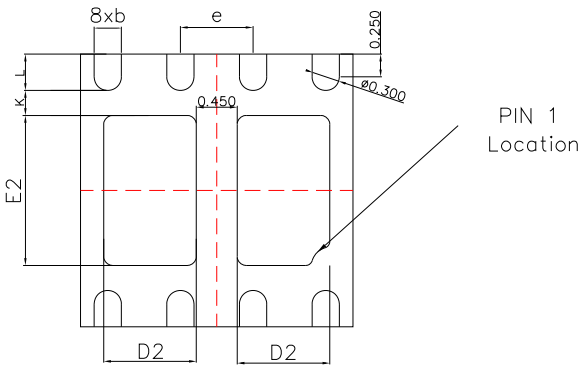


Outline Dimension

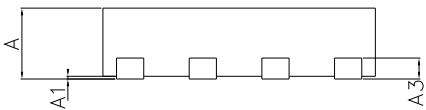
unit : mm



TOP VIEW



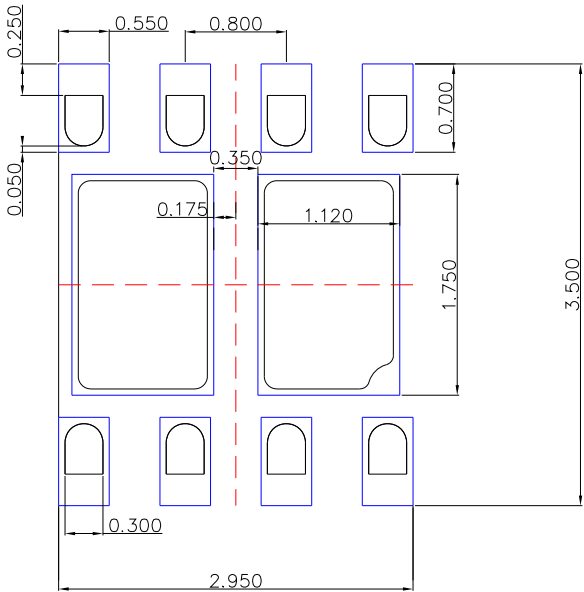
BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.20 REF.		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	0.87	1.02	1.12
E2	1.50	1.65	1.75
b	0.25	0.30	0.35
L	0.30	0.40	0.50
K	Min : 0.21		
e	0.80 BSC		

※ Recommended Land Pattern [unit: mm]



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