74LV4053

Triple single-pole double-throw analog switch

Rev. 04 — 10 August 2009 Product data sheet

1. General description

The 74LV4053 is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. It is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC4053 and 74HCT4053. Each switch has a digital select input (Sn), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). All three switches share an enable input ($\overline{E}$). A HIGH on $\overline{E}$ causes all switches into the high-impedance OFF-state, independent of Sn.

V_{CC} and GND are the supply voltage connections for the digital control inputs (Sn and $\overline{E}$). The V_{CC} to GND range is 1 V to 6 V. The analog inputs/outputs (nY0, nY1 and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2. Features

- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low ON resistance:
  - 180 Ω (typical) at $V_{CC} - V_{EE}$ = 2.0 V
  - 100 Ω (typical) at $V_{CC} - V_{EE}$ = 3.0 V
  - 75 Ω (typical) at $V_{CC} - V_{EE}$ = 4.5 V
- Logic level translation:
  - To enable 3 V logic to communicate with ±3 V analog signals
- Typical ‘break before make’ built in
- ESD protection:
  - HBM JESD22-A114-C exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

founded by Philips

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4053N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV4053D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4053DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4053PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV4053BQ	–40 °C to +125 °C	DHVQFN16	plastic dual-in line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

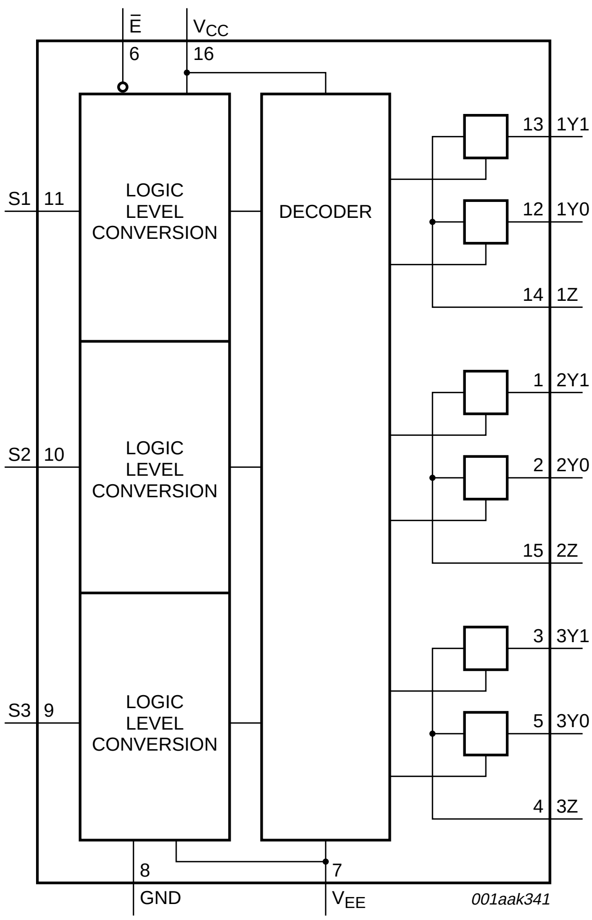


Fig 1. Functional diagram

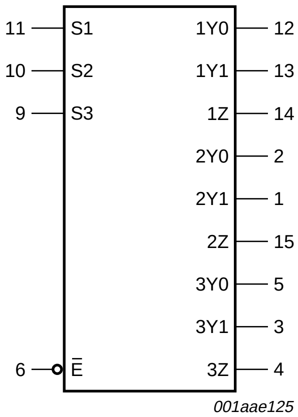


Fig 2. Logic symbol

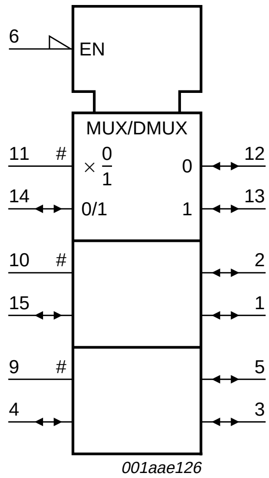


Fig 3. IEC logic symbol

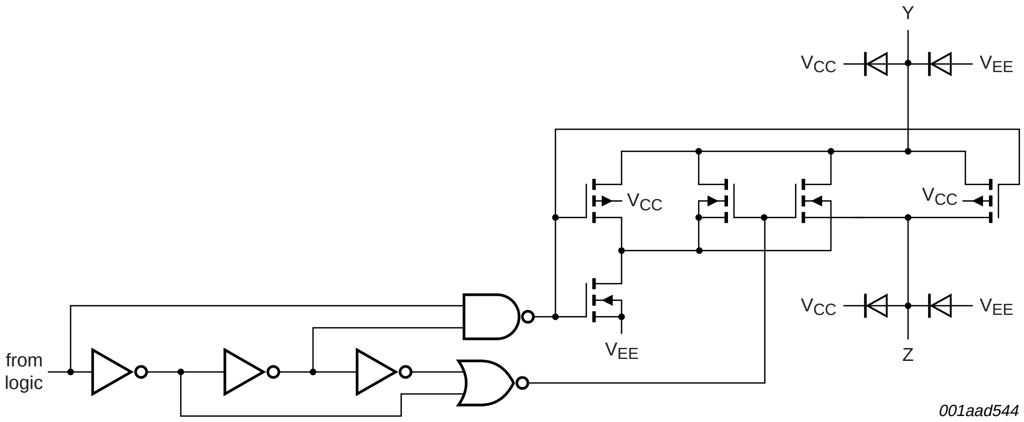


Fig 4. Schematic diagram (one switch)

5. Pinning information

5.1 Pinning

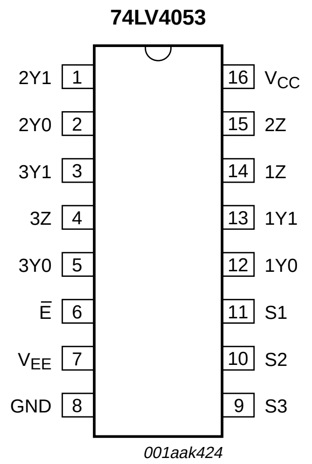


Fig 5. Pin configuration SOT38-4 and SOT109-1

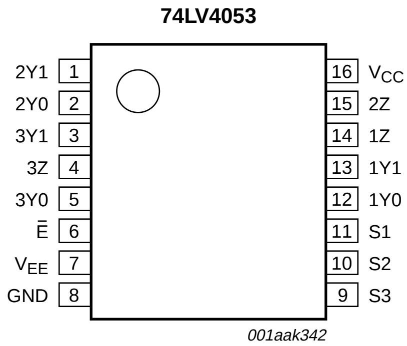


Fig 6. Pin configuration SOT338-1 and SOT403-1

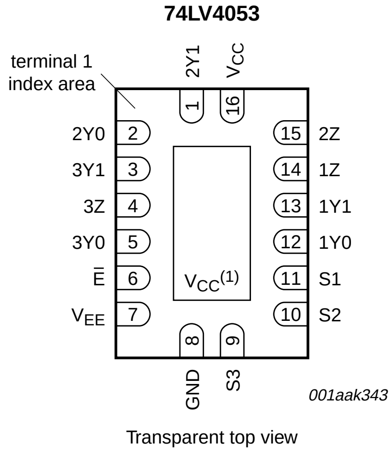


Fig 7. Pin configuration for SOT763-1

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage
GND	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
1Y0, 2Y0, 3Y0	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	14, 15, 4	common output or input
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table [1]

Inputs		Channel on
$\overline{E}$	Sn	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		[1]	–0.5	+7.0	V
I_{IK}	input clamping current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V	[2]	-	±20	mA
I_{SK}	switch clamping current	V_{SW} < –0.5 V or V_{SW} > V_{CC} + 0.5 V	[2]	-	±20	mA
I_{SW}	switch current	V_{SW} > –0.5 V or V_{SW} < V_{CC} + 0.5 V; source or sink current	[2]	-	±25	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]			
		DIP16 package		-	750	mW
		SO16 package		-	500	mW
		TSSOP16 package		-	500	mW
		DHVQFN16 package		-	500	mW

[1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE}.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	see Figure 8	1	3.3	6	V
V_I	input voltage		0	-	V_{CC}	V
V_{SW}	switch voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to 6.0 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

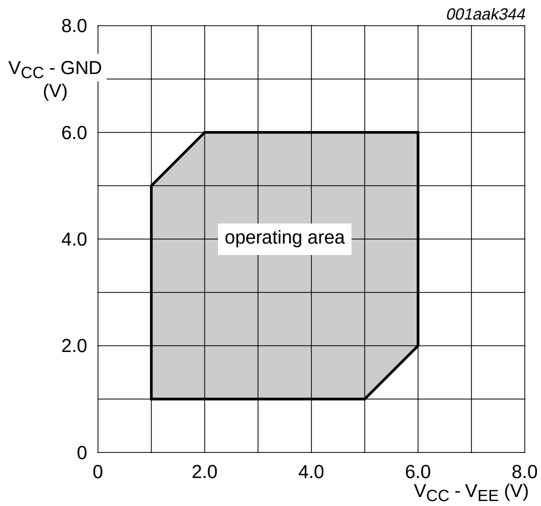


Fig 8. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

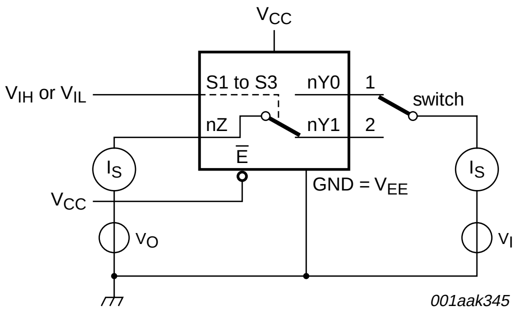
Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V	3.15	-	-	3.15	-	V
		V_{CC} = 6.0 V	4.20	-	-	4.20	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	-	1.80	V
I_I	input leakage current	$V_I = V_{CC}$ or GND						
		V_{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	-	2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_I = V_{IH}$ or V_{IL}; see Figure 9						
		V_{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	-	2.0	μA
$I_{S(ON)}$	ON-state leakage current	$V_I = V_{IH}$ or V_{IL}; see Figure 10						
		V_{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A						
		V_{CC} = 3.6 V	-	-	20	-	40	μA
		V_{CC} = 6.0 V	-	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC} - 0.6$ V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF
C_{sw}	switch capacitance	independent pins nYn	-	5	-	-	-	pF
		common pins nZ	-	8	-	-	-	pF

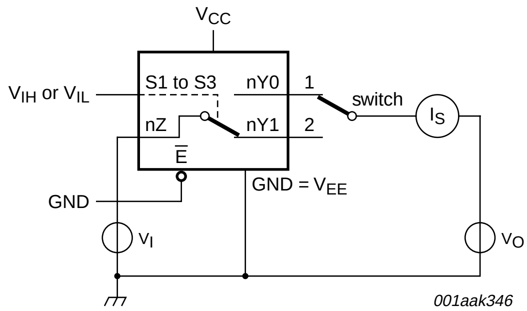
[1] Typical values are measured at T_{amb} = 25 °C.

9.1 Test circuits



$V_I = V_{CC}$ or V_{EE} and $V_O = V_{EE}$ or V_{CC}.

Fig 9. Test circuit for measuring OFF-state leakage current



$V_I = V_{CC}$ or V_{EE} and V_O = open circuit.

Fig 10. Test circuit for measuring ON-state leakage current

9.2 ON resistance

Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 11 and Figure 12.

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = 0 V to $V_{CC} - V_{EE}$						
		V_{CC} = 1.2 V; I_{SW} = 100 μA [2]	-	-	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 μA	-	180	365	-	435	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 μA	-	115	225	-	270	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 μA	-	100	200	-	245	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA	-	75	150	-	180	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA	-	70	140	-	165	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0 V to $V_{CC} - V_{EE}$						
		V_{CC} = 1.2 V; I_{SW} = 100 μA [2]	-	-	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 μA	-	5	-	-	-	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 μA	-	4	-	-	-	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 μA	-	4	-	-	-	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA	-	3	-	-	-	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA	-	2	-	-	-	Ω

Table 7. ON resistance *...continued*

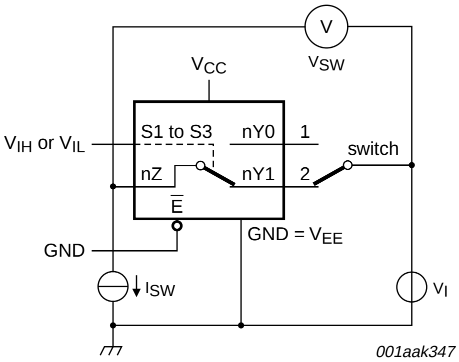
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 11 and Figure 12.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND						
		V_{CC} = 1.2 V; I_{SW} = 100 µA [2]	-	250	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 µA	-	120	280	-	325	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 µA	-	75	170	-	195	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 µA	-	70	155	-	180	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 µA	-	50	120	-	135	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 µA	-	45	105	-	120	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_I = V_{CC} - V_{EE}$						
		V_{CC} = 1.2 V; I_{SW} = 100 µA [2]	-	350	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 µA	-	170	340	-	400	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 µA	-	105	210	-	250	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 µA	-	95	190	-	225	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 µA	-	70	140	-	165	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 µA	-	65	125	-	150	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

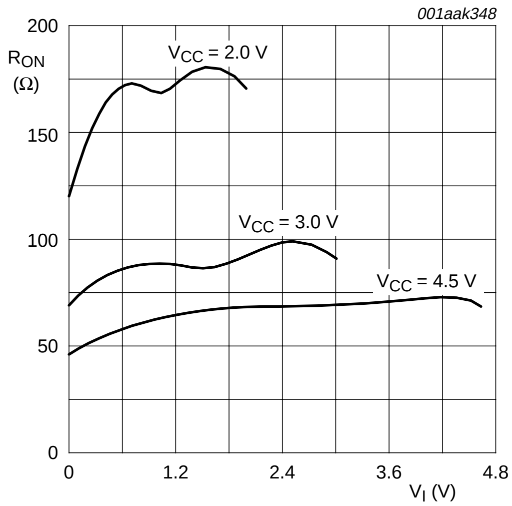
[2] When supply voltages ($V_{CC} - V_{EE}$) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

9.3 On resistance waveform and test circuit



$R_{ON} = V_{SW} / I_{SW}$.

Fig 11. Test circuit for measuring R_{ON}



V_i = 0 V to $V_{CC} - V_{EE}$

Fig 12. Typical R_{ON} as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 15.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nYn, nZ to nZ, nYn; see Figure 13	[2]						
		V_{CC} = 1.2 V		-	25	-	-	-	ns
		V_{CC} = 2.0 V		-	9	17	-	20	ns
		V_{CC} = 2.7 V		-	6	13	-	15	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	5	10	-	12	ns
		V_{CC} = 4.5 V		-	4	9	-	10	ns
		V_{CC} = 6.0 V		-	3	7	-	8	ns
t_{en}	enable time	$\overline{E}$ to nYn, nZ; see Figure 14	[2]						
		V_{CC} = 1.2 V		-	100	-	-	-	ns
		V_{CC} = 2.0 V		-	34	65	-	77	ns
		V_{CC} = 2.7 V		-	25	48	-	56	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	16	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	19	38	-	45	ns
		V_{CC} = 4.5 V		-	17	32	-	38	ns
		V_{CC} = 6.0 V		-	13	25	-	29	ns
		Sn to nYn, nZ; see Figure 14	[2]						
		V_{CC} = 1.2 V		-	125	-	-	-	ns
		V_{CC} = 2.0 V		-	43	82	-	97	ns
		V_{CC} = 2.7 V		-	31	60	-	71	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	20	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	24	48	-	57	ns
		V_{CC} = 4.5 V		-	21	41	-	48	ns
		V_{CC} = 6.0 V		-	16	31	-	37	ns

Table 8. Dynamic characteristics *…continued*
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 15.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{dis}	disable time	$\overline{E}$ to nYn, nZ; see Figure 14	[2]						
		V_{CC} = 1.2 V		-	95	-	-	-	ns
		V_{CC} = 2.0 V		-	34	61	-	73	ns
		V_{CC} = 2.7 V		-	26	46	-	54	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	17	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	20	37	-	44	ns
		V_{CC} = 4.5 V		-	18	32	-	38	ns
		V_{CC} = 6.0 V		-	15	25	-	30	ns
		Sn to nYn, nZ; see Figure 14	[2]						
		V_{CC} = 1.2 V		-	90	-	-	-	ns
		V_{CC} = 2.0 V		-	32	59	-	70	ns
		V_{CC} = 2.7 V		-	24	44	-	52	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	16	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	19	36	-	42	ns
		V_{CC} = 4.5 V		-	17	31	-	36	ns
		V_{CC} = 6.0 V		-	14	24	-	28	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	36	-	-	-	pF

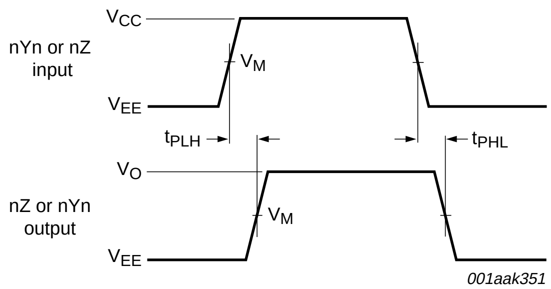
[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{SW}) \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz, f_o = output frequency in MHz
C_L = output load capacitance in pF
C_{SW} = maximum switch capacitance in pF;
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

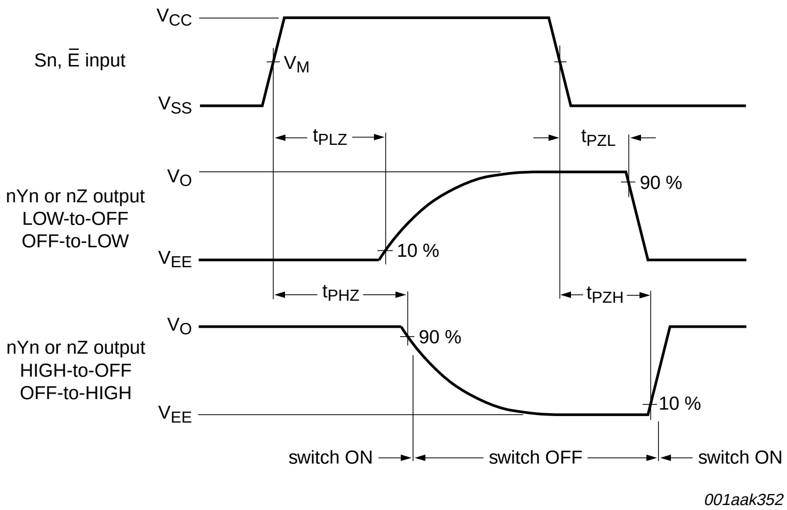
10.1 Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 13. nYn, nZ to nZ, nYn propagation delays



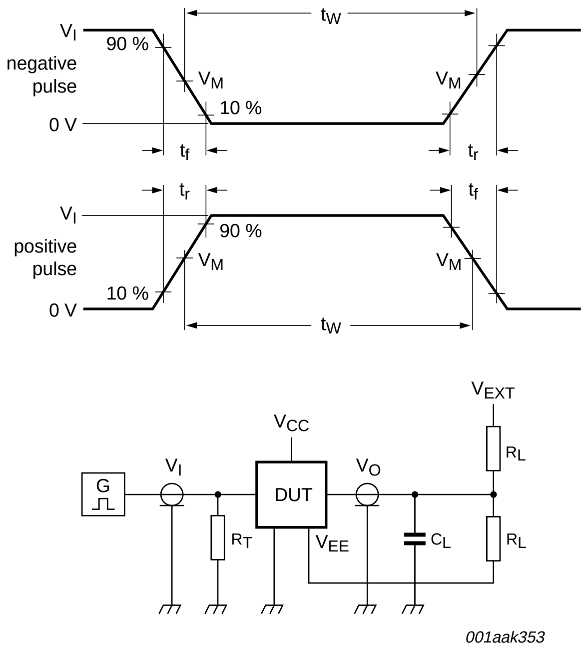
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 14. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
> 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 15. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 6 ns	50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 6 ns	15 pF, 50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$
> 3.6 V	V_{CC}	≤ 6 ns	50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$

10.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 6.0$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; C_L = 50 pF; R_L = 10 kΩ; see Figure 20					
		V_{CC} = 3.0 V; V_I = 2.75 V (p-p)		-	0.8	-	%
		V_{CC} = 6.0 V; V_I = 5.5 V (p-p)		-	0.4	-	%
		f_i = 10 kHz; C_L = 50 pF; R_L = 10 kΩ; see Figure 20					
		V_{CC} = 3.0 V; V_I = 2.75 V (p-p)		-	2.4	-	%
		V_{CC} = 6.0 V; V_I = 5.5 V (p-p)		-	1.2	-	%
$f_{(-3dB)}$	–3 dB frequency response	C_L = 50 pF; R_L = 50 Ω; see Figure 16	[1]				
		V_{CC} = 3.0 V		-	180	-	MHz
		V_{CC} = 6.0 V		-	200	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Figure 18	[2]				
		V_{CC} = 3.0 V		-	–50	-	dB
		V_{CC} = 6.0 V		-	–50	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Figure 21	[2]				
		V_{CC} = 3.0 V		-	0.11	-	V
		V_{CC} = 6.0 V		-	0.12	-	V
Xtalk	crosstalk	between switches; f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Figure 22					
		V_{CC} = 3.0 V		-	–60	-	dB
		V_{CC} = 6.0 V		-	–60	-	dB

[1] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω).

[2] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω).

10.2.1 Test circuits

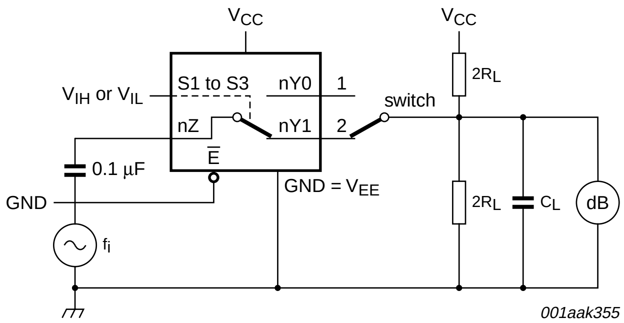
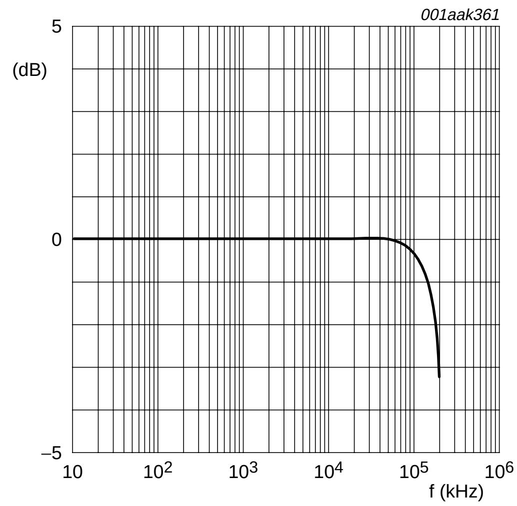


Fig 16. Test circuit for measuring frequency response



V_{CC} = 3.0 V; GND = 0 V; V_{EE} = −3.0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig 17. Typical frequency response

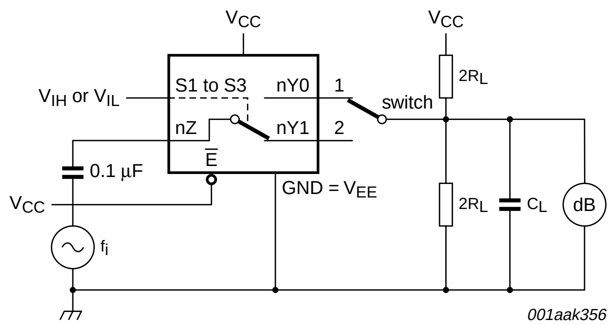
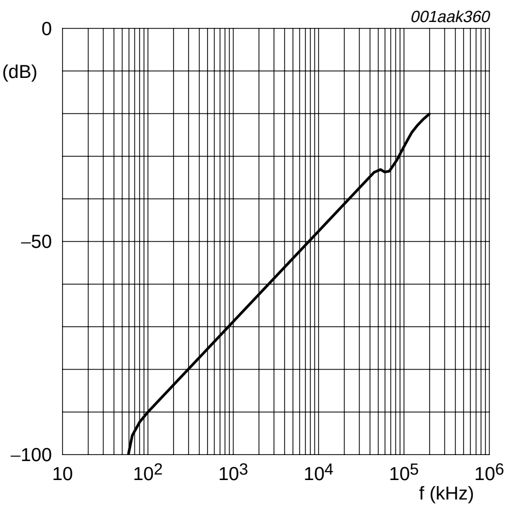


Fig 18. Test circuit for measuring isolation (OFF-state)



V_{CC} = 3.0 V; GND = 0 V; V_{EE} = −3.0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig 19. Typical isolation (OFF-state) as function of frequency

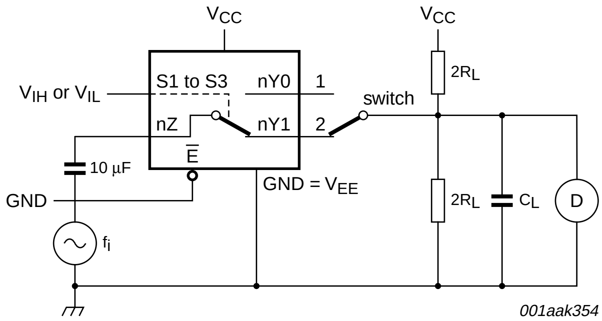
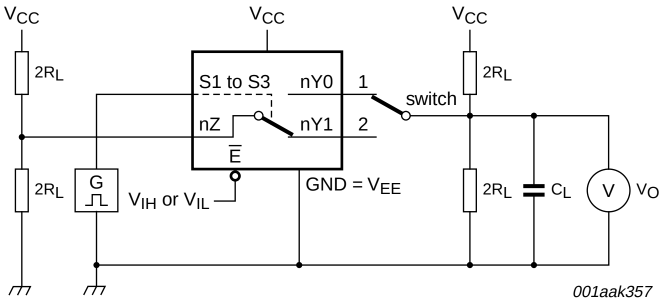
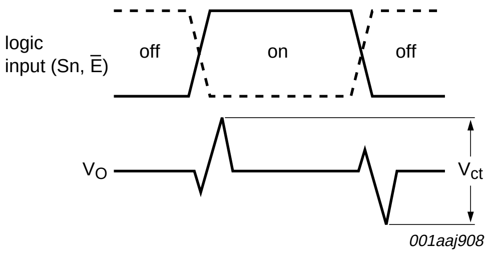


Fig 20. Test circuit for measuring total harmonic distortion



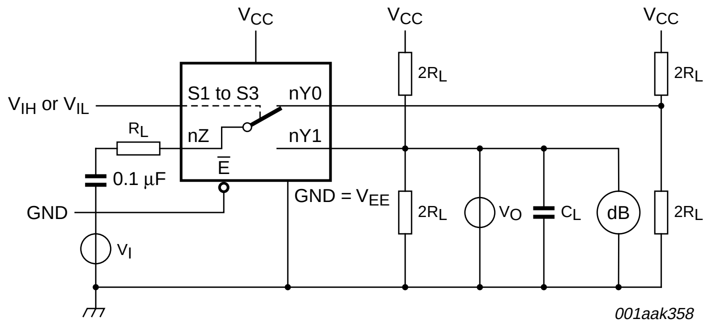
a. Test circuit



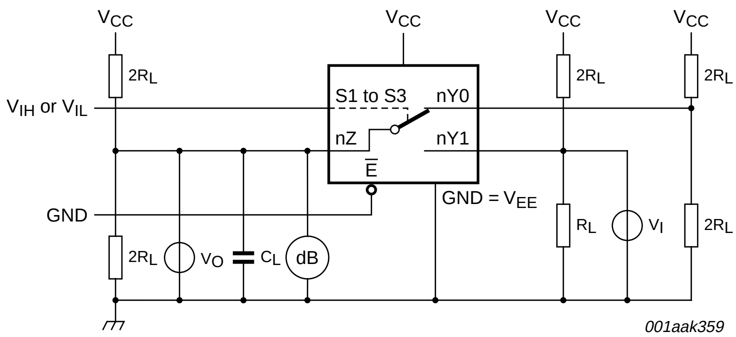
b. Input and output pulse definitions

V_I may be connected to Sn or $\overline{E}$.

Fig 21. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition

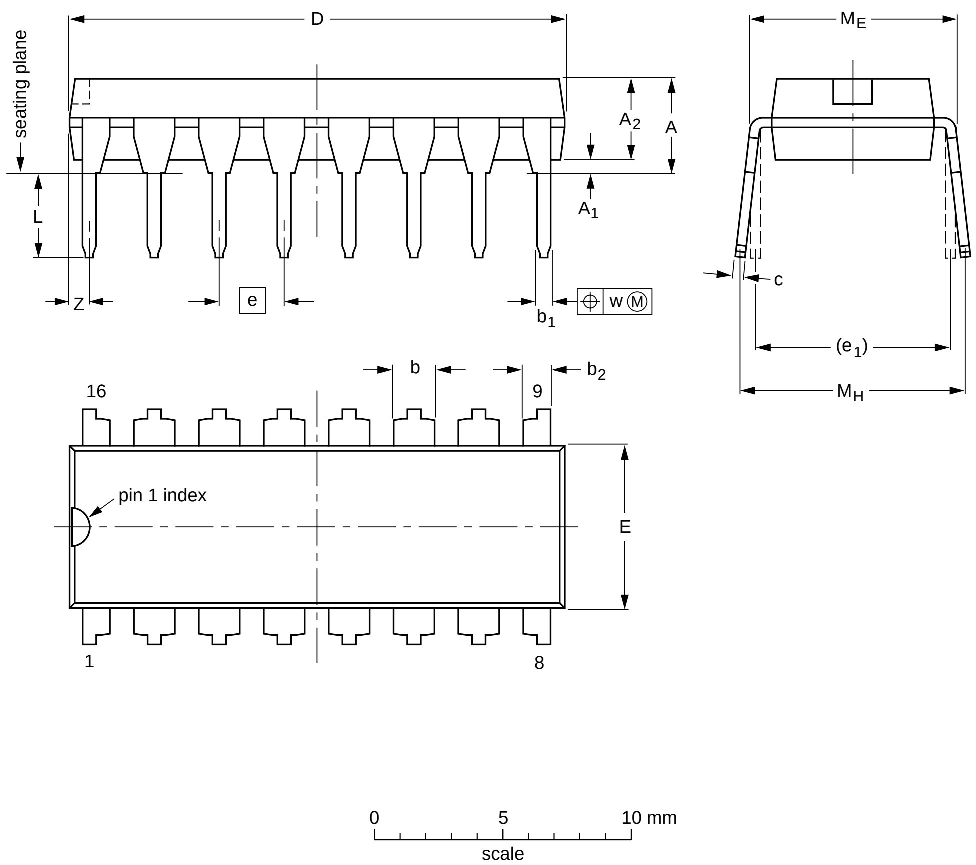


b. Switch open condition

Fig 22. Test circuit for measuring crosstalk between switches

11. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

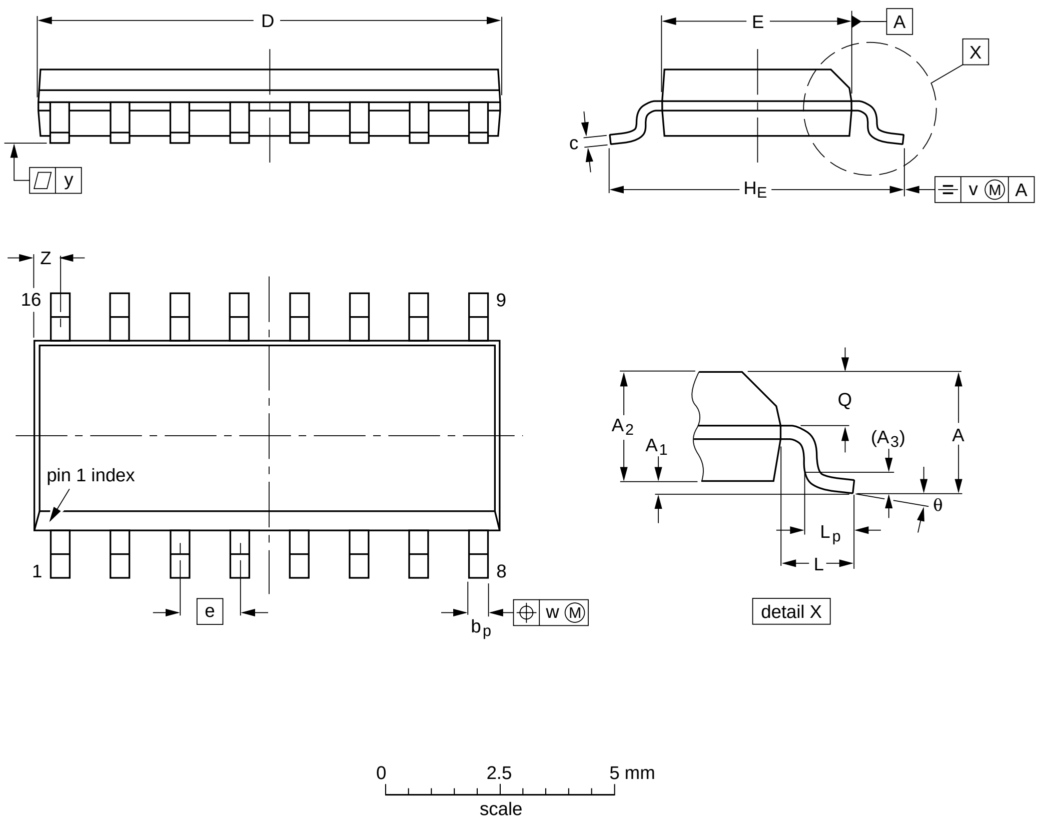
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 23. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm — **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

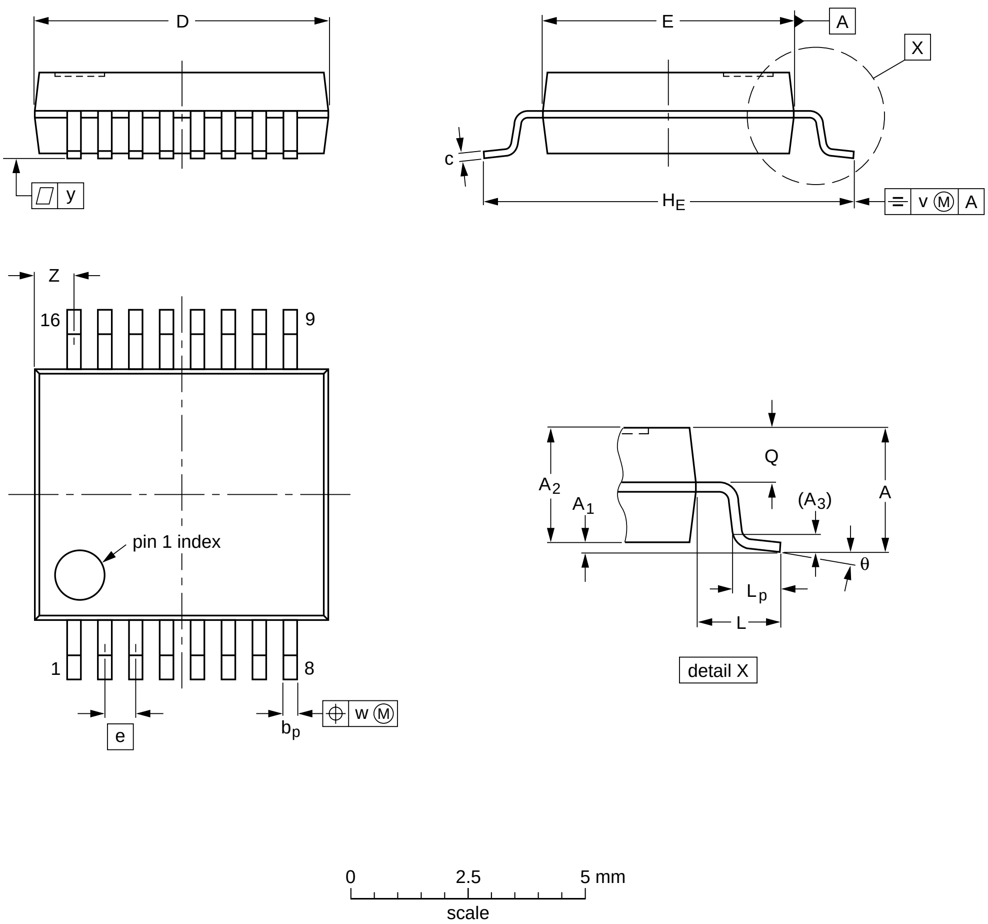
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 24. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

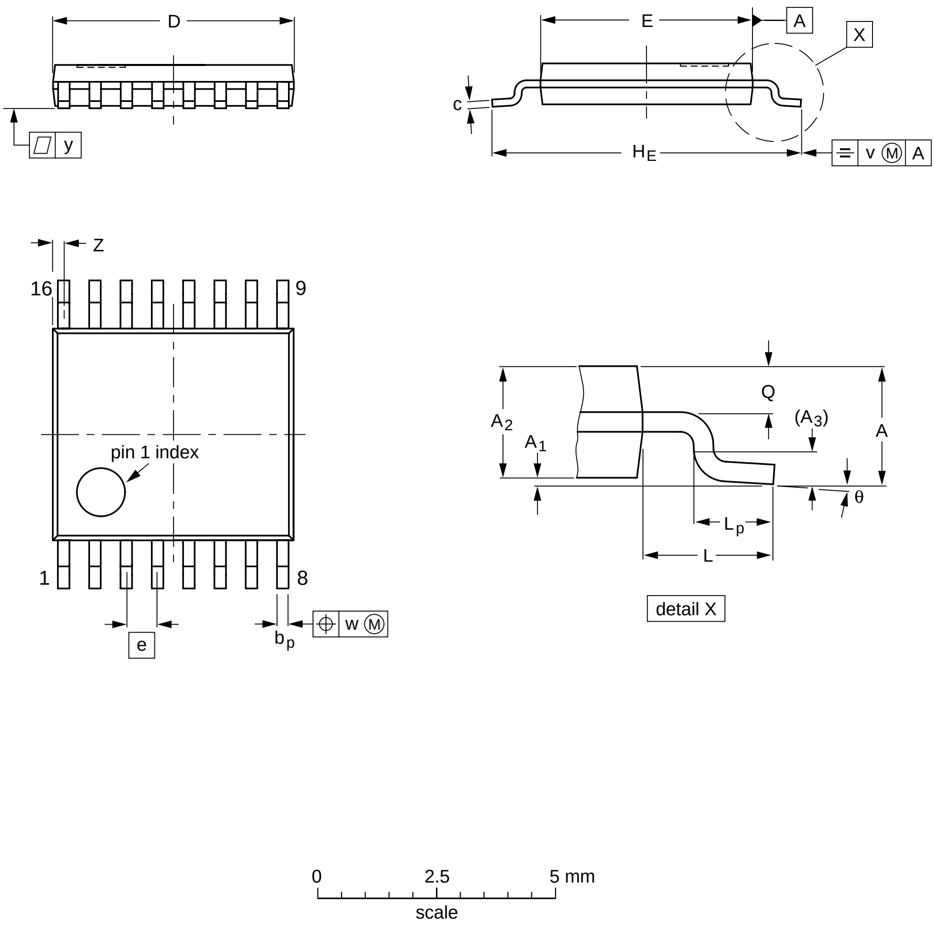
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 25. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

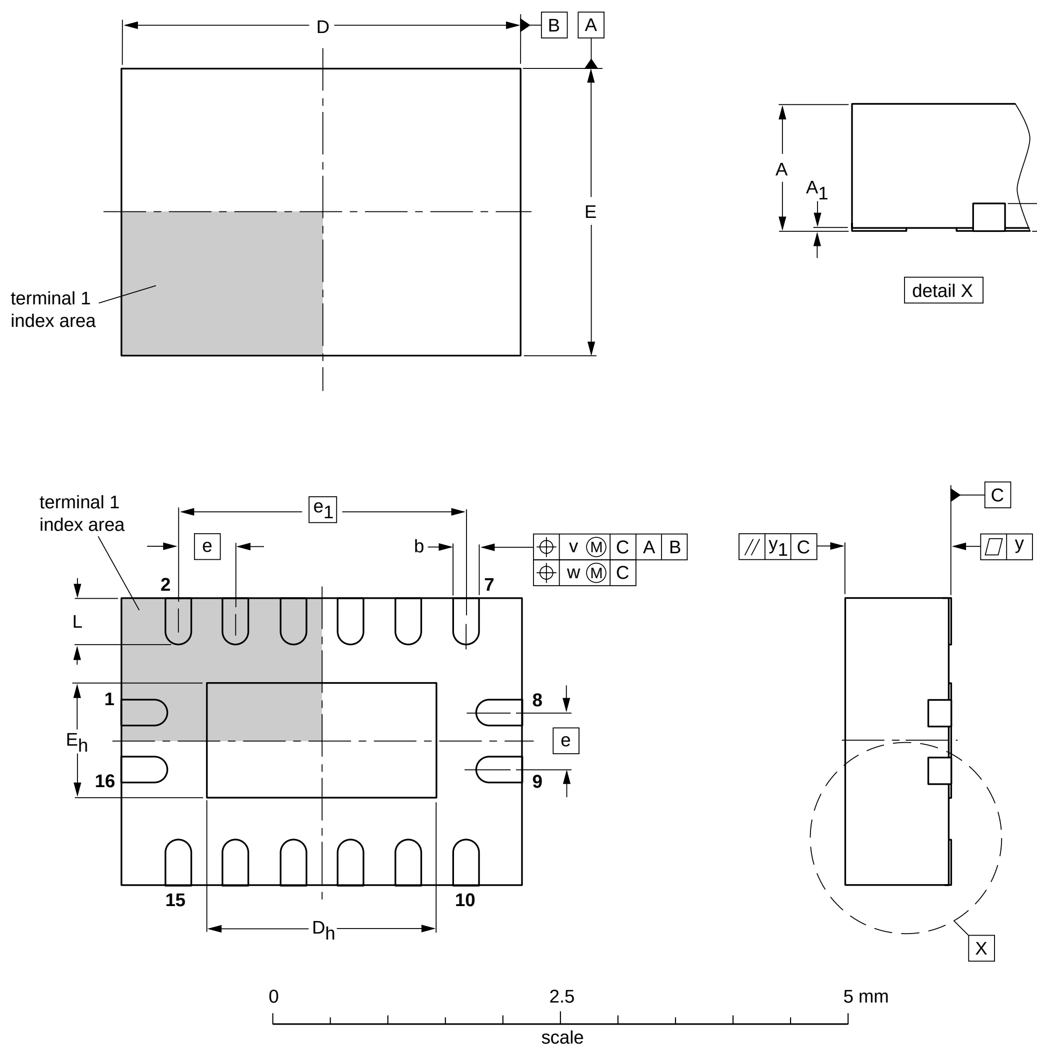
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 26. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 27. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4053_4	20090810	Product data sheet	-	74LV4053_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added type number 74LV4053BQ (DHVQFN16 package) • R_{ON} values changed in Section 2. • Package version SOT38-1 changed to SOT38-4 in Section 3, and Figure 23.			
74LV4053_3	19980623	Product specification	-	74LV4053_2
74LV4053_2	19970715	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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