Revision History :

Revision 1.0 (Jul. 4, 2007)
- Original

PSRAM

16-Mbit (1M x 16)

Pseudo Static RAM

Features

- Wide voltage range: 2.2V–3.6V
- Access Time: 70 ns
- Ultra-low active power
- — Typical active current: 3 mA @ f = 1 MHz
- — Typical active current: 18 mA @ f = fmax
- Ultra low standby power
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Offered in a 48-ball BGA Package
- Operating Temperature: –40°C to +85°C
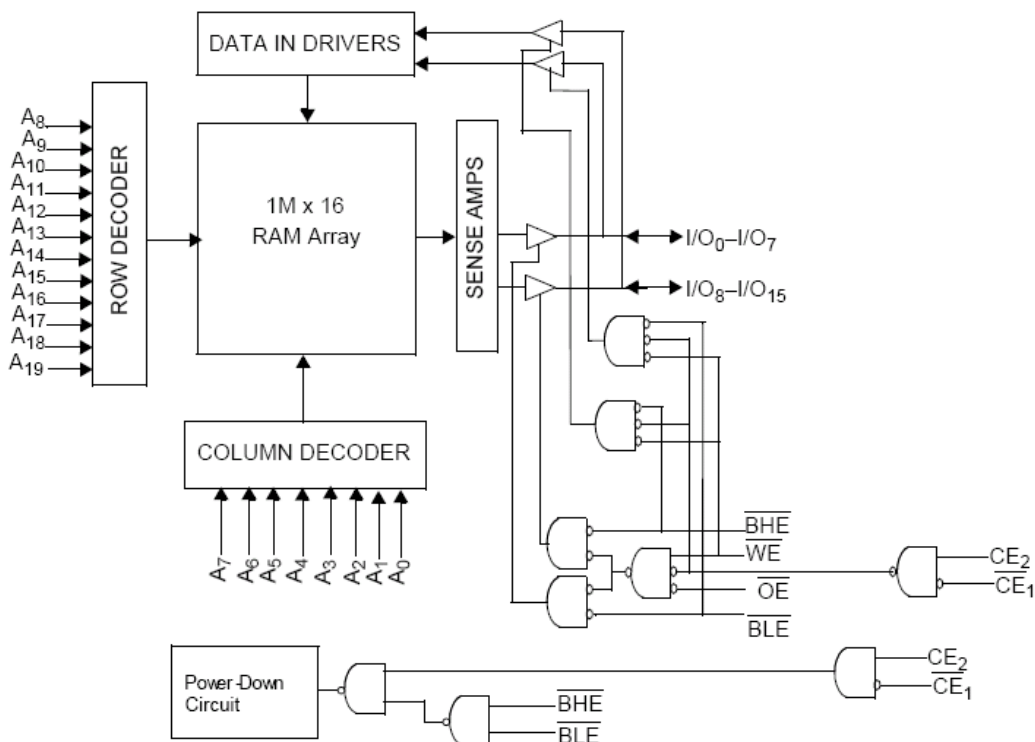
Functional Description[1]

The M24L16161DA is a high-performance CMOS Pseudo Static RAM organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{CE1}$ HIGH or CE2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE1}$ HIGH or CE2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE1}$ LOW and CE2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE1}$ LOW and CE2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A$_0$ through A$_{19}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A0 through A19).

To read from the device, take Chip Enables ($\overline{CE1}$ LOW and CE2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. Refer to the truth table for a complete description of read and write modes.
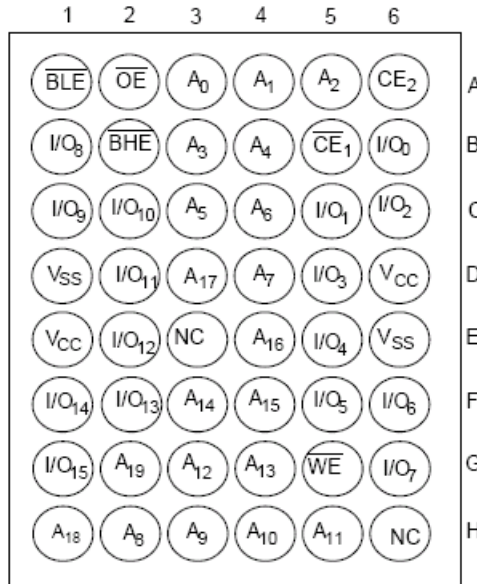
Logic Block Diagram

Pin Configuration[2, 3]

48-ball VFBGA

Top View

	1	2	3	4	5	6	
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2	A
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE_1}$	I/O_0	B
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2	C
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}	D
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}	E
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6	F
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7	G
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC	H

Product Portfolio[4]

Product	V_{CC} Range (V)			Speed(ns)	Power Dissipation					
					Operating I_{CC}(mA)				Standby I_{SB2}(µA)	
					f = 1MHz		f = fmax			
	Min.	Typ.[4]	Max		Typ.[4]	Max.	Typ.[4]	Max	Typ. [4]	Max
M24L16161DA	2.2	3.0	3.6	70	3	5	18	25	55	70

Power-up Characteristics

The initialization sequence is shown in the figure below. Chip Select should be $\overline{OE}$1 HIGH or CE2 LOW for at least 200 µs after V_{CC} has reached a stable value. No access must be attempted during this period of 200 µs.
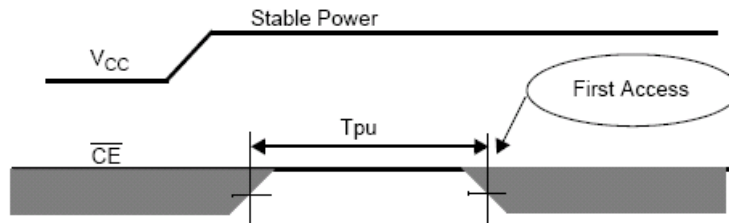
Parameter	Description	Min.	Typ.	Max.	Unit
T_{PU}	Chip Enable Low After Stable V_{CC}	200			µs

Notes:
2. Ball H6 and E3 can be used to upgrade to a 32-Mbit and a 64-Mbit density, respectively.
3. NC "no connect"-not connected internally to the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC\,(typ)}$ and T_A = 25°C. Tested initially and after design changes that may affect the parameters.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage to Ground Potential.–0.3V to V_{CCMAX} + 0.3V

DC Voltage Applied to Outputs
in High Z State[5, 6, 7].......................–0.3V to V_{CCMAX} + 0.3V

DC Input Voltage[5, 6, 7]...................–0.3V to V_{CCMAX} + 0.3V

Output Current into Outputs (LOW)............................20 mA

Static Discharge Voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current...> 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	−40°C to +85°C	2.2V to 3.6V

DC Electrical Characteristics (Over the Operating Range) [5, 6, 7]

Parameter	Description	Test Conditions		-70			Unit
				Min.	Typ.[4]	Max.	
V_{CC}	Supply Voltage			2.2	3.0	3.6	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1$ mA $V_{CC} = 2.2V$ to 3.6V		V_{CC}-0.2			V
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1$ mA, $V_{CC} = 2.2V$ to 3.6				0.2	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 1.7V$ to 1.95V		0.8* V_{CC}		V_{CC}+0.3V	V
V_{IL}	Input LOW Voltage	2.2V to 3.6		-0.3		0.2* V_{CC}	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		-1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}		-1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC}= V_{CCmax}$ $I_{OUT} = 0$mA CMOS levels		18	25	mA
		$f = 1$ MHz			3	5	mA
I_{SB1}	Automatic CE Power-Down Current —CMOS Inputs	$\overline{CE1} ≥ V_{CC} - 0.2V$, $CE2 ≤ 0.2V$, $V_{IN} > V_{CC} - 0.2V$, $V_{IN} < 0.2V$, $f = f_{MAX}$ (Address and Data Only), $f = 0$ ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), $V_{CC}=3.60V$			55	70	µA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	$\overline{CE1} ≥ V_{CC}-0.2V$, $CE2 ≤ 0.2V$, $V_{IN} ≥ V_{CC} - 0.2V$ or $V_{IN} ≤ 0.2V$, $f = 0$, $V_{CC} = V_{CCMAX}$,			55	70	µA

Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz,	8	pF
C_{OUT}	Output Capacitance	$V_{CC} = V_{CC(typ)}$	8	pF

Thermal Resistance[8]

Parameter	Description	Test Conditions	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedence, per EIA/JESD51.	56	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		11	°C/W

Notes:

5. $V_{IL(MIN)}$ = –0.5V for pulse durations less than 20 ns.

6. $V_{IH(Max)}$ = V_{CC} + 0.5V for pulse durations less than 20 ns.

7. Overshoot and undershoot specifications are characterized and are not 100% tested.

8. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms
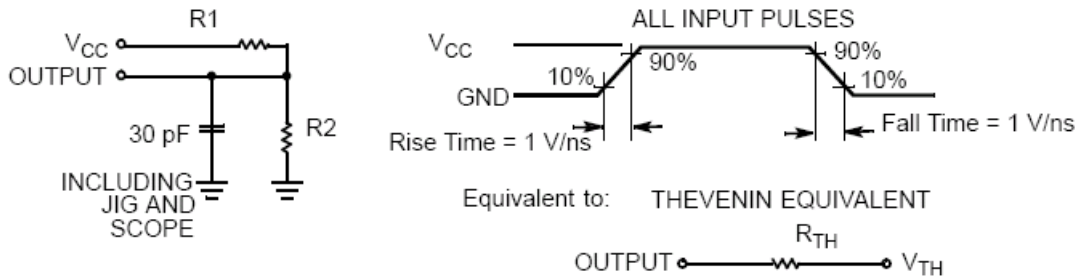
Parameters	3.0V V_{CC}	Unit
R1	26000	Ω
R2	26000	Ω
R_{TH}	13000	Ω
V_{TH}	1.50	V

Switching Characteristics Over the Operating Range[9, 10, 11, 14, 15]

Parameter	Description	-70		Unit
		Min.	Max.	
Read Cycle				
t_{RC}[13]	Read Cycle Time	70	40000	ns
t_{CD}	Chip Deselect Time $\overline{CE1}$ =HIGH or CE2=LOW, $\overline{BLE}$ / $\overline{BHE}$ High Pulse Time	15		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[10, 11, 12]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10, 11, 12]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[10, 11, 12]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[10, 11, 12]		25	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		70	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[10, 11, 12]	5		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z[10, 11, 12]		25	ns

Notes:
9. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ.)}$/2, input pulse levels of 0V to V_{CC}, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
10. At any given temperature and voltage conditions t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device. All low-Z parameters will be measured with a load capacitance of 30 pF (3V).
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
12. High-Z and Low-Z parameters are characterized and are not 100% tested.
13 .If invalid address signals shorter than min. t_{RC} are continuously repeated for 40 µs, the device needs a normal read timing (t_{RC}) or needs to enter standby state at least once in every 40 µs.
14. In order to achieve 70-ns performance, the read access must be Chip Enable ($\overline{CE1}$ or CE2) controlled. That is, the addresses must be stable prior to Chip Enable going active.

Switching Characteristics Over the Operating Range[9, 10, 11, 15, 14]   (continued)

Parameter	Description	-70		Unit
		Min.	Max.	
Write Cycle[15]				
t_{WC}	Write Cycle Time	70	40000	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{CD}	Chip Deselect Time $\overline{CE1}$= HIGH or CE2 = LOW, $\overline{BLE}$ / $\overline{BHE}$ High Pulse Time	15		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	60		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[10, 11, 12]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[10, 11, 12]	10		ns

Note:

15. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE1}$ = V_{IL} or CE2 = V_{IH}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Wave forms
Read Cycle 1 (Address Transition Controlled)[17, 18]
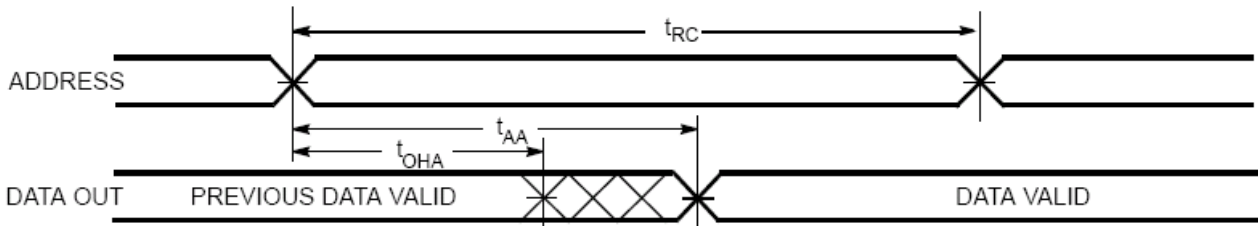
Read Cycle 2 ($\overline{OE}$ Controlled)[16, 18,19]
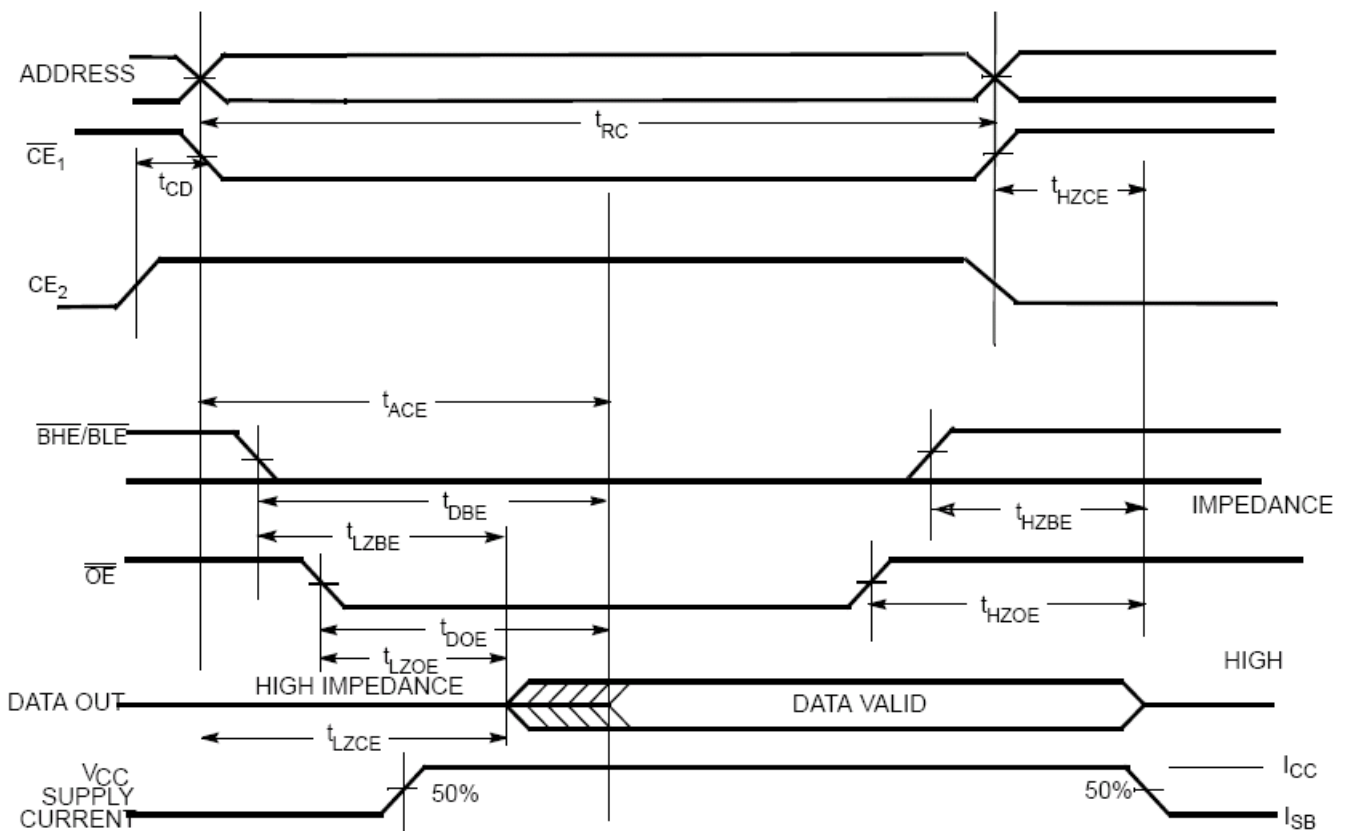
Notes:

16. Whenever $\overline{CE1}$ = HIGH or CE2 = LOW, $\overline{BHE}$ / $\overline{BLE}$ are taken inactive, they must remain inactive for a minimum of 5 ns.

17. Device is continuously selected. $\overline{OE}$ = $\overline{CE1}$ = V_{IL} and CE2 = V_{IH}.

18. $\overline{WE}$ is HIGH for Read Cycle.

19. $\overline{CE}$ is the Logical AND of $\overline{CE1}$ and CE2.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{\text{WE}}$ Controlled)[15, 12, 16, 19, 20, 21]
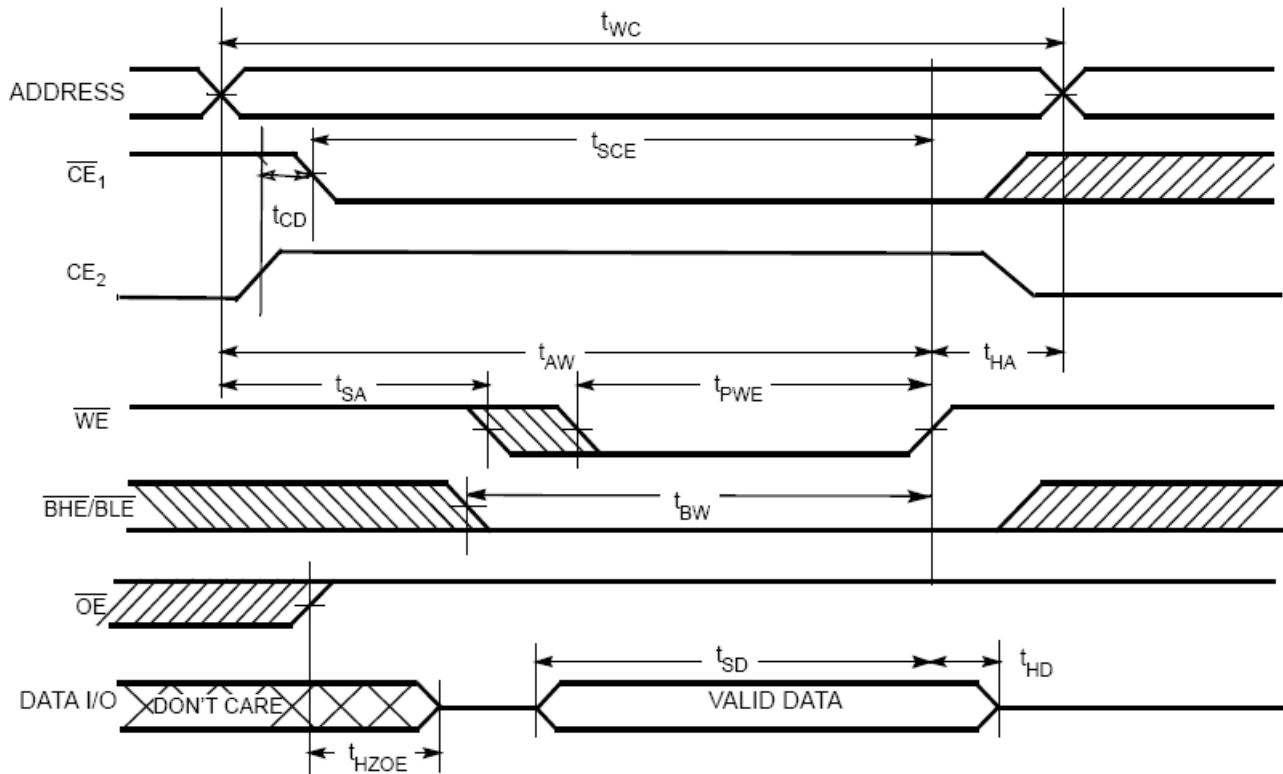
Notes:

20. Data I/O is high-impedance if $\overline{\text{OE}} \geq V_{IH}$.

21. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle 2 ($\overline{CE}$ 1 or CE2 Controlled)[15, 12, 16, 20, 21]
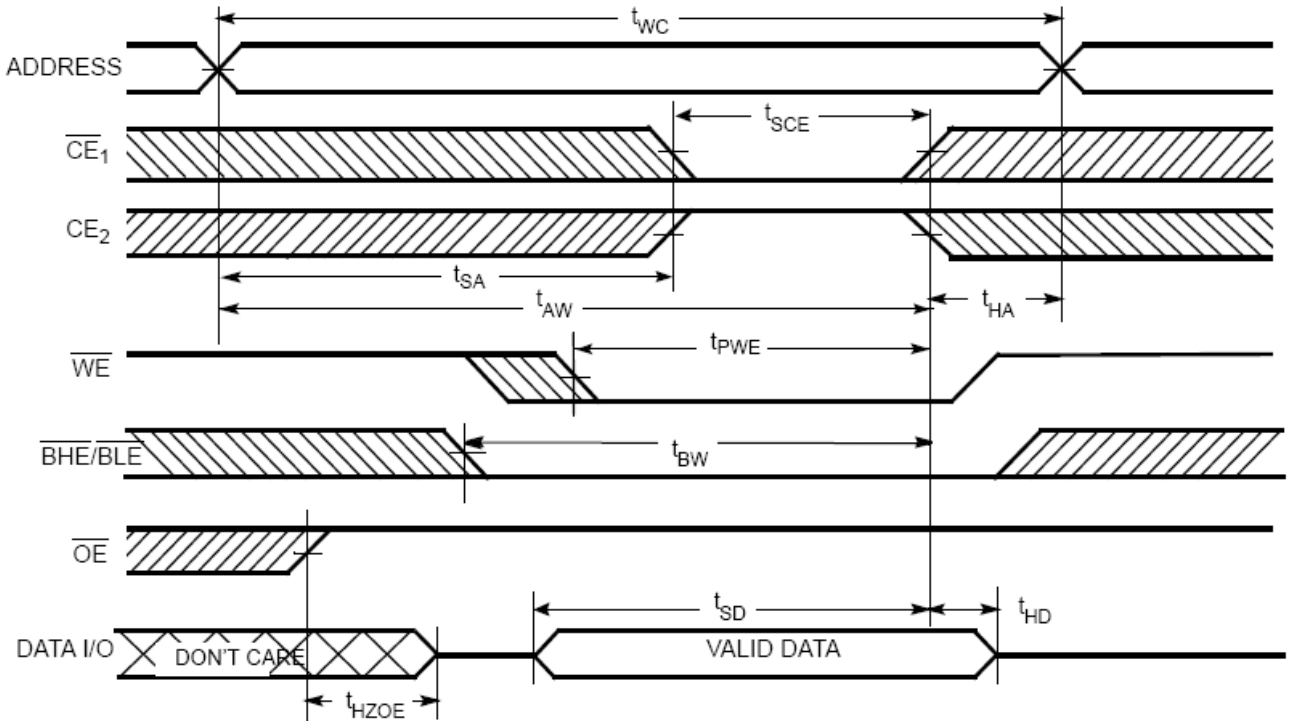
Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16, 21]
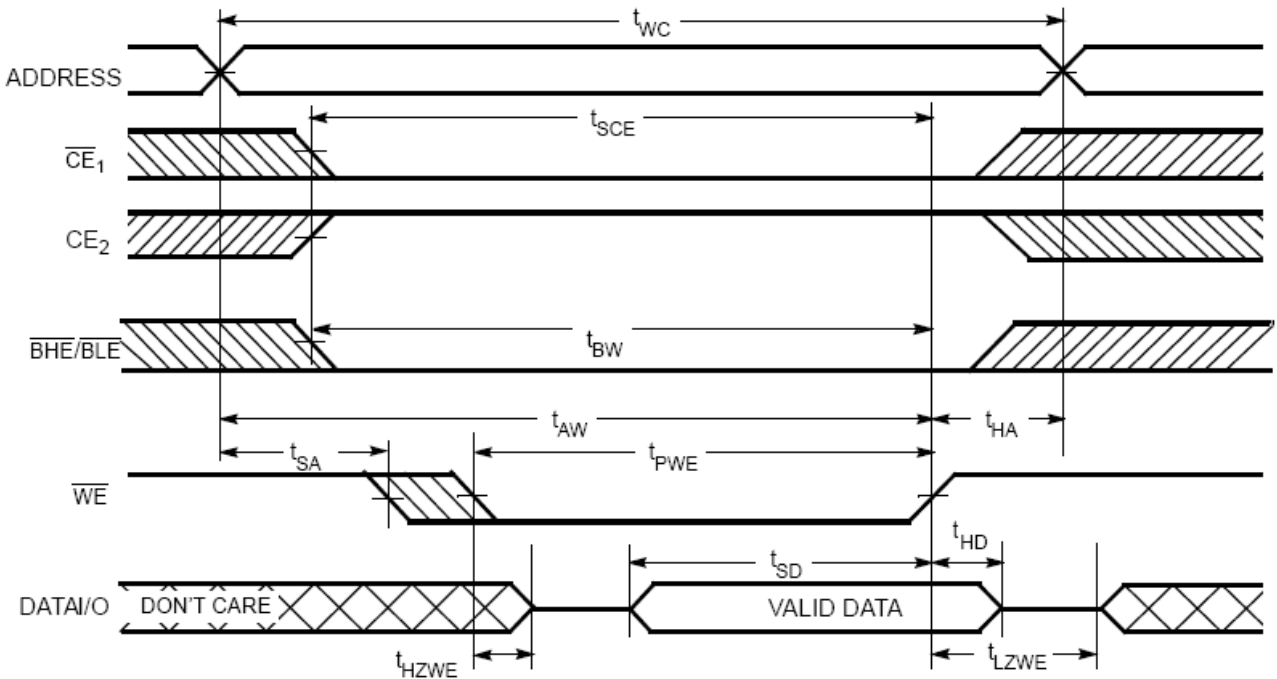
Switching Waveforms (continued)
Write Cycle 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[15, 16, 20, 21]
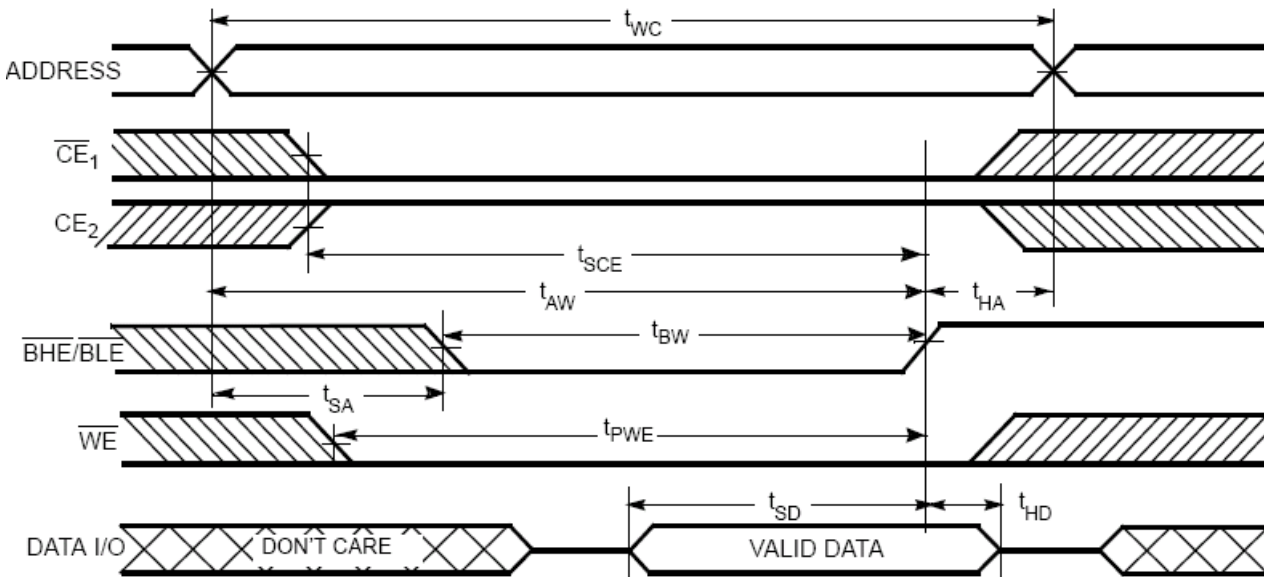
Truth Table[22]

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O$_0$–I/O$_{15}$)	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O$_0$–I/O$_7$); (I/O$_8$–I/O$_{15}$) in High Z	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O$_8$–I/O$_{15}$); (I/O$_0$–I/O$_7$) in High Z	Read	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O$_0$–I/O$_{15}$)	Write (Upper Byte and Lower Byte)	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O$_0$–I/O$_7$); (I/O$_8$–I/O$_{15}$) in High Z	Write (Lower Byte Only)	Active (I_{CC})
L	H	L	X	L	H	Data Out (I/O$_8$–I/O$_{15}$); (I/O$_0$–I/O$_7$) in High Z	Write (Upper Byte Only)	Active (I_{CC})

Notes:
22.H = Logic HIGH, L = Logic LOW, X = Don't Care.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
70	M24L16161DA -70BIG	48-ball Very Fine Pitch BGA (6 x 8 x 1 mm) (Pb-Free)	Industrial

Package Diagrams

48-ball VFBGA (6 x 8 x 1 mm)

Important Notice