



Chunghwa Picture Tubes, Ltd.

Product Specification

To :
Date : 070914

TFT LCD

CLAA070JA05CW

ACCEPTED BY : (V0.3)

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1. OVERVIEW

CLAA070JA05CW is 17.67cm(7") color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs and backlight.

The 17.67cm(7") screen produces 480(*3)X234 WQVGA resolution image. By applying R.G.B. input signal, full color images are displayed. Inverter for backlight is not included in this module.

General specifications are summarized in the following table:

ITEM	ECIFICATION
Display Area (mm)	154.08 (H) × 86.58 (V)
Number of Pixels	480(H) × 3(RGB)× 234(V)
Pixel Pitch (mm)	0.321(H)×0.37(V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	Normally white, TN
Number of color	Full color
Viewing Direction	6 o'clock
Brightness(cd/m ²)	350 (I _L =6.0 mA)
Power Consumption(W)	3.6 (Typ.)
Outline Dimension(mm)	164.9(W) × 100.0(H) × 5.7(D)
module weight(g)	160(Max.)
BL unit	CCFL (*1 tube)
Surface Treatment	Anti-Glare

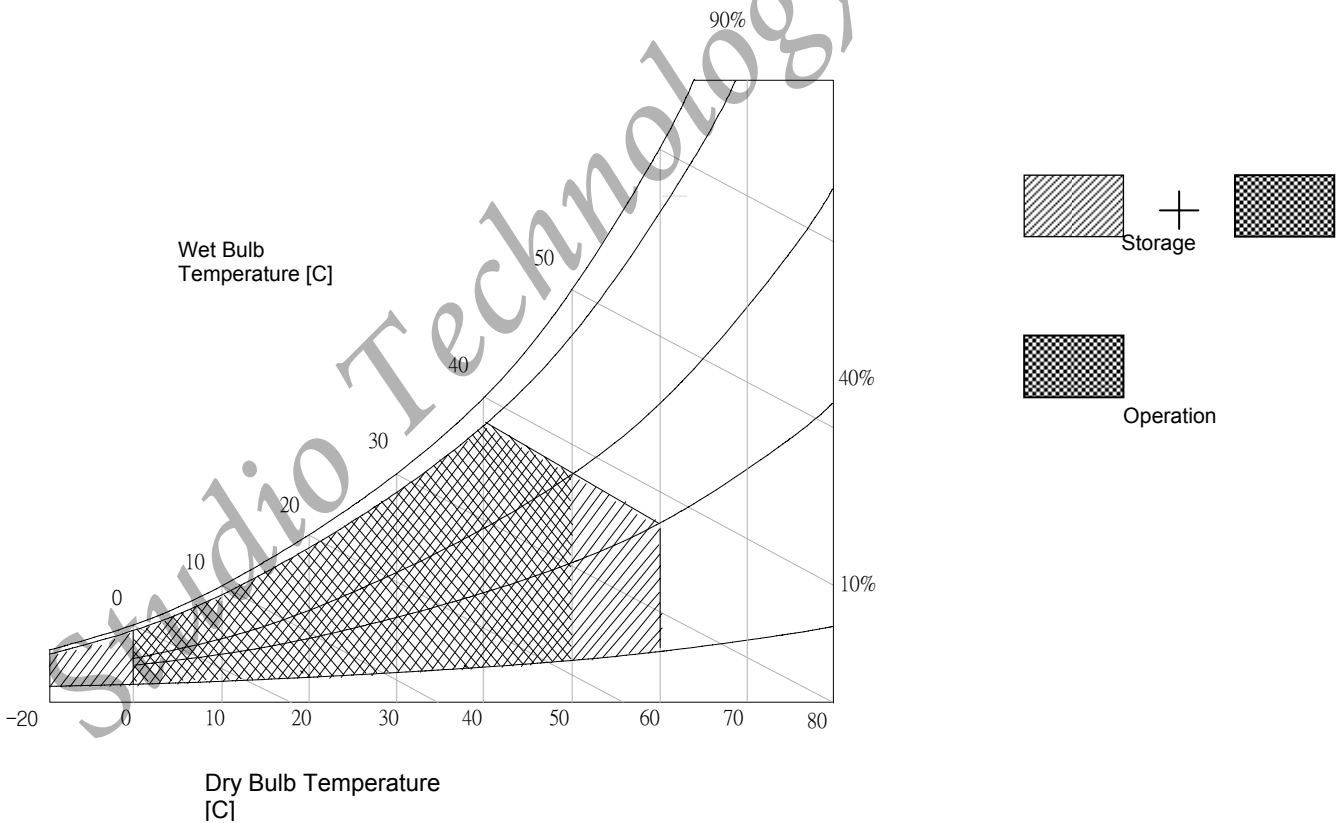
2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	conditions	MIN.	MAX.	UNIT	Note
Power Supply Voltage for LCD	VCC	GND=0	-0.3	6	V	
	AVDD	AVSS=0	-0.3	7	V	
	VGH	GND=0	-0.3	40	V	
	VGL		-20	0.3	V	
Signal input voltage	Vi		-0.2	AVDD+0.2	V	Note1
	VI		-0.3	VCC+0.3	V	Note2

Note1 : Analog input voltage VR, VG, VB

Note2 : Logical signal STHL, STHR, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D.

Note3 : If the relative temperature and humidity out of range too long, it will affect visual quality of LCD.



3. ELECTRICAL CHARACTERISTICS

3.1 Typical operation conditions

GND = Avss = 0V (Ta=25°C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Note
Power Supply Voltage	V _{CC}	4.5	5	5.5	V	
	AV _{DD}	4.5	5	5.5	V	
	V _{GH}	17	18	19	V	
	V _{GL}	-7	-6	-5	V	
Signal Amplitude (VR, VG, VB)	V _{iA}	0.4	-	AV _{DD} -0.4	V	Note1
	V _{iAC}	-	4	-	V	Note1
	V _{iDC}	-	AV _{DD} /2	-	V	Note1
VCOM	V _{CAC}	4	4.88	6	V _{P-P}	Note1,2
	V _{CDC}	1.85	1.95	2.05	V	Note1,3
Input Signal Voltage	V _{IH}	0.7V _{CC}	-	V _{CC}	V	Note4
	V _{IL}	0	-	0.3V _{CC}	V	

Note1 : Please refer to Fig.1

Note2 : Brightness level is adjusted by varying this amplitude V_{CAC}

Note3 : Please adjust V_{CDC} to make the flicker level be minimum.

Note4 : Logical signal STHL,STHR,OEHL,L/R,CPH1~CPH3,STVR,STVL,OEVC,CKV,U/D.

Note5 : Power sequence refer to Fig.2

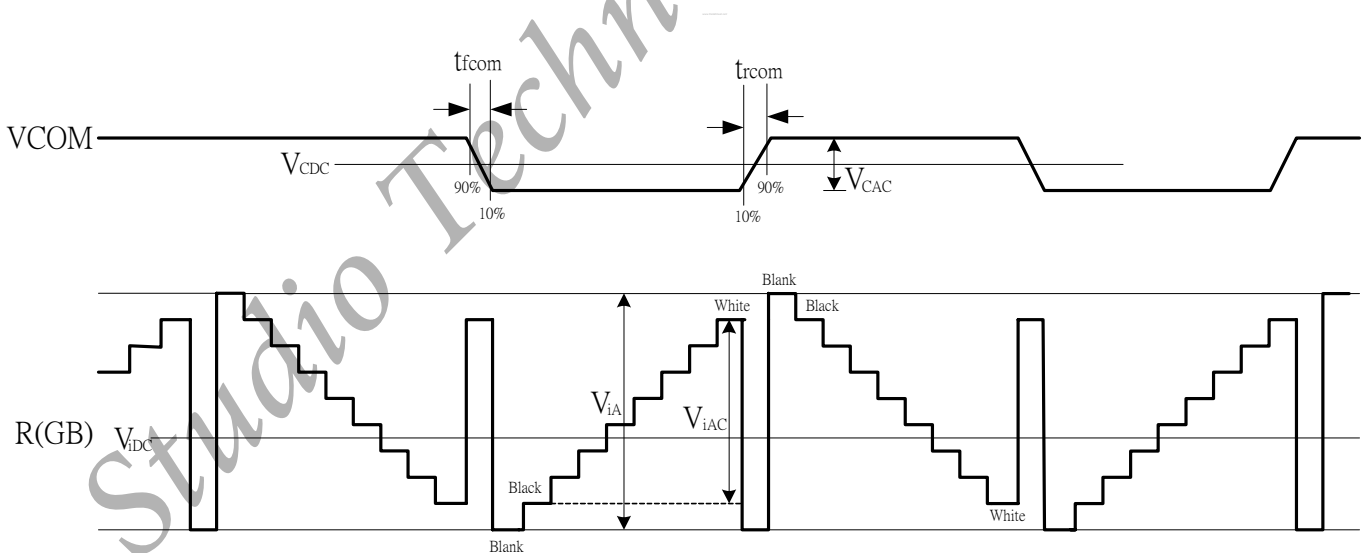
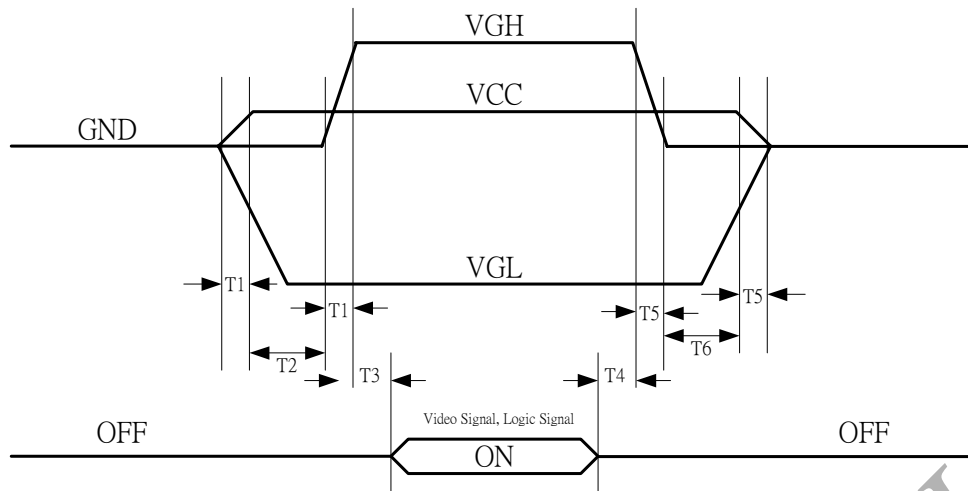


Fig.1 VCOM-RGB



- T1 ≤ 15ms (From 10%*VCC to 90%*VCC , when VCC is Low to High) ;
- T2 ≤ 10ms (From 90%*VCC to 10%*VGH , when VCC is Low to High) ;
- T3 ≤ 10ms (From 90%*VGH to Video Signal , when VGH is Low to High) ;
- T4 ≤ 10ms (From Video signal to 90%*VGH , when VGH is High to Low) ;
- T5 ≤ 20ms (From 90%*VCC to 10%*VCC , when VCC is High to Low) ;
- T6 ≤ 10ms (From 10%*VGH to 90%*VCC , when VCC is Low to High) ;

Fig.2 Power Sequence

3.2 Current consumption

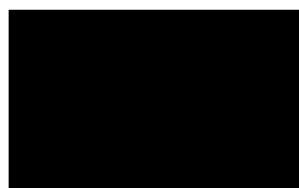
(GND = Avss = 0V)

ITEM	SYMBOL	conditions	MIN.	TYP.	MAX.	UNIT	Note
Drive Current	I _{GH}	V _{GH} = 18V	-	60	65	μA	Note1
	I _{GL}	V _{GL} = -6V	-	62	67	μA	Note1
	I _{CC}	V _{CC} = 5V	-	11	22	μA	Note1
	I _{DD}	AV _{DD} = 5V	-	8.3	21.6	mA	Note1

Note1 : Typ. specification : Gray-level test Pattern
 Max. specification : Black test Pattern



(a) Gray-level Pattern



(b) Black Pattern

3.3 Backlight system

(Ta=25°C)

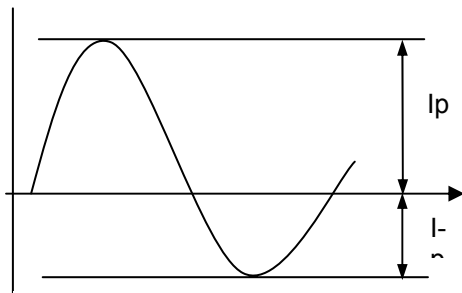
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Note
Lamp Voltage (I _L =6mA)	V _L	-	610	671	Vrms	
Lamp Current	I _L	-	6.0	8.0	mA	
Inverter Frequency	F _L	40	-	80	kHz	*1)
Lamp life time *1)	Life L	30000	-	-	hr	*2)
Starting Lamp Voltage	Ta=0°C	-	-	1130	V	*3)
	Ta=25°C	-	-	845		

- *1) The time that module luminance reduced to 50% of initial value, Base on $T_a=25^\circ\text{C}$, $I_L=6\text{mA}$ continuous.
- *2) "Life time" is defined as the lamp brightness decrease to 50% original brightness at $I_L=6.0\text{mA}$, continuous lighting, $T_a=25^\circ\text{C}$.
- *3) For starting the backlight unit, the output voltage of DC/AC's transformer should be larger than the maximum lamp starting voltage.
- *4) If the driving waveform of Lamp is asymmetric, the distribution of mercury inside the lamp tube will become unequally or will deplete the Ar gas in it. Then it may cause the abnormal phenomenon of lighting-up. Therefore, designers have to try their best to fill the conditions under the inverter designing-stage

as

below :

- The degrees of unbalance : $< 10\%$
- The ratio of wave height : $< \sqrt{2} \pm 10\%$



I_p : high side peak

$I-p$: low side peak

A : The degrees of unbalance = $| I_p - I-p | / I_{rms} \times 100 (\%)$

B : The ratio of wave height = I_p (or $I-p$) / I_{rms}

- *5) Frequency in this range can make the characteristics of electric and optics maintain in $\pm 10\%$ except hue. Lamp frequency of inverter may produce interference with horizontal synchronous frequency, and this may cause horizontal beat on the display. Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

3.4 Timing characteristics of input signals

characteristics	SYMBOL	MIN.	TYP.	MAX.	UNIT	Note
1 Field scanning period	T_{IV}	-	262.5	-	H	
1 Line scanning period	T_{IH}	-	63.5	-	μs	
Source driver operating frequency	F_{OP}	-	9.6	-	MHz	
CLK pulse width	T_{CW}	50	103.8	2000	ns	
CLK pulse period duty	T_{CWH}	40	-	60	%	
CLK pulse delay	TC12 TC23 TC31	12	69	$1/2 * T_{CW}$	ns	CPH1~CPH3
STH start pulse width	T_{STH}	32	114.2	-	ns	STHR,STHL
STH start pulse setup time	T_{SUH}	16	76.8	-	ns	STHR,STHL
STH start pulse hold time	T_{HDH}	16	37.6	-	ns	STHR,STHL
OEH output enable pulse width	T_{OEH}	$1T_{CW}$	2.7	-	μs	OEH
Sample and hold disable time OEH& STH	$T_{OEH-STH}$	1	8.9	-	μs	OEH-STH
CLKV pulse width	T_{CKVW}	1	63.5	-	μs	CKV
CLKV pulse high period	T_{CKVH}	0.5	2.64	-	μs	CKV
CLKV pulse low period	T_{CKVL}	0.5	60.9	-	μs	CKV
STV start pulse width	T_{STV}	0.5	63.5	-	μs	STVR, STVL
STV start pulse setup time	T_{SUV}	0.2	60.8	-	μs	STVR, STVL
STV start pulse hold time	T_{HDV}	0.3	2.72	-	μs	STVR,STVL

OEV pulse width	t_{OEV}	1	5.3	-	μs	OEV
Clean enable time	t_{DIS2}	-	2.54	-	μs	OEV-CKV

Note1 : 1. High level of source driver and gate driver logic signal are 70%
 2. Low level of source driver and gate driver logic signal are 30%

Note2 : Please refer to Fig.3 and Fig.4

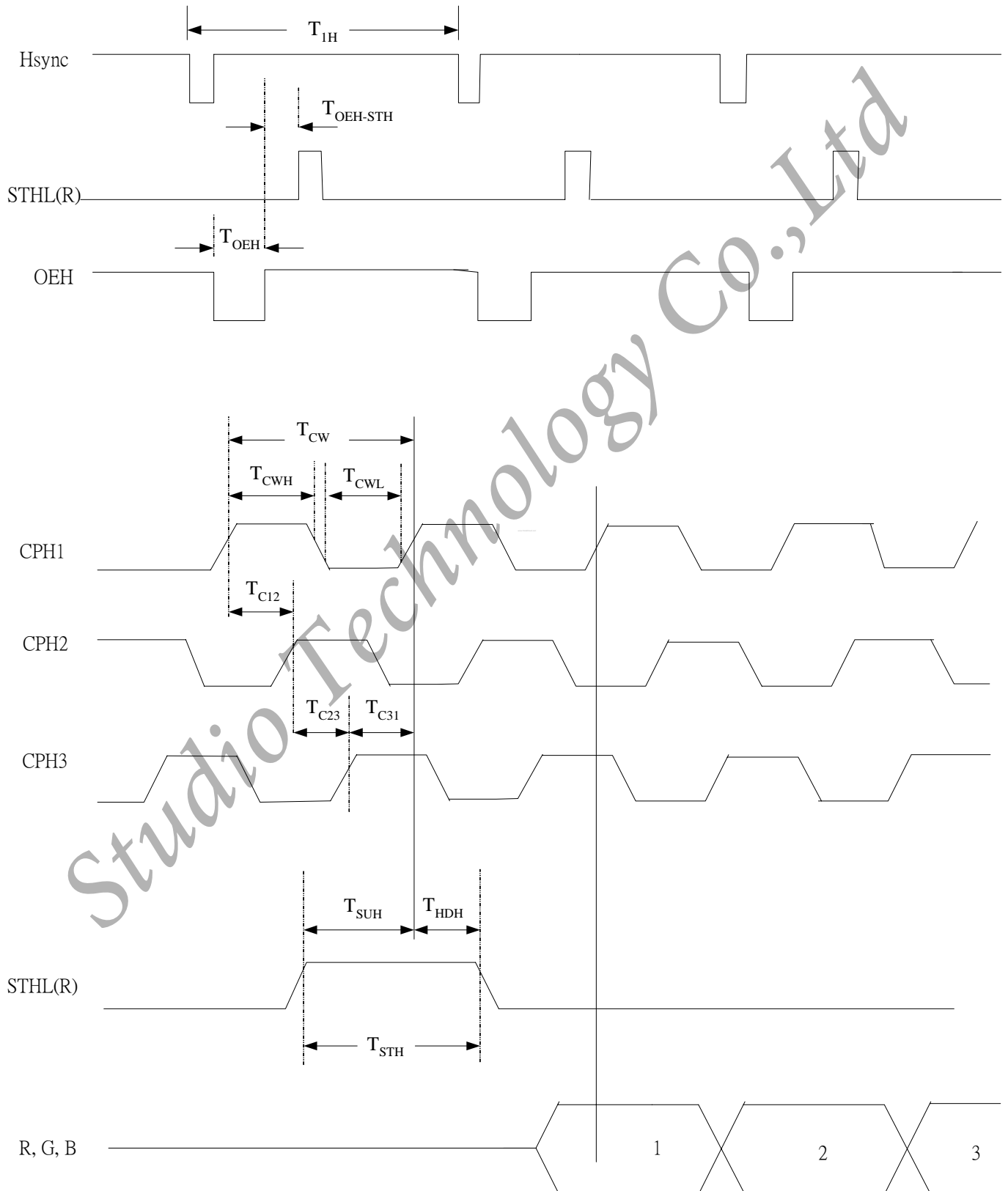


Fig.3 Horizontal Timing

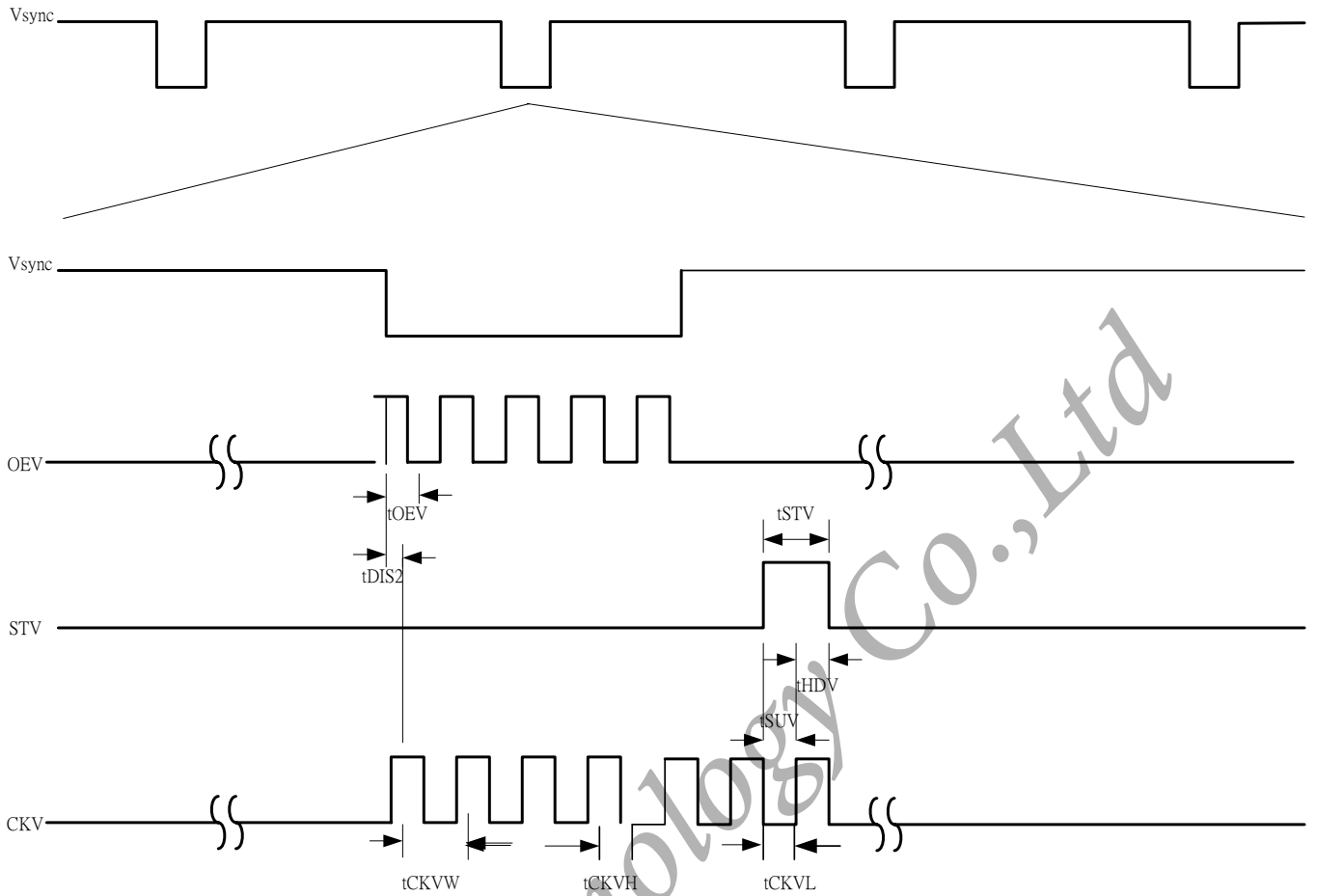


Fig.4 Vertical Timing sequence

4. INTERFACE CONNECTION:

4.1 CN1(Signal of interface)

Pin No.	SYMBOL	I/O	FUNCTION	NOTE
1	GND	-	Ground for logic circuit	
2	V _{CC}		Supply voltage of logic control circuit for scan driver	
3	V _{GL}		Negative power for scan driver	
4	V _{GH}		Positive power for scan driver	
5	STVR	I/O	Vertical start pulse	Note 1
6	STVL	I/O	Vertical start pulse	Note 1
7	CKV		Shift clock input for scan driver	
8	U/D		UP/DOWN scan control input	Note 1
9	OEV		Output enable input for driver	
10	VCOM		Common electrode driving signal	
11	VCOM		Common electrode driving signal	
12	L/R		LEFT/RIGHT scan control input	Note 1
13	MOD		Sequential sampling and simultaneous sampling setting	Note 2
14	OEH		Output enable input for data driver	
15	STHL	I/O	Start pulse for horizontal scan line	Note 1
16	STHR	I/O	Start pulse for horizontal scan line	Note 1
17	CPH3		Sampling and shifting clock pulse3 for data drive	
18	CPH2		Sampling and shifting clock pulse2for data drive	
19	CPH1		Sampling and shifting clock pulse1 for data drive	
20	V _{CC}		Supply voltage of logic control circuit for data driver	
21	GND	-	Ground for logic circuit	
22	VR		Alternated video signal input(Red)	
23	VG		Alternated video signal input(Green)	
24	VB		Alternated video signal input(Blue)	
25	AV _{DD}		Supply voltage for analog circuit	
26	AV _{SS}	-	Ground for analog circuit	

Note1 :

Setting of scan control input		IN/OUT state for start pulse				Scanning direction
U/D	L/R	STVR	STVL	STHR	STHL	
GND	V _{CC}	OUT	IN	OUT	IN	From up to down ,and from left to right
V _{CC}	GND	IN	OUT	IN	OUT	From down to up ,and from right to left
GND	GND	OUT	IN	IN	OUT	From up to down ,and from right to left
V _{CC}	V _{CC}	IN	OUT	OUT	IN	From down to up ,and from left to right

Note2 : MOD=H: Simultaneous sampling (Set CPH2 and CPH3 to LOW)

MOD=L: Sequential sampling

4.2 CN2 (backlight)

Backlight-side connector: BHSR-02VS-1 (JST made)

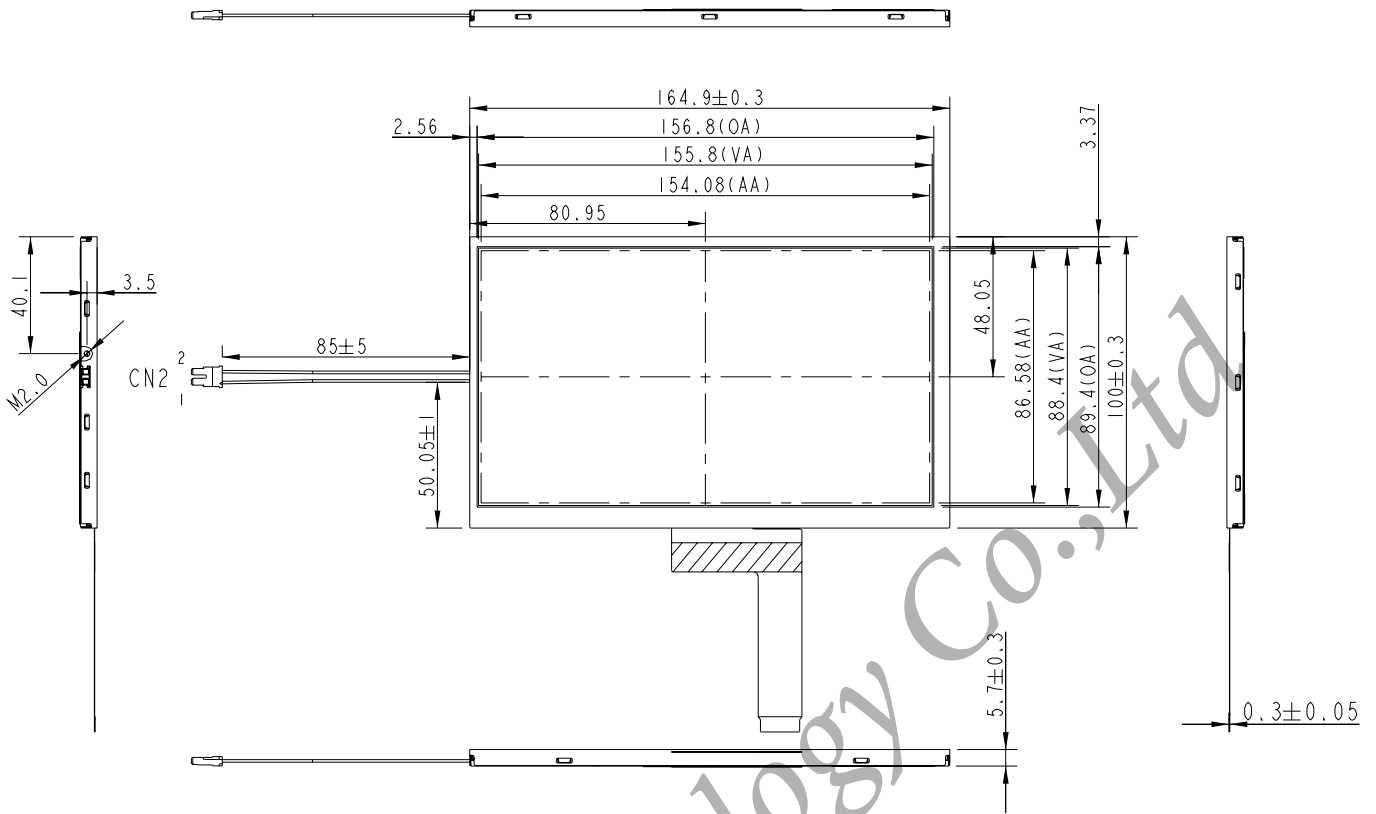
Inverter-side connector: SM02B-BHSS-1 (JST made)

Pin No.	SYMBOL	FUNCTION
1	CTH	VBLH (high Voltage)
2	CTL	VBLL (low Voltage)

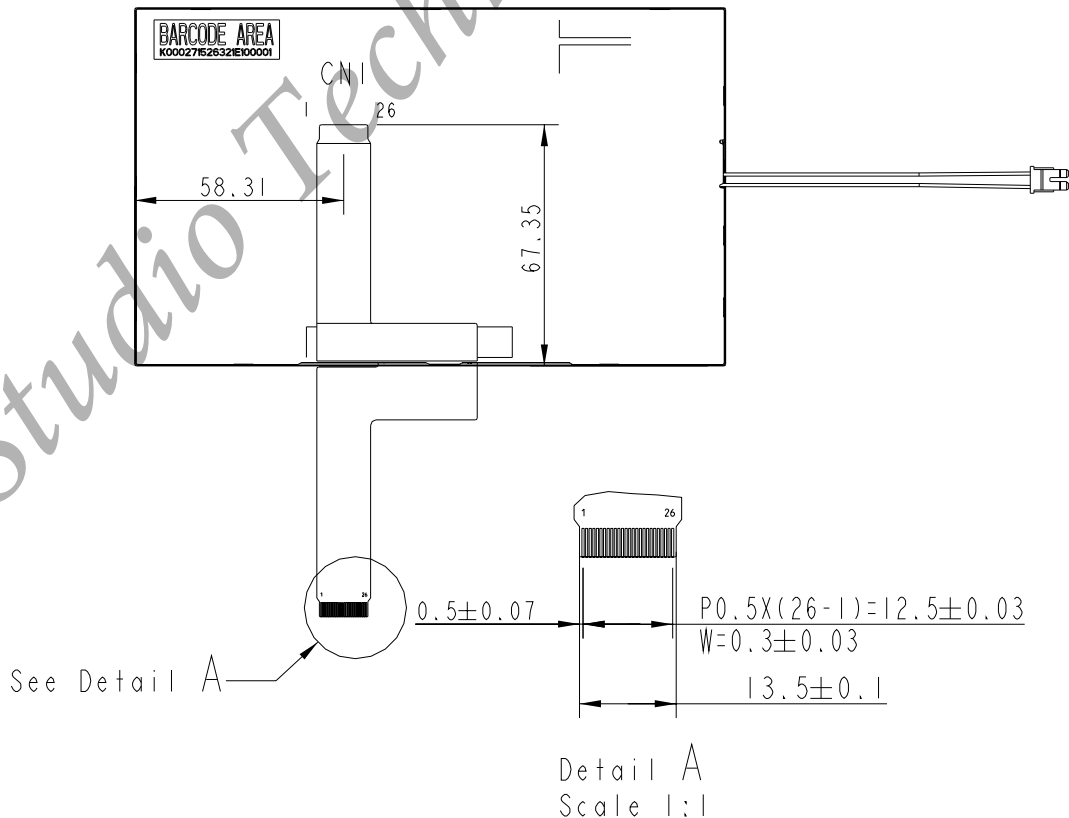
[Note] : VBLH-VBLL=VL

5. MECHANICAL DIMENSION

(1) Front Side



(2) Rear Side



[Note] : (Tolerance is ±0.5mm unless noted)

[Unit : mm]

6. OPTICAL CHARACTERISTICS

Ta=25°C ,

VCC=3.3V

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Contrast Ratio		CR	*1)	(350)	400	--	--
Luminance		L	*3) I _L = 6.0mA	280	350	--	cd/m ²
Luminance Uniformity		ΔL	*4)	80	--	--	%
Response Time		Tr	*5)	--	20	40	ms
		Tf		--			ms
Viewing Angle	Horizontal	φ ^{*2)}	CR ≥ 10	110	120	--	°
	Vertical	θ ^{*2)}		90	100	--	°
Color Coordinate	Red	x y	θ = φ = 0°	TBD	TBD	TBD	--
	Green	x y		TBD	TBD	TBD	
	Blue	x y		TBD	TBD	TBD	
	White	x y		(0.270) (0.280)	(0.300) (0.310)	(0.330) (0.340)	
	NTSC				45	50	

[Note]

- These items are measured by BM-5A (TOPCON) or CA-1000(MINOLTA) in the dark room. (no ambient light).
- Measurement Condition: I_L=6.0 mA , Inverter : HIU-766(52K) (Harison made)
Measuring point : Fig.5 Measuring point : 1~9 points
Measuring Viewing Angle : Fig.6 : θ=ψ=0°

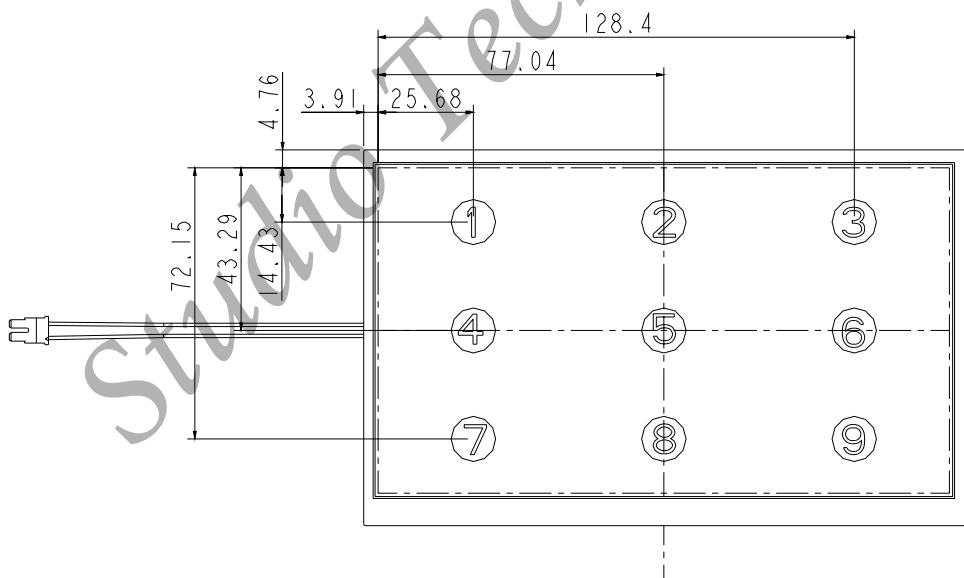


Fig.5 Measuring point

*1) Definition of contrast ratio :

Measure contrast ratio on the 5 points (refer to figure5, #1~#9 point)

Contrast ratio is calculated with the following formula :

Contrast Ratio (CR) = (White) Luminance of ON ÷ (Black) Luminance of OFF

*2) Definition of Viewing Angle(θ, ψ) :

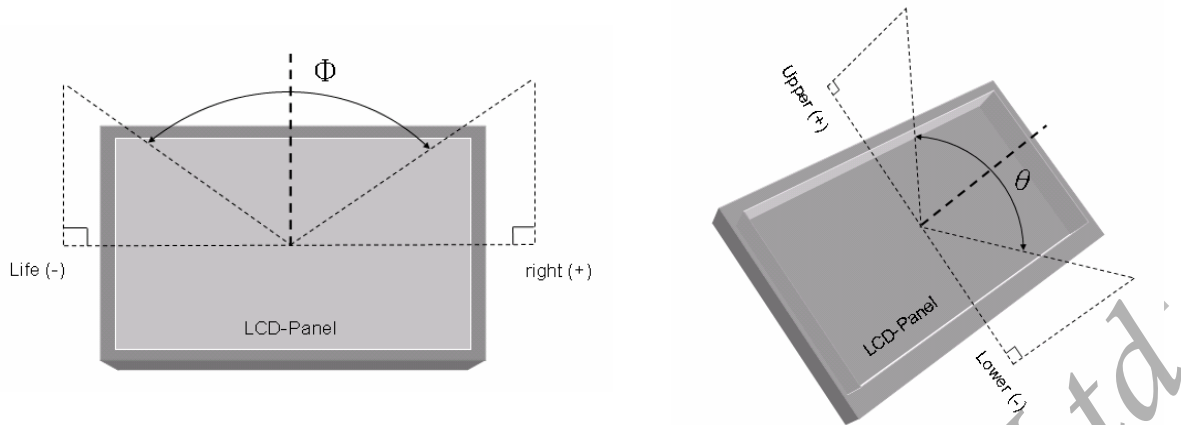


Fig.6 Definition of Viewing Angle

*3) Definition of luminance :

Measure white luminance on the 5 points as figure 5 and take the average value.

*4) Definition of Luminance Uniformity :

Measure maximum luminance(L(MAX))and minimum luminance (L(MIN))on the 5 points as figure 4.Luminance Uniformity is calculated with the following formula :

$$\Delta L = L(\text{MIN}) / L(\text{MAX}) \times 100\%$$

*5) Definition of Response Time

The response time is defined as the time interval between the 10% and 90% amplitudes.Refer to figure 7 as below.

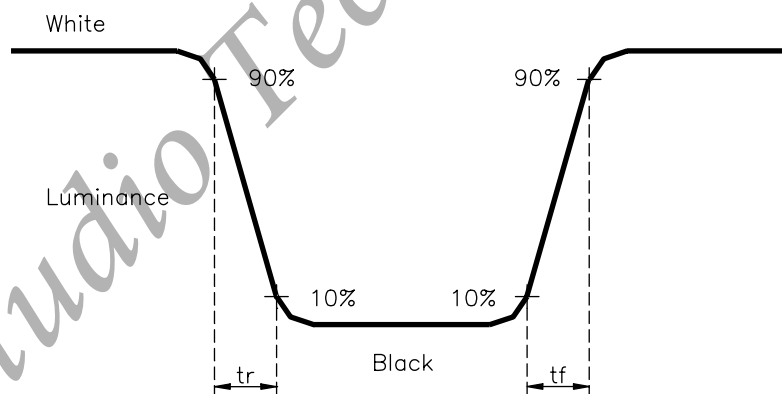


Fig.7 Definition of Response Time

7. RELIABILITY TEST CONDITIONS

(1) Temperature and Humidity

TEST ITEMS	CONDITIONS
HIGH TEMPERATURE OPERATION	85° C ; 240 Hrs
HIGH TEMPERATURE AND HIGH HUMIDITY OPERATION	60° C ; 90% RH ; 240 Hrs
HIGH TEMPERATURE STORAGE	95° C ; 240 Hrs
LOW TEMPERATURE OPERATION	-30° C ; 240Hrs (Backlight unit always turn on)
LOW TEMPERATURE STORAGE	-40° C ; 240 Hrs
THERMAL SHOCK (No operation)	-30° C (0.5Hr)~85° C (0.5Hr) 200 CYCLE

(2) Shock & Vibration

TEST ITEMS	CONDITIONS
SHOCK (NON-OPERATION)	<ul style="list-style-type: none"> ● Shock level: 980m/s²(equal to 100G). ● Waveform: half sinusoidal wave,6ms. ● Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of three shock inputs.
VIBRATION (NON-OPERATION)	<ul style="list-style-type: none"> ● Frequency range:8~33.3Hz ● Stoke : 1.3 mm ● Vibration: sinusoidal wave, perpendicular axis (both x,z axis: 2Hrs , and y axis: 4Hrs). ● Sweep: 2.9G,33.3 Hz -400 Hz ● Cycle: 15 min

(3) Judgment standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.