Datasheet

Gate Driver Providing Galvanic isolation Series

Isolation voltage 2500Vrms 1ch Gate Driver Providing Galvanic Isolation

BM60013FV-C

●General Description

The BM60013FV-C is a gate driver with isolation voltage 2500Vrms, I/O delay time of 200ns, and minimum input pulse width of 100ns, and incorporates the fault signal output functions, undervoltage lockout (UVLO) function, thermal protection function, and short current protection (SCP, DESAT) function.

●Features

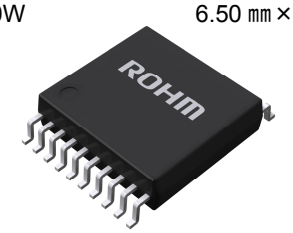
- Providing Galvanic Isolation
- Active Miller Clamping
- Fault signal output function (Adjustable output holding time)
- Undervoltage lockout function
- Thermal protection function (Adjustable threshold voltage)
- Short current protection function (Adjustable threshold voltage)
- Soft turn-off function for short current protection

●Key Specifications

- Isolation voltage: 2500 [Vrms] (Min.)
- Maximum gate drive voltage: 20 [V] (Max.)
- I/O delay time: 200 [ns] (Max.)
- Minimum input pulse width: 100 [ns] (Max.)

●Package

	W(Typ.) x D(Typ.) x H(Max.)
SSOP-B20W	6.50 ㎜ × 8.10 ㎜ × 2.01 ㎜



●Applications

- Automotive isolated IGBT/MOSFET inverter gate drive
- Automotive DC-DC converter
- Industrial inverters systems
- UPS systems

● Typical Application Circuits

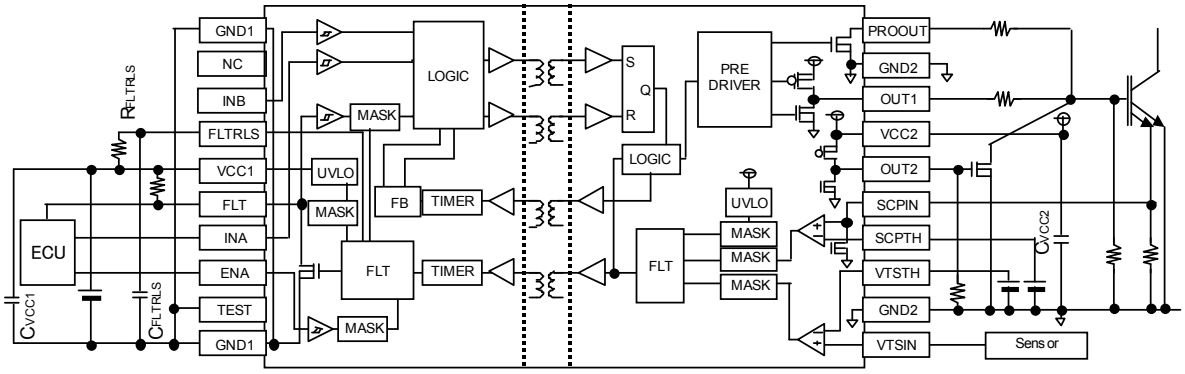


Figure 1. For using 4-pin IGBT (for using SCP function)

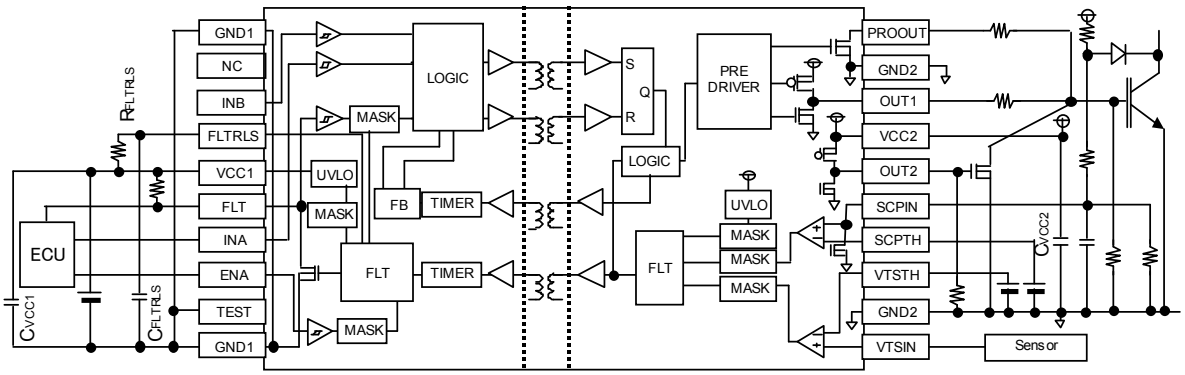


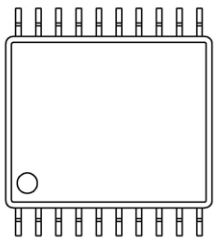
Figure 2. For using 3-pin IGBT (for using DESAT function)

●**Recommended range of external constants**

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
FLTRLS	C_{FLTRLS}	-	0.01	0.47	uF
	R_{FLTRLS}	50	200	1000	kΩ
VCC1	C_{VCC1}	0.1	1.0	-	uF
VCC2	C_{VCC2}	0.33	-	-	uF

●**Pin Configuration**

SSOP-B20W
(TOP VIEW)



1pin

Figure 3. Pin configuration

●**Pin Description**

Pin No.	Pin Name	Function
1	VTSIN	Thermal detection pin
2	GND2	Output-side ground pin
3	VTSTH	Thermal detection threshold setting pin
4	SCPTH	Short current detection threshold setting pin
5	SCPIN	Short current detection pin
6	OUT2	MOS FET control pin for Miller Clamp
7	VCC2	Output-side power supply pin
8	OUT1	Output pin
9	GND2	Output-side ground pin
10	PROOUT	Soft turn-off pin
11	GND1	Input-side ground pin
12	NC	No Connect
13	INB	Invert / non-invert selection pin
14	FLTRLS	Fault output holding time setting pin
15	VCC1	Input-side power supply pin
16	FLT	Fault output pin
17	INA	Control input pin
18	ENA	Input enabling signal input pin
19	TEST	Test mode setting pin
20	GND1	Input-side ground pin

●Description of pins and cautions on layout of board

1）VCC1 (Input-side power supply pin)
The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2）GND1 (Input-side ground pin)
The GND1 pin is a ground pin on the input side.

3）VCC2 (Output-side power supply pin)
The VCC2 pin is a power supply pin on the output side. To reduce voltage fluctuations due to OUT1, OUT2 pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VCC2 and the GND2 pins.

4）GND2 (Output-side ground pin)
The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of a power device.

5）IN (Control input terminal)
The IN pin is a pin used to determine output logic.

ENA	INB	INA	OUT1
L	X	X	L
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	L

6）FLT (Fault output pin)
The FLT pin is an open drain pin used to output a fault signal when a fault occurs (i.e., when the undervoltage lockout function (UVLO), short current protection function (SCP) or thermal protection function is activated).
This pin is I/O pin and if L voltage is externally input, the output is set to L status regardless of other input logic.
Consequently, be sure to connect the pull-up resistor between VCC1 pin and the FLT pin even if this pin is not used.

Pin	FLT
While in normal operation	Hi-Z
When an Fault occurs (When UVLO, SCP or thermal protection is activated)	L

7）FLTRLS (Fault output holding time setting pin)
The FLTRLS pin is a pin used to make setting of time to hold a fault signal. Connect a capacitor between the FLTRLS pin and the GND1 pin, and a resistor between it and the VCC1 pin.
The fault signal is held until the FLTRLS pin voltage exceeds a voltage set with the V_{FLTRLS} parameter. To set holding time to 0 ms, do not connect the capacitor. Short-circuiting the FLTRLS pin to the VCC1 pin will cause a high current to flow in the FLTRLS pin and, in an open state, may cause the IC to malfunction. To avoid such trouble, be sure to connect a resistor between the FLTRLS and the VCC1 pins.

8）OUT1 (Output pin)
The OUT1 pin is a pin used to drive the gate of a power device.

9）OUT2 (MOS FET control pin for Miller Clamp)
The OUT2 pin is a pin for controlling the external MOS switch for preventing increase in gate voltage due to the miller current of the power device connected to OUT1 pin.

10）PROOUT (Soft turn-off pin)
The PROOUT pin is a pin used to put the soft turn-off function of a power devise in operation when the SCP function is activated. This pin combines with the gate voltage monitoring pin for Miller Clamp function.

11）SCPIN (Short current detection pin), SCPTH (Short current detection threshold setting pin)
The SCPIN pin is a pin used to detect current for short current protection. When the SCPIN pin voltage exceeds a voltage set with the SCPTH pin voltage, the SCP function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the SCPIN pin to the GND2 pin and SCPTH pin to the VCC2 pin if the short current protection is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{SCPMSK} is set.

12）VTSIN(Thermal detection pin), VTSTH (Thermal detection threshold setting pin)
The VTSIN pin is a temperature sensor voltage input pin, which can be used for thermal protection of a power device. If VTSIN pin voltage becomes VTSTH pin voltage or less, OUT1 pin is set to L. In the open status, the IC may malfunction, so be sure to supply the VTSIN more than VTSTH if the thermal protection function is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{TSMSK} is set.

●**Description of functions and examples of constant setting**

1) Miller Clamp function

When OUT1=L and PROOUT pin voltage < V_{OUT2ON}, H is output from OUT2 pin and the external MOS switch is turned ON. When OUT1=H, L is output from OUT2 pin and the external MOS switch is turned OFF. While the short-circuit protection function is activated, L is output from OUT2 pin and the external MOS switch is turned OFF.

Short current	SCPIN	IN (INA EXOR INB)	PROOUT	OUT2
Detected	Not less than V_{SCPTH}	X	X	L
Not detected	X	L	Not less than V_{OUT2ON}	L
	X	L	Less than V_{OUT2ON}	H
	X	H	X	L

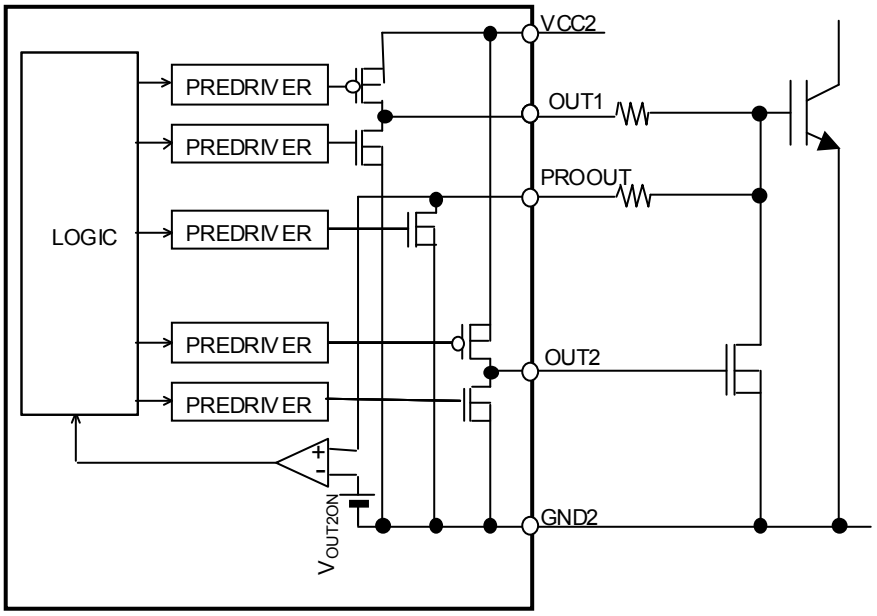


Figure 4. Block diagram of Miller Clamp function

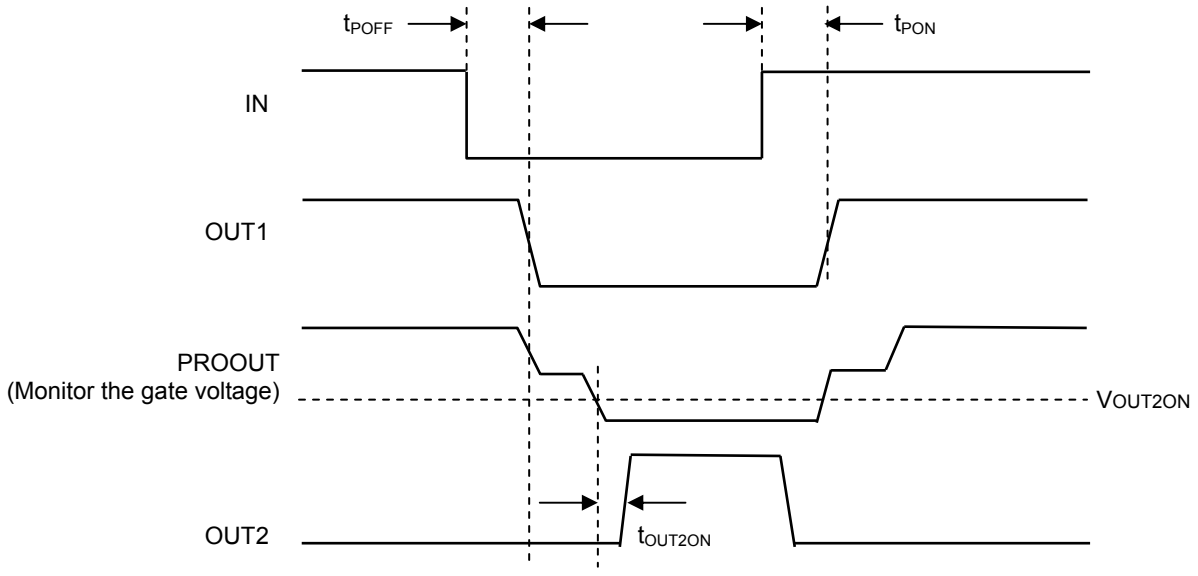


Figure 5. Timing chart of Miller Clamp function

2) Fault status output

This function is used to output a fault signal from the FLT pin when an fault occurs (i.e., when the undervoltage lockout function (UVLO), short current protection function (SCP) or thermal protection function is activated) and hold the fault signal until the set Fault output holding time is completed. The fault output holding time t_{FLTRLS} is given as the following equation with the settings of capacitor C_{FLTRLS} and resistor R_{FLTRLS} connected to the FLTRLS pin. For example, when C_{FLTRLS} is set to 0.01μF and R_{FLTRLS} is set to 200kΩ, the holding time will be set to 2 ms.

t_{FLTRLS} [ms]= C_{FLTRLS} [μF]•R_{FLTRLS} [kΩ]

To set the fault output holding time to “0” ms, only connect the resistor R_{FLTRLS}.

Status	FLT pin
Normal	Hi-Z
Fault occurs	L

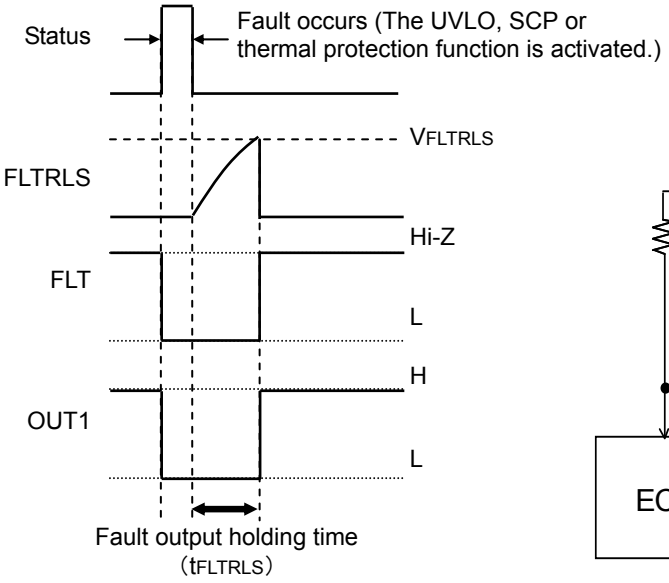


Figure 6. Fault Status Output Timing Chart

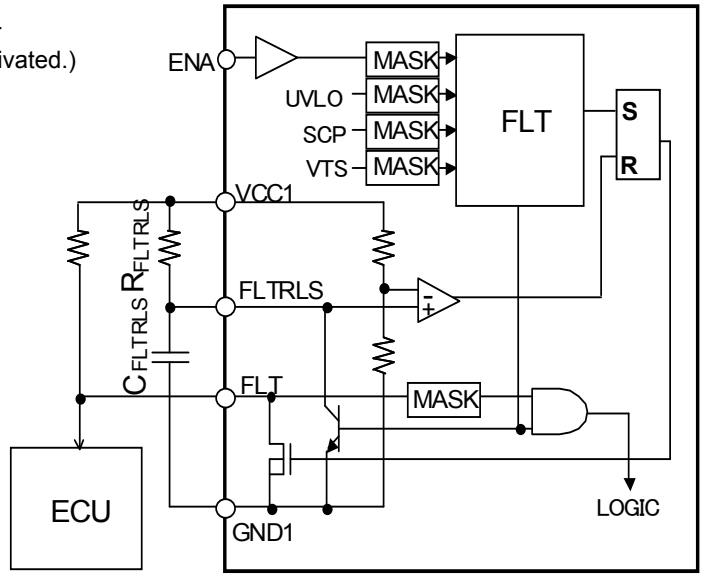


Figure 7. Fault Output Block Diagram

3) Undervoltage Lockout (UVLO) function

The BM60013FV-C incorporates the undervoltage lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage, the OUT1 pin and the FLT pin both will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. However, during the fault output holding time set in “2) Fault status output” section, the OUT1 pin and the FLT pin will hold the “L” signal. In addition, to prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ and $t_{UVLO2MSK}$ are set on both low and high voltage sides.

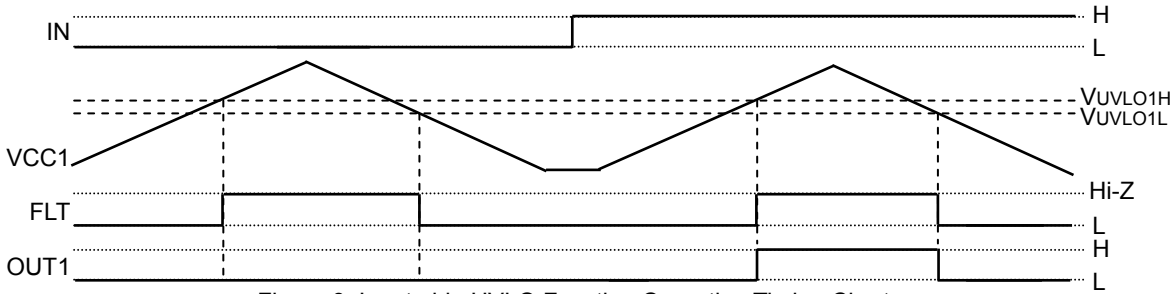


Figure 8. Input-side UVLO Function Operation Timing Chart

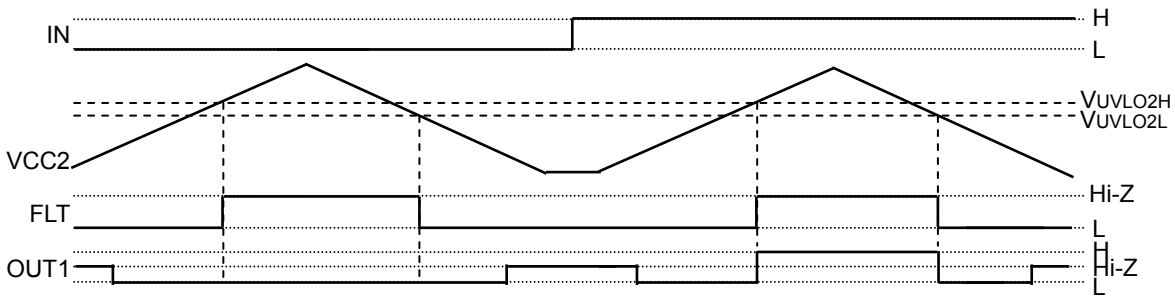


Figure 9. Output-side UVLO Operation Timing Chart

4) Short current protection function (SCP, DESAT)

When the SCPIN pin voltage exceeds a voltage set with the SCPTH pin voltage, the SCP function will be activated. When the SCP function is activated, the OUT1 pin voltage will be set to the “Hi-Z” level first, and then the PROOUT pin voltage to the “L” level (soft turn-off).Next, after t_{STO} has passed after the short-circuit current falls below the threshold value, OUT1 pin becomes L and PROOUT pin becomes Hi-Z. Finally, when the fault output holding time set in “2) fault status output” section on page 5 is completed, the SCP function will be released.

$V_{COLLECTOR}/V_{DRAIN}$ which Desaturation Protection starts operation (V_{DESAT}) and the blanking time (t_{BLANK}) can be calculated by the formula below;

$$V_{DESAT}[V] = V_{SCPTH} \bullet \frac{R3+R2}{R3} - V_{F_{D1}}$$

$$V_{CC2_{MIN}}[V] > V_{SCPTH} \bullet \frac{R3+R2+R1}{R3}$$

$$t_{BLANK\text{outernal}}[s] = -\frac{R2+R1}{R3+R2+R1} \bullet R3 \bullet C_{BLANK} \bullet \ln\left(1 - \frac{R3+R2+R1}{R3} \bullet \frac{V_{SCPTH}}{V_{CC2}}\right) + 0.2 \bullet 10^{-6}$$

V_{DESAT}	Reference Value (In case of SCPTH=0.7V)		
	R1	R2	R3
4.0V	15 kΩ	39 kΩ	6.8 kΩ
4.5V	15 kΩ	43 kΩ	6.8 kΩ
5.0V	15 kΩ	36 kΩ	5.1 kΩ
5.5V	15 kΩ	39 kΩ	5.1 kΩ
6.0V	15 kΩ	43 kΩ	5.1 kΩ
6.5V	15 kΩ	62 kΩ	6.8 kΩ
7.0V	15 kΩ	68 kΩ	6.8 kΩ
7.5V	15 kΩ	82 kΩ	7.5 kΩ
8.0V	15 kΩ	91 kΩ	8.2 kΩ
8.5V	15 kΩ	82 kΩ	6.8 kΩ
9.0V	15 kΩ	130 kΩ	10 kΩ
9.5V	15 kΩ	91 kΩ	6.8 kΩ
10.0V	15 kΩ	130 kΩ	9.1 kΩ

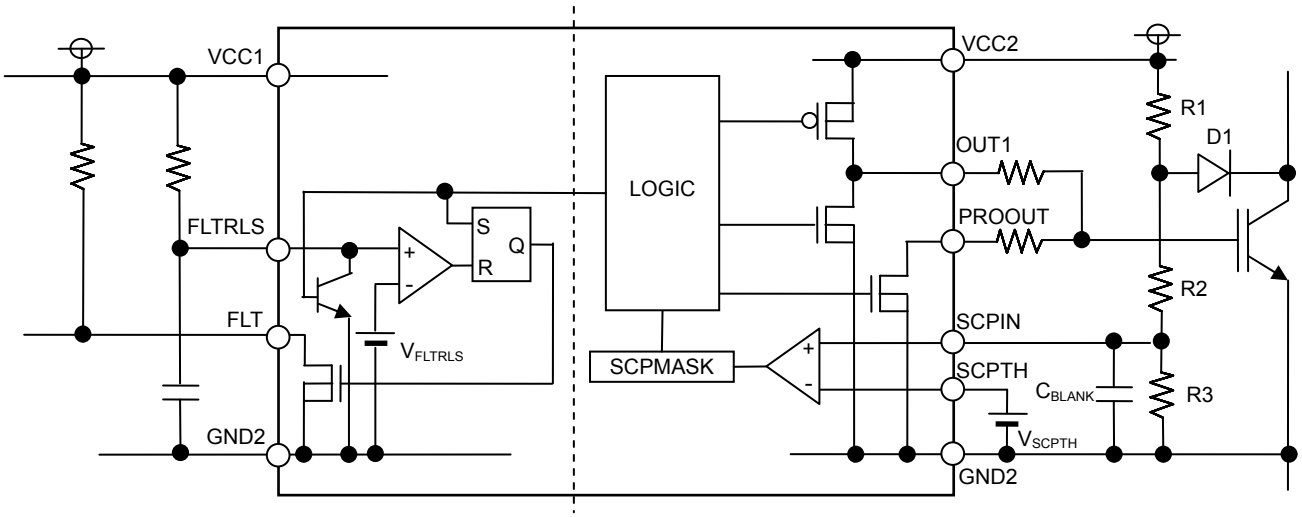


Figure 10. Block Diagram for DESAT

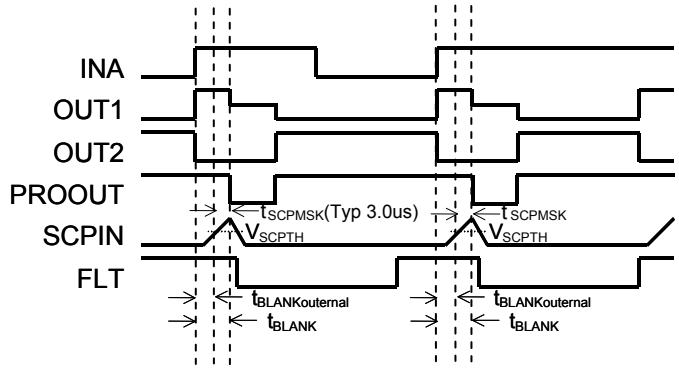
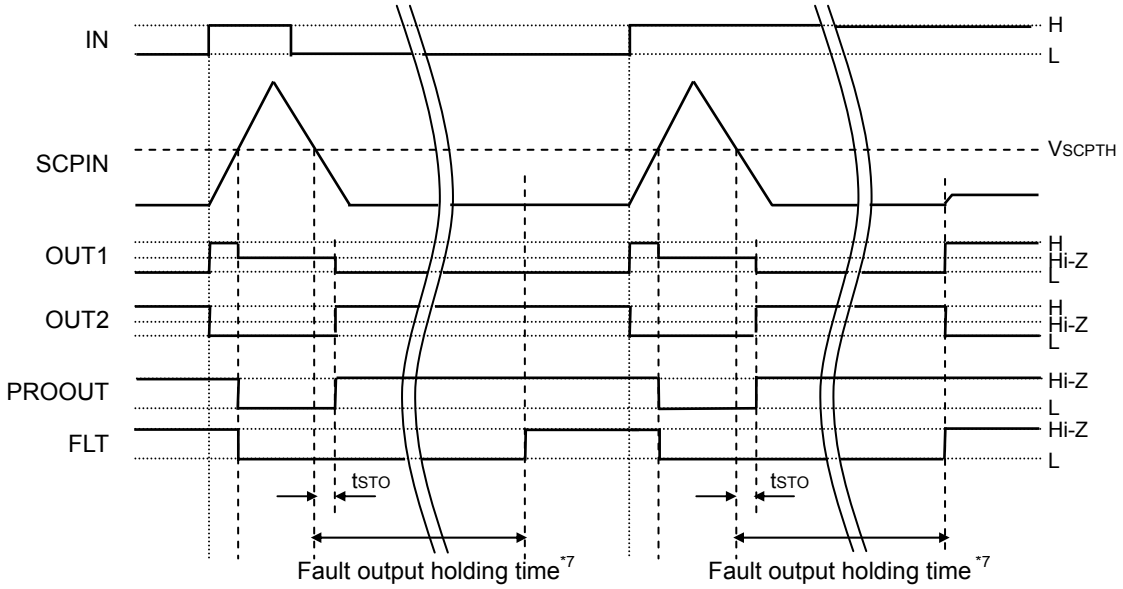


Figure 11. DESAT sequence



*7: "2) Fault status output" section on page 5

Figure 12. SCP Operation Timing Chart

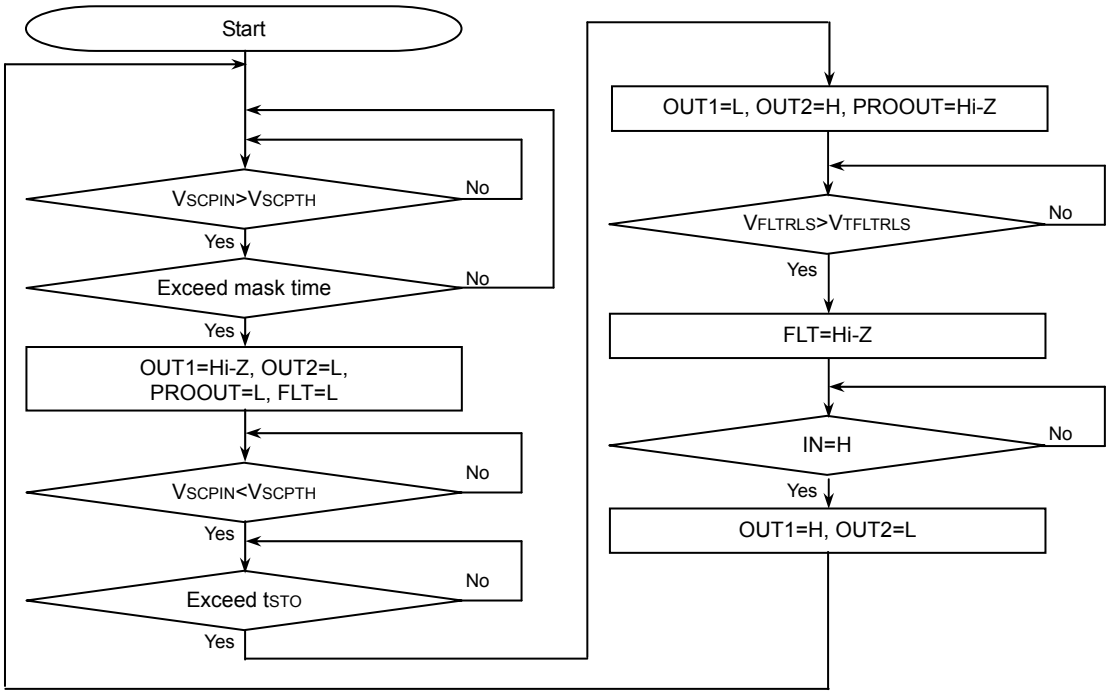


Figure 13. SCP Operation Status Transition Diagram

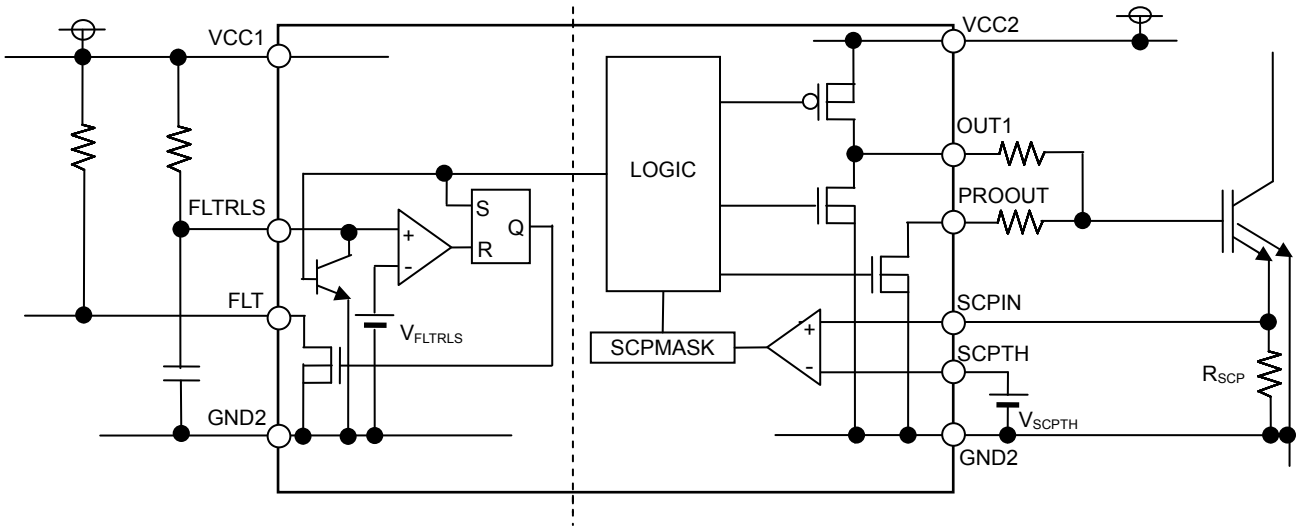


Figure 14. Block Diagram for SCP

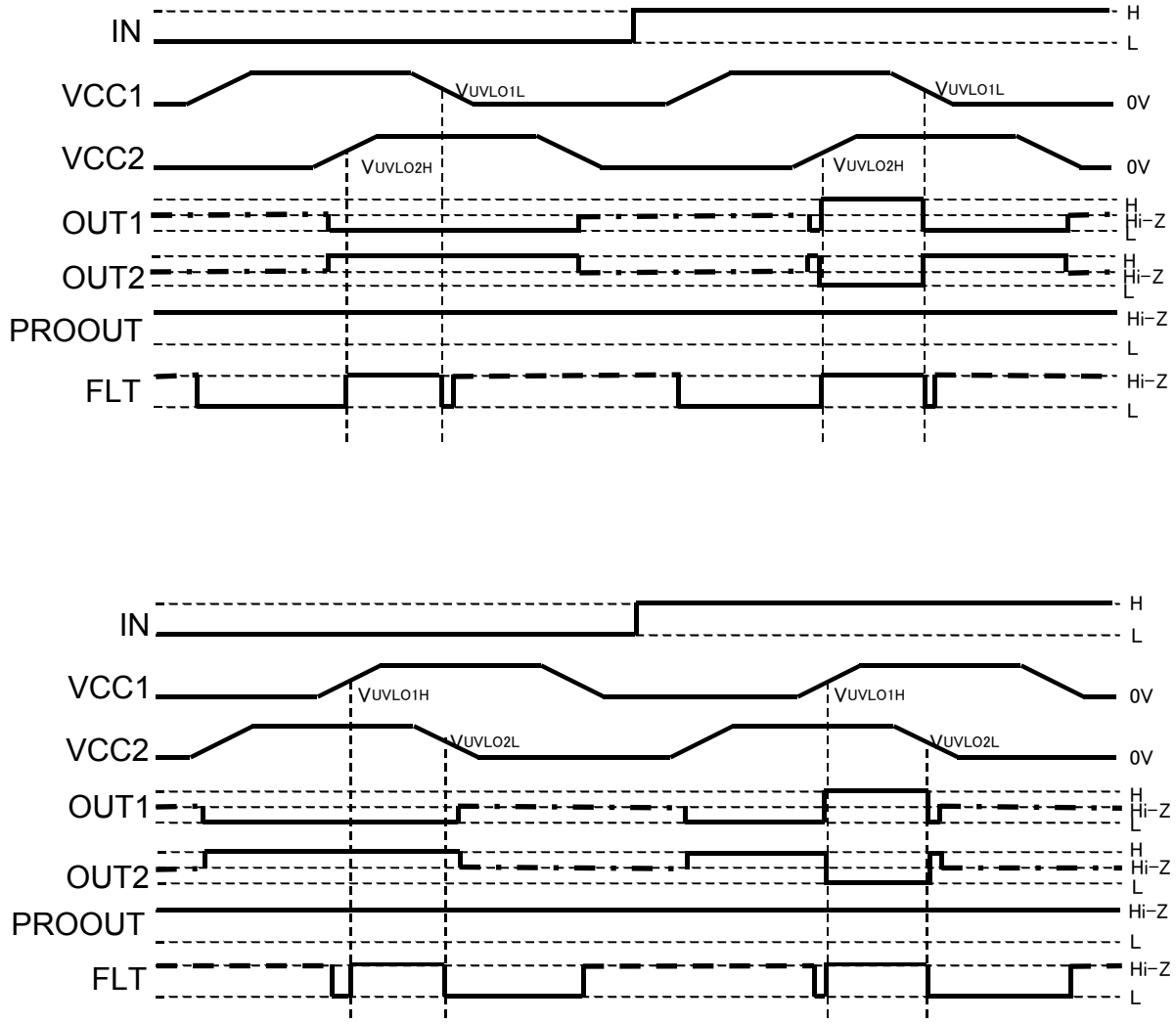
5）I/O condition table

No.	Status	Input									Output			
		VCC1	VCC2	VTSIN	SCPIN	FLT	ENA	INB	INA	PROOUT	OUT1	OUT2	PROOUT	FLT
1	VCC1UVLO	UVLO	X	X	L	X	X	X	X	H	L	L	Hi-Z	L
2		UVLO	X	X	L	X	X	X	X	L	L	H	Hi-Z	L
3	VCC2UVLO	X	UVLO	X	L	X	X	X	X	H	L	L	Hi-Z	L
4		X	UVLO	X	L	X	X	X	X	L	L	H	Hi-Z	L
5	Disable	○	○	H	L	H	L	X	X	H	L	L	Hi-Z	Hi-Z
6		○	○	H	L	H	L	X	X	L	L	H	Hi-Z	Hi-Z
7	FLT external input	○	○	H	L	L	X	X	X	H	L	L	Hi-Z	Hi-Z
8		○	○	H	L	L	X	X	X	L	L	H	Hi-Z	Hi-Z
9	SCP	○	○	X	H	X	X	X	X	X	Hi-Z	L	L	L
10	Thermal protection	○	○	L	L	X	X	X	X	H	L	L	Hi-Z	L
11		○	○	L	L	X	X	X	X	L	L	H	Hi-Z	L
12	Non-invert operation L input	○	○	H	L	H	H	L	L	H	L	L	Hi-Z	Hi-Z
13		○	○	H	L	H	H	L	L	L	L	H	Hi-Z	Hi-Z
14	Non-invert operation H input	○	○	H	L	H	H	L	H	X	H	L	Hi-Z	Hi-Z
15	Invert operation L input	○	○	H	L	H	H	H	L	X	H	L	Hi-Z	Hi-Z
16	Invert operation H input	○	○	H	L	H	H	H	H	H	L	L	Hi-Z	Hi-Z
17		○	○	H	L	H	H	H	H	L	L	H	Hi-Z	Hi-Z

○: VCC1 or VCC2 > UVLO, X:Don't care

(Caution) When other errors are complicated immediately after the SCP function is activated, SCP function (soft turn-off) is given to priority.

6) Power supply startup / shutoff sequence



: Since the VCC2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions.

: Since the VCC1 pin voltage is low and the FLT output MOS does not turn ON, the output pins become Hi-Z conditions.

Figure 15. Power supply startup / shutoff sequence

●Absolute maximum ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CC1}	-0.3 to +7.0[*1]	V
Output-side supply voltage	V_{CC2}	-0.3 to +25.0[*2]	V
INA, INB, ENA pin input voltage	V_{IN}	-0.3 to +VCC1+0.3 or +7.0[*1]	V
FLT pin input voltage	V_{FLT}	-0.3 to +VCC1+0.3 or +7.0[*1]	V
FLTRLS pin input voltage	V_{FLTRLS}	-0.3 to +VCC1+0.3 or +7.0[*1]	V
VTSIN pin input voltage	V_{VTSIN}	-0.3 to +7.0[*2]	V
SCPIN pin input voltage	V_{SCPIN}	-0.3 to +VCC2+0.3V or +25.0[*2]	V
VTSTH pin input voltage	V_{VTSTH}	-0.3 to +7.0[*2]	V
SCPTH pin input voltage	V_{SCPTH}	-0.3 to +VCC2+0.3V or +25.0[*2]	V
OUT1 pin output current (DC)	I_{OUT1}	0.4[*3]	A
OUT1 pin output current (Peak 1us)	$I_{OUT1PEAK}$	5.0	A
OUT2 pin output current (DC)	I_{OUT2}	0.1[*3]	A
OUT2 pin output current (Peak 1us)	$I_{OUT2PEAK}$	1.0	A
PROOUT pin output current	I_{PROOUT}	0.2[*3]	A
FLT output current	I_{FLT}	10	mA
Power dissipation	P_d	1.19[*4]	W
Operating temperature range	T_{opr}	-40 to +125	℃
Storage temperature range	T_{stg}	-55 to +150	℃
Junction temperature	T_{jmax}	+150	℃

*1 Relative to GND1.
*2 Relative to GND2.
*3 Should not exceed Pd and Tj=150°C.
*4 Derate above Ta=25°C at a rate of 9.5mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm.

●Recommended operating conditions

Parameter	Symbol	Min.	Max.	Units
Input-side supply voltage	V_{CC1}[*5]	4.5	5.5	V
Output-side positive supply voltage	V_{CC2}[*6]	14.0	20.0	V
Short current detection common mode input voltage	V_{SCCM}	0.0	2.5	V
Thermal detection common mode input voltage	V_{TSCM}	0.0	3.0	V

*5 Relative to GND1.
*6 Relative to GND2.

●Insulation related characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

●**Electrical characteristics**

（Unless otherwise specified Ta=-40℃ to 125℃, V_{CC1}=4.5V to 5.5V, V_{CC2}=14V to 20V）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
Input side circuit current 1	I_{CC11}	0.10	0.35	0.60	mA	OUT1=L
Input side circuit current 2	I_{CC12}	0.10	0.35	0.60	mA	OUT1=H
Input side circuit current 3	I_{CC13}	1.1	1.9	2.7	mA	INA =10kHz, Duty=50%
Input side circuit current 4	I_{CC14}	2.0	3.4	4.8	mA	INA =20kHz, Duty=50%
Output side circuit current 1	I_{CC25}	1.6	2.6	3.6	mA	OUT1=L
Output side circuit current 2	I_{CC26}	1.0	1.7	2.4	mA	OUT1=H
Logic block						
Logic high level input voltage	V_{INH}	$0.7 \times V_{CC1}$	-	V_{CC1}	V	INA, INB, ENA, FLT
Logic low level input voltage	V_{INL}	0	-	$0.3 \times V_{CC1}$	V	INA, INB, ENA, FLT
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	INA, INB, ENA
Logic input minimum pulse width	t_{INMin}	-	-	100	ns	INA, INB
ENA, FLT mask time	t_{FLTMSK}	4	10	20	μs	ENA, FLT
Output						
OUT1 ON resistance (Source)	R_{ONH}	0.7	1.8	4.0	Ω	I_{OUT1}=40mA
OUT1 ON resistance (Sink)	R_{ONL}	0.4	0.9	2.0	Ω	I_{OUT1}=40mA
OUT1 maximum current	$I_{OUT1MAX}$	3.0	4.5	-	A	VCC2=15V, design assurance
PROOUT ON resistance	R_{ONPRO}	0.4	0.9	2.0	Ω	I_{PROOUT}=40mA
Turn ON time	t_{PON}	100	150	200	ns	No load between OUT1-GND2
Turn OFF time	t_{POFF}	100	150	200	ns	No load between OUT1-GND2
Propagation distortion	t_{PDIST}	-20	0	20	ns	t_{POFF} - t_{PON}
Rise time	t_{RISE}	25	50	100	ns	10nFbetween OUT1-GND2
Fall time	t_{FALL}	25	50	100	ns	10nFbetween OUT1-GND2
OUT2 ON resistance (Source)	R_{ON2H}	5	10	20	Ω	I_{OUT2}=40mA
OUT2 ON resistance (Sink)	R_{ON2L}	1.7	3.5	7	Ω	I_{OUT2}=40mA
OUT2 ON threshold	V_{OUT2ON}	1.8	2	2.2	V	
OUT2 output delay time	t_{OUT2ON}	-	40	80	ns	
Common Mode Transient Immunity	CM	100	-	-	kV/μs	design assurance
Protection functions						
Input-side UVLO OFF voltage	V_{UVLO1H}	4.05	4.25	4.45	V	
Input-side UVLO ON voltage	V_{UVLO1L}	3.95	4.15	4.35	V	
Input-side UVLO mask time	$t_{UVLO1MSK}$	2	10	30	μs	
Output-side UVLO OFF voltage	V_{UVLO2H}	11.5	12.5	13.5	V	
Output-side UVLO ON voltage	V_{UVLO2L}	10.5	11.5	12.5	V	
Output-side UVLO mask time	$t_{UVLO2MSK}$	4	10	30	μs	
Short current detection offset voltage	V_{SCDET}	-3.25	1.00	5.25	mV	
Short current detection mask time	t_{SCPMSK}	2.1	3.0	3.9	μs	
SCPIN Input voltage	V_{SCPIN}	-	0.25	0.55	V	I_{SCPIN}=1mA
Soft turn OFF release time	t_{STO}	30		110	μs	
Thermal detection offset voltage	V_{TSDET}	-5.50	-1.25	3.00	mV	
Thermal detection mask time	t_{TSMSK}	4	10	30	μs	
FLT output low voltage	V_{FLTL}	-	0.18	0.40	V	I_{FLT}=5mA
FLTRLS threshold	$V_{TFLTRLS}$	$0.64 \times V_{CC1}$ -0.1	$0.64 \times V_{CC1}$	$0.64 \times V_{CC1}$ +0.1	V	

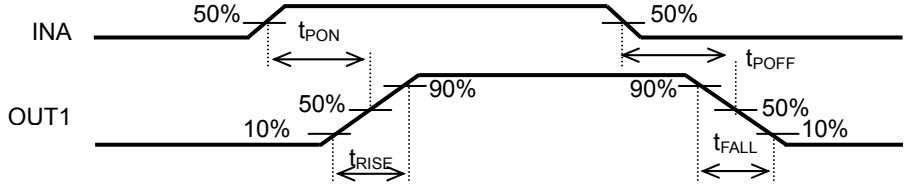


Figure 16. INA-OUT1 Timing Chart

●**Typical Performance Curves**

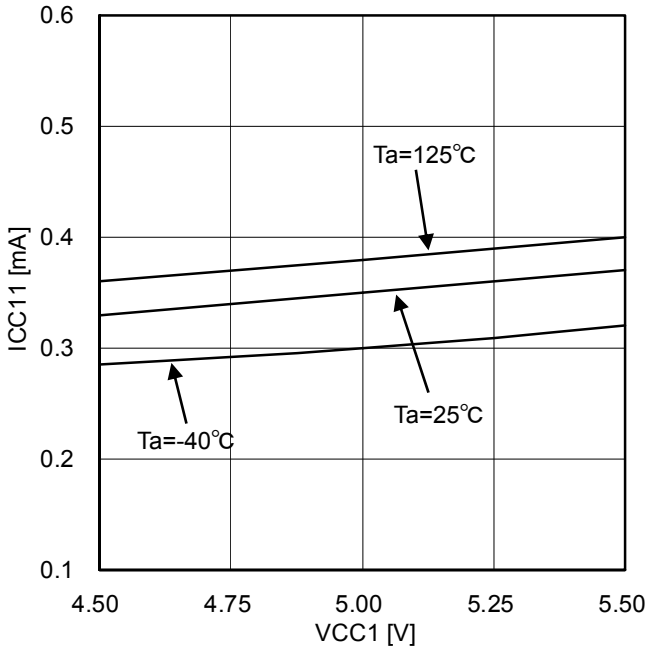


Figure 17. Input side circuit current (at OUT1=L)

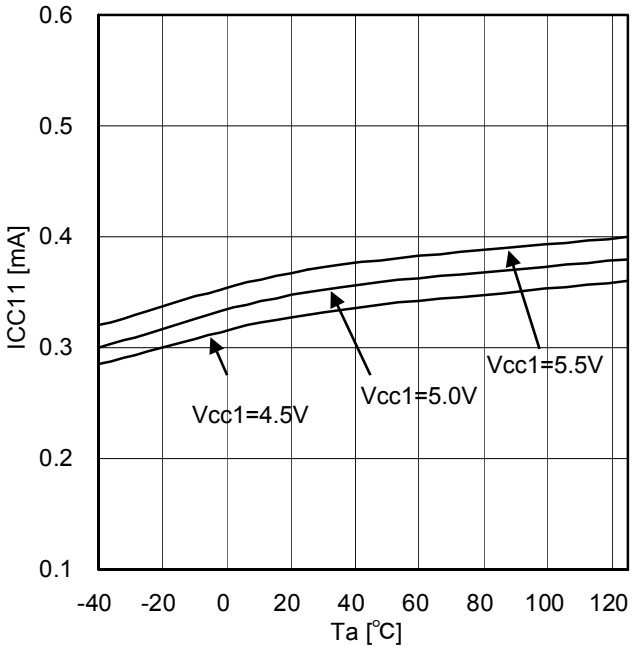


Figure 18. Input side circuit current (at OUT1=L)

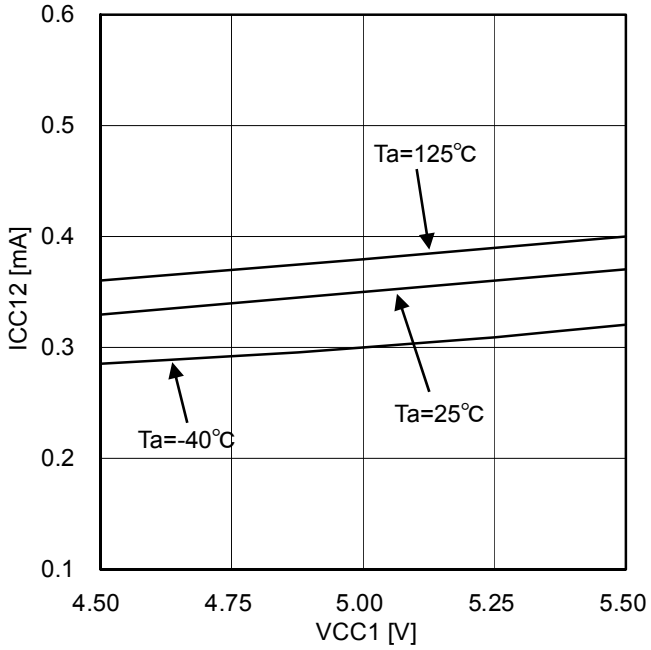


Figure 19. Input side circuit current (at OUT1=H)

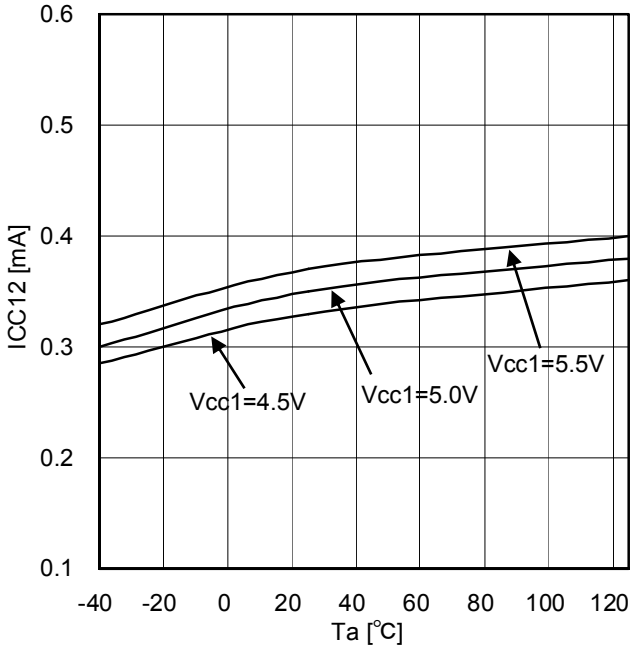


Figure 20. Input side circuit current (at OUT1=H)

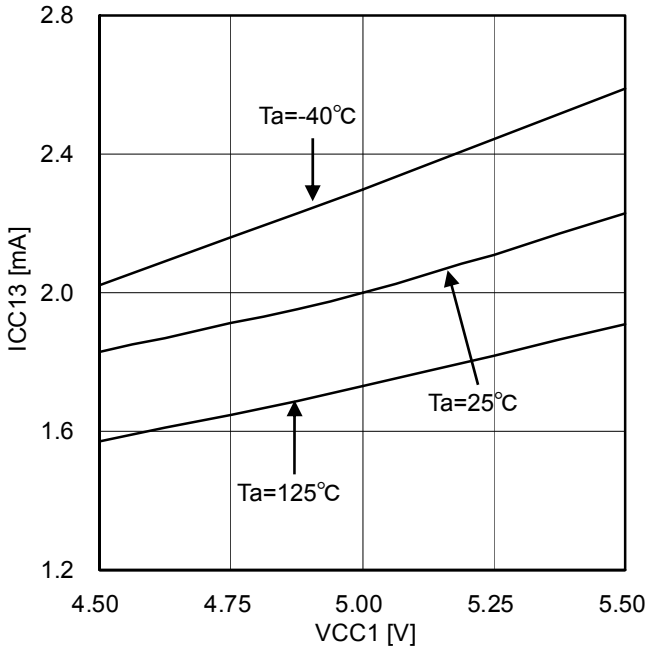


Figure 21. Input side circuit current
(at INA=10kHz and Duty=50%)

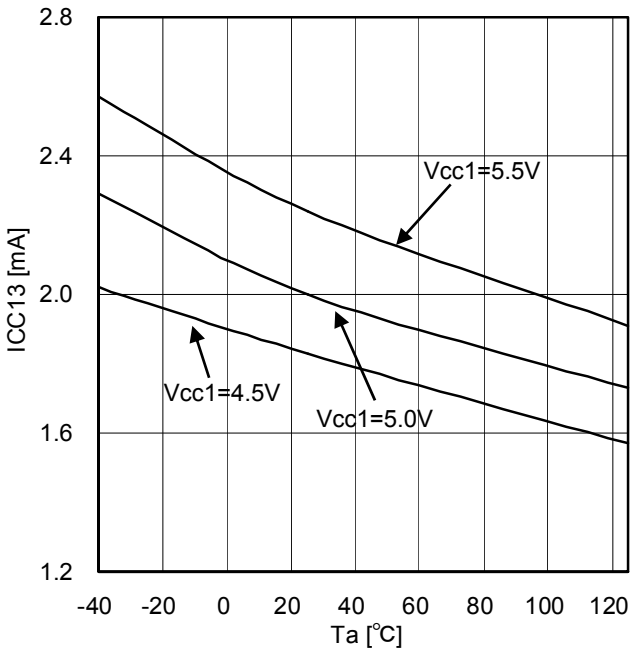


Figure 22. Input side circuit current
(at INA=10kHz and Duty=50%)

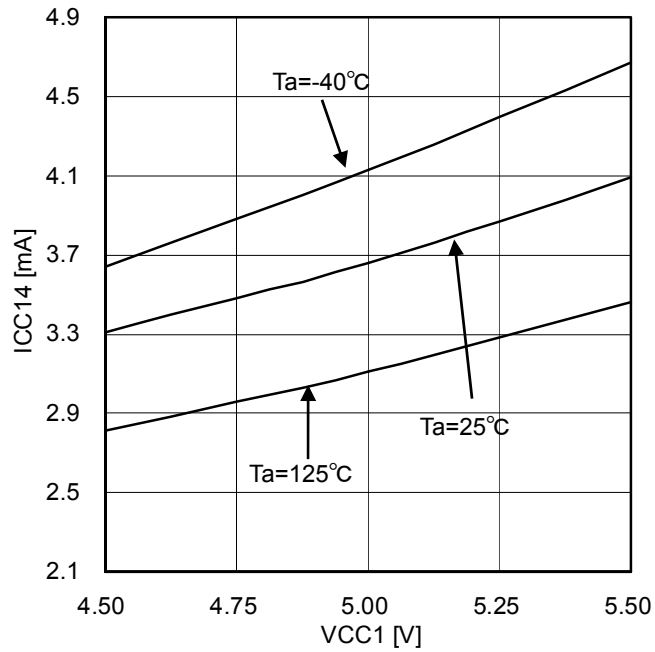


Figure 23. Input side circuit current
(at INA=20kHz and Duty=50%)

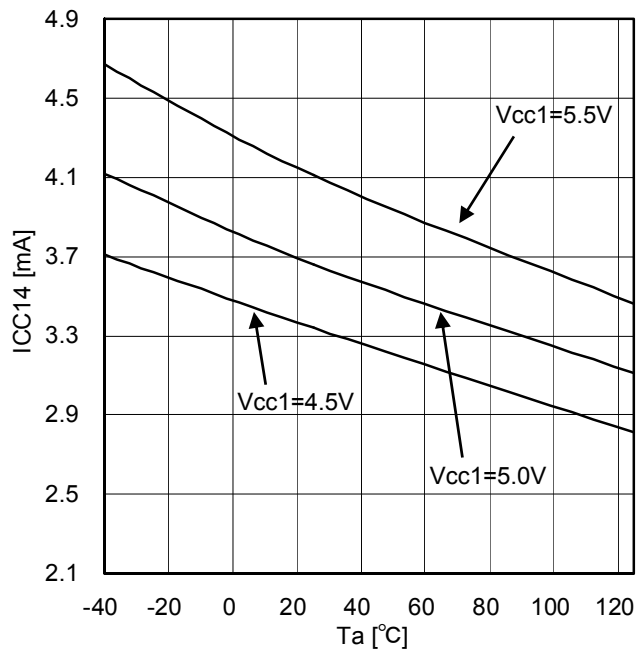


Figure 24. Input side circuit current
(at INA=20kHz and Duty=50%)

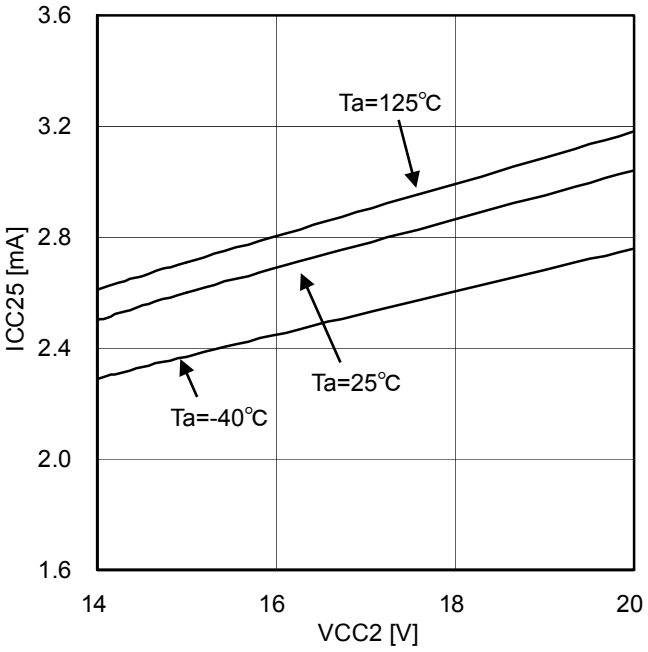


Figure 25. Output side circuit current (at OUT1=L)

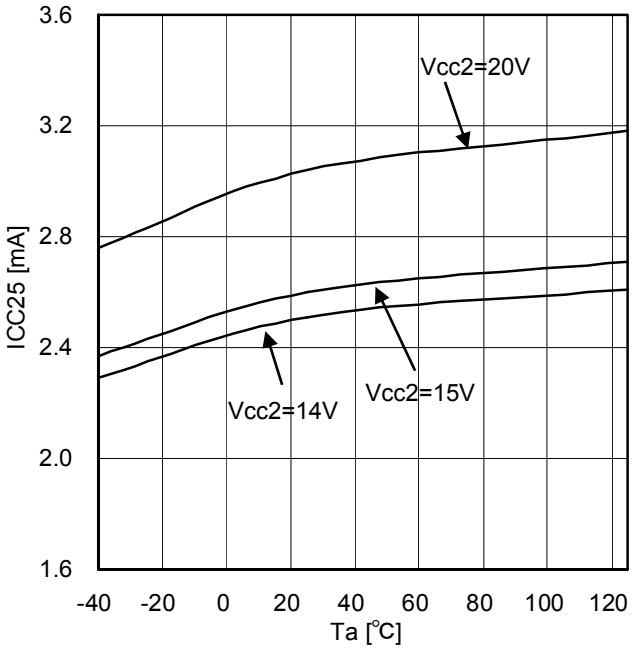


Figure 26. Output side circuit current (at OUT1=L)

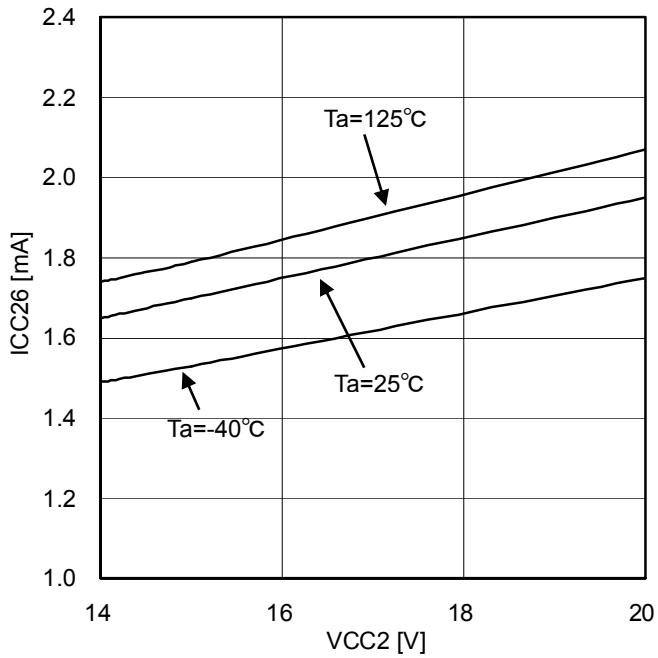


Figure 27. Output side circuit current (at OUT1=H)

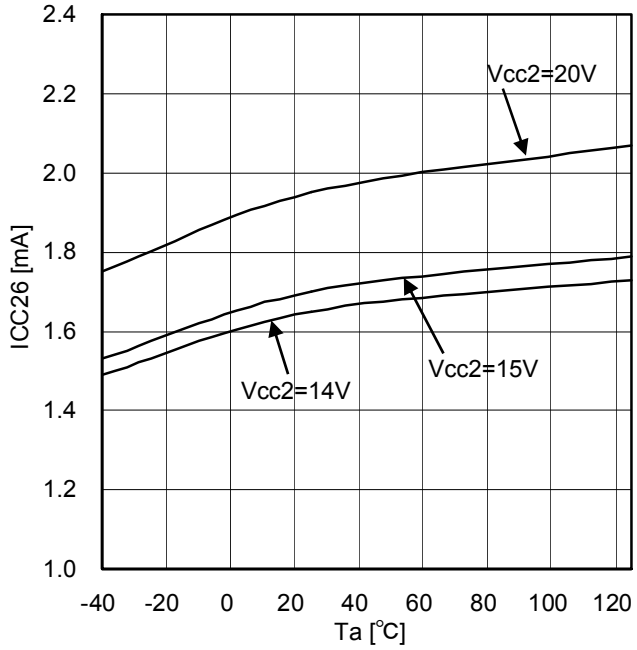


Figure 28. Output side circuit current (at OUT1=H)

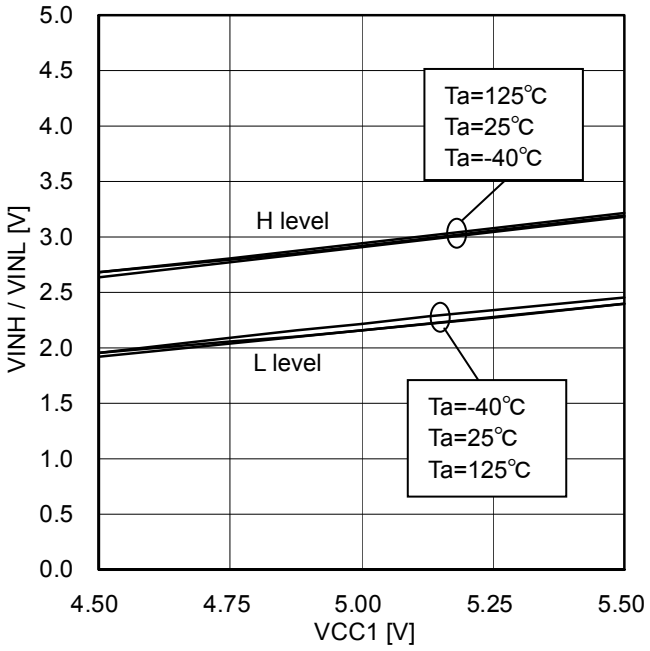


Figure 29. Logic (INA/INB) High/Low level input voltage

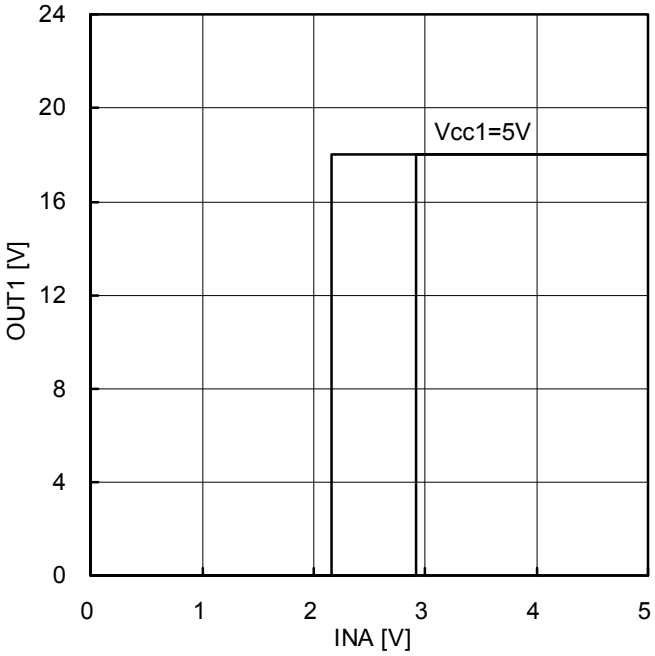


Figure 30. Logic (INA/INB) High/Low level input voltage at Ta=25℃

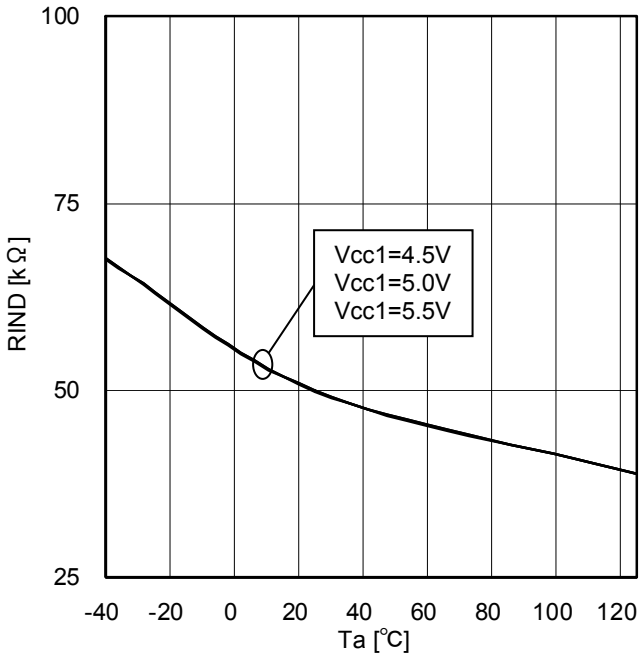


Figure 31. Logic pull-down resistance

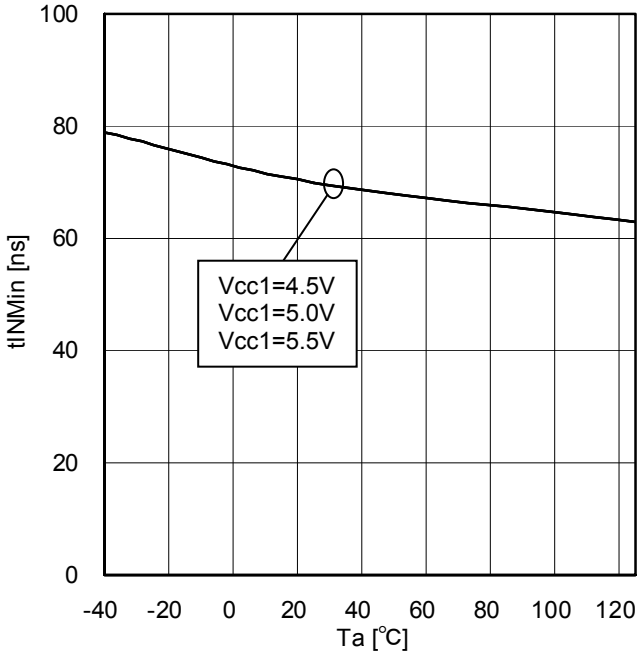


Figure 32. Logic input minimum pulse width（H pulse）

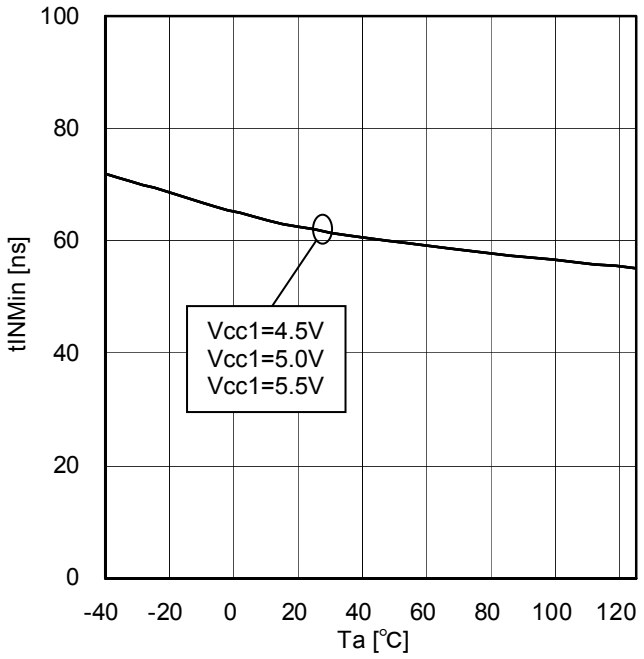


Figure 33. Logic input minimum pulse width（L pulse）

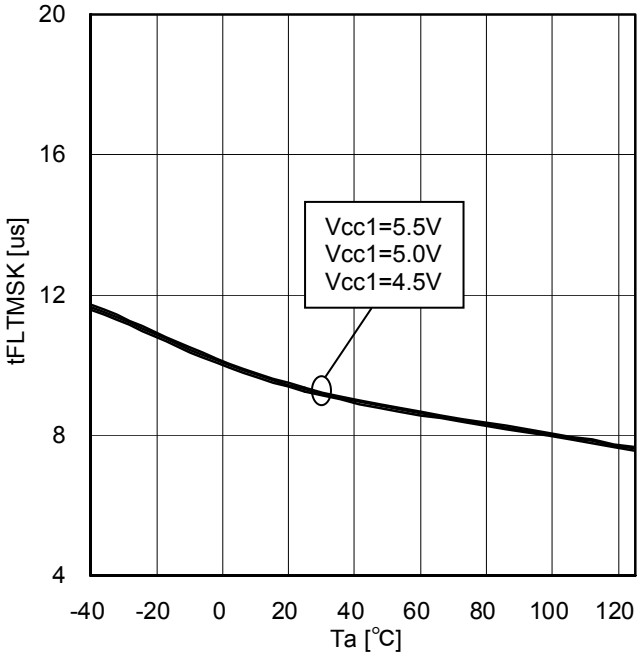


Figure 34. ENA input mask time

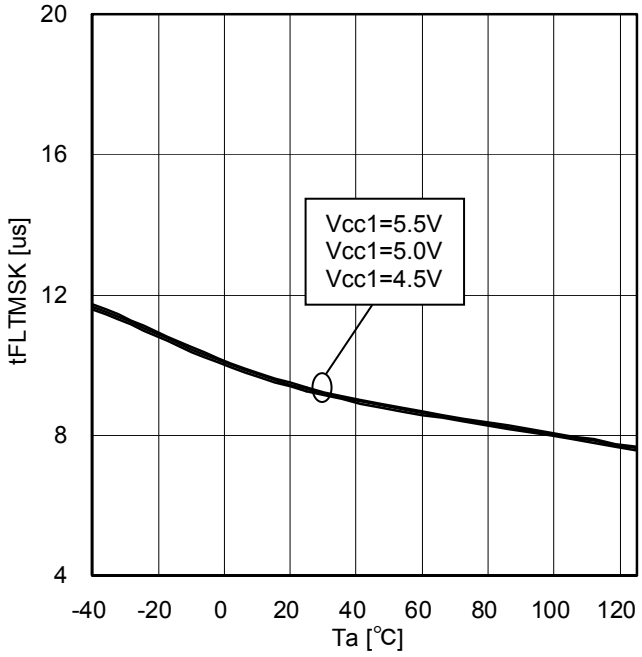


Figure 35. FLT input mask time

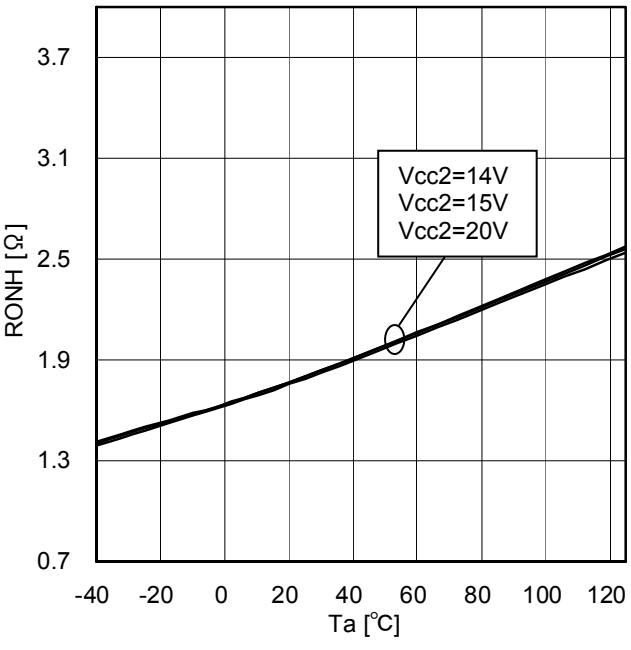


Figure 36. OUT1 ON resistance (Source)

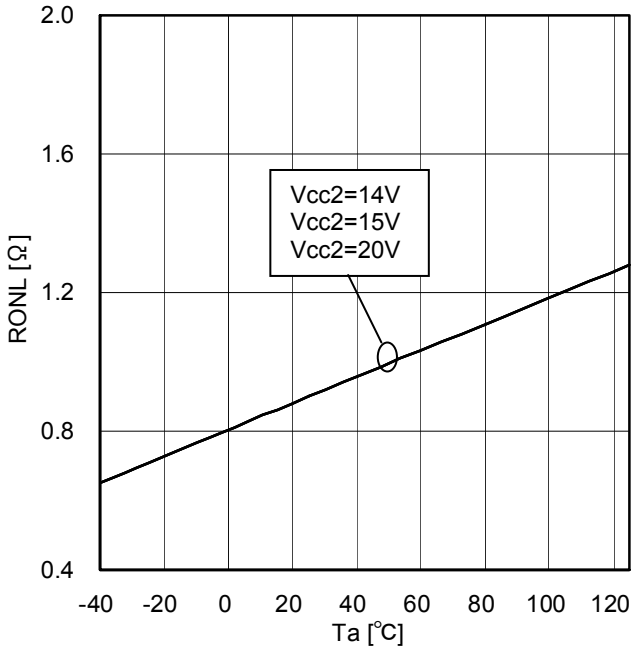


Figure 37. OUT1 ON resistance (Sink)

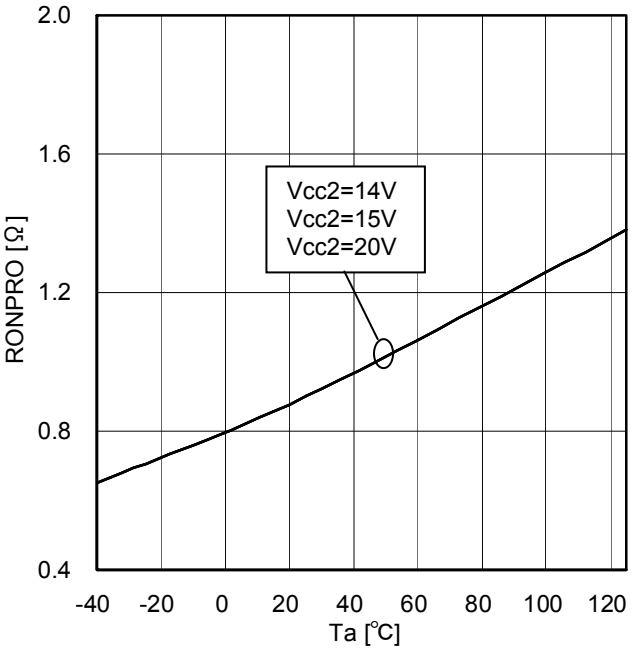


Figure 38. PROOUT ON resistance

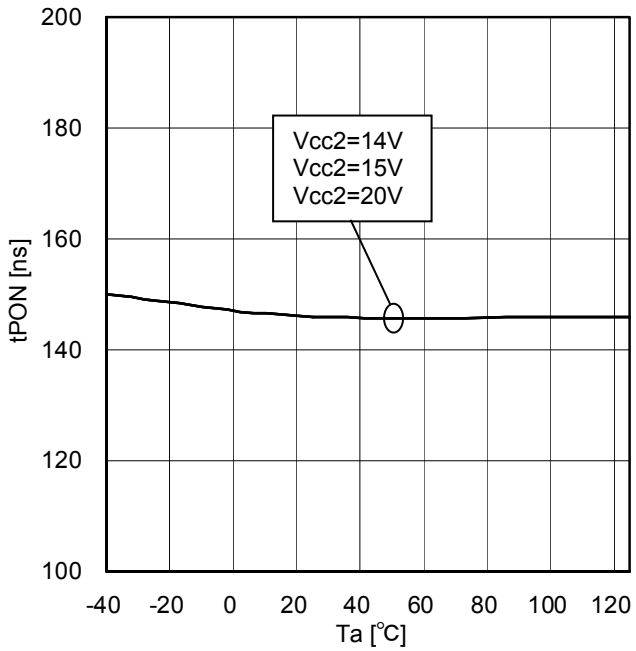


Figure 39. Turn ON time

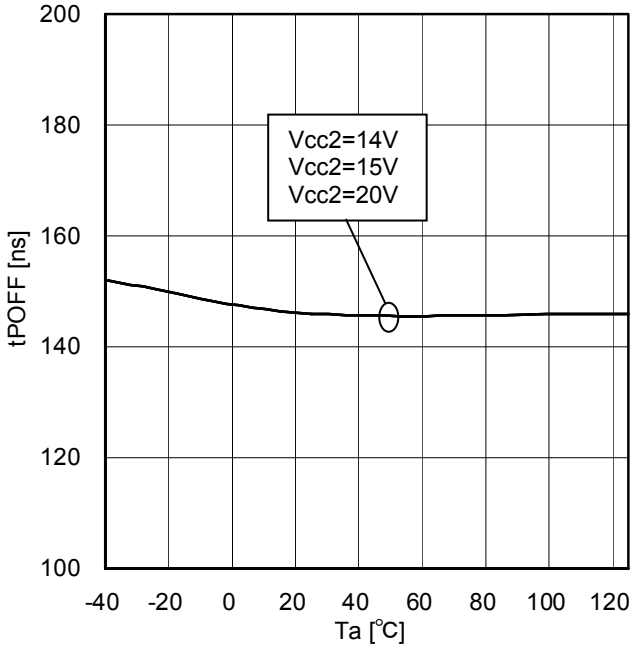


Figure 40. Turn OFF time

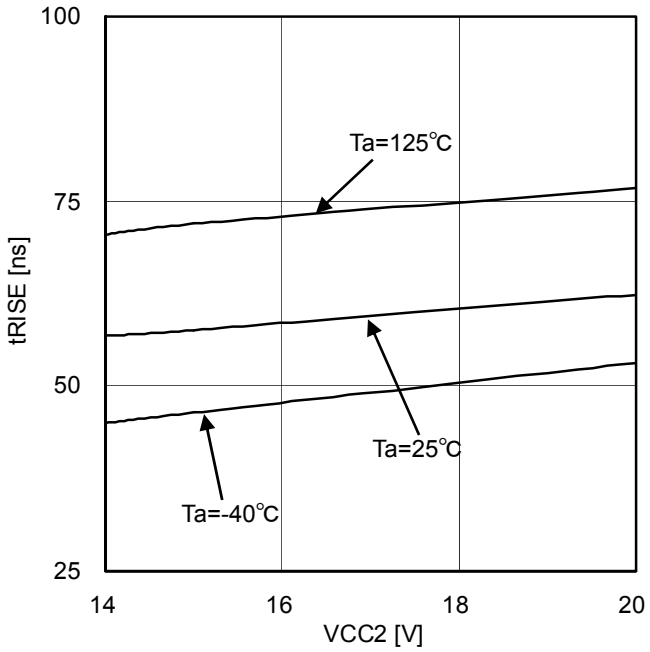


Figure 41. Rise time
(10000pF between OUT1-GND2)

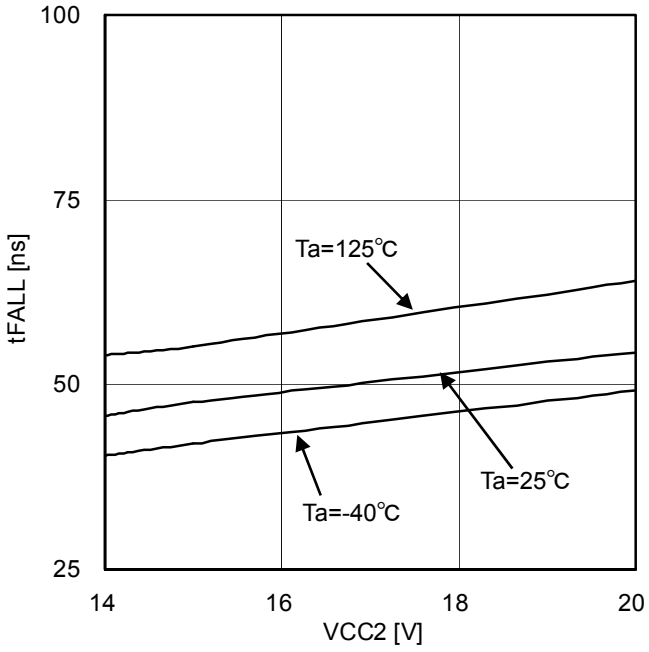


Figure 42. Fall time
(10000pF between OUT1-GND2)

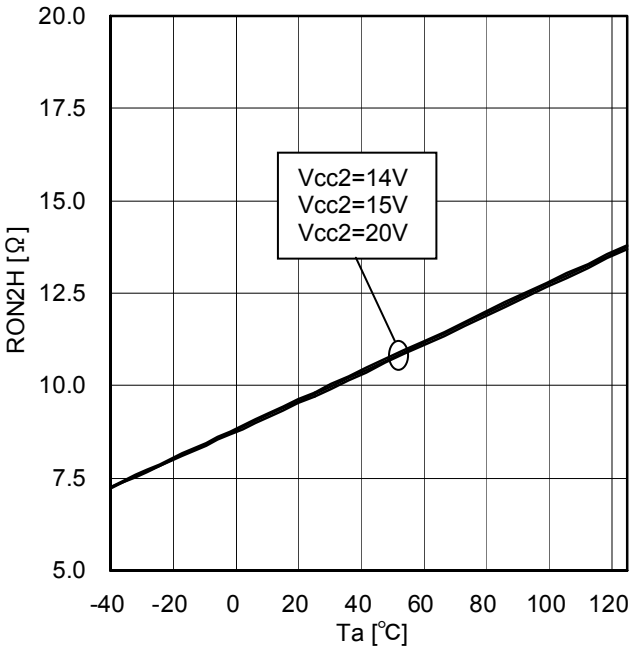


Figure 43. OUT2 ON resistance (Source)

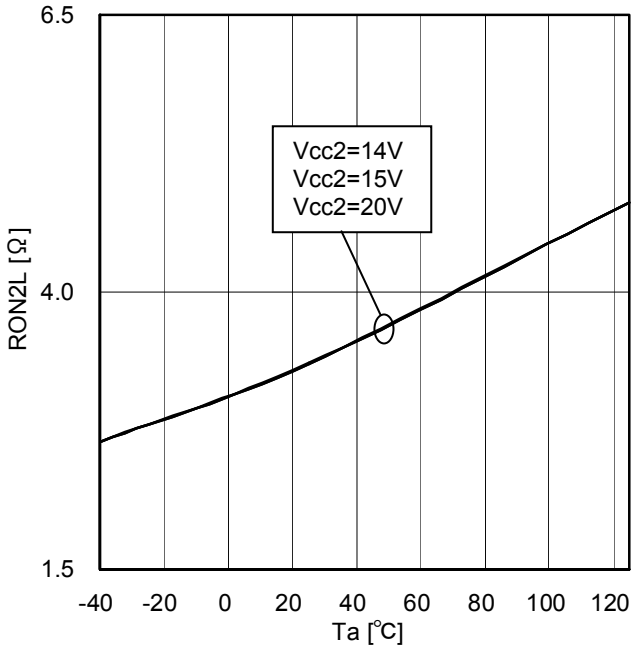


Figure 44. OUT2 ON resistance (Sink)

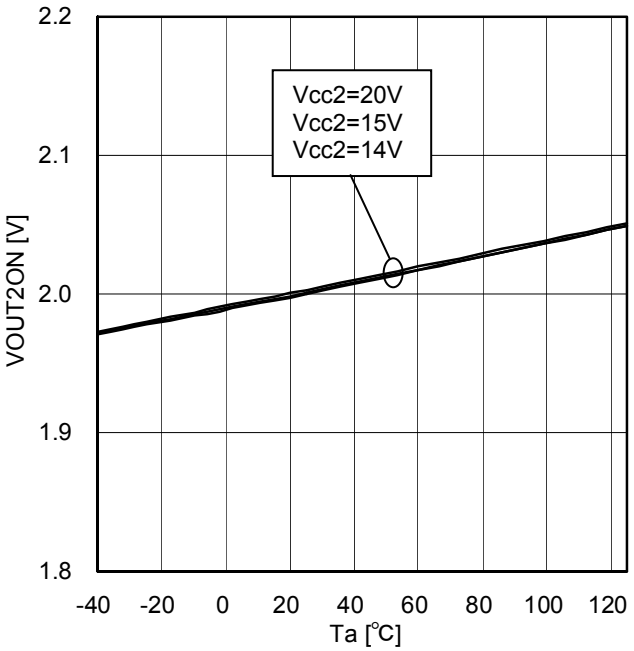


Figure 45. OUT2 ON threshold voltage

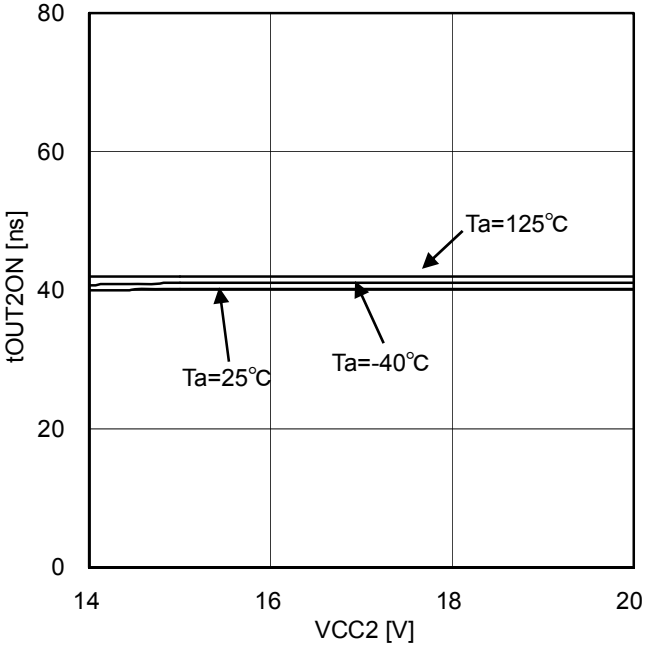


Figure 46. OUT2 output delay time

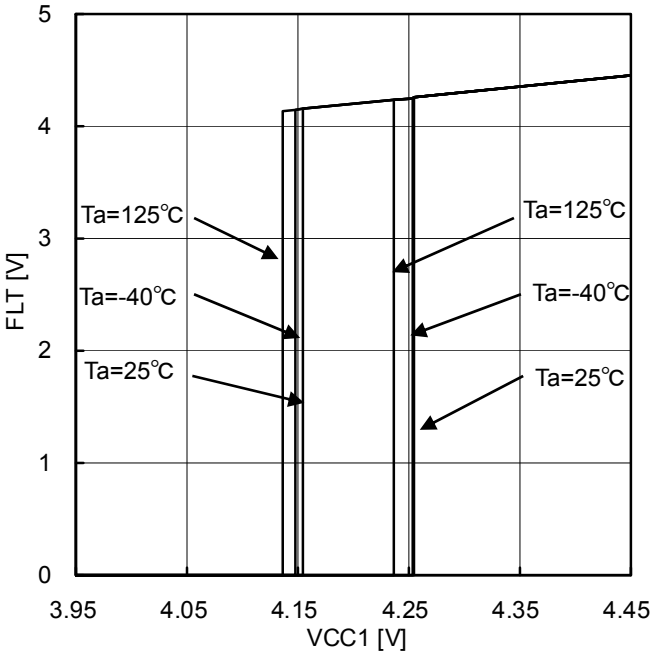


Figure 47. VCC1 UVLO ON/OFF voltage

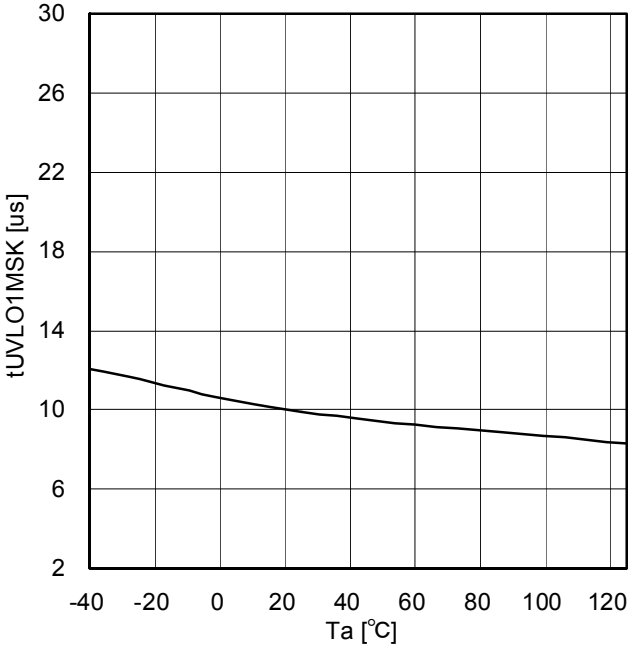


Figure 48. VCC1 UVLO mask time

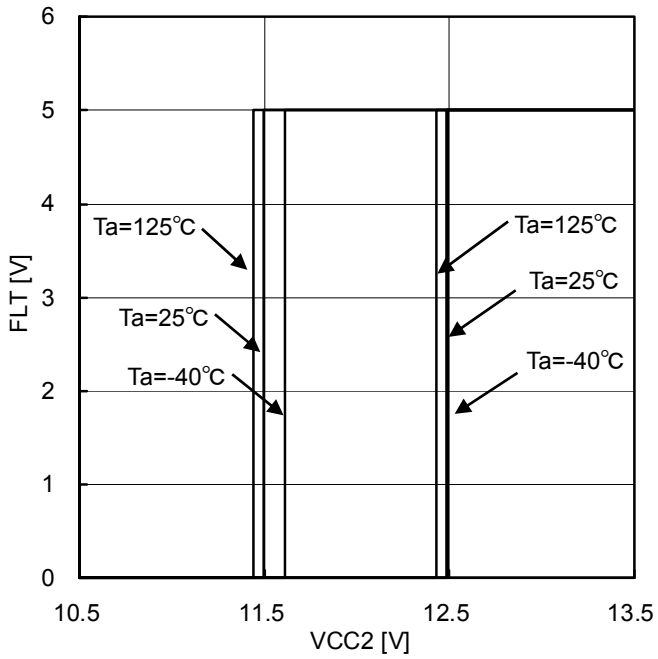


Figure 49. VCC2 UVLO ON/OFF voltage (at VCC1=5V)

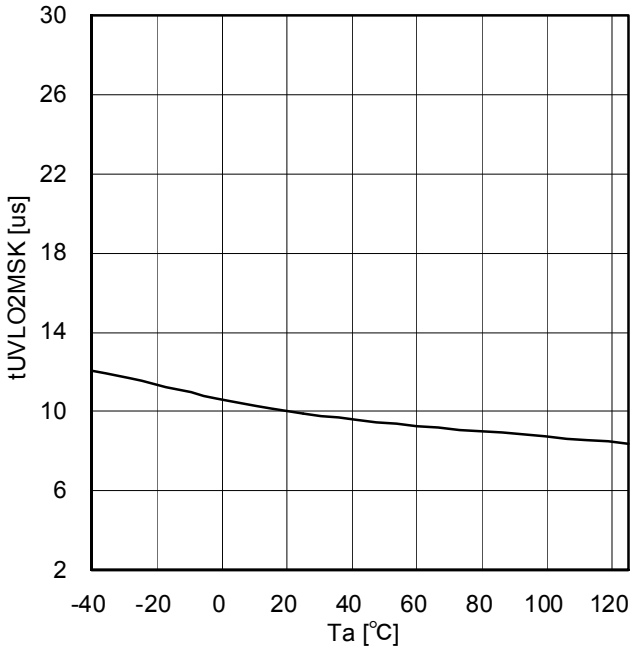


Figure 50. VCC2 UVLO mask time

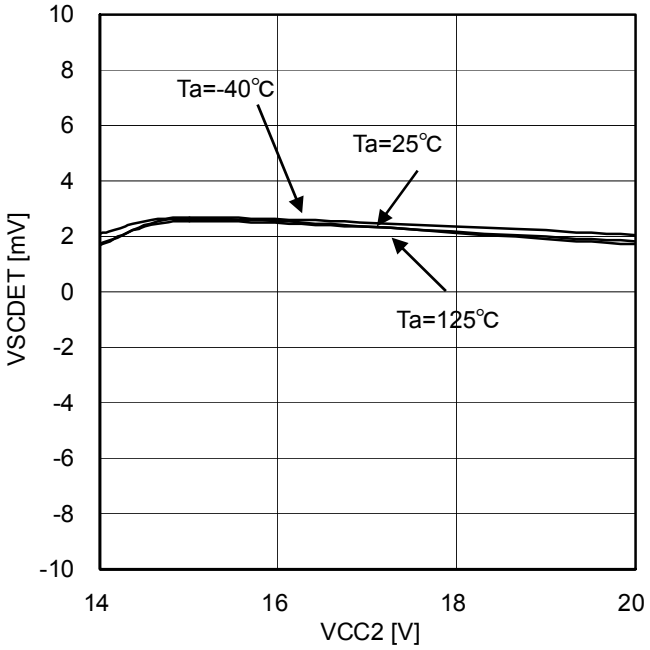


Figure 51. SCP offset voltage (at SCPTH=0.7V)

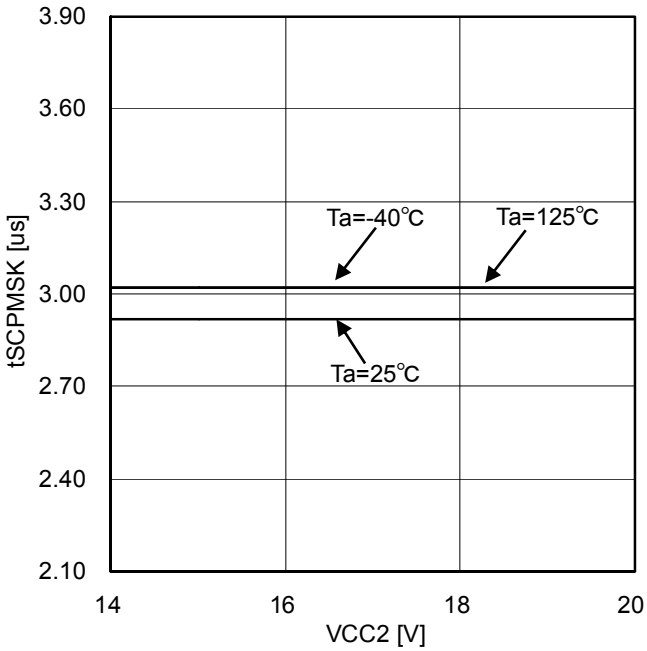


Figure 52. SCP detection mask time

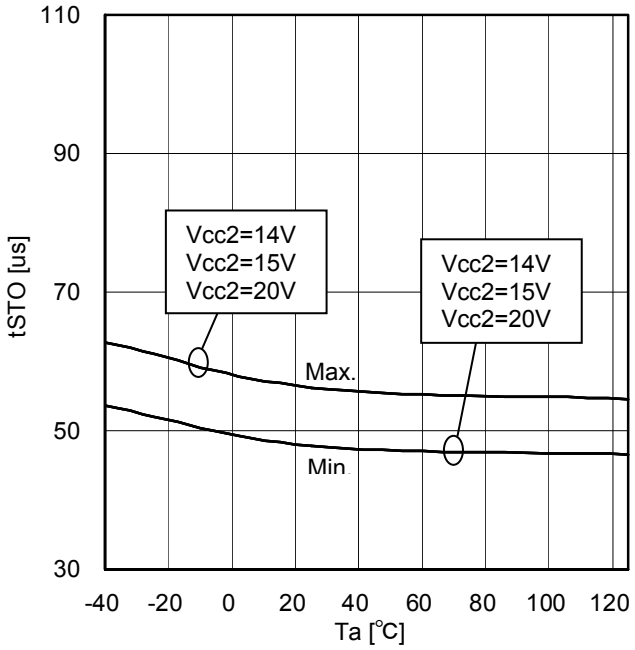


Figure 53. Soft turn OFF release time

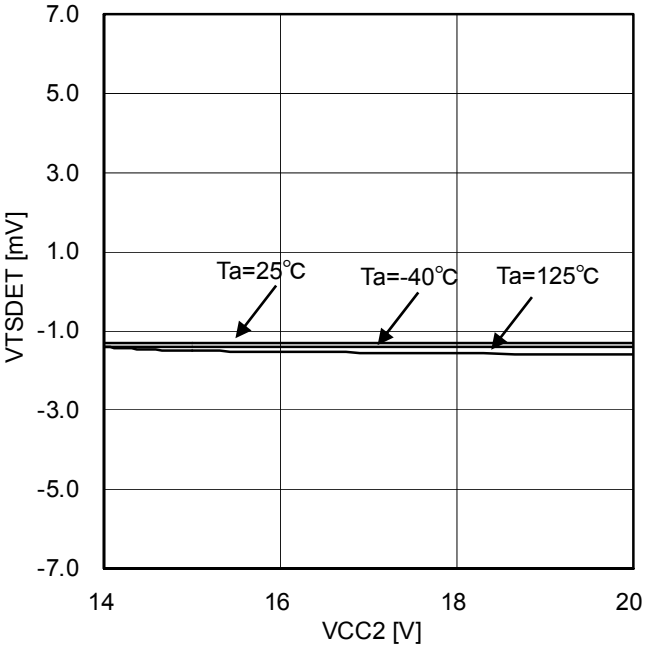


Figure 54. VTS offset voltage (at VTSTH=1.7V)

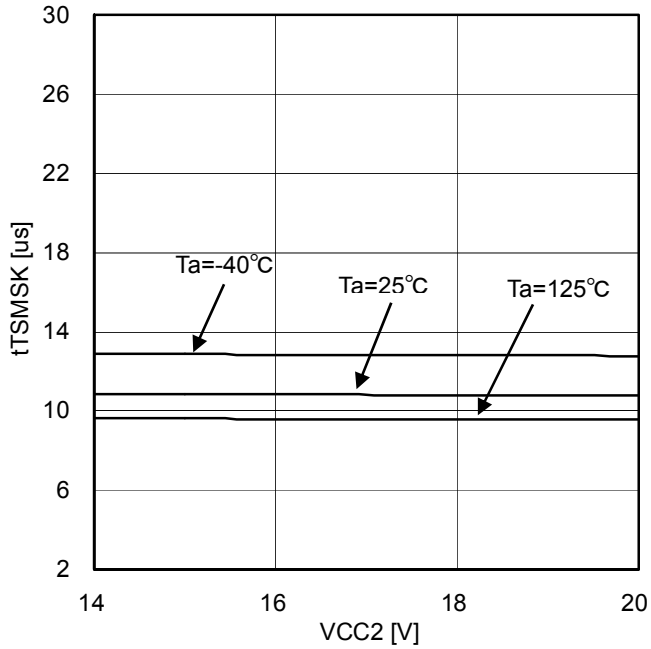


Figure 55. Thermal detection mask time

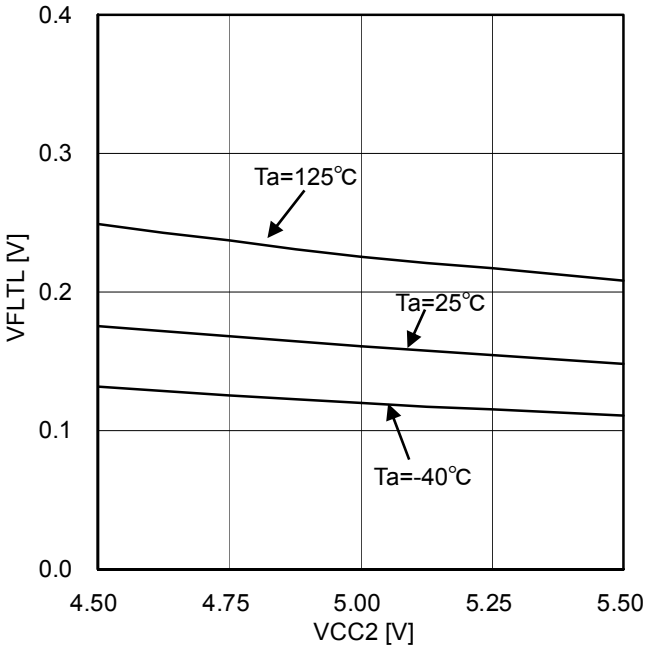


Figure 56. FLT output low voltage (IFLT=5mA)

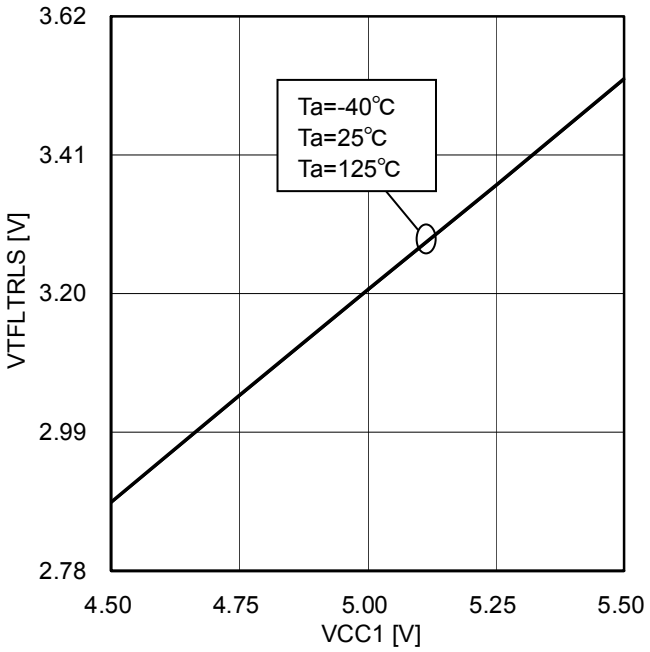


Figure 57. FLTRLS threshold

●**Selection of Components Externally Connected**

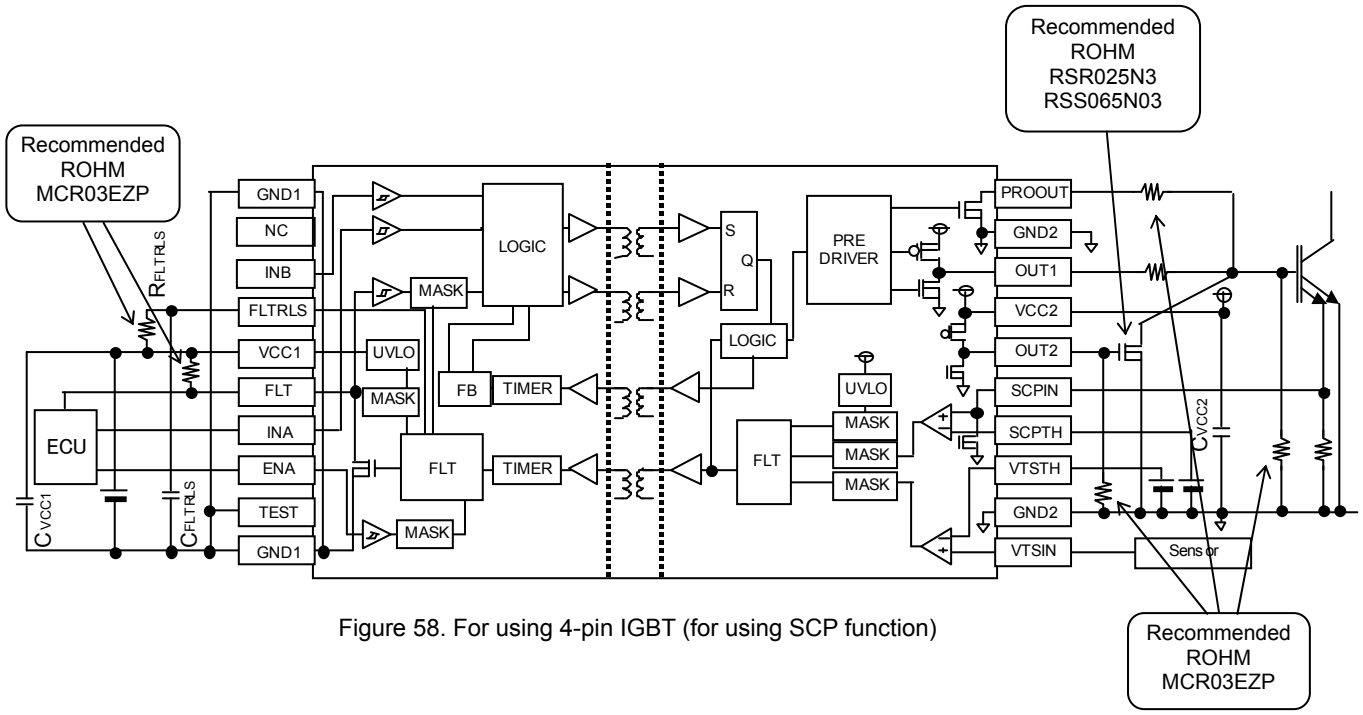


Figure 58. For using 4-pin IGBT (for using SCP function)

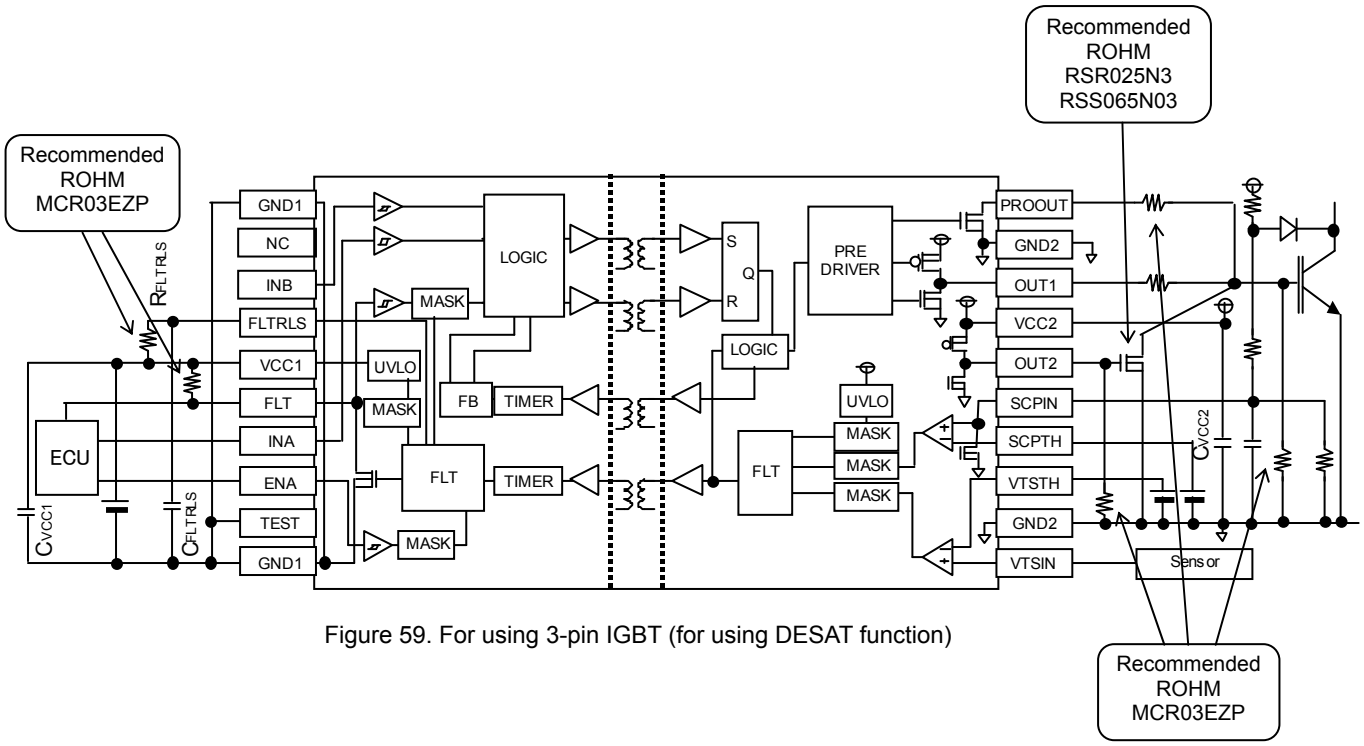
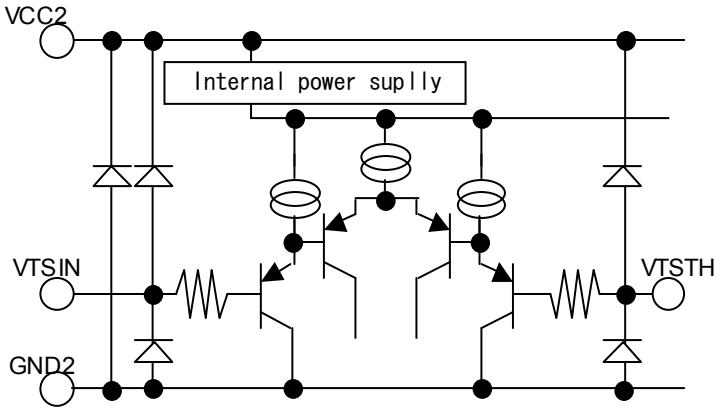
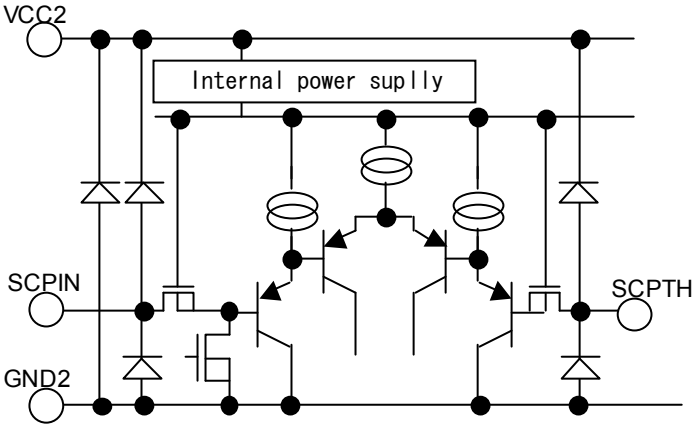
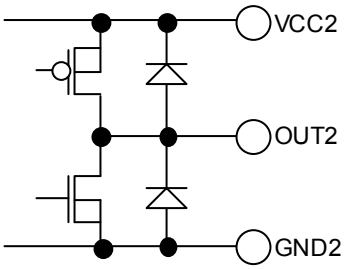
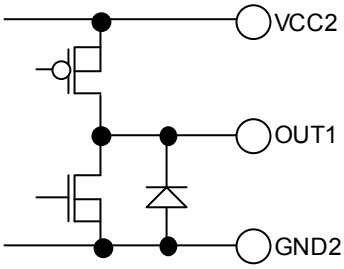
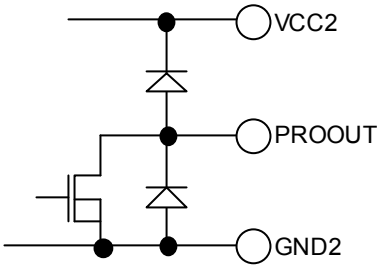
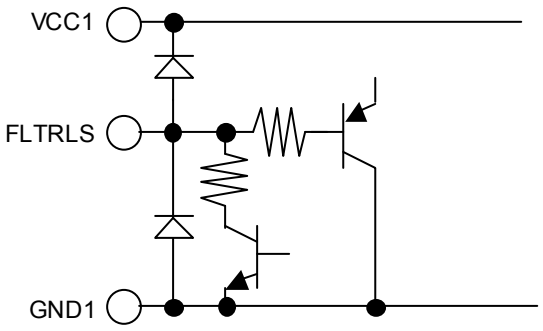
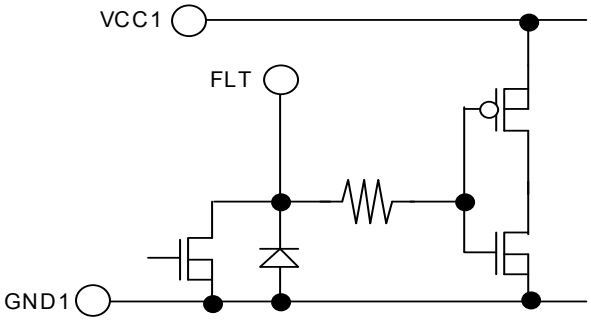
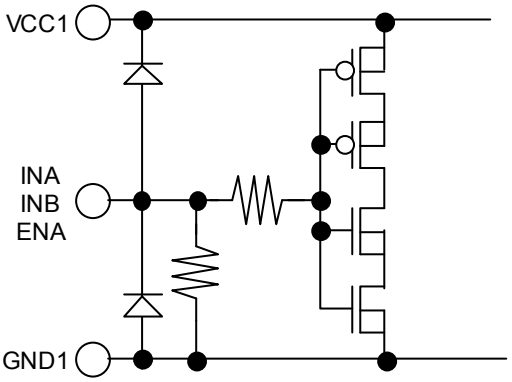
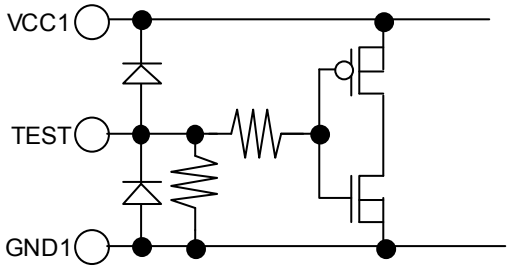


Figure 59. For using 3-pin IGBT (for using DESAT function)

●**I/O equivalence circuits**

Pin No.	Name / Function	I/O equivalence circuits
1	VTSIN Thermal detection pin	
3	VTSTH Thermal detection threshold setting pin	
4	SCPTH Short current detection threshold setting pin	
5	SCPIN Short current detection pin	
6	OUT2 MOS FET control pin for Miller Clamp	
8	OUT1 Output pin	
10	PROOUT Soft turn-off pin	

Pin No.	Name / Function	I/O equivalence circuits
14	FLTRLS Fault output holding time setting pin	
16	FLT Fault output pin	
13	INB Invert / non-invert selection pin	
17	INA Control input pin	
18	ENA Input enabling signal input pin	
19	TEST Test mode setting pin	

●**Power Dissipation**

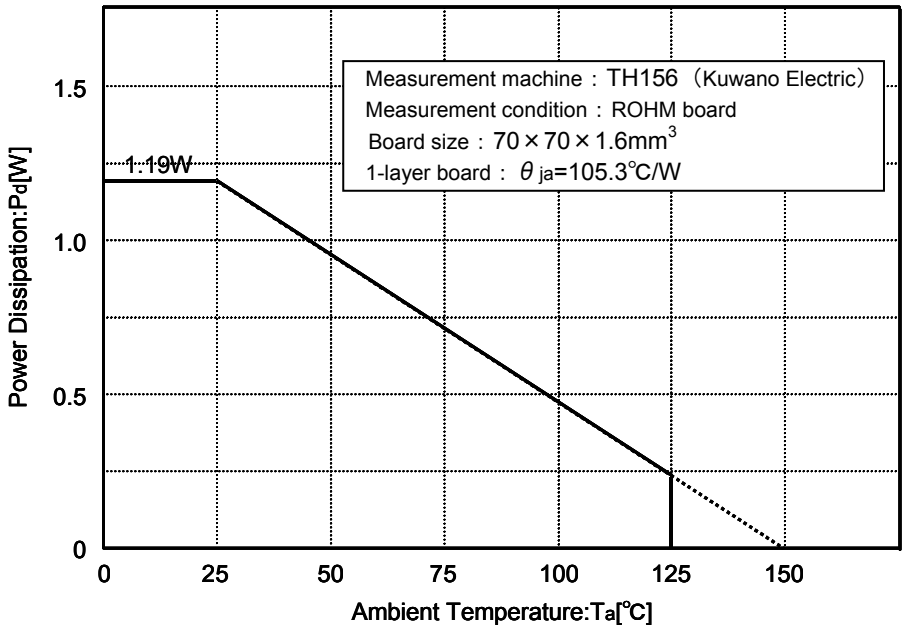


Figure 60. SSOP-B20W Derating Curve

●**Thermal design**

Please confirm that the IC's chip temperature Tj is not over 150℃, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150℃ is exceeded the functions as a semiconductor do not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150℃ must be strictly obeyed under all circumstances.

The IC's consumed power (P) can be estimated roughly with following equation.

$$P = V_{CC1} \cdot I_{CC1} + V_{CC2} \cdot I_{CC2} + I_{ON}^2 \cdot R_{ONH} \cdot t_{ON} \cdot f_{PWM} + I_{OFF}^2 \cdot R_{ONL} \cdot t_{OFF} \cdot f_{PWM}$$

f_{PWM} : PWM frequency
I_{ON} : OUT1 pin outflow current when OUT1 is H state.
t_{ON} : Current outflow time from OUT1 pin when OUT1 is H state.
I_{OFF} : OUT1 pin inflow current when OUT1 is L state.
t_{OFF} : Current inflow time to OUT1 pin when OUT1 is L state.

●**Operational Notes**

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND Potential

The potential of GND1 pin must be minimum potential in all operating conditions. (Input side ; 11pin to 20pin)
The potential of VEE2 pin must be minimum potential in all operating conditions. (Output side ; 1pin to 10pin)

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(7) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(9) Input terminal of IC

Between each element there is a P+ isolation for element partition and a P substrate. This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up.

For example, when the resistance and transistor are connected to the terminal as shown in figure 61,

○When GND＞(Terminal A) at the resistance and GND＞(Terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.

○Also, when GND＞(Terminal B) at the transistor (NPN), The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

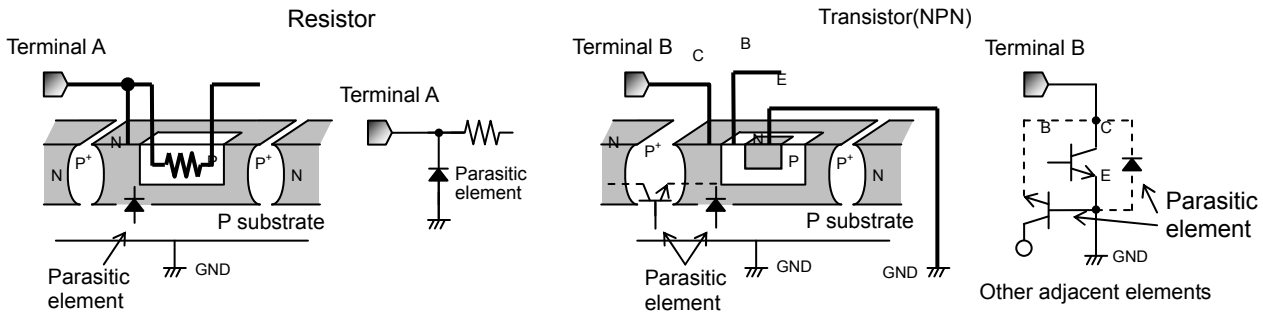


Figure 61. Pattern Diagram of Parasitic Element

(10) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

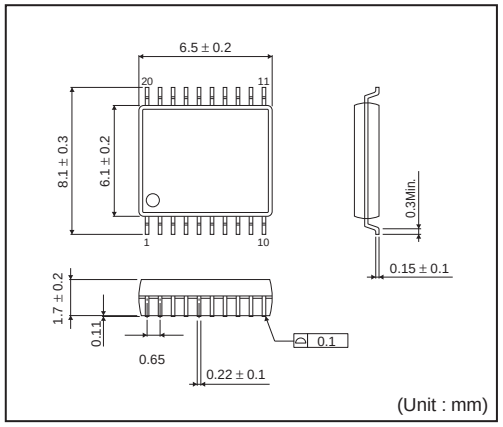
●Ordering Information

B M 6 0 0 1 3 F V	-	CE 2

- Part Number
- Package FV: SSOP-B20W
- Packaging and forming specification E2: Embossed tape and reel

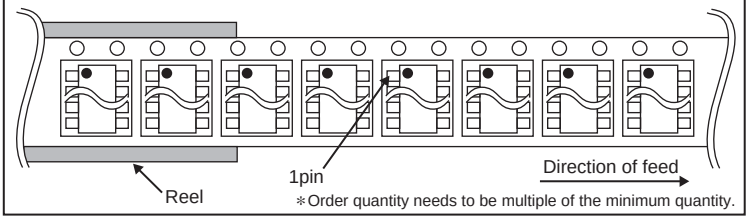
●Physical Dimension Tape and Reel Information

SSOP-B20W



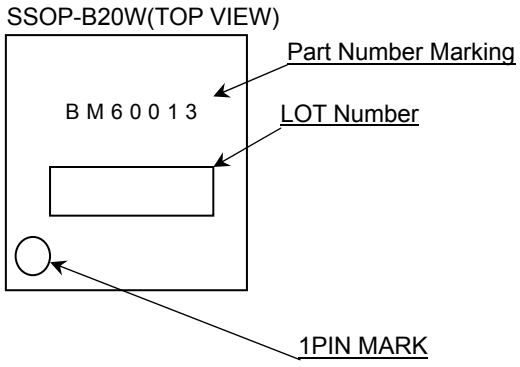
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram



●**Revision History**

Date	Revision	Changes	
8.May.2012	001	New Release	
29.May.2012	002	Page 6	Change Description of functions and examples of constant setting‘4)’ Equation of $t_{BLANKouternal}$.
		Page 24	Delete recommended part number ‘RHK005N03’.
		Page 28	Change Operational Notes‘(9)’

Notice

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2) You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

●Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

●Precaution for Storage / Transportation

1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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