F81867

6 UARTs µSuper IO With 128 Bytes FIFO and Power Saving Functions

Release Date: Dec, 2011
Version: V0.12P

F81867 Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2011/7/13	-	Preliminary
V0.11P	2011/8/24	-	Made Clarification and Correction Add Register Section 7
V0.12P	2011/12/12	-	1. Made Clarification and Correction 2. I2C Protocol Select – Index EFh, bit 3-0 3. Update All Register Reset Type 4. Add Multifunction Registers 5. Add KBC/ACPI Related Description/Timing/ OVP/ AMD TSI/Intel PECI 3.0/ (See Section 6.5 to 6.11) 6. Update Application Circuit (Add Soft Start Circuit to 5VSB)

Table of Content

1. General Description

The F81867 is the featured IO chip with µC based on 8-bit 8032 core & built in 8k*8 flash targeted for Industrial PC system. Equipped with one IEEE 1284 parallel port, 6 UART ports with Multi drop function (9-bit protocol), KBC, SIR, ACPI management function, portable CIR with RC6 and one FDC. Each UART provides 16/32/64/128 bytes FIFO. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems. The F81867 supports the enhanced parallel port (EPP) and the extended capabilities port (ECP). The F81867 supports keyboard and mouse interface which is 8042-based keyboard controller. The F81867 integrated with hardware monitor, 7 sets of voltage sensor, 3 sets of creative auto-controlling smart fans and 2 temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external transistors 2N3906 and one local temperature.

The F81867 provides flexible features for multi-directional application. For instance, supports 72 GPIO pins, IRQ sharing function designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature. Others, the F81867 supports newest Intel PECI 3.0 interfaces for new generational CPU temperature usage, INTEL IBX PEAK, I2C and AMD TSI for temperature reading.

In order to save the current consumption when the system is in the soft off state which is so called power saving function. The power saving function supports the system boot-on not only by pressing the power button but also by the wake-up events via GPIO0x, GPIO1x, RI1#, and RI2#. When the system enters the S3/S4/S5 state, F81867 can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be emulated to G3-like state when the system enters S3/S4/S5 states. At the G3-like state, the F81867 consumes 5VSB power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfill a low power consumption system which supports a wake up function.

These features as above description will help you more and improve the product value. The F81867 is in the package of 128-LQFP. (14mm*14mm)

2. Features

- **General Functions**
  - Comply with LPC 1.1
  - Support ACPI 3.0
  - Built in 8K*8 flash

- 8032 embedded microprocessor
- Support WDT Reset Function
- Support WDT wake up while ERP function is enabled
- Provide 4 sets of GPIO (GPIO0x/1x/5x/8x) SMI event via PME# or SIRQ
- Provide different SIRQ channels for GPIO0x/1x/5x/8x
- Support portable remote control via CIR RC6
- Provide one FDC, KBC and Parallel Port
- Provide 6 fully functional UART and 1 SIR
  - ✓ Programmable 16/32/64/128 bytes FIFO
  - ✓ Multi drop function & 128 Bytes for UARTs
  - ✓ Support IRQ Sharing function.
  - ✓ Provide auto flow control function
- H/W monitor functions
  - ✓ Support OVP & UVP for 3VCC and VIN2&3
  - ✓ Support smart fan FQST for FAN 1
  - ✓ Support PECI 3.0
  - ✓ Support IBX PCH temperature reading via I2C
  - ✓ Support AMD TSI
- 72 GPIO Pins for flexible application
- Provide 16 bytes Serial ID
- Support LED blinking function
- Provide Power Saving Function (Comply ERP lot 6.0)
- Support Intel Deep Sleep Well (DSW) Timing Sequence
- Provide wake-up events via power button, GPIO0x, GPIO1x, RI1#, and RI2#
- Provide ATX emulates AT function
- 14.318/24/48 MHz clock input
- Packaged in 128-LQFP

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and under run conditions
- Built-in address mark detection circuit to simplify the read electronics
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

- **Parallel Port**
  - One PS/2 compatible bi-directional parallel port
  - Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284
  - Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284
  - Enhanced printer port back-drive current protection

- **Hardware Monitor Functions**
  - 2 dual current type (±3°C) thermal inputs for CPU thermal diode and 2N3906 transistors
  - Provide one local temperature
  - Support temperature monitoring via thermistor
  - Temperature range: -60°C~127°C
  - 8 sets voltage monitoring (4 external and 4 internal powers)
  - High limit signal (PME#) for Vcore
  - 3 fan speed monitoring inputs
  - 3 fan speed PWM/DC control outputs
  - FANCTRL 1~3 provides 4 frequency (23.5/11.75/5.875KHz, & 200Hz) select via the registers
  - Issue PME# and OVT# hardware signals output
  - Case intrusion detection circuit

- **Support PECI 3.0**

- **I2C Interface**
  - Support slave interface to report the hardware monitor data
  - Support master interface to get the thermal data via PCH & MXM module

- **Support AMD TSI Interface**

- **Keyboard Controller**
  - compatibility with the 8042
  - Support PS/2 mouse
  - Hardware Gate A20 and Hardware Keyboard Reset
  - Support KB, Mouse wake up and swap function

- **GPIO Function**
  - Total 72 pins GPIO
  - Interrupt status (wake up) support via GPIO0x and GPIO1x
  - Support different SIRQ channels via GPIO0x, GPIO1x, GPIO5x and GPIO8x

- All GPIO supports digit IO for Input/Output control, Output data control, input status.
- Support High/Low Level/Pulse, Open Drain/Push Pull function selection
- All GPIO could be accessed via 3 ways: configuration register port (4E/2E), index/data port and directly access to GPIO only (digital I/O). Please refer to the related register for detail.

Watch Dog Timer

- Time resolution minute/second by option
- Maximum 256 minutes or 256 seconds
- Output signal via WDTRST#/PWROK
- WDT could also wake up via PME#, PSWOUT#

Power Saving Function

- G3-like Timing Control
- Comply With ERP Lot 6.0
- Built in Soft Start Function for Two Control Pins with VSB Power Sources Control.
- Event In via GPIO0x, GPIO1x, RI1#, and RI2#

Support Intel Cougar Point Timing (DSW)

UART

- Provide 6 fully functional UART
- 6 high-speed 16C550/16C650/16C750/16C850 compatible UARTs
- Provide auto flow control function
- Baud rate supports 115.2K, max. up to 1.5M
- Support IRQ 3,4,5,6,7,8,9,10,11 sharing
- Provide Multi drop (9-bits) Function for Gaming Machine
- Support IrDA version 1.0 SIR protocol (Multi with UART 6)
- Support Ring-In Wake Up via RI1# and RI2#

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps (Multi with UART 6)

Provide ATX Emulates AT Function

Provide Serial ID Function

- Provide 16 bytes for fixed Fintek serial ID

- Provide 16 bytes for customer serial ID
  - Use serial ID tool (DOS & Window) to update the customer serial ID

- **Provide Scan Code Function (KB Emulation Key Code)**
  - Support scan code via GPIO81~GPIO87
  - Windows OS can detect the system volume control signal without any driver installation.
  - Support standard KB set 1 commands (except “Pause” key)
  - See register for the detail setting

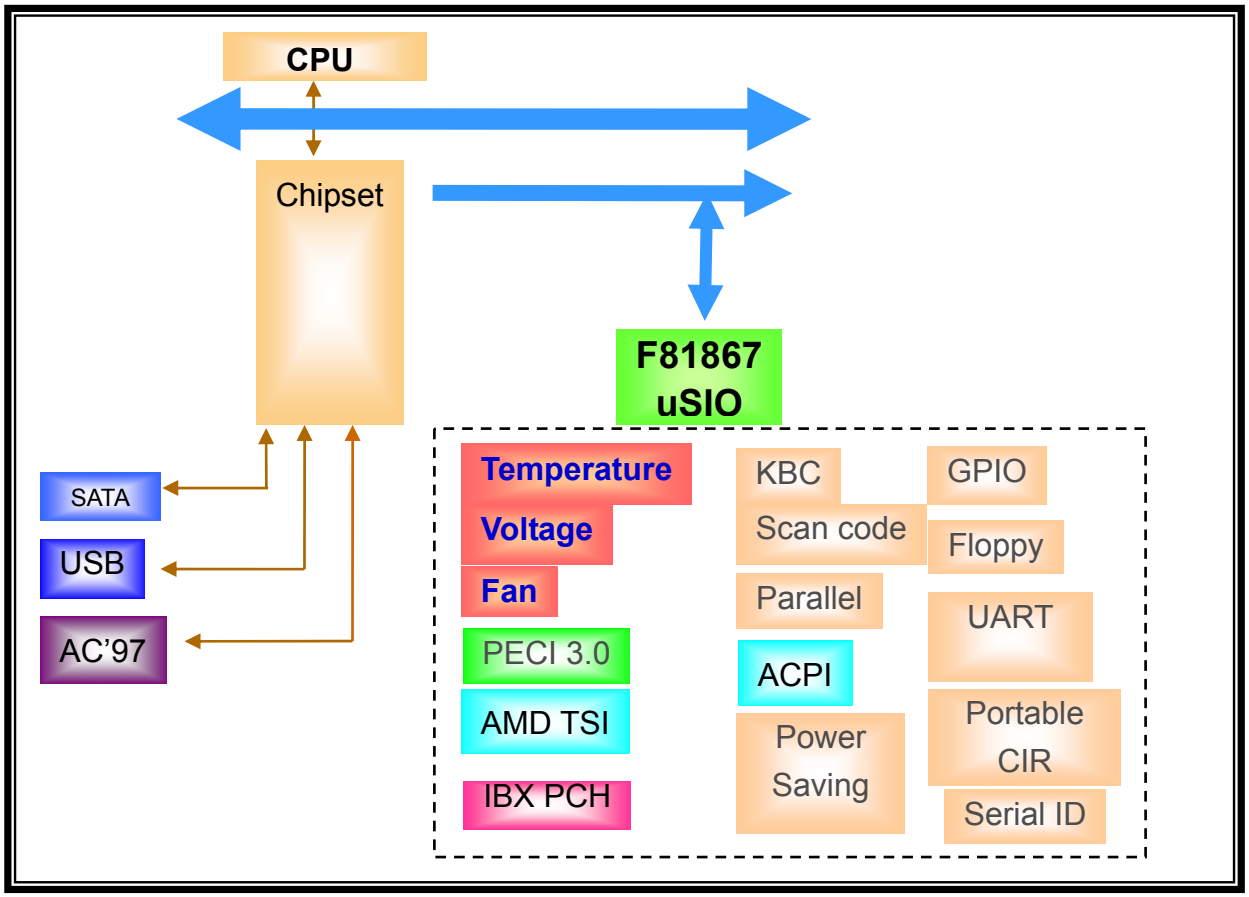
- **CIR**
  - Provide simple functions such as Up/Down/Left/Right/Enter/Power ON/Power OFF
  - Provide simple/portable RC6 remote control commands
  - The commands are based on the standard set 1 (except “Pause” key)

- **8 bit 8032**
  - Built in 8K*8 bits flash
  - Could access GPIO, PWM, hardware monitor, KBC, ACPI & CIR functions

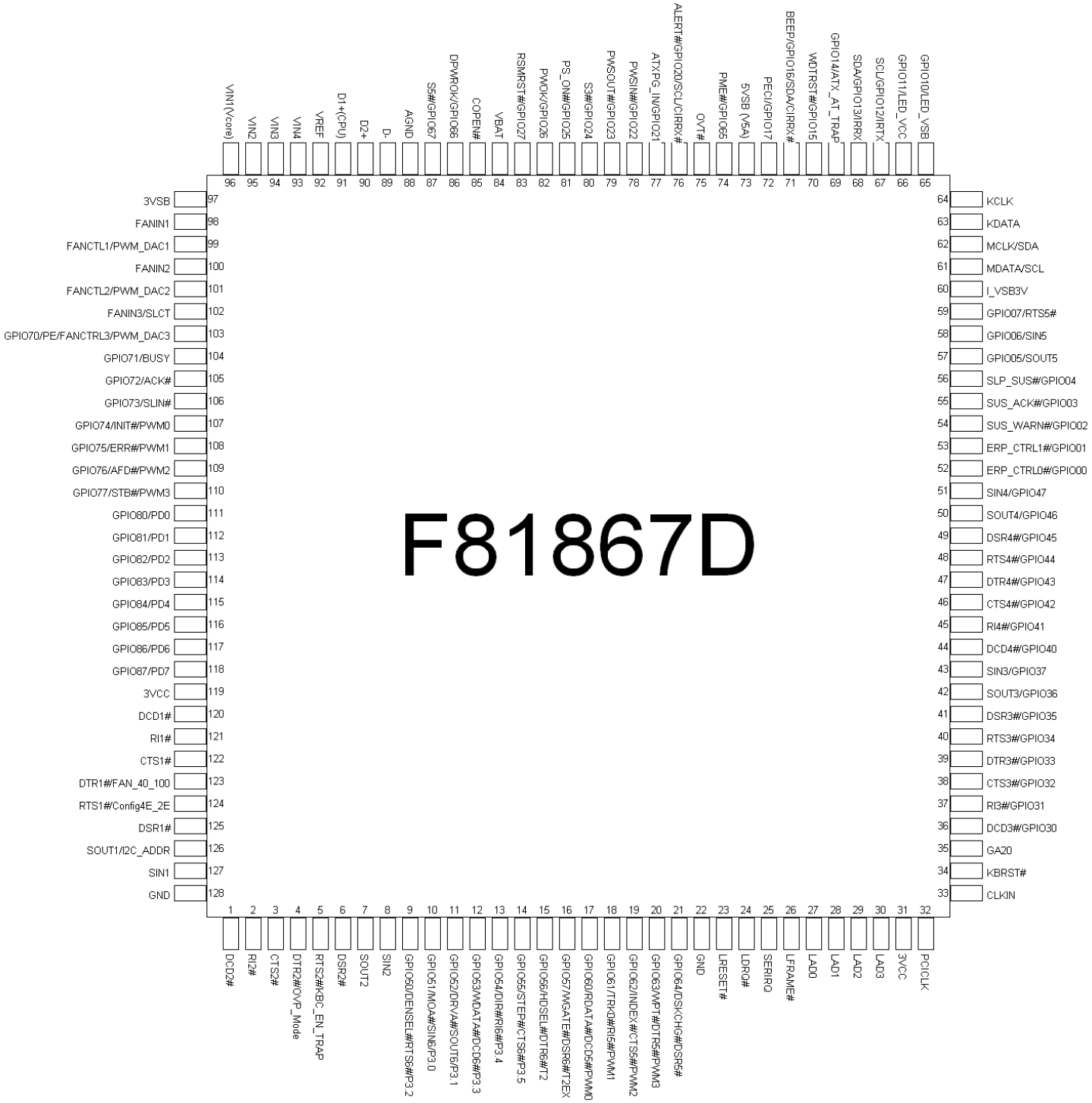
- **Package**
  - 128-pin LQFP (14mm * 14mm) green package

Noted: Patented TW207103 TW207104 TW220442 US6788131 B1 TWI235231 TW237183 TWI263778

3. Block Diagram



4. Pin Configuration



5. Pin Description

I/O_{16st} - TTL level bi-directional pin with schmitt trigger, 16mA source/sink capability.
$I_{lv}/O_{D8, S1v}$ - Low level bi-directional pin. Outupt with 8 mA drive and 1mA sink capability.
$I/OOD_{12st, 5v}$ - TTL level bi-directional pin, output can be selected to open drian or push pull by the register, with 12 mA source/sink capability, 5V tolerance.
$I/OOD_{14st,5v}$ - TTL level bi-directional pin with schmitt trigger, output can be selected to open drian or push pull by the register, with 14 mA source/sink capability, 5V tolerance.
$I/OOD_{8st,5v}$ - TTL level bi-directional pin, output can be selected to open drian or push pull by register, with 8 mA source/sink capability, 5V tolerance.
$I/OD_{16st,5v}$ - TTL level bi-directional pin with schmitt trigger, open drain output with 16 mA sink capability, 5V tolerance.
$OD_{16,u10}$ - Open drain output pin with 16 mA sink capability, pull-up 10kΩ.
$I/O_{12st,5v}$ - TTL level bi-directional pin with schmitt trigger,12 mA sink capability, 5V tolerance.
O_8 - Output pin with 8 mA source/sink capability.
O_{12} - Output pin with 12 mA source/sink capability.
O_{14} - Output pin with 14 mA source/sink capability.
O_{16} - Output pin with 16 mA source/sink capability.
$OOD_{12,5v}$ - Open drian or push pull by the register, with 12 mA source/sink capability, 5V tolerance.
AOUT - Analog output pin.
$OD_{12,5v}$ - Open-drain output pin with 12 mA sink capability, 5V tolerance.
$OD_{14,5v}$ - Open-drain output pin with 14 mA sink capability, 5V tolerance.
$OD_{24t,5v}$ - TTL level Open-drain output pin with 24 mA sink capability, 5V tolerance.
$I/OD_{12st,5v}$ - TTL level bi-directional pin with schmitt trigger, open drain output with 12mA source-sink capability, 5V tolerance.
$I/O_{8st, 5v}$ - TTL level bi-directional pin with schmitt trigger, 8 mA sink capability, 5V tolerance.
$IN_{st,lv}$ - Low voltage, TTL level input pin with schmitt trigger.
$IN_{t,5v}$ - TTL level input pin,5V tolerance.
IN_{st} - TTL level input pin with schmitt trigger.
$IN_{st,5v}$ - TTL level input pin with schmitt trigger, 5V tolerance.
$IN_{t, u47,5v}$ - TTL level input pin, pull-up 47kΩ, 5V tolerance.
AIN - Analog Input pin.
P - Power.

5.1 Power Pin

Pin	Pin Name	Type	Description
31, 119	3VCC	P	Power supply voltage input with 3.3V.
60	I_VSB3V	P	3.3V internal standby power regulates from 5VSB for internal circuit usage. Strongly recommend to place 0.1uF for the compensation.
84	VBAT	P	Battery voltage. Place 1000pF for monitoring.
73	5VSB (V5A)	P	5V standby power supply.
97	3VSB	P	Analog Power with 3.3V standby.
88	AGND	P	Analog GND.
22, 128	GND	P	Digital GND.

5.2 Clock

Pin	Pin Name	Type	PWR	Description
32	PCICLK	IN_{st}	3VCC	33MHz PCI clock input.
33	CLKIN	IN_{st}	3VCC	System clock input. According to the input frequency 14.318/24/48MHz (default 48MHz).

5.3 LPC Interface

Pin	Pin Name	Type	PWR	Description
23	LRESET#	IN_{st}	3VCC	Reset signal. It can connect to PCIRST# signal on the host.
24	LDRQ#	O_{16}	3VCC	Encoded DMA Request signal.
25	SERIRQ	I/O_{16st}	3VCC	Serial IRQ input/Output.
26	LFRAME#	IN_{st}	3VCC	Indicates start of a new cycle or termination of a broken cycle.
27-30	LAD[0:3]	I/O_{16st}	3VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
32	PCICLK	IN_{st}	3VCC	33MHz PCI clock input.
33	CLKIN	IN_{st}	3VCC	System clock input. According to the input frequency 14.318/24/48MHz (default 48MHz).

5.4 FDC

Pin No.	Pin Name	Type	PWR	Description
9	GPIO50	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
	DENSEL#	$OD_{14,5v}$		Drive Density Select. Set to 1 – High data rate.(500Kbps, 1Mbps) Set to 0 – Low data rate. (250Kbps, 300Kbps)
	RTS6#	O_{14}		UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
10	GPIO51	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
	MOA#	$OD_{14,5v}$		Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
	SIN6	$IN_{st,5v}$		UART Serial Input. Used to receive serial data through the communication link.
11	GPIO52	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
	DRVA#	$OD_{14,5v}$		Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
	SOUT6	O_{14}		UART Serial Output. Used to transmit serial data out to the communication link.
12	GPIO53	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
	WDATA#	$OD_{14,5v}$		Write data. This logic low open drain writes pre-compensation serial data to the selected FDD.

				An open drain output.
	DCD6#	$IN_{st,5v}$		Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
13	GPIO54	$I/OOD_{14st,5v}$	3VCC	General Purpose IO.
	DIR#	$OD_{14,5v}$		Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
	RI6#	$IN_{st,5v}$		Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
14	GPIO55	$I/OOD_{14st,5v}$	3VCC	General Purpose IO.
	STEP#	$OD_{14,5v}$		Step output pulses. This active low open drain output produces a pulse to move the head to another track.
	CTS6#	$IN_{st,5v}$		Clear To Send is the modem control input.
15	GPIO56	$I/OOD_{14st,5v}$	3VCC	General Purpose IO.
	HDSEL#	$OD_{14,5v}$		Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
	DTR6#	O_{14}		UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
16	GPIO57	$I/OOD_{14st,5v}$	3VCC	General Purpose IO.
	WGATE#	$OD_{14,5v}$		Write enable. An open drain output.
	DSR6#	$IN_{st,5v}$		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
17	GPIO60	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
	RDATA#	$IN_{st,5v}$		The read data input signal from the FDD.
	DCD5#	$IN_{st,5v}$		Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	PWM 0	$OOD_{14st,5v}$		PWM0 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and backlight brightness control.
18	GPIO61	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
	TRK0#	$IN_{st,5v}$		Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
	RI5#	$IN_{st,5v}$		Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	PWM 1	OOD_{12}		PWM1 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and

				backlight brightness control.
19	GPIO62	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
	INDEX#	$IN_{st,5v}$		This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
	CTS5#	$IN_{st,5v}$		Clear To Send is the modem control input.
	PWM 2	OOD_{12}		PWM2 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and backlight brightness control.
20	GPIO63	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
	WPT#	$IN_{st,5v}$		Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
	DTR5#	O_{12}		UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	PWM 3	OOD_{12}		PWM3 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and backlight brightness control.
21	GPIO64	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
	DSKCHG#	$IN_{st,5v}$		Diskette change. This signal is active low at power on and whenever the diskette is removed.
	DSR5#	$IN_{st,5v}$		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.

5.5 Parallel Port (LPT Port)

Pin No.	Pin Name	Type	PWR	Description
102	FANIN3	$IN_{st,5v}$	3VCC	Fan 3 tachometer input.
	SLCT	$IN_{st,5v}$		An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
103	GPIO70	$I/OOD_{12st, 5v}$	3VCC	General purpose IO.
	PE	$IN_{st,5v}$		An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	FANCTL3	$OOD_{12,5v}$ AOUT		Fan 3 control output. This pin provides PWM duty-cycle output or a DAC voltage output.
	PWM _DAC3	$IN_{st,5v}$		Power on Strapping pin: 1: PWM mode. 0: Default is DAC mode for FANCTL3 (internal pull

				down 100kΩ).
104	GPIO71	$I/OOD_{12st, 5v}$	3VCC	General purpose IO.
	BUSY	$IN_{st,5v}$		An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
105	GPIO72	$I/OOD_{12st, 5v}$	3VCC	General purpose IO.
	ACK#	$IN_{st,5v}$		An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
106	GPIO73	$I/OOD_{12st, 5v}$	3VCC	General purpose IO.
	SLIN#	$I/OOD_{12st,5v}$		Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
107	GPIO74	$I/OOD_{12st, 5v}$	3VCC	General purpose IO.
	INIT#	$I/OOD_{12st,5v}$		Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	PWM0	$OOD_{12st, 5v}$		PWM0 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and backlight brightness control.
108	GPIO75	$I/OOD_{12st, 5v}$	3VCC	General purpose IO.
	ERR#	$IN_{st,5v}$		An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	PWM1	$OOD_{12st, 5v}$		PWM1 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and backlight brightness control.
109	GPIO76	$I/OOD_{12st, 5v}$	3VCC	General purpose IO.
	AFD#	$I/OOD_{12st,5v}$		An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	PWM2	$OOD_{12st, 5v}$		PWM2 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and backlight brightness control.

110	GPIO77	I/$OOD_{12st, 5v}$	3VCC	General purpose IO.
	STB#	I/$OOD_{12st,5v}$		An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	PWM3	$OOD_{12st, 5v}$		PWM3 Output where its frequency range is 183Hz~46.875KHz. It can support various applications such as manual fan control, and backlight brightness control.
111	GPIO80	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD0	$I/O_{12st,5v}$		Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
112	GPIO81	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD1	$I/O_{12st,5v}$		Parallel port data bus bit 1.
113	GPIO82	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD2	$I/O_{12st,5v}$		Parallel port data bus bit 2.
114	GPIO83	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD3	$I/O_{12st,5v}$		Parallel port data bus bit 3.
115	GPIO84	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD4	$I/O_{12st,5v}$		Parallel port data bus bit 4.
116	GPIO85	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD5	$I/O_{12st,5v}$		Parallel port data bus bit 5.
117	GPIO86	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD6	$I/O_{12st,5v}$		Parallel port data bus bit 6.
118	GPIO87	I/$OOD_{12st, 5v}$	3VCC	General purpose IO. Support scan code function.
	PD7	$I/O_{12st,5v}$		Parallel port data bus bit 7.

5.6 Hardware Monitor

Pin	Pin Name	Type	PWR	Description
71	BEEP	$OD_{24t,5v}$	I_VSB3V	Beep pin.
	GPIO16	I/$OOD_{12st,5v}$		General purpose IO.
	SDA	$I_{LV}/OD_{12st,5v}$		I2C Interface DATA pin. AMD TSI & Intel PCH (IBX Peak) data pin.
	CIRRX#	$IN_{st,5v}$		CIR receiver input.
72	PECI	I_{lv} /$O_{D8, S1}$	I_VSB3V	PECI interface pin.
	GPIO17	I/$OOD_{12st,5v}$		General purpose IO.
75	OVT#	$OD_{12,5v}$	I_VSB3V	Over temperature signal output.
76	ALERT#	$OD_{12,5v}$	I_VSB3V	Alert a signal when temperature over limit setting.
	GPIO20	I/$OOD_{24st,5v}$		General purpose IO.
	SCL	$I_{LV}/OD_{24st,5v}$		I2C interface Clock. Clock output for AMD TSI & Intel PCH (IBX Peak).
	CIRRX#	$IN_{st,5v}$		CIR receiver input.
85	COPEN#	$IN_{st,5v}$	VBAT	Case Open Detection #. This pin is connected to

				a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.
89	D-	AIN	3VSB	Analog GND for thermal diode/transistor temperature.
90	D2+	AIN	3VSB	Thermal diode/transistor temperature sensor input.
91	D1+(CPU)	AIN	3VSB	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
92	VREF	AOUT	3VSB	Voltage reference output.
93	VIN4	AIN	3VSB	Voltage Input 4.
94	VIN3	AIN	3VSB	Voltage Input 3. Support OVP & UVP function, and default is disable alarm mode.
95	VIN2	AIN	3VSB	Voltage Input 2. Support OVP & UVP function, and default is disable alarm mode.
96	VIN1 (Vcore)	AIN	3VSB	Voltage Input for Vcore.
98	FANIN1	$IN_{st,5v}$	3VCC	Fan 1 tachometer input.
99	FANCTL1	$OOD_{12,5v}$ AOUT	3VCC	Fan 1 control output. This pin provides PWM duty-cycle output or a DAC voltage output (internal pull down 100kΩ, default).
	PWM _DAC1	$IN_{st,5v}$		Power on Strapping pin: 1: PWM mode. 0: Default is DAC mode for FANCTL1 (internal pull down 100kΩ).
100	FANIN2	$IN_{st,5v}$	3VCC	Fan 2 tachometer input.
101	FANCTL2	$OOD_{12,5v}$ AOUT	3VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a DAC voltage output (internal pull down 100kΩ, default).
	PWM _DAC2	$IN_{st,5v}$		Power on Strapping pin: 1: PWM mode. 0: Default is DAC mode for FANCTL2 (internal pull down 100kΩ).

5.7 KBC Function

Pin No.	Pin Name	Type	PWR	Description
34	KBRST#	$OD_{16,u10}$	3VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10kΩ.
35	GA20	$OD_{16,u10}$	3VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10kΩ.
63	KDATA	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Keyboard Data.
64	KCLK	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Keyboard Clock.
61	MDATA	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Mouse Data.
	SCL	$I_{lv}/OD_{16st,\ 5v}$		I2C Interface CLOCK pin. Clock output for AMD TSI & Intel PCH (IBX Peak).
62	MCLK	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Mouse Clock.

	SDA	$I_{lv}/OD_{16st,\ 5v}$		I2C Interface DATA pin. AMD TSI & Intel PCH (IBX Peak) data pin.

5.8 ACPI, ERP

Pin	Pin Name	Type	PWR	Description
52	ERP_CTRL0#	$OD_{12,5V}$	I_VSB3V	Standby power rail control pin 0. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
	GPIO00	$I/OOD_{12st,5v}$		General purpose IO.
53	ERP_CTRL1#	$OD_{12,5V}$	I_VSB3V	Standby power rail control pin 1. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
	GPIO01	$I/OOD_{12st,5v}$		General purpose IO.
54	SUS_WARN#	IN_{st}	I_VSB3V	This pin asserts low when the PCH is planning to enter the DSW power state. It can detect 5VDUAL level with delay setting supported. The delay time is 1ms~8S (default 4s)
	GPIO02	$I/OOD_{12st,5v}$		General purpose IO.
55	SUS_ACK#	$OD_{12,5v}$	I_VSB3V	This pin must wait SUSWARN# signal for entering DSW power state.
	GPIO03	$I/OOD_{12st,5v}$		General purpose IO.
56	SLP_SUS#	$IN_{st,lv}$	I_VSB3V	This pin asserts low which comes from PCH to shut off suspend power rails externally to enhance power saving function.
	GPIO04	$I/OOD_{12st,5v}$		General purpose IO.
57	GPIO05	$I/OOD_{12st,5v}$	I_VSB3V	General purpose IO.
	SOUT5	O_{12}		UART Serial Output. Used to transmit serial data out to the communication link.
58	GPIO06	$I/OOD_{12st,5v}$	I_VSB3V	General purpose IO.
	SIN5	$IN_{t,5v}$		UART Serial Input. Used to receive serial data through the communication link.
59	GPIO07	$I/OOD_{12st,5v}$	I_VSB3V	General purpose IO.
	RTS5#	O_{12}		UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
65	GPIO10	$I/OOD_{12st,5v}$	I_VSB3V	General purpose IO.
	LED_VSB	$OOD_{12,5V}$		Power LED for VSB.
66	GPIO11	$I/OOD_{12st,5v}$	I_VSB3V	General purpose IO.
	LED_VCC	$OOD_{12,5V}$		Power LED for VCC.
67	SCL	$I_{lv}/OD_{12st,\ 5v}$	I_VSB3V	I2C Interface CLOCK pin. Clock output for AMD TSI & Intel PCH (IBX Peak).

	GPIO12	I/OOD$_{12st,5v}$		General purpose IO.
	IRTX	O$_{12}$		Infrared Transmitter Output. UART 6 can't be used if this function is valid.
68	SDA	I$_{Iv}$/OD$_{12st,\ 5v}$	I_VSB3V	I2C Interface DATA pin. AMD TSI & Intel PCH (IBX Peak) data pin.
	GPIO13	I/OOD$_{12st,5v}$		General purpose IO.
	IRRX	IN$_{st,5v}$		Infrared Receiver input. UART 6 can't be used if this function is valid.
69	GPIO14	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
	ATX_AT_TRAP	IN$_{t,5v}$		Power on trapping: ATX emulates AT function 1: ATX mode (Default, internal pull high 47kΩ). 0: AT mode.
70	WDTRST#	OD$_{12,5v}$	I_VSB3V	Watch dog timer signal output.
	GPIO15	I/OOD$_{12st,5v}$		General purpose IO.
74	PME#	OD$_{12,5v}$	I_VSB3V	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up.
	GPIO65	I/OOD$_{12st,5v}$		General purpose IO.
77	ATXPG_IN	IN$_{st,5v}$	I_VSB3V	ATX Power Good input.
	GPIO21	I/OOD$_{12st,5v}$		General purpose IO.
78	PWSIN#	IN$_{st,5v}$	I_VSB3V	Main power switch button input.
	GPIO22	I/OOD$_{12st,5v}$		General purpose IO.
79	PWSOUT#	OD$_{12,5V}$	I_VSB3V	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
	GPIO23	I/OOD$_{12st,5v}$		General purpose IO.
80	S3#	IN$_{st,5v}$	I_VSB3V	S3# Input is Main power on-off switch input.
	GPIO24	I/OOD$_{12st,5v}$		General purpose IO.
81	PS_ON#	OD$_{12,5v}$	I_VSB3V	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
	GPIO25	I/OOD$_{12st,5v}$		General purpose IO.
82	PWROK	OD$_{12,5V}$	VBAT	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V.
	GPIO26	I/OD$_{12st,5v}$		General purpose IO.
83	RSMRST#	OD$_{12,5V}$	VBAT	Resume Reset# function, It is power good signal of 3VSB, which is delayed 66ms as 3VSB arrives at 2.8V.
	GPIO27	I/OD$_{12st,5v}$		General purpose IO.
86	DPWROK	OD$_{12,5v}$	VBAT	It is power good signal of 5VSB which is delayed 66ms as 5VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.
	GPIO66	I/OD$_{12st,5v}$		General purpose IO.
87	S5#	IN$_{st,5v}$	I_VSB3V	S5# input. This pin companies with S3# to indicate the operating state from S0 to S3 and S4/S5 sleep states.
	GPIO67	I/OD$_{12st,5v}$		General purpose IO.

5.9 UART, SIR

Pin	Pin Name	Type	PWR	Description
1	DCD2#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
2	RI2#	$IN_{st,5v}$	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. Support wake up function.
3	CTS2#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
4	DTR2#	O_8	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	OVP_Mode	$IN_{t,u47,\ 5v}$		Power on Strapping pin for over voltage protection (OVP). 1: Default is disabled; internal pull high 47kΩ. Voltage protection function is enabled via setting the related registers. 0: Enable OVP function.
5	RTS2#	O_8	3VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	KBC_EN_TRAP	$IN_{t,u47,\ 5v}$		Power on Strapping pin 1: KBC enable (Default, internal pull high 47kΩ). 0: KBC disable.
6	DSR2#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	SOUT2	O_8	3VCC	UART Serial Output. Used to transmit serial data out to the communication link.
8	SIN2	$IN_{st,5v}$	3VCC	UART Serial Input. Used to receive serial data through the communication link.
36	DCD3#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	GPIO30	$I/OOD_{8st,\ 5v}$		General Purpose IO.
37	RI3#	$IN_{st,,5v}$	3VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	GPIO31	$I/OOD_{8st,\ 5v}$		General Purpose IO.
38	CTS3#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
	GPIO32	$I/OOD_{8st,\ 5v}$		General Purpose IO.
39	DTR3#	O_8	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	GPIO33	$I/OOD_{8st,\ 5v}$		General Purpose IO.

40	RTS3#	O_8	3VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	GPIO34	$I/OOD_{8st, 5v}$		General Purpose IO.
41	DSR3#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
	GPIO35	$I/OOD_{8st, 5v}$		General Purpose IO.
42	SOUT3	O_8	3VCC	UART Serial Output. Used to transmit serial data out to the communication link.
	GPIO36	$I/OOD_{8st, 5v}$		General Purpose IO.
43	SIN3	$IN_{st,5v}$	3VCC	UART Serial Input. Used to receive serial data through the communication link.
	GPIO37	$I/OOD_{8st, 5v}$		General Purpose IO.
44	DCD4#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	GPIO40	$I/OOD_{8st, 5v}$		General Purpose IO.
45	RI4#	$IN_{st,5v}$	3VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	GPIO41	$I/OOD_{8st, 5v}$		General Purpose IO.
46	CTS4#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
	GPIO42	$I/OOD_{8st, 5v}$		General Purpose IO.
47	DTR4#	O_8	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	GPIO43	$I/OOD_{8st, 5v}$		General Purpose IO.
48	RTS4#	O_8	3VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	GPIO44	$I/OOD_{8st, 5v}$		General Purpose IO.
49	DSR4#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
	GPIO45	$I/OOD_{8st, 5v}$		General Purpose IO.
50	SOUT4	O_8	3VCC	UART Serial Output. Used to transmit serial data out to the communication link.
	GPIO46	$I/OOD_{8st, 5v}$		General Purpose IO.
51	SIN4	$IN_{st,5v}$	3VCC	UART Serial Input. Used to receive serial data through the communication link.
	GPIO47	$I/OOD_{8st, 5v}$		General Purpose IO.
120	DCD1#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
121	RI1#	$IN_{st,5v}$	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data

				set. Support wake up function.
122	CTS1#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
123	DTR1#	O_8	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	FAN_40_100	$IN_{t,u47,5v}$	3VCC	Power on strapping pin: 1(Default): (Internal pull high 47kΩ) Power on fan speed default duty is 40%.(PWM) 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
124	RTS1#	O_8	3VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	Config4E_2E	$IN_{t,u47,5v}$	3VCC	Power on strapping: 1(internal pull high 47kΩ,Default) Configuration register:4E/4F 0 Configuration register:2E/2F
125	DSR1#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
126	SOUT1	O_8	3VCC	UART Serial Output. Used to transmit serial data out to the communication link.
	I2C_ADDR	$IN_{t,u47,5v}$		Power on strapping pin: 1: (internal pull high 47kΩ, default) Power on I2C slave address is 0x5C. 0: (external pull down) Power on I2C slave address is 0x5A.
127	SIN1	$IN_{st,5v}$	3VCC	UART Serial Input. Used to receive serial data through the communication link.

6. Function Description

6.1 Power on Strapping Option

The F81867 provides eight pins for power on hardware strapping to select required functions. See below table for the detail:

Pin No.	Symbol	Value	Description
4	OVP_Mode	1	Disable (default): internal pull high 47k Ω . Voltage protection function is enabled via setting the related registers.
		0	Enable OVP function.
69	ATX_AT_TRAP	1	ATX mode (default, internal pull high 47kΩ).
		0	AT mode.
99	PWM_DAC1	1	PWM mode.
		0	DAC mode (default, internal pull down 100kΩ)
101	PWM_DAC2	1	PWM mode.
		0	DAC mode (default, internal pull down 100kΩ)
103	PWM_DAC3	1	PWM mode.
		0	DAC mode (default, internal pull down 100kΩ)
123	FAN40_100	1	Power on fan speed default duty is 40%. (Default)
		0	Power on fan speed default duty is 100%.
124	Config4E_2E	1	Configuration Register I/O port is 4E/4F. (Default)
		0	Configuration Register I/O port is 2E/2F.
126	I2C_ADDR	1	The I2C slave address is 0X5C (Default)
		0	The I2C slave address is 0X5A

6.2 FDC

The Floppy Disk Controller provides the interface between a host processor and one floppy disk drive. It integrates a controller and a digital data separator with write pre-compensation, data rate selection logic, microprocessor interface, and a set of registers. The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, 1 Mbps and 2 Mbps. It operates in PC/AT mode.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD.

6.3 Parallel Port

The parallel port in F81867 supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP) mode. Refer to the configuration registers for more information on selecting the mode of operation.

The below content is about the Parallel Port device register descriptions. All the registers are for software porting reference.

Parallel Port Data Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	DATA	R/W	00h	The output data to drive the parallel port data lines.

ECP Address FIFO Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	ECP_AFIFO	R/W	00h	Access only in ECP Parallel Port Mode and the ECP_MODE programmed in the Extended Control Register is 011. The data written to this register is placed in the FIFO and tagged as an Address/RLE. It is auto transmitted by the hardware. The operation is only defined for forward direction. It divide into two parts : Bit 7 : 0: bits 6-0 are run length, indicating how many times the next byte to appear (0 = 1time, 1 = 2times, 2 = 3times and so on). 1: bits 6-0 are ECP address. Bit 6-0 : Address or RLE depends on bit 7.

Device Status Register — Base + 1

Bit	Name	R/W	Default	Description
7	BUSY_N	R	-	Inverted version of parallel port signal BUSY.
6	ACK_N	R	-	Version of parallel port signal ACK#.
5	PERROR	R	-	Version of parallel port signal PE.
4	SELECT	R	-	Version of parallel port signal SLCT.
3	ERR_N	R	-	Version of parallel port signal ERR#.
2-1	Reserved	R	11	Reserved. Return 11b when read.
0	TMOUT	R	-	This bit is valid only in EPP mode. Return 1 when in other modes. It indicates that a 10uS time out has occurred on the EPP bus. 0: no time out error. 1: time out error occurred, write 1 to clear.

Device Control Register — Base + 2

Bit	Name	R/W	Default	Description
7-6	Reserved	-	11	Reserved. Return 11b when read.

5	DIR	R/W	0	0: the parallel port is in output mode. 1: the parallel port is in input mode. It is auto reset to 1 when in SPP mode.
4	ACKIRQ_EN	R/W	0	Enable an interrupt at the rising edge of ACK#.
3	SLIN	R/W	0	Inverted and then drives the parallel port signal SLIN#. When read, the status of inverted SLIN# is return.
2	INIT_N	R/W	0	Drives the parallel port signal INIT#. When read, the status of INIT# is return.
1	AFD	R/W	0	Inverted and then drives the parallel port signal AFD#. When read, the status of inverted AFD# is return.
0	STB	R/W	0	Inverted and then drives the parallel port signal STB#. When read, the status of inverted STB# is return.

EPP Address Register — Base + 3

Bit	Name	R/W	Default	Description
7-0	EPP_ADDR	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Address Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Address Read protocol.

EPP Data Register — Base + 4 – Base + 7

Bit	Name	R/W	Default	Description
7-0	EPP_DATA	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Data Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Data Read protocol.

Parallel Port Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	C_FIFO	R/W	00h	Data written to this FIFO is auto transmitted by the hardware to the device by using standard parallel port protocol. It is only valid in ECP and the ECP_MODE is 010b.The operation is only for forward direction.

ECP Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	ECP_DFIFO	R/W	00h	Data written to this FIFO when DIR is 0 is auto transmitted by the hardware to the device by using ECP parallel port protocol. Data is auto read from device into the FIFO when DIR is 1 by the hardware by using ECP parallel port protocol. Read the FIFO will return the content to the system. It is only valid in ECP and the ECP_MODE is 011b.

ECP Test FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	T_FIFO	R/W	00h	Data may be read, written from system to the FIFO in any Direction. But no hardware handshake occurred on the parallel port lines. It could be used to test the empty, full and threshold of the FIFO. It is only valid in ECP and the ECP_MODE is 110b.

ECP Configuration Register A — Base + 400h

Bit	Name	R/W	Default	Description
7	IRQ_MODE	R	0	0: interrupt is ISA pulse. 1: interrupt is ISA level. Only valid in ECP and ECP_MODE is 111b.
6-4	IMPID	R	001	000: the design is 16-bit implementation. 001: the design is 8-bit implementation (default). 010: the design is 32-bit implementation. 011-111: Reserved. Only valid in ECP and ECP_MODE is 111b.
3	Reserved	-	-	Reserved.
2	BYTETRAN_N	R	1	0: when transmitting there is 1 byte waiting in the transceiver that does not affect the FIFO full condition. 1: when transmitting the state of the full bit includes the byte being transmitted. Only valid in ECP and ECP_MODE is 111b.
1-0	Reserved	R	00	Return 00 when read. Only valid in ECP and ECP_MODE is 111b.

ECP Configuration Register B — Base + 401h

Bit	Name	R/W	Default	Description
7	COMP	R	0	0: only send uncompressed data. 1: compress data before sending. Only valid in ECP and ECP_MODE is 111b.
6	Reserved	R	1	Reserved. Return 1 when read. Only valid in ECP and ECP_MODE is 111b.
5-3	ECP_IRQ_CH	R	001	000: the interrupt selected with jumper. 001: select IRQ 7 (default). 010: select IRQ 9. 011: select IRQ 10. 100: select IRQ 11 101: select IRQ 14. 110: select IRQ 15. 111: select IRQ 5. Only valid in ECP and ECP_MODE is 111b.
2-0	ECP_DMA_CH	R	011	Return the DMA channel of ECP parallel port. Only valid in ECP and ECP_MODE is 111b.

Extended Control Register — Base + 402h

Bit	Name	R/W	Default	Description
7-5	ECP_MODE	R/W	000	000: SPP Mode. 001: PS/2 Parallel Port Mode. 010: Parallel Port Data FIFO Mode. 011: ECP Parallel Port Mode. 100: EPP Mode. 101: Reserved. 110: Test Mode. 111: Configuration Mode. Only valid in ECP.
4	ERRINTR_EN	R/W	0	0: disable the interrupt generated on the falling edge of ERR#. 1: enable the interrupt generated on the falling edge of ERR#.
3	DAMEN	R/W	0	0: disable DMA. 1: enable DMA. DMA starts when SERVICEINTR is 0.
2	SERVICEINTR	R/W	1	0: enable the following case of interrupt. DMAEN = 1: DMA mode. DMAEN = 0, DIR = 0: set to 1 whenever there are writeIntrThreshold or more bytes are free in the FIFO. DMAEN = 0, DIR = 0: set to 1 whenever there are readIntrThreshold or more bytes are valid to be read in the FIFO.
1	FIFOFULL	R	0	0: The FIFO has at least 1 free byte. 1: The FIFO is completely full.
0	FIFOEMPTY	R	0	0: The FIFO contains at least 1 byte. 1: The FIFO is completely empty.

6.4 Hardware Monitor

6.4.1 General Description

Voltage

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3Vcc is an exception for it is main power of the F81867. Therefore 3Vcc can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F81867 and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150KΩ, so that the internal reduced voltage is half of +3.3V (See figure 7-1).

There are four voltage inputs in the F81867 and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example.

If we choose R1=20K, R2=2K, the exact input voltage for V+12v will be 1.09V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

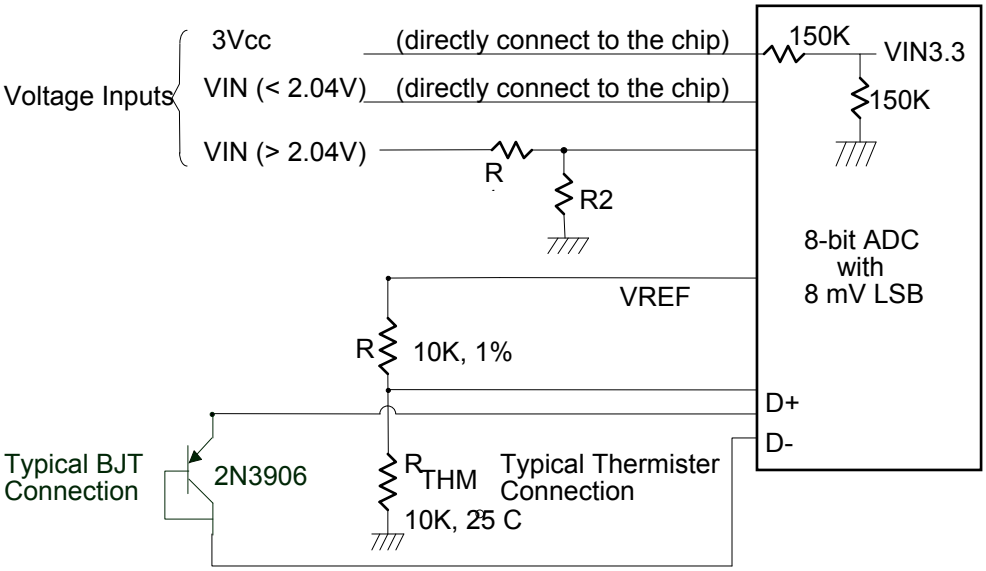
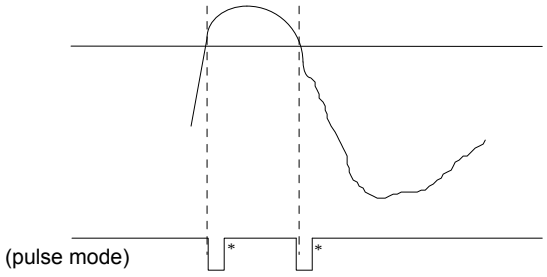


Fig 7-1

PME# interrupt for voltage is shown as figure 7-2. Voltage exceeding or going below high limit will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Voltage PME# Mode

Fig 7-2

Temperature Sensor

The F81867 monitors two remote temperature sensors. These sensors can be measured from -60°C to 127°C for thermal diode & thermistor. More detail please refers to the register description.

Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

(1) Monitor Temperature from "thermistor"

The F81867 can connect two thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) β value is 3435K (2) resistor value is 10KΩ at 25°C. In the Figure 7-1, the thermistor is connected by a serial resistor with 10KΩ, then connected to VREF.

(2) Monitor Temperature from "thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F81867 is capable to these situations. The build-in reference table is for PNP 2N3906 transistor. In the Figure 7-1, the transistor is directly connected into temperature pins.

ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF or 3300pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Over Temperature Signal (OVT#)

OVT# alert for temperature is shown as figure 7-3. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

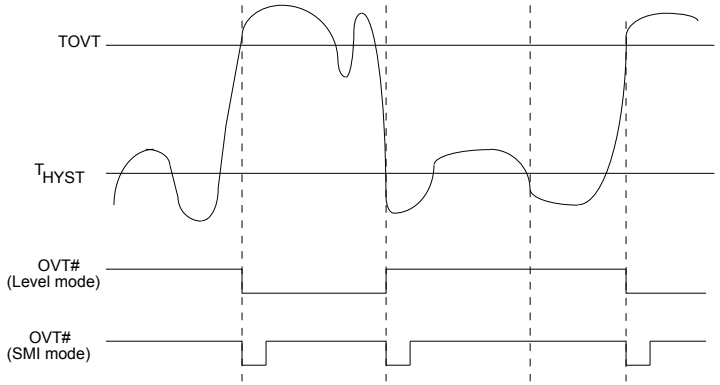
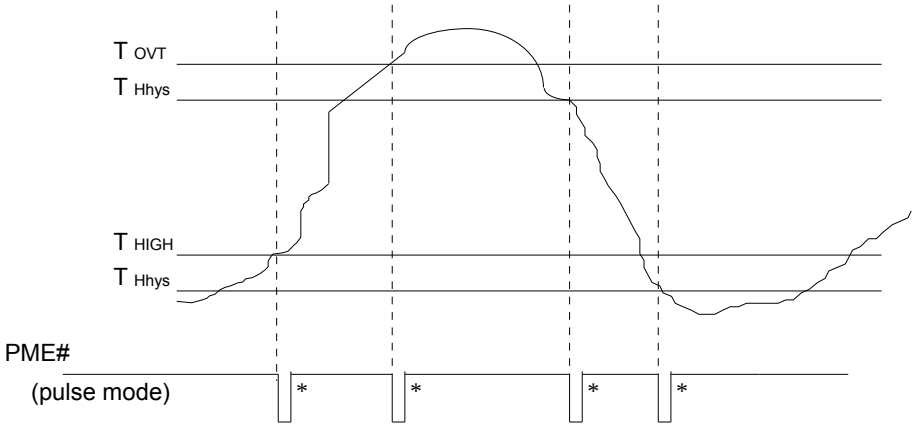


Fig 7-3

Temperature PME#

PME# interrupt for temperature is shown as figure 7-4. Temperature exceeding high limit or going below hysteresis will cause an interrupt if the previous interrupt has been reset by writing

"1" all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Fig 7-4

Fan

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$\text{Count} = \frac{1.5 \times 10^6}{\text{RPM}}$$

In other words, the fan speed counter (12 bit resolution) has been read from register, the fan speed can be evaluated by the following equation.

$$\text{RPM} = \frac{1.5 \times 10^6}{\text{Count}}$$

As for fan, it would be best to use 2 pulses (4 phases fan) tachometer output per round. So the parameter "Count" under 5 bit filter is 4096~64 and RPM is 366~23438 based on the above equation. If using 8 phases fan, RPM would be from 183~11719.

Fan speed control

The F81867 provides 2 fan speed control methods:

1. DAC FAN CONTROL 2. PWM DUTY CYCLE

DAC Fan Control

The range of DC output is 0~VCC, controlled by 8-bit register. 1 LSB is about 0.013V (VCC=3.3V). The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = \text{VCC} \times \frac{\text{Programmed 8bit Register Value}}{256}$$

And the suggested application circuit for linear fan control would be:

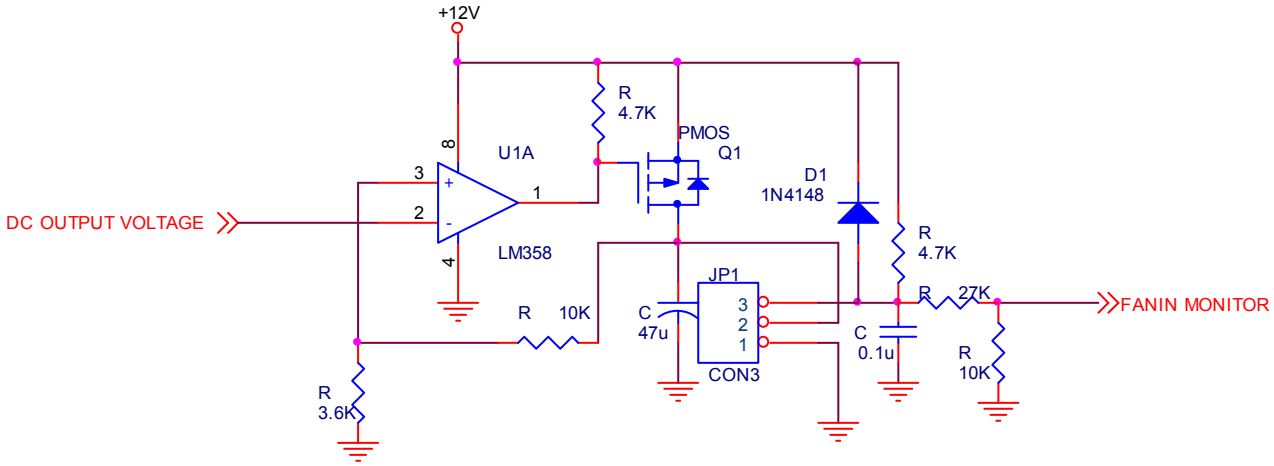


Fig 7-5

PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

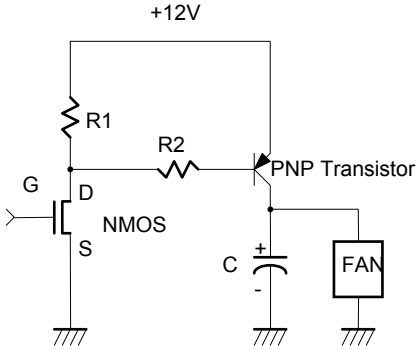


Fig 7-6

Fan speed control mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2. Auto mode (Stage & Linear). More detail, please refer to the description of registers & below figure.

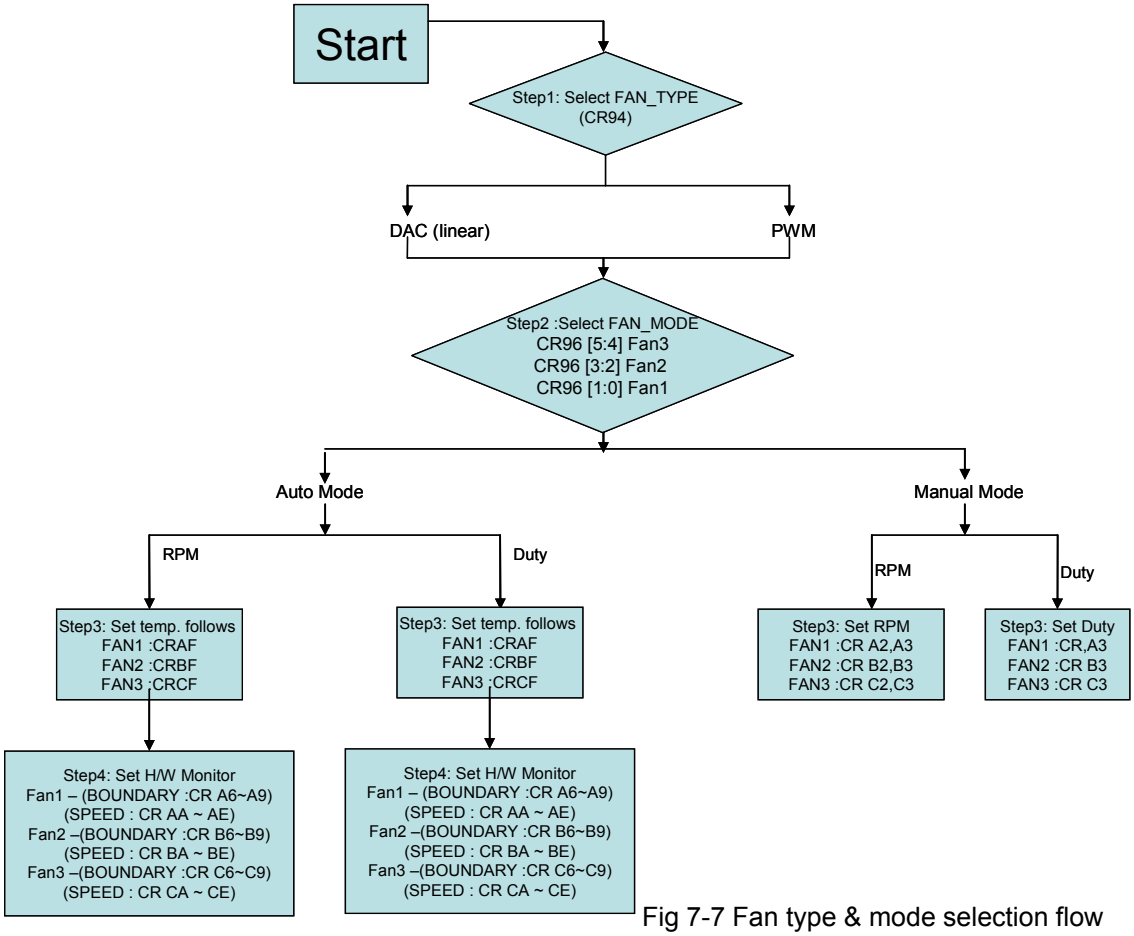


Fig 7-7 Fan type & mode selection flow

Each fan can be controlled by 8 kinds of temperature inputs: (1) T1 temperature (2) T2 temperature (3) T3 temperature (4) PECI temperature (5) 4 suits I2C master temperature.

FAN 1	Related Register
FAN_PROG_SEL	Index 9Fh [7]
FAN Type Select	Index 94 [1:0]
FAN mode Select	Index 96 [1:0]
FAN count reading	Index A0h~A1h
FAN expect speed	Index A2h~A3h
FAN full speed count	Index A4h~A5h
BOUNDARY	Index A6h~A9h
SEGMENT SPEED	Index AAh~AEh

FAN1 Temperature Mapping	Index AFh

FAN 2	Related Register
FAN_PROG_SEL	Index 9Fh [7]
FAN Type Select	Index 94 [3:2]
FAN mode Select	Index 96 [3:2]
FAN count reading	Index B0h~B1h
FAN expect speed	Index B2h~B3h
FAN full speed count	Index B4h~B5h
BOUNDARY	Index B6h~B9h
SEGMENT SPEED	Index BAh~BEh
FAN1 Temperature Mapping	Index BFh

FAN 3	Related Register
CLK_TUNE_PROG_EN	Global Control Register : index 27h [0]
Multi Function	Global Control Register : index 2Bh [1:0]
FAN_PROG_SEL	Index 9Fh [7]
FAN Type Select	Index 94 [5:4]
FAN mode Select	Index 96 [5:4]
FAN count reading	Index C0h~C1h
FAN expect speed	Index C2h~C3h
FAN full speed count	Index C4h~C5h
BOUNDARY	Index C6h~C9h
SEGMENT SPEED	Index CAh~CEh
FAN1 Temperature Mapping	Index CFh

Manual mode

For manual mode, it generally acts as the software fan speed control.

Auto mode

In auto mode, the F81867 provides the automatic fan speed control related to the temperature variation of CPU/GPU or the system. The F81867 can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take FAN1 for example, the 4 temperature boundaries could be set from the register 0xA6 to 0xA9 and the five intervals for fan speed control could be set from register 0xAA to 0xAE.The hysteresis setting (0 ~ 15°C) could also be found in the register 0x98.

There are two kinds for the auto modes they are the stage auto mode and the linear auto mode. The “FAN1_INTERPOLATION_EN” in the register 0xAFh is used for the linear auto mode enable. The following examples explain the differences for the stage auto mode and linear auto mode.

Stage auto mode

In this mode, the fan keeps in a same speed for each temperature interval. And there are two types of fan speed setting: PWM Duty and RPM %.

A. Stage auto mode (PWM Duty)

Set the temperature limits as 70°C, 60°C, 50°C, 40°C and the duty as 100%, 90%, 80%, 70%, 60%

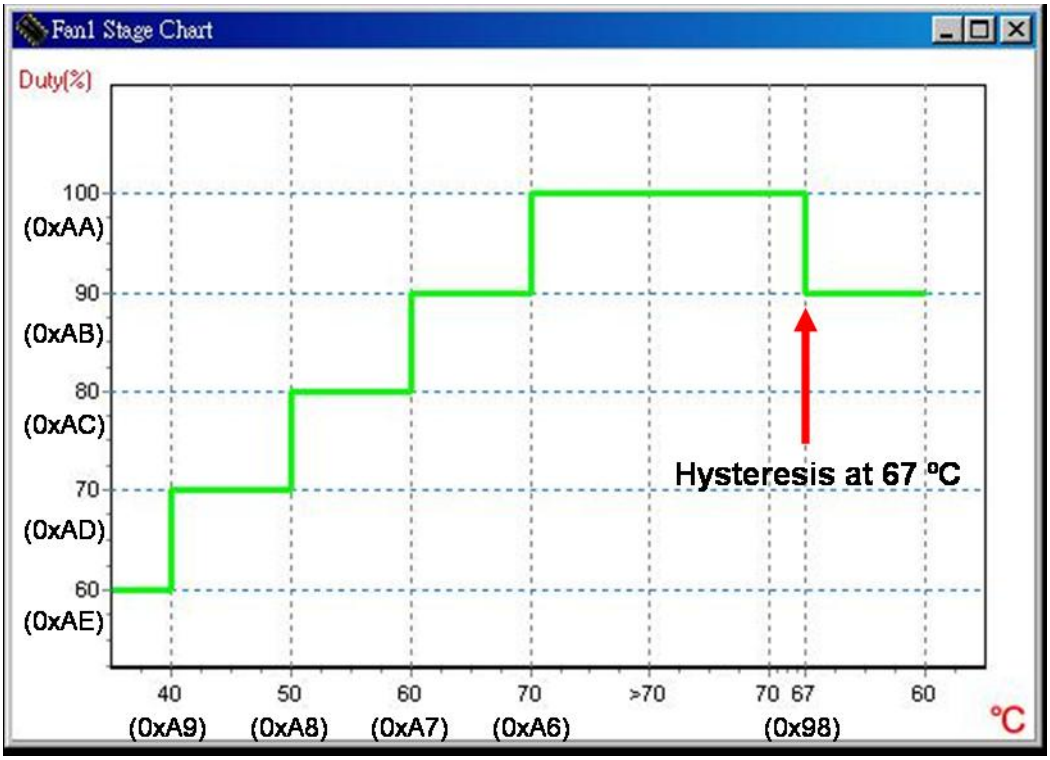


Fig 7-8 Stage mode fan control illustration

a. Once the temperature is under 40°C, the lowest fan speed keeps in the 60% PWM duty.
b. Once the temperature is over 40°C, 50°Cand 60°C, the fan speed will vary from 70%, 80% to 90% PWM duty and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in 100% PWM duty.
d. If set the hysteresis is 3°C (default 4°C), once the temperature becomes lower than 67°C, the fan speed would reduce to 90% PWM duty.

B. Stage auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 RPM, 5,400 RPM, 4,800 RPM, 4,200 RPM, and 3,600 RPM (assume the Max Fan Speed is 6,000

RPM).

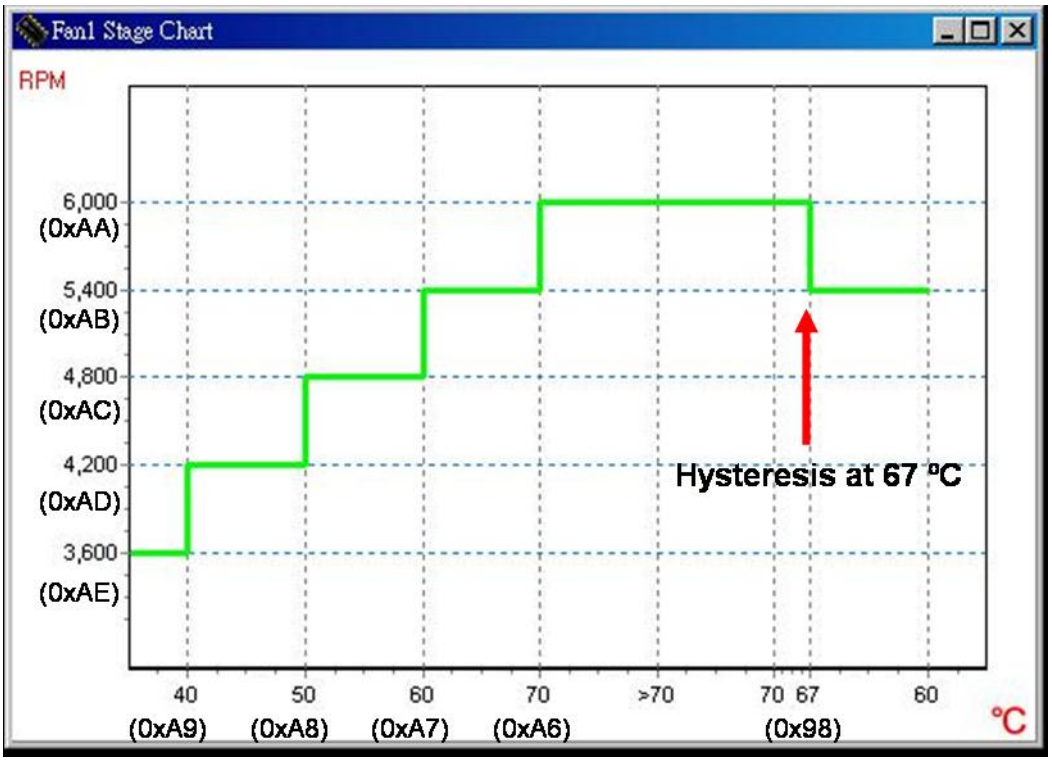


Fig 7-9 Stage mode fan control illustration

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,600 RPM (60% of full speed).
b. Once the temperature is higher than 40°C, 50°C and 60°C, the fan speed will vary from 4,200 RPM to 5,400 RPM and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in the full speed 6,000 RPM.
d. If the hysteresis is set as 3°C (default 4°C), once temperature gets lower than 67°C, the fan speed would reduce to 5,400 RPM.

Linear auto mode

Furthermore, F81867 also supports linear auto mode. The fan speed would increase or decrease linearly with the temperature. There are also PWM Duty and RPM% modes for it.

A. Linear auto mode (PWM Duty I)

Set the temperature as 70°C, 60°C, 50°C and 40°C and the duty is 100%, 80%, 70%, 60% and 50%.

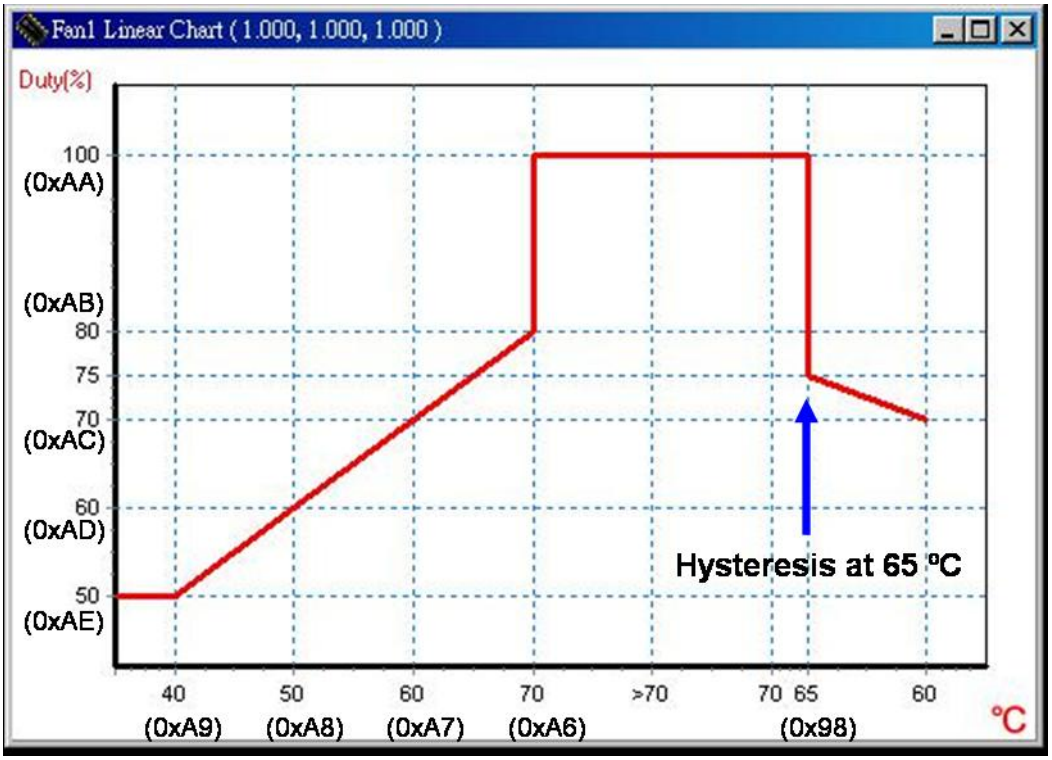


Fig 7-10 Linear mode fan control illustration

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in the 50% PWM duty
b. Once the temperature becomes higher than 40°C, 50°C and 60°C, the fan speed will vary from 50% to 80% PWM duty linearly with the temperature variation. The temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to 100% PWM duty (full speed).
d. If set the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from 100% PWM duty and decrease linearly with the temperature.

B. Linear auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 RPM, 4,800 RPM, 4,200 RPM, 3,600 RPM and 3,000 RPM (assume the Max Fan Speed is 6,000 RPM).

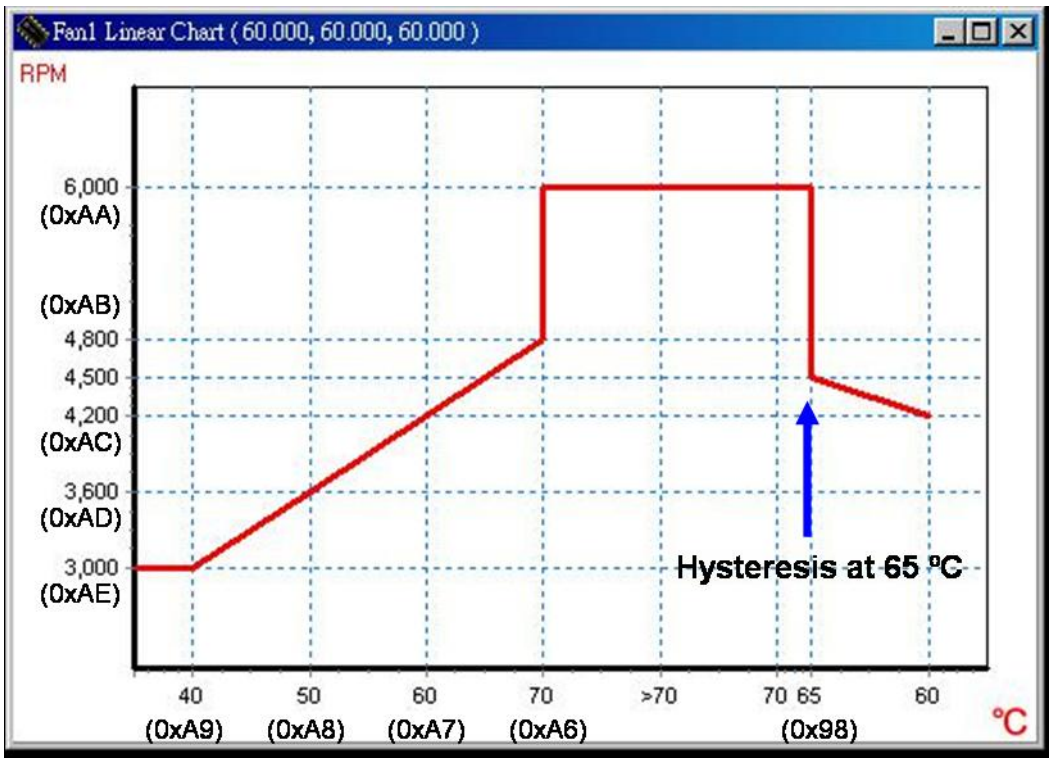


Fig 7-11 Linear mode fan control illustration

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,000 RPM (50% of full speed).
b. Once the temperature is over 40°C,50°C and 60°C, the fan speed will vary from 3,000 to 4,800 RPM almost linearly with the temperature variation because the temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to full speed 6,000 RPM.
d. If the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed wull reduce from full speed and decrease linearly with the temperature.

PWMOUT Duty-cycle operating process

In both “Manual RPM” and “Temperature RPM” modes, the F81867 adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

1. When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.
2. When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.
3. If both (1) and (2) are not true,
   When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, the F81867 will keep duty-cycle at 00h for 1.6 seconds. After that,

the F81867 starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F81867 will ignore it.

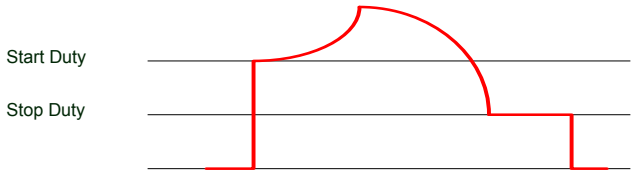


Fig 7-12

Fan Speed Control with Multi-temperature

F81867 supports Multi-temperature for Fan 1 control. Fan 1 can be controlled up to 2 kinds of temperature inputs. This function works with linear auto mode which can extend to two linear slopes for Fan 1 control. As below graph shows, this machine can support more silence fan control in low temperature and high fan speed in the high temperature segment. More detail setting please refers to the related registers.

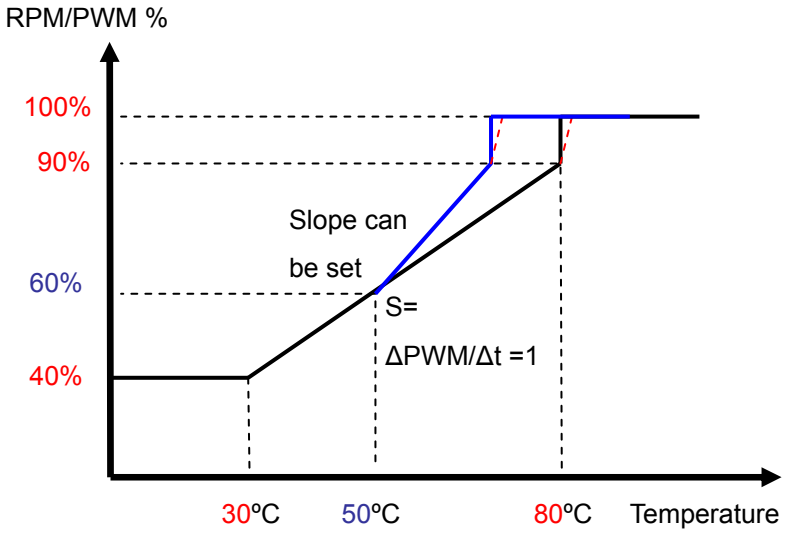
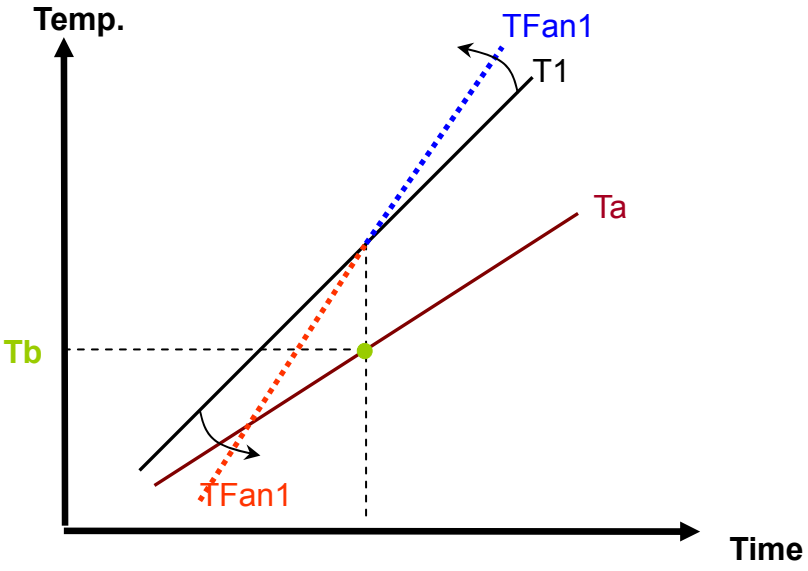


Figure 7-13 Support 2 Linear Application with Multi-Temp. Setting

In the figure below, TFan1 is the scaled temperature for fan1. T1 is the real temperature for the fan1 sensor. Ta is another temperature data which can be used for linearly scale up or scale down the fan1 speed curve. Tb would be the point which starts the temperature scaling. The slope for the temperature curve over and under Tb would be Ctup and Ctdn.



1. Ctup, Ctdn Can be Programmed to 1, ½, ¼, 0
2. Ta Can be Selected to the Same Temp. Source (Ex:T1)

TFan1= T1 + (Ta-Tb)*Ctup ; TFan1= T1 + (Ta-Tb)*Ctdn

Figure 7-14

In application, we can set the Ta as the 2nd sensor temperature and Tb as the temperature which starts the scaling. So if the 2nd sensor temperature Ta is higher or lower than Tb, the fan1 speed would be changed with it.

EX: Ta = T1, Tb = 60, Ctu = 1, Ctd = 1/4

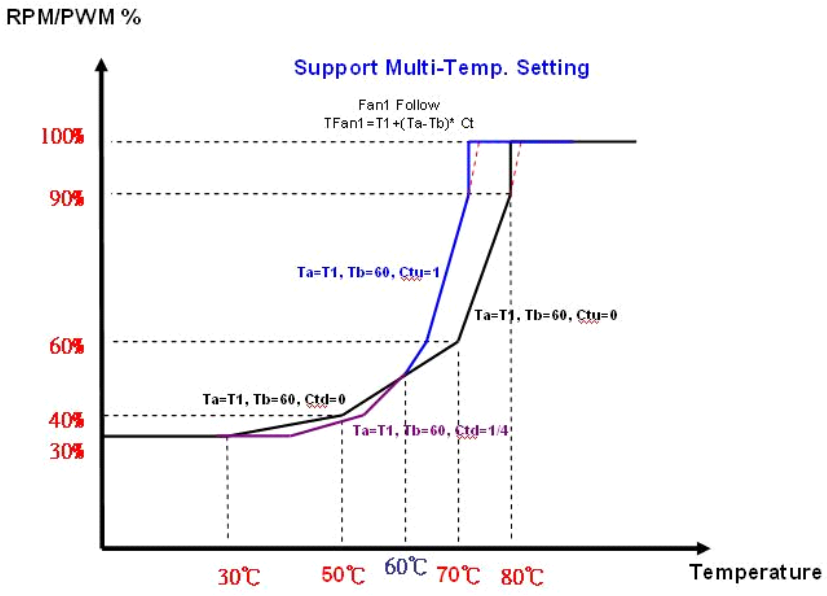


Figure 7-15

FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a

programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count on time. (Figure 7-16)

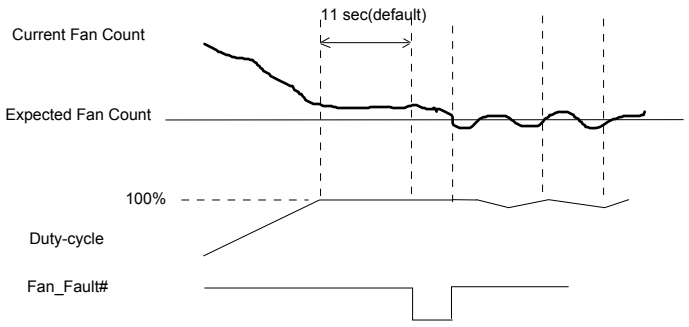


Fig 7-16

(2). After the period of detecting fan full speed, when PWM_Duty > Min. Duty, and fan count is still in 0xFFF.

6.4.2 Hardware Monitor Device Registers

Before the device registers, the following is a register map order which shows a summary of all registers. Please refer to each register if you want more detail information.

Register CR01 ~ CR03 → Configuration Registers

Register CR08 ~ CREF → PECI/TSI/I2C Control Register

Register CR40 ~ CR8E → PECI 3.0 Command and temperature Setting Register

Register CR10 ~ CR3A → Voltage Setting Register

Register CR90 ~ CRCF → Fan Control Setting Register

→Fan1 Detail Setting CRA0 ~ CRAF

→Fan2 Detail Setting CRB0 ~ CRBF

→Fan3 Detail Setting CRC0 ~ CRCF

6.4.2.1 Configuration Setting

FAN, Voltage Start up Register — Index 01h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	0h	-	0	Reserved
2	POWER_DOWN	R/W	5VSB	0	Hardware monitor function power down function.
1	FAN_START	R/W	5VSB	1	1: enable startup of fan monitoring operations. 0: Put the part in the standby mode.
0	V_T_START	R/W	5VSB	1	1: enable startup of temperature and voltage monitoring operations 0: Put the part in the standby mode.

Case Open, Alert, OVT Mode Register — Index 02h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Dummy register.
6	CASE_BEEP_EN	R/W	5VSB	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.
5-4	OVT_MODE	R/W	5VSB	0	00: The OVT# will be low active level mode. 01: The OVT# will be low pulse mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	Reserved	R/W	-	0	Dummy register.
2	CASE_SMI_EN	R/W	5VSB	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	5VSB	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

Case Open Status Register — Index 03h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	R/W	-	0	Reserved
0	CASE_STS	R/W	VBAT	0	Case open event status write 1 to clear if case open event cleared. (This bit is powered by VBAT.)

6.4.2.2 PECI/TSI/I2C Setting

TSI Or IBEX Control Register — Index 08h

Bit	Name	R/W	Reset	Default	Description
7-1	TSI_ADDR	R/W	5VSB	26h	AMD TSI or Intel IBEX slave address.
0	Reserved	-	-	-	Reserved

I2C Address Control Register — Index 09h

Bit	Name	R/W	Reset	Default	Description
7-1	I2C _ADDR	R/W	5VSB	0	I2C _ADDR[7:1] is the slave address sent by the embedded master when using a block write command
0	Reserved	R/W	-	0	Reserved

PECI, TSI, IBEX, Beta Register — Index 0Ah

Bit	Name	R/W	Reset	Default	Description
7	BETA_EN2	R/W	5VSB	0	0: disable the T2 beta compensation. 1: enable the T2 beta compensation.
6	BETA_EN1	R/W	5VSB	0	0: disable the T1 beta compensation. 1: enable the T1 beta compensation.
5	INTEL_SEL	R/W	5VSB	1	This bit is used to select AMD TSI or Intel IBEX when TSI_EN is set to 1. 0: Select AMD 1: Select Intel
4	MXM_MODE	R/W	LRESET#	0	Reserved
3-2	VTT_SEL	R/W	5VSB	0	PECI (VTT) voltage selection. 00: VTT is 1.23V 01: VTT is 1.13V 10: VTT is 1.00V 11: VTT is 1.00V
1	TSI_EN	R/W	5VSB	0	Set this bit 1 to enable AMD TSI or Intel IBEX function
0	PECI_EN	R/W	LRESET#	0	Set this bit 1 to enable Intel PECI function

CUP Socket Select Register — Index 0Bh

Bit	Name	R/W	Reset	Default	Description
7-4	CPU_SEL	R/W	5VSB	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping () command to find the CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 0, i.e. PECI address is 0x31. 0100: CPU is in socket 0, i.e. PECI address is 0x32. 1000: CPU is in socket 0, i.e. PECI address is 0x33. Others are reserved.
3-1	Reserved	-	-	0	Reserved.
0	DOMAIN1_EN	R/W	5VSB	0	If the CPU is selected as dual core. Set this register 1 to read the temperature of domain1.

TCC Register — Index 0Ch

Bit	Name	R/W	Reset	Default	Description
7-0	TCC_TEMP	R/W	5VSB	8'h55	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127°C.

TSI Offset Register — Index 0Dh

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_OFFSET	R/W	5VSB	0	This byte is used as the offset to be added to the CPU temperature reading of AMD_TSI. The range of this register is -128 ~ 127°C.

Configuration Register — Index 0Fh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1-0	DIG_RATE_SEL	R/W	5VSB	0	Reserved for Fintek use only

TSI Temperature 0 – Index E0h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP0	R/W	5VSB	-	This is the AMD TSI reading if AMD TSI enable. And will be highest temperature among CPU, MCH and PCH if Intel temperature interface enable. The range is 0~255°C. To access this byte, MCH_BANK_SEL must set to “0”.
	I2C_DATA0	R/W	5VSB	8’h00	This byte is used as multi-purpose: 1. The received data of receive protocol. 2. The first received byte of read word protocol. 3. The 10th received byte of read block protocol. 4. The sent data for send byte protocol and write byte protocol. 5. The first send byte for write word protocol. 6. The first send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to “1”.

TSI Temperature 1 – Index E1h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP1	R	5VSB	-	This is the high byte of Intel temperature interface PCH reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to “0”.
	I2C_DATA1	R/W	5VSB	8’h00	This byte is used as multi-purpose: 1. The second received byte of read word protocol. 2. The 11th received byte of read block protocol. 3. The second send byte for write word protocol. 4. The second send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to “1”.

TSI Temperature 2 Low Byte – Index E2h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP2_LO	R	5VSB	-	This is the low byte of Intel temperature interface CPU reading. The reading is the fraction part of CPU temperature. Bit 0 indicates the error status. 0: No error. 1: Error code. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA2	R/W	5VSB	8'h00	This is the 12th byte of the block read protocol. This byte is also used as the 3rd byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 2 High Byte – Index E3h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP2_HI	R	5VSB	-	This is the high byte of Intel temperature interface CPU reading. The reading is the decimal part of CPU temperature. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA3	R/W	5VSB	8'h00	This is the 13th byte of the block read protocol. This byte is also used as the 4th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 3 – Index E4h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP3	R	5VSB	-	This is the high byte of Intel temperature interface MCH reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA4	R/W	5VSB	8'h00	This is the 14th byte of the block read protocol. This byte is also used as the 5th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 4 – Index E5h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP4	R	5VSB	-	This is the high byte of Intel temperature interface DIMM0 reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".

	I2C_DATA5	R/W	5VSB	8'h00	This is the 15th byte of the block read protocol. This byte is also used as the 6th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 5 – Index E6h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP5	R	5VSB	-	This is the high byte of Intel temperature interface DIMM1 reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA6	R/W	5VSB	8'h00	This is the 16th byte of the block read protocol. This byte is also used as the 7th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 6 – Index E7h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP6	R	5VSB	-	This is the high byte of Intel temperature interface DIMM2 reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA7	R/W	5VSB	8'h00	This is the 17th byte of the block read protocol. This byte is also used as the 8th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 7 – Index E8h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP7	R	5VSB	-	This is the high byte of Intel temperature interface DIMM3 reading. The range is 0~255°C. The above 9 bytes could also be used as the read data of block read protocol if the TSI is disable or pending.
	I2C_DATA8	R/W	5VSB	8'h00	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

I2C Data Buffer 9 – Index E9h

Bit	Name	R/W	Reset	Default	Description
7-0	I2C_DATA9	R/W	5VSB	FFh	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

Block Write Count Register – Index ECh

Bit	Name	R/W	Reset	Default	Description
7	MCH_BANK_SEL	R/W	5VSB	0	This bit is used to select the register in index E0h to E9h. Set "0" to read the temperature bank and "1" to access the data bank.
6	Reserved	-	-	0	Reserved
5-0	BLOCK_WR_CNT	R/W	5VSB	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

I2C Command Byte/TSI Command Byte – Index EDh

Bit	Name	R/W	Reset	Default	Description
7-0	I2C_CMD/TSI_CMD	R/W	5VSB	0/1	There are actual two bytes for this index. TSI_CMD_PROG select which byte to be programmed: 0: I2C_CMD, which is the command code for write byte/word, read byte/word, block write/read and process call protocol. 1: TSI_CMD, which is the command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

I2C Status – Index EEh

Bit	Name	R/W	Reset	Default	Description
7	TSI_PENDING	R/W	LRESET#	0	Set 1 to pending auto TSI accessing. (In AMD model, auto accessing will issue a send-byte followed a receive-byte; In Intel model, auto accessing will issue a block read). To use the SCL/ SDA as I2C master, set this bit to "1" first.
6	TSI_CMD_PROG	R/W	5VSB	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	5VSB	0	Kill the current I2C transfer and return the state machine to idle. It will set a fail status if the current transfer is not completed.
4	FAIL_STS	R	5VSB	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next I2C transfer.
3	I2C_ABT_ERR	R	5VSB	0	This is the arbitration lost status if I2C command is issued. Auto cleared by next I2C command.
2	I2C_TO_ERR	R	5VSB	0	This is the timeout status if I2C command is issued. Auto cleared by next I2C command.
1	I2C__NAC_ERR	R	5VSB	0	This is the NACK error status if I2C command is issued. Auto cleared by next I2C command.
0	I2C__READY	R	5VSB	1	0: I2C transfer is in process. 1: Ready for next I2C command.

I2C Protocol Select – Index EFh

Bit	Name	R/W	Reset	Default	Description
7	I2C_START	W	-	0	Write "1" to trigger I2C transfer with the protocol specified by I2C_PROTOCOL.
6-4	Reserved	-	-	-	Reserved.
3-0	I2C__PROTOCOL	R/W	5VSB	0	Select what protocol if I2C transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: Reserved. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: read word. 1101b: block read. 1111b: Reserved Otherwise: reserved.

6.4.2.3 PECI 3.0 & Temperature Setting

PECI 3.0 Command and Register

PECI Configuration Register — Index 40h

Bit	Name	R/W	Reset	Default	Description
7	RDIAMSR_CMD_EN	R/W	5VSB	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR() command before a GetTemp() command.
6	C3_UPDATE_EN	R/W	5VSB	0	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR() is 0x82.
5-4	Reserved	R	-	-	Reserved
3	C3_PTEMP_EN	R/W	5VSB	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is 0x82.
2	C0_PTEMP_EN	R/W	5VSB	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	5VSB	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is 0x82.
0	C0_ALL0_EN	R/W	5VSB	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.

PECI Master Control Register — Index 41h

Bit	Name	R/W	Reset	Default	Description
7	PECI_CMD_START	W	5VSB	-	Write 1 to this bit to start a PECI command when using as a PECI master. (PECI_PENDING must be set to 1)

6-5	Reserved	R	-	-	Reserved
4	PECI_PENDING	R/W	5VSB	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	-	Reserved
2-0	PECI_CMD	R/W	5VSB	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

PECI Master Status Register — Index 42h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	-	Reserved
2	ABORT_FCS	R/WC	5VSB	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	5VSB	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
0	PECI_FINISH	R/WC	5VSB	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

PECI Master DATA0 Register — Index 43h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA0	R/W	5VSB	0	For RdIAMSR(), RdPkgConfig() and WrPkgConfig() command, this byte represents "Host ID[7:1] & Retry[0]". Please refer to PECI interface specification for more detail.

PECI Master DATA1 Register — Index 44h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA1	R/W	5VSB	0	For RdIAMSR() , this byte represents "Processor ID". For RdPkgConfig() and WrPkgConfig() , this byte represents "Index". Please refer to PECI interface specification for more detail.

PECI Master DATA2 Register — Index 45h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA2	R/W	5VSB	0	For RdIAMSR(), this byte is the least significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the least significant byte of "Parameter". Please refer to PECI interface specification for more detail.

PECI Master DATA3 Register — Index 46h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA3	R/W	5VSB	0	For RdIAMSR(), this byte is the most significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the most significant byte of "Parameter". Please refer to PECI interface specification for more detail.

PECI Master DATA4 Register — Index 47h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA4	R/W	5VSB	0	For GetDIB() , this byte represents "Device Info" For GetTemp(), this byte represents the least significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte is "Completion Code". For WrPkgConfig(), this byte represents "DATA[7:0]"

PECI Master DATA5 Register — Index 48h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA5	R/W	5VSB	0	For GetDIB() , this byte represents "Revision Number" For GetTemp(), this byte represents the most significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[7:0]" For WrPkgConfig(), this byte represents "DATA[15:8]"

PECI Master DATA6 Register — Index 49h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA6	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[15:8]". For WrPkgConfig(), this byte represents "DATA[23:16]"

PECI Master DATA7 Register — Index 4Ah

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA7	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[23:16]". For WrPkgConfig(), this byte represents "DATA[31:24]"

PECI Master DATA8 Register — Index 4Bh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA8	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[31:24]". For WrPkgConfig(), this byte represents "AW FCS"

PECI Master DATA9 Register — Index 4Ch

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA9	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[39:32]". For WrPkgConfig(), this byte represents "Completion Code"

PECI Master DATA10 Register — Index 4Dh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA10	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[47:40]".

PECI Master DATA11 Register — Index 4Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA11	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[55:48]".

PECI Master DATA12 Register — Index 4Fh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA12	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[63:56]".

HWM Manual Control Register1 — Index 50h

Bit	Name	R/W	Reset	Default	Description
7	LOAD_CH	W	-	-	Write 1 to load a temperature or voltage channel to be converted
6	STOP_CH	R/W	5VSB	0	Set to 1 when load a channel will generate a one-shot conversion.
5	HOLD_CH	R/W	5VSB	0	Set to 1 when load a channel will keep converting this channel.
4:0	CHANNEL	R/W	5VSB	0	First channel to be converted when LOAD_CH is set to 1. 00000: VCC 00001: VIN1 00010: VIN2 00011: VIN3 00100: VIN4 00101: VSB3V 00110: VBAT 00111: 5VSB 10000: Intel PECI 10001: T1 10010: T2 11000: AMD TSI/Intel IBEX

HWM Manual Control Status Register 1— Index 51h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	V_CONV_STS	R	5VSB	-	At least one of the voltage channels had finish converting.
5	PECI_CONV_STS	WC	5VSB	-	PECI channel had finish converting
4	TSI_CONV_STS	WC	5VSB	-	TSI channel had finish converting
3	Reserved	-		-	Reserved
2	T2_CONV_STS	WC	5VSB	-	T2 channel had finish converting
1	T1_CONV_STS	WC	5VSB	-	T1 channel had finish converting
0	Reserved	-		-	Reserved

HWM Manual Control Status Register 2— Index 52h

Bit	Name	R/W	Reset	Default	Description
7	5VSB_CONV_STS	WC	5VSB	-	5VSB voltage channel had finish converting
6	VBAT_CONV_STS	WC	5VSB	-	VBAT voltage channel had finish converting
5	VSB3V_CONV_STS	WC	5VSB	-	VSB3V voltage channel had finish converting
4	VIN4_CONV_STS	WC	5VSB	-	VIN4 voltage channel had finish converting
3	VIN3_CONV_STS	WC	5VSB	-	VIN3 voltage channel had finish converting
2	VIN2_CONV_STS	WC	5VSB	-	VIN2 voltage channel had finish converting
1	VIN1_CONV_STS	WC	5VSB	-	VIN1 voltage channel had finish converting
0	VCC_CONV_STS	WC	5VSB	-	VCC voltage channel had finish converting

HWM RAW Data Register 1— Index 55h

Bit	Name	R/W	Reset	Default	Description
7-0	RAW_DATA_L	R	5VSB	0	Low byte of HM converting raw data

HWM RAW Data Register 2— Index 56h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved
1-0	RAW_DATA_H	R	5VSB	0	The highest two bits of HM converting raw data

Temperature Register

Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	EN_ T2_OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	EN_ T0_ OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP0 exceeds OVT setting.
3	Reserved	R/W	-	0	Reserved
2	EN_ T2_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	EN_ T0_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP0 exceeds high limit setting.

Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	T2_OVT _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
5	T1_OVT _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
4	T0_OVT _STS	R/W	3VCC	0	A one indicates TEMP0 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
3	Reserved	R/W	-	0	Reserved
2	T2_EXC _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
1	T1_EXC _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
0	T0_EXC _STS	R/W	3VCC	0	A one indicates TEMP0 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.

Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	T2_OVT	R/W	3VCC	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	3VCC	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	T0_OVT	R/W	3VCC	0	Set when the TEMP0 exceeds the OVT limit. Clear when the TEMP0 is below the “OVT limit –hysteresis” temperature.
3	Reserved	R/W	-	0	Reserved
2	T2_EXC	R/W	3VCC	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	3VCC	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	T0_EXC	R/W	3VCC	0	Set when the TEMP0 exceeds the high limit. Clear when the TEMP0 is below the “high limit –hysteresis” temperature.

Temperature BEEP Enable Register — Index 63h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	EN_ T2_ OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	EN_ T0_ OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP0 exceeds OVT limit setting.
3	Reserved	R/W	-	0	Reserved
2	EN_ T2_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	EN_ T0_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP0 exceeds high limit setting.

T1 OVT and High Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R/W	-	0	Reserved
5-4	OVT_TEMP_SEL	R/W	5VSB	0	Select the source temperature for T1 OVT Limit. 0: Select T1 to be compared to Temperature 1 OVT Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 OVT Limit. 2: Select CPU temperature from AMD TSI or Intel PCH I2C to be compared to Temperature 1 OVT Limit. 3: Select the MAX temperature from Intel PCH I2C to be compared to Temperature 1 OVT Limit.
3-2	Reserved	R/W	-	0	Reserved
1-0	HIGH_ TEMP_SEL	R/W	5VSB	0	Select the source temperature for T1 High Limit. 0: Select T1 to be compared to Temperature 1 High Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 High Limit. 2: Select CPU temperature from AMD TSI or Intel PCH I2C to be compared to Temperature 1 High Limit. 3: Select the MAX temperature from Intel PCH I2C to be compared to Temperature 1 High Limit.

OVT and Alert Output Enable Register 1 — Index 66h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	EN_T2_ALERT	R/W	5VSB	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R/W	5VSB	0	Enable temperature 1 alert event (asserted when temperature over high limit)
4	EN_T0_ALERT	R/W	5VSB	0	Enable temperature 0 alert event (asserted when temperature over high limit)
3	Reserved	R/W	-	0	Reserved
2	EN_T2_OVT	R/W	5VSB	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	5VSB	1	Enable over temperature (OVT) mechanism of temperature1.
0	EN_T0_OVT	R/W	5VSB	0	Enable over temperature (OVT) mechanism of temperature0.

Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	RO	-	0	Reserved
3	Reserved	RO	-	0	Reserved
2	T2_MODE	R/W	5VSB	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	5VSB	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	R	-	0	Reserved

TEMP1 Limit Hystersis Select Register — Index 6Ch

Bit	Name	R/W	Reset	Default	Description
7-4	TEMP1_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	TEMP0_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

TEMP2 and TEMP3 Limit Hystersis Select Register — Index 6Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	R	-	0	Reserved
3-0	TEMP2_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

DIODE OPEN Status Register — Index 6Fh

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R	-	-	Reserved
5	PECI_OPEN	R	3VCC	-	When PECI interface is enabled, “1” indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4	TSI_OPEN	R	3VCC	-	When TSI interface is enabled, “1” indicates the error of not receiving NACK bit or a timeout occurred.
3	Reserved	R	-	-	Reserved
2	T2_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 2 is open or short
1	T1_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 1 is open or short
0	T0_DIODE_OPEN	RO	3VCC	-	This register indicates the abnormality of temperature 0 measurement.

Temperature — Index 70h- 8Dh

Address	Attribute	Reset	Default Value	Description
70h	RO	3VCC	--	Temperature 0 reading. The unit of reading is 1°C.At the moment of reading this register.
71h	Reserved	3VCC	FFh	Reserved
72h	R	3VCC	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	R	3VCC	--	Reserved
74h	R	3VCC	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75-79h	R	3VCC	--	Reserved
7Ah	R	3VCC	--	The data of CPU temperature from digital interface after IIR filter. (Available if Intel IBX or AMD TSI interface is enabled)
7Bh	R	3VCC	--	The raw data of PCH temperature from digital interface. (Only available if Intel IBX interface is enabled)
7Ch	R	3VCC	--	The raw data of MCH read from digital interface. (Only available if Intel IBX interface is enabled)
7Dh	R	3VCC	--	The raw data of maximum temperature between CPU/PCH/MCH from digital interface. (Only available if Intel IBEX interface is enabled)
7Eh	R	3VCC	--	The data of CPU temperature from digital interface after IIR filter. (Only available if PECI interface is enabled)
80h	R/W	5VSB	64h	Temperature sensor 0 OVT limit. The unit is 1°C.
81h	R/W	5VSB	55h	Temperature sensor 0 high limit. The unit is 1°C.
82h	R/W	5VSB	64h	Temperature sensor 1 OVT limit. The unit is 1°C.

83h	R/W	5VSB	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	5VSB	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	5VSB	55h	Temperature sensor 2 high limit. The unit is 1°C.
86-8Bh	R	--	--	Reserved
8C~8Dh	R	--	FFH	Reserved

T1 Slope Adjust Register — Index 7Fh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	T1_ADD	R/W	5VSB	0h	This bit is the sign bit for T1 reading slope adjustment. See T1_SCALE below for detail.
2-0	T1_SCALE	R/W	-	0h	T1_ADD / T1_SCALE / Slope X / 00 / No adjustment 0 / 01 / 15/16 0 / 10 / 31/32 0 / 11 / 63/64 1 / 01 / 17/16 1 / 10 / 33/32 1 / 11 / 65/64

Temperature Filter Select Register —Index 8Eh

Bit	Name	R/W	Reset	Default	Description
7-6	IIR-QUEUR3	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. 00: 8 times. 01: 12 times. 10: 16 times. (default) 11: 24 times.
5-4	IIR-QUEUR2	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. 00: 8 times. 01: 12 times. 10: 16 times. (default) 11: 24 times.
3-2	IIR-QUEUR1	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.

1-0	IIR-QUEUR_DIG	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. (for CPU temperature from PECI or TSI interface) 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.

6.4.2.4 Voltage Setting

Voltage-Protect Shut Down Enable Register — Index 10h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	0	Reserved.
6	V3_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for VIN3
5	V2_VP_EN	R/W	VBAT*	0	Voltage-Protect enable for VIN2
4-1	Reserved	-	-	0	Reserved
0	VCC_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for 3VCC

Voltage-Protect Status Register — Index 11h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved.
0	V_EXC_VP	R/WC	VBAT/ 5VSB*	0	This bit is voltage-protect status. Once one of the monitored voltages (3VCC, VIN2, VIN3) over its related over-voltage limits or under its related under-voltage limits and if the related voltage-protect shut down enable bit is set, this bit will be set to 1. Write a 1 to this bit will clear it to 0. (This bit is powered by VBAT)

*Reset by VBAT when OVP_MODE is "0", Reset by 5VSB when OVP_MODE is "1"

Voltage-Protect Configuration Register — Index 12h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.

3-2	PU_TIME	R/W	VBAT	2'h1	PSON# de-active time select for voltage protection. 00: PSON# tri-state 0.5 sec and then inverted of S3# when over voltage or under voltage occurred. 01: PSON# tri-state 1 sec and then inverted of S3# when over voltage or under voltage occurred. 10: PSON# tri-state 2 sec and then inverted of S3# when over voltage or under voltage occurred. 11: PSON# tri-state 4 sec and then inverted of S3# when over voltage or under voltage occurred.
1-0	VP_EN_DELAY	R/W	VBAT	2'h2	VP_EN_DELAY could set the delay time to start voltage protecting after VDD power is ok when OVP_MODE is 1. (OVP_MODE is strapped by RTS1# pin) 00: bypass 01: 50ms 10: 100ms 11: 200ms

Voltage1 PME# Enable Register — Index 14h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved
1	EN_V1_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for VIN1.
0	Reserved	-	-	-	Reserved

Voltage1 Interrupt Status Register — Index 15h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	0	Reserved
1	V1_ EXC _STS	R/W	5VSB	0	This bit is set when the VIN1 is over the high limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	-	-	-	Reserved

Voltage1 Exceeds Real Time Status Register 1 — Index 16h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	0	Reserved
1	V1_EXC	RO	5VSB	0	A one indicates VIN1 exceeds the high limit. A zero indicates VIN1 is in the safe region.
0	Reserved	--	-	0	Reserved

Voltage1 BEEP Enable Register — Index 17h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	0	Reserved
1	EN_V1_BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP output of VIN1.
0	Reserved	--	-	0	Reserved

Voltage Protection Power Good Select Register — Index 3Fh

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	--	-	0	Reserved
0	OVP_RST_SEL	R/W	VBAT	0	0: OVP/UVP power good signal is 3VCCOK (3VCC > 2.8V) 1: OVP/UVP power good signal is PWROK. OVP/UVP function wont' start detecting until power good.

Voltage reading and limit— Index 20h- 3Ah

Address	Attribute	Reset	Default Value	Description
20h	R	3VCC	--	3VCC reading. The unit of reading is 8mV.
21h	R	3VCC	--	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	R	3VCC	--	VIN2 reading. The unit of reading is 8mV.
23h	R	3VCC	--	VIN3 reading. The unit of reading is 8mV.
24h	R	3VCC	--	VIN4 reading. The unit of reading is 8mV.
25h	R	3VCC	--	VSB3V reading. The unit of reading is 8mV.
26h	R	3VCC	--	VBAT reading. The unit of reading is 8mV.
27h	R	3VCC	--	5VSB reading. The unit of reading is 8 mV. The 5VSB voltage to be monitored is internally divided by 3.
28h-2Ch	R	--	FF	Reserved
2Dh	RO	3VCC	--	FAN1 present fan duty reading
2Eh	RO	3VCC	--	FAN2 present fan duty reading
2Fh	RO	3VCC	--	FAN3 present fan duty reading
30	RO	VBAT	89	3VCC under-voltage protection limit. The unit is 8mV
31	R/W	VBAT	F2	3VCC over-voltage protection limit. The unit is 8 mV
32~35h	R		FF	Reserved
36h	R/W	VBAT	E2	VIN2 over-voltage limit (V2_OVV_LIMIT). The unit is 8mv. (This byte is powered by VBAT.)
37h	R/W	VBAT	E1	VIN3 over-voltage limit (V3_OVV_LIMIT). The unit is 8mv. (This byte is powered by VBAT.)
38h	R/W	VBAT	83	VIN2 under-voltage limit (V2_UVV_LIMIT). The unit is 8mv (This byte is powered by VBAT)

39h	R/W	VBAT	96	VIN3 under-voltage limit (V3_UVV_LIMIT). The unit is 8mv (This byte is powered by VBAT)
3Ah	R/W	5VSB	FF	VIN1 OVP limit. The unit is 8mv (This byte is powered by VBAT)

6.4.2.5 Fan Control Setting

FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	0	Reserved
2	EN_FAN3_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt Set this bit 1 to enable PME# function for Fan3.
1	EN_FAN2_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	0	Reserved
2	FAN3_STS	R/W	3VCC	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	3VCC	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	3VCC	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	--	-	0	Reserved
2	FAN3_EXC	R	3VCC	--	This bit set to high mean that fan3 count can't meet the expected count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	R	3VCC	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	R	3VCC	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.

FAN BEEP# Enable Register — Index 93h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	FULL_WITH_ T2_EN	R/W	5VSB	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_ T1_EN	R/W	5VSB	0	Set one will enable FAN to force full speed when T1 over high limit.
4	Reserved	-	-	-	Reserved
3	Reserved	-	-	-	Reserved.
2	EN_FAN3_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.
1	EN_FAN2_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.

FAN Type Select Register — Index 94h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5-4	FAN3_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL3 0: FANCTRL3 is pull up by external resistor. 1: FANCTRL3 is pull down by internal 100KΩ resistor.
3-2	FAN2_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL2 0: FANCTRL2 is pull up by external resistor. 1: FANCTRL2 is pull down by internal 100KΩ resistor.

1-0	FAN1_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL1 0: FANCTRL1 is pull up by external resistor. 1: FANCTRL1is pull down by internal 100KΩ resistor.

S: Register default values are decided by trapping.

Fan1 Base Temperature Register – Offset 94h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	FAN1_BASE _TEMP	R/W	5VSB	0	This register is used to set the base temperature for FAN1 temperature adjustment. The FAN1 temperature is calculated according to the equation: Tfan1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG and FAN1_TEMP_SEL. Tb is this register, Ta is selected by TFAN1_ADJ_SEL and Ct is selected by TFAN1_ADJ_UP_RATE/TFAN1_ADJ_DN_RATE. To access this register, FAN_PROG_SEL (CR9F[7]) must set to "1".

FAN1 Temperature Adjustment Rate Register — Index 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6-4	TFAN1_ADJ_UP _RATE		5VSB	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3'h1: 1 (Ct = 1) 3'h2: 1/2 (Ct= 1/2) 3'h3: 1/4 (Ct = 1/4) 3'h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to "1".
3	Reserved	-		-	Reserved

2-0	TFAN1_ADJ_DN _RATE	R/W	5VSB	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3'h1: 1 (Ct = 1) 3'h2: 1/2 (Ct= 1/2) 3'h3: 1/4 (Ct = 1/4) 3'h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to "1".

FAN mode Select Register — Index 96h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved
5-4	FAN3_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xC6-0xCE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xC6-0xCE. 10: Manual mode fan control. User can write expected **RPM** count to 0xC2-0xC3, and F81867 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control. User can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xC3, and F81867 will output this desired duty or voltage to control fan speed.
3-2	FAN2_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xB6-0xBE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** (voltage) defined in 0xB6-0xBE. 10: Manual mode fan control. User can write expected **RPM** count to 0xB2-0xB3, and F81867 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F81867 will output this desired duty or voltage to control fan speed.

1-0	FAN1_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xA6-0xAE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expected **RPM** count to 0xA2-0xA3, and F81867 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F81867 will output this desired duty or voltage to control fan speed.

FAN mode Select Register — Index 96h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved
2-0	TFAN1_ADJ_SEL	R/W	5VSB	0h	This selects which temperature to be used as Ta for Fan1 temperature adjustment. 000: PECI (CR7Eh) 001: T1 (CR72h) 010: T2 (CR74h) 011: T3 (CR76h) 100: IBX/TSI CPU temperature (CR7Ah) 101:IBX PCH temperature (CR7Bh). 110: IBX MCH temperature (CR7Ch). 111: IBX maximum temperature (CR7Dh). otherwise: Ta will be 0. To access this register FAN_PROG_SEL must set to “1”.

Faster Fan Filter Control Register — Index 97h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved.
2	FLT_FAST3	R/W	5VSB	0	Set this bit 1 if FAN3 is using a faster fan.
1	FLT_FAST2	R/W	5VSB	0	Set this bit 1 if FAN2 is using a faster fan.
0	FLT_FAST1	R/W	5VSB	0	Set this bit 1 if FAN1 is using a faster fan.

Auto FAN1 and FAN2 Boundary Hystersis Select Register — Index 98h

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_HYS	R/W	5VSB	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	5VSB	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Auto FAN3 Boundary Hystersis Select Register — Index 99h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	FAN3_HYS	R/W	5VSB	2h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Fan3 Control Register — Index 9Ah

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	FREQ_SEL_ADD3	R/W	5VSB	0	This bit and FAN3_PWM_FREQ_SEL are used to select FAN3 PWM frequency. NEW_FREQ_SEL3 = { FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FREQ_SEL_ADD2	R/W	5VSB	0	This bit and FAN2_PWM_FREQ_SEL are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz

4	FREQ_SEL_ADD1	R/W	5VSB	0	This bit and FAN1_PWM_FREQ_SEL are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
3-2	Reserved	R/W	-	0	Reserved (Keep the value of these two bits “0”)
1-0	Reserved	-	-	-	Reserved

Auto Fan Up Speed Update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5-4	FAN3_UP_RATE	R/W	5VSB	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_UP_RATE	R/W	5VSB	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_UP_RATE	R/W	5VSB	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

Auto Fan Down Speed update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	UP_DN_RATE_EN	R/W	5VSB	0	0: Fan down rate disable 1: Fan down rate enable Set this bit 1 to use different fan up/down rate. If this bit is not set to 1, the fan up/down rate will follow FAN_UP_RATE.
6	DIRECT_LOAD_EN	R/W	5VSB	0	0: Direct load disable 1: Direct load enable for manual duty mode

5-4	FAN3_DN_RATE	R/W	5VSB	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_DN_RATE	R/W	5VSB	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DN_RATE	R/W	5VSB	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_STOP _DUTY	R/W	5VSB	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP _DUTY	R/W	5VSB	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	FAN3_STOP_ DUTY	R/W	5VSB	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN PROGRAMMABLE DUTY-CYCLE/VOLTAGE LOADED AFTER POWER-ON — Index 9Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PROG_DUTY_VAL	R/W	5VSB	66h	This byte will be immediately loaded as Fan duty value after VDD is powered on if it has been programmed before shut down.

Fan Fault Time Register — Index 9Fh

Bit	Name	R/W	Reset	Default	Description
7	FAN_PROG_SEL	R/W	5VSB	0	Set this bit to "1" will enable accessing registers of other bank.
6	FAN_MNT_SEL	R/W	5VSB	0	Set this bit to monitor a slower fan.
5	Reserved	-	-	-	Reserved
4	FULL_DUTY_SEL	R/W	3VCC	-	0: The Fan Duty is 100% and will be loaded immediately after VDD is powered on if CR9E is not been programmed before shut down. (pull down by external resistor) 1: The Fan Duty is 40% and will be loaded immediately after VDD is powered on if CR9E is not been programmed before shut down. (pull up by internal 47KΩ resistor). This register is power on trap by DTR1#/FAN40_100.
3-0	F_FAULT_TIME	R/W	5VSB	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0, means 1 seconds; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 9C-9Dh.

A. FAN1 Index A0h~AFh

Address	Attribute	Reset	Default	Description
A0h	RO	3VCC	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	3VCC	8'hff	FAN1 count reading (LSB).

A2h	R/W	VBAT	8'h00	RPM mode(CR96 bit0=0): FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. Duty mode(CR96 bit0=1): This byte is reserved byte.
A3h	R/W	VBAT	8'h01	RPM mode(CR96 bit0=0): FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit0=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	5VSB	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	5VSB	8'hff	FAN1 full speed count reading (LSB).

VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP1	R/W	5VSB	3Ch (60°C)	The first boundary temperature for VT1 in temperature mode. When VT1 temperature **exceeds** this boundary, expected FAN1 value will be loaded from segment **1** register (index AAh). When VT1 temperature is **under** this boundary – hysteresis, expected FAN1 value will be loaded from segment **2** register (index ABh). This byte is a 2's complement value ranged from -128°C ~ 127°C.

VT1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP1	R/W	5VSB	32 (50°C)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 2 register (index ABh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 3 register (index ACh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

VT1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP1	R/W	5VSB	28h (40°C)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 3 register (index ACh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 4 register (index ADh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

VT1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP1	R/W	5VSB	1Eh (30°C)	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 4 register (index ADh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 5 register (index AEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED1	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED1	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 3 SPEED COUNT Register – Index ACh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED1	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 4 SPEED COUNT Register – Index ADh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED1	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 5 SPEED COUNT Register – Index AEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED1	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Reset	Default	Description
7	FAN1_TEMP _SEL_DIG	R/W	5VSB	0	This bit companies with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	FAN1_PWM _FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD1 are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN1_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.

4	FAN1_ INTERPOLATION_E N	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP _HIGH_EN	R/W	5VSB	1	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.
2	FAN1_JUMP _LOW_EN	R/W	5VSB	1	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.
1-0	FAN1_TEMP_SEL	R/W	5VSB	01	This registers company with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 0 (CR70h). 100: fan1 follows IBX/TSI CPU temperature (CR7Ah) 101: fan1 follows IBX PCH temperature (CR7Bh). 110: fan1 follows IBX MCH temperature (CR7Ch). 111: fan1 follows IBX maximum temperature (CR7Dh). Others are reserved.

B. FAN2 Index B0h~BFh

Address	Attribute	Reset	Default Value	Description
B0h	RO	3VCC	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	3VCC	8'hff	FAN2 count reading (LSB).

B2h	R/W	VBAT	8'h00	RPM mode(CR96 bit2=0): FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. Duty mode (CR96 bit2=1): This byte is reserved byte.
B3h	R/W	VBAT	8'h01	RPM mode(CR96 bit2=0): FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit2=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	5VSB	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	5VSB	8'hff	FAN2 full speed count reading (LSB).

VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP2	R/W	5VSB	3Ch (60°C)	The first boundary temperature for VT2 in temperature mode. When VT2 temperature **exceeds** this boundary, FAN2 expect value will load from segment **1** register (index Bah). When VT2 temperature is **under** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BAh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

VT2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP2	R/W	5VSB	32 (50°C)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 2 register (index BBh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 3 register (index BCh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

VT2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP2	R/W	5VSB	28h (40°C)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 3 register (index BCh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 4 register (index BDh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

VT2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP2	R/W	5VSB	1Eh (30°C)	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 4 register (index BDh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 5 register (index BEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED2	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED2	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 3 SPEED COUNT Register – Index BCh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED2	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 4 SPEED COUNT Register – Index BDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED2	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 5 SPEED COUNT Register – Index BEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED2	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Reset	Default	Description
7	FAN2_TEMP_ SEL_DIG	R/W	5VSB	0	This bit companies with FAN2_TEMP_SEL to select the temperature source for controlling FAN2.
6	FAN2_PWM_ FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD2 are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN2_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.

4	FAN2_ INTERPOLATION_EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_ HIGH_EN	R/W	5VSB	1	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.
2	FAN2_JUMP_ LOW_EN	R/W	5VSB	1	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.
1-0	FAN2_TEMP_SEL	R/W	5VSB	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR7Eh) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011: fan2 follows temperature 0 (CR70h). 100: fan2 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan2 follows IBEX PCH temperature (CR7Bh). 110: fan2 follows IBEX MCH temperature (CR7Ch). 111: fan2 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

C. FAN3 Index C0h- CFh

Address	Attribute	Reset	Default Value	Description
C0h	RO	3VCC	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	3VCC	8'hff	FAN3 count reading (LSB).

C2h	R/W	VBAT	8'h00	RPM mode(CR96 bit4=0): FAN3 expect speed count value (MSB), in auto fan mode (CR96 bit5➔0) this register is auto updated by hardware. Duty mode(CR96 bit4=1): This byte is reserved byte.
C3h	R/W	VBAT	8'h01	RPM mode(CR96 bit4=0): FAN3 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit4=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	5VSB	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	5VSB	8'hff	FAN3 full speed count reading (LSB).

VT3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP3	R/W	5VSB	3Ch (60°C)	The first boundary temperature for VT3 in temperature mode. When VT3 temperature **exceeds** this boundary, FAN3 expect value will load from segment **1** register (index CAh). When VT3 temperature is **under** this boundary – hysteresis, FAN3 expect value will load from segment **2** register (index CAh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

VT3 BOUNDARY 2 TEMPERATURE – Index C7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP3	R/W	5VSB	32 (50°C)	The 2nd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 2 register (index CBh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 3 register (index CCh). This byte is a 2's complement value ranging from-128°C ~ 127°C.

VT3 BOUNDARY 3 TEMPERATURE – Index C8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP3	R/W	5VSB	28h (40°C)	The 3rd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 3 register (index CCh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 4 register (index CDh). This byte is a 2's complement value ranging from-128°C ~ 127°C.

VT3 BOUNDARY 4 TEMPERATURE – Index C9h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP3	R/W	5VSB	1Eh (30°C)	The 4th BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 4 register (index CDh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 5 register (index CEh). This byte is a 2's complement value ranging from-128°C ~ 127°C.

FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED3	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN3_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex:100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED3	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED3	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED3	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5SPEED3	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Reset	Default	Description
7	FAN3_TEMP_ SEL_DIG	R/W	5VSB	0	This bit companies with FAN3_TEMP_SEL select the temperature source for controlling FAN3.
6	FAN3_PWM_ FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD3 are used to select FAN3 PWM frequency. NEW_FREQ_SEL3 = { FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN3_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_ INTERPOLATION_EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.

3	FAN3_JUMP_ HIGH_EN	R/W	5VSB	1	This register controls the FAN3 duty movement when temperature over highest boundary. 0: The FAN3 duty will increases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register. This bit only activates in duty mode.
2	FAN3_JUMP_ LOW_EN	R/W	5VSB	1	This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN3 duty will decreases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC2SPEED3 register. This bit only activates in duty mode.
1-0	FAN3_TEMP_SEL	R/W	5VSB	11	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 000: fan3 follows PECI temperature (CR7Eh) 001: fan3 follows temperature 1 (CR72h). 010: fan3 follows temperature 2 (CR74h). 011: fan3 follows temperature 0 (CR70h). 100: fan3 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan3 follows IBEX PCH temperature (CR7Bh). 110: fan3 follows IBEX MCH temperature (CR7Ch). 111: fan3 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

6.5 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60h. The keyboard controller uses the output buffer to send the code received from the keyboard and data bytes required by

commands to the system.

Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60h or 64h. Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

Status Register

The status register is an 8-bit read-only register at I/O address 64h that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

Commands

COMMAND	FUNCTION
20h	Read Command Byte

<table>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Return 55h if self test succeeds</td></tr>
<tr><td>ABh</td><td>keyboard Interface Test
8’h00: indicate keyboard interface is ok.
8’h01: indicate keyboard clock is low.
8’h02: indicate keyboard clock is high
8’h03: indicate keyboard data is low
8’h04: indicate keyboard data is high</td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>CAh</td><td>Read the data written by CBh command.</td></tr>
<tr><td>CBh</td><td>Written a scratch data. This byte could be read by CAh command.</td></tr>
<tr><td>D0h</td><td>Send Port2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set/reset GateA20 line based on the system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from Keyboard</td></tr>
<tr><td>D3h</td><td>Send data back to the system as if it came from Muse</td></tr>
<tr><td>D4h</td><td>Output next received byte of data from system to Mouse</td></tr>
<tr><td>FEh</td><td>Low pulse on KBRST# about 6μS</td></tr>
</table>

KBC Command Description

PS/2 wakeup function

The KBC supports keyboard and mouse wakeup function. KBC will assert PME or PWSOUT# signal. Those wakeup conditions are controlled by the configuration register.

6.6 GPIO

F81867 has 72 pins GPIO in total. All GPIO supports digit IO for Input/Output control, Output data control, input status and High/Low Level/Pulse, Open Drain/Push Pull function selection. The GPIO0x and GPIO1x support interrupt status. The GPIO0x, GPIO1x, GPIO5x, and GPIO8x have different SIRQ channels. The GPIO8x supports scan code function, please see registers for detail. Please see below for GPIO access methods and status:

6.6.1 GPIO Access Method

There are nine sets of GPIO in F81867 which can be accessed by three ways as below:

1. Configuration register port: Use 0x4E/0x4F (or 0x2E/0x2F) port with logic device number 0x06. Please refer to configuration register for detail.
2. Index/Data port: The index port is base address + 0 and data port is base address + 1. To access the GPIO register, user should first write index to index port and then read/write from/to data port. The index for each register is same as the definition in configuration register.
3. Digital I/O: This way could access GPIO data register only. It is used for quickly control the GPIO pins. The register for each address is as list:

***Available when GPIO_DEC_RANGE is set "1" (Configuration register index 0x27, bit 5)**

GPIO Digital I/O Registers									
Offset	**Register Name**	**Default Value**							
		MSB							**LSB**
0h	Index Port	1	1	1	1	1	1	1	1
1h	Data Port	-	-	-	-	-	-	-	-
2h	GPIO8 Data Port	-	-	-	-	-	-	-	-
3h	GPIO7 Data Port	-	-	-	-	-	-	-	-
4h	GPIO6 Data Port	-	-	-	-	-	-	-	-
5h	GPIO5 Data Port	-	-	-	-	-	-	-	-
6h	GPIO0 Data Port	-	-	-	-	-	-	-	-
7h	GPIO1 Data Port	-	-	-	-	-	-	-	-
8h*	GPIO2 Data Port	-	-	-	-	-	-	-	-
9h*	GPIO3 Data Port	-	-	-	-	-	-	-	-
Ah*	GPIO4 Data Port	-	-	-	-	-	-	-	-
B-Fh*	Reserved	-	-	-	-	-	-	-	-

GPIO8 Data Port — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO8_DATA	R/W	LRESET#	-	GPIO8 Data Control Write data to this byte will change the value of GPIO80_VAL ~ GPIO87_VAL in configuration register as writing data to index 0x89. Read data from this byte will read the pin status of GPIO80_IN ~ GPIO87_IN as the value in index 0x8A

GPIO7 Data Port — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO7_DATA	R/W	LRESET#	-	GPIO7 Data Control Write data to this byte will change the value of GPIO70_VAL ~ GPIO77_VAL in configuration register as writing data to index 0x81. Read data from this byte will read the pin status of GPIO70_IN ~ GPIO77_IN as the value in index 0x82

GPIO6 Data Port — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO6_DATA	R/W	LRESET#	-	GPIO6 Data Control Write data to this byte will change the value of GPIO60_VAL ~ GPIO67_VAL in configuration register as writing data to index 0x91. Read data from this byte will read the pin status of GPIO60_IN ~ GPIO67_IN as the value in index 0x92

GPIO5 Data Port — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO5_DATA	R/W	LRESET#	-	GPIO5 Data Control Write data to this byte will change the value of GPIO50_VAL ~ GPIO57_VAL in configuration register as writing data to index 0xA1. Read data from this byte will read the pin status of GPIO50_IN ~ GPIO57_IN as the value in index 0xA2

GPIO0 Data Port — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO0_DATA	R/W	5VSB	-	GPIO0 Data Control Write data to this byte will change the value of GPIO00_VAL ~ GPIO07_VAL in configuration register as writing data to index 0xF1. Read data from this byte will read the pin status of GPIO00_IN ~ GPIO07_IN as the value in index 0xF2

GPIO1 Data Port — Offset 07h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO1_DATA	R/W	5VSB	-	GPIO1 Data Control Write data to this byte will change the value of GPIO10_VAL ~ GPIO17_VAL in configuration register as writing data to index 0xE1. Read data from this byte will read the pin status of GPIO10_IN ~ GPIO17_IN as the value in index 0xE2

***GPIO2 Data Port — Offset 08h**

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO2_DATA	R/W	5VSB	-	GPIO2 Data Control, this byte is available when GPIODEC_RANGE is set. Write data to this byte will change the value of GPIO20_VAL ~ GPIO27_VAL in configuration register as writing data to index 0xD1. Read data from this byte will read the pin status of GPIO20_IN ~ GPIO27_IN as the value in index 0xD2

***GPIO3 Data Port — Offset 09h**

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO3_DATA	R/W	LRESET#	-	GPIO3 Data Control, this byte is available when GPIODEC_RANGE is set. Write data to this byte will change the value of GPIO30_VAL ~ GPIO37_VAL in configuration register as writing data to index 0xC1. Read data from this byte will read the pin status of GPIO30_IN ~ GPIO37_IN as the value in index 0xC2

GPIO4 Data Port — Offset 0Ah

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO4_DATA	R/W	LRESET#	-	GPIO4 Data Control, this byte is available when GPIODEC_RANGE is set. Write data to this byte will change the value of GPIO40_VAL ~ GPIO47_VAL in configuration register as writing data to index 0xB1. Read data from this byte will read the pin status of GPIO40_IN ~ GPIO47_IN as the value in index 0xB2

6.6.2 GPIOx status

- Z means high impendence.
- If the external circuit is pull high then the pin status is "H"; else if the external circuit is pull low then the pin status is "L".
- User define means by programming the configure register.

GPIO0x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
52	GPIO00	L	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
53	GPIO01	L	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
54	GPIO02	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
55	GPIO03	L	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
56	GPIO04	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
57	GPIO05	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
58	GPIO06	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
59	GPIO07	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V

GPIO1x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
65	GPIO10	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
66	GPIO11	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
67	GPIO12	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
68	GPIO13	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
69	GPIO14	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
70	GPIO15	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
71	GPIO16	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
72	GPIO17	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V

GPIO2x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
76	GPIO20	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
77	GPIO21	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
78	GPIO22	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
79	GPIO23	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
80	GPIO24	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
81	GPIO25	Z	user define	user define	user define	I_VSB3V	5VSB	I_VSB3V
82	GPIO26	L	user define	user define	user define	I_VSB3V	5VSB	VBAT
83	GPIO27	L	user define	user define	user define	I_VSB3V	5VSB	VBAT

* GPIO26 and GPIO27 have no push pull function.

GPIO3x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
36	GPIO30	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
37	GPIO31	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
38	GPIO32	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
39	GPIO33	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
40	GPIO34	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
41	GPIO35	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
42	GPIO36	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
43	GPIO37	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC

GPIO4x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
44	GPIO40	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
45	GPIO41	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
46	GPIO42	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
47	GPIO43	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
48	GPIO44	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
49	GPIO45	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
50	GPIO46	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
51	GPIO47	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC

GPIO5x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
9	GPIO50	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
10	GPIO51	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
11	GPIO52	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
12	GPIO53	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
13	GPIO54	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
14	GPIO55	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
15	GPIO56	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
16	GPIO57	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC

GPIO6x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
17	GPIO60	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
18	GPIO61	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
19	GPIO62	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
20	GPIO63	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
21	GPIO64	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
74	GPIO65	Z	user define	Z	Z	I_VSB3V	LRESET# *	I_VSB3V
86	GPIO66	L	user define	Z	Z	I_VSB3V	LRESET# *	VBAT
87	GPIO67	Z	user define	Z	Z	I_VSB3V	LRESET# *	VBAT

* GPIO66 and GPIO67 have no push pull function.

GPIO7x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
103	GPIO70	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
104	GPIO71	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
105	GPIO72	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
106	GPIO73	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
107	GPIO74	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
108	GPIO75	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
109	GPIO76	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
110	GPIO77	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC

GPIO8x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
111	GPIO80	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
112	GPIO81	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
113	GPIO82	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
114	GPIO83	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
115	GPIO84	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
116	GPIO85	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
117	GPIO86	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC
118	GPIO88	Z	user define	Z	Z	I_VSB3V	LRESET#	3VCC

6.7 Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depend on register setting.

The time unit has two ways from 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Others, please refer the device register description as below.

Watchdog Timer Configuration Register 1— base address + 05h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R	-	0	Reserved
6	WDTMOUT_STS	R/W	5VSB	0	If watchdog timeout event occurred, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	5VSB	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	5VSB	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	5VSB	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	5VSB	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	5VSB	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

Watchdog Timer Configuration Register 2 — base address + 06h

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME	R/W	5VSB	0	Time of watchdog timer

Watchdog PME Control Register — base address + 0Ah

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME	R	5VSB	--	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	5VSB	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5-1	Reserved	--		--	Reserved.
0	WDOUT_EN	R/W	5VSB	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.

6.8 ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

ACPI includes three sub items as below:

1. Power Control (Include wake up via sleep state, wake up stage detection, AC loss & resume control methods)
2. Intel Power Saving Function (Deep Sleep Well, DSW: see next section for the detail)
3. EU Power Saving Function (EUP/ERP Command Lot 6.0: see next section for the detail)

Where item 2 & 3 could be coexisted via ERP_CTRL0# (follow SLP_SUS#) & ERP_CTRL1# (After the system enters S3 1.024s & S5 6.4s, EUP/ERP mode could be achieved).

Before entering into the main section, let's check out the related hardware control signal first.

Control Signal	Power On/Off Control (AC Resume)	Power Management Event	Wake up	Intel DSW Hand Shaking	EUP/ERP Control
RSMRST#	◇				
S3#	◇				
S5#	◇				
PWSIN#	◇				
PWSOUT#	◇		☆★		
ATXPG_IN	◇				
PS_ON#	◇				
PWOK	◇				
PME#		◇	☆★		
PS/2 KB/MS			☆★		
RI1#/RI2#			☆★		
GPIO0x/GPIO1x			☆★		
SLP_SUS#				◇	
SUS_ACK#				◇	
SUS_WARN#				◇	
ERP_CTRL0#				◇	◇
ERP_CTRL1#					◇

◇: Supported

★: Wake up via ERP

☆: Wake up via System

6.8.1 Power Control

6.8.1.1 Wake Up Via Sleep State

When the system is at the normal sleep state (S3, S4, S5) or deep sleep (G3') state, F81867 could wake up via PWSOUT# & PME#. See below for the related registers:

Wake up by PME#	Index 0x2D		CR0A Index 0xE0, 0xE8	CR0A Index 0xF0~0xF3
Normal Sleep State	◇			◇
EUP/ERP	◇		◇	
Wake up by PWSOUT#	**Index 0x2D**	**CR 0A Index 0x30**	**CR0A Index 0xE0, 0xE8**	**CR0A Index 0xF4**
Normal Sleep State	◇	◇		◇
EUP/ERP	◇	◇	◇	

◇: Supported

6.8.1.2 Wake Up Stage Detection

F81867 is counted on the chipset SLP_S3#, SLP_S4#/SLP_S5# stage, to decide the wake up stage as below:

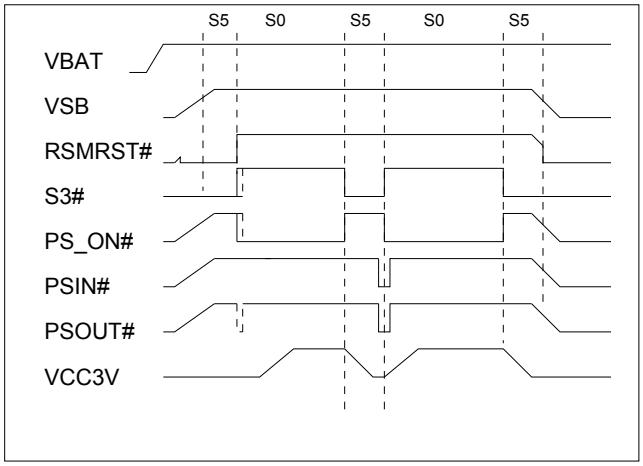
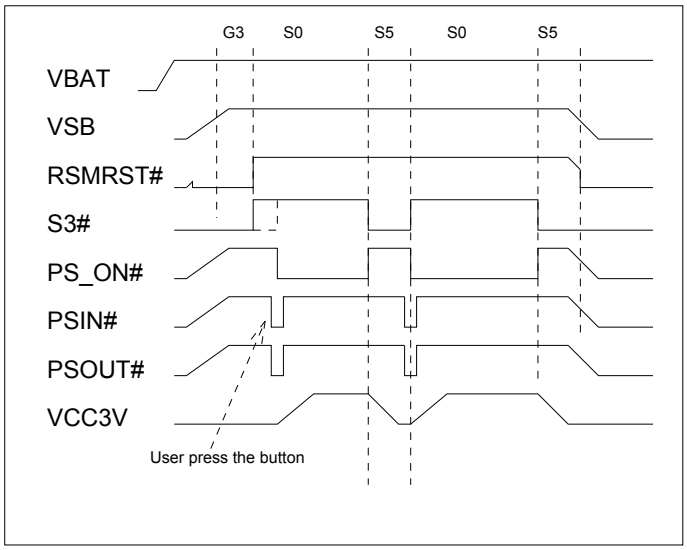
ACPI Stage	SLP_S3#	SLP_S4# /SLP_S5#
S0	H	H
S3	L	H
S5	L	L

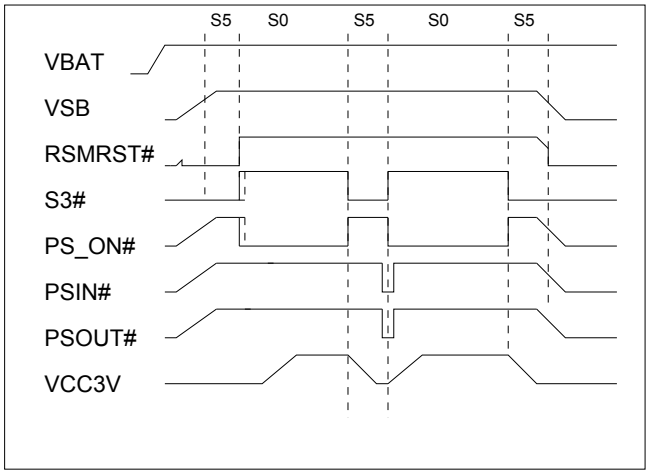
H: High; L: Low

Power saving mode would be activated via CR0A index E0 bit 7.

6.8.1.3 AC Loss & Resume Control Methods

There are 4 modes under power loss state via setting ACPI control register. The always on, always off, keep last state & bypass mode. In keep last state mode, one register will latch the status before power loss. If it is power on before power loss, it will automatically power on when power is resumed. If it is power off before power loss, it will remain power off when power is resumed. See below for the detail:

Mode	Explanation
Always on (S0)	When AC resume, the system will power on automatically (send a PWSOUT# low pulse and then sinking the PS_ON# low). See below for the timing: 
Always off (S5)	When AC resume, the system is in off state and waiting for the wakeup events. See below for the timing: 
Bypass (follow the	When AC resume, inverting the S3 signal to PS_ON#. See below for the timing:

<table>
<tr><td>chipset after G3 stage)</td><td> 
</td></tr>
<tr><td>Keep last state</td><td>ATXPG_IN, VCC (PWOK), VSB (RSMRST) and S3 signals to detect the sleep state while AC loss occur. One of the signal (ATXPG_IN or VCC under 2.8V or VSB under 2.8V) sinks low, SIO will latch the S3 signal to decide the system to be at “always on” or “always off” mode. See below table:
<table>
<tr><th>Signal
AC loss state</th><th>ATXPG</th><th>VSB</th><th>VCC</th><th>AC resume</th></tr>
<tr><td>AC loss in S0/S1 (S3=1)</td><td>  </td><td>  </td><td>  </td><td>Always on</td></tr>
<tr><td>AC loss in S3/S4/S5 (S3=0)</td><td>  </td><td>  </td><td>  </td><td>Always off</td></tr>
</table></td></tr>
</table>

6.8.2 Intel Power Saving Function Deep Sleep Well (DSW)

The F81867 supports Intel Cougar Point (CPT) Chipset timing for Sandy Bridge (Sugar Bay or Huron River Platform). There are 4 pins for CPT control: SUS_WARN#, SUS_ACK#, SLP_SUS# and DPWROK.

For entering the Intel Deep Sleep Well (DSW) state, the PCH will assert SUS_WARN# (low level) and turn off 5VDUAL. After the level of 5VDUAL is lower than 1.05V, F81867 will assert SUS_ACK# to inform PCH it is ready for entering DSW. Finally, PCH will ramp down the internal VccSUS and assert SLP_SUS# to F81867. F81867 will turn off the 5VSB and 3VSB by ERP_CTRL0# and enter the DSW state.

To exit DSW state, PCH will de-assert SLP_SUS#, turn on the SUS rail FETs and ramp up internal 1.05V VccSUS. After the SUS rails voltages are up, RSMRST# will be desserted and the PCH will release SUS_WARN# so that the 5VDUAL will ramp up.

Because the DSW function is controlled by the F81867 instead of controlled by the PCH directly, there will be more wakeup events such as LAN, KB/Mouse, GPIO0x, GPIO1x, SIO RI# wake up rather than the 3 wakeup events (RTC, Power Button and GPIO27) for Intel DSW.

In order to achieve the lower power consumption, F81867 provides the ERP_CTRL1# to turn off the V3A so that the system can enter the Fintek G3' state.

The block diagram below shows how the connection and control method for F81867 and PCH.

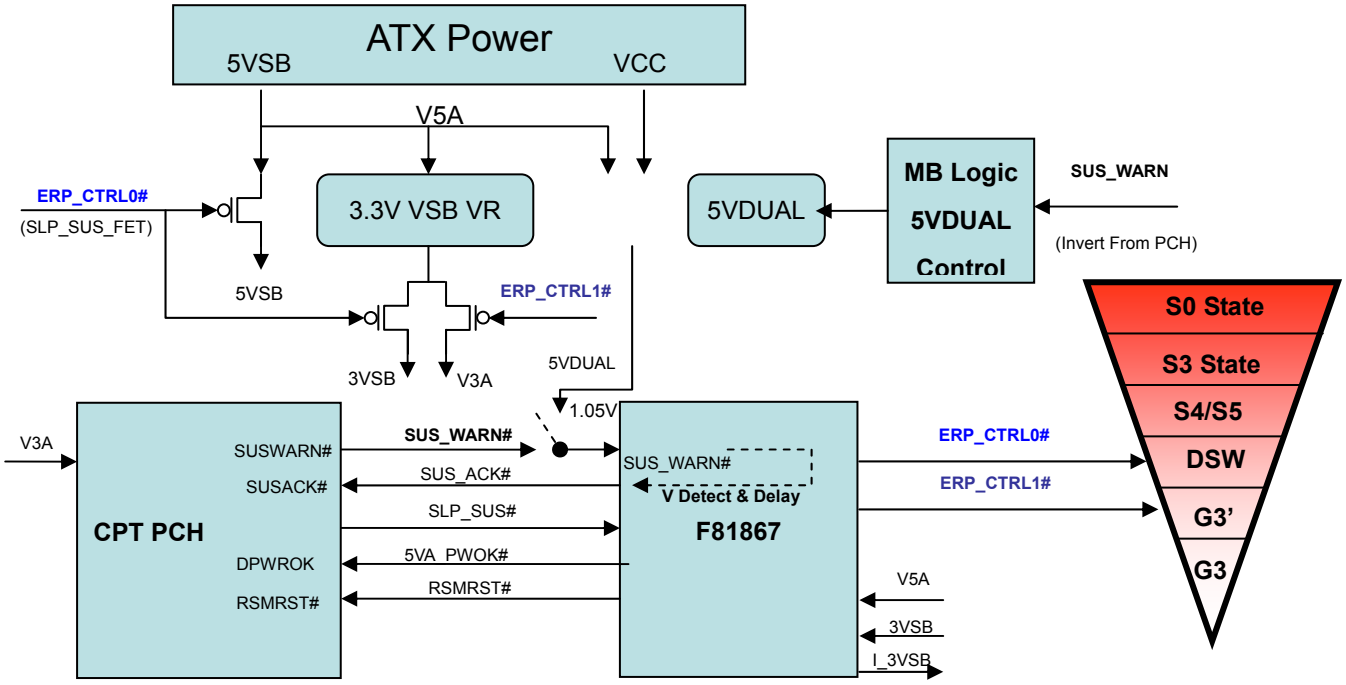


Fig 6-17

The register for setting this mode is at CR0A, index 0xEC [7:6]. When choose Intel DSW mode, ERP_CTRL0#, & ERP_CTRL1# would follow SLP_SUS#. When choose Intel DSW + Fintek G3' mode, ERP_CTRL0# would follows SLP_SUS#, & ERP_CTRL1# will enter Fintek ERP mode after entering DSW mode for 6.4s (default, the time is programmable).

In sum, there are three blocks in this mode (Please refer to the application circuit for the HW schematic):

a. DSW Control Block:

a-1 SLP_SUS#: SIO input pin from CPT PCH SLP_SUS#.

a-2 SUS_WARN#: SIO input pin from CPT PCH SUS_WARN#.

a-3 SUS_ACK#: SIO output pin to CPT PCH SUSACK#.

a-4 DPWROK: SIO output pin to CPT PCH DPWROK.

b. ERP Control Block:

b-1 ERP_CTRL0#: Support "CPT PCH DSW" control mode which is a low active signal to turn on/off 3VSB/5VSB power source by P MOSFET.

b-2 ERP_CTRL1#: Support "Fintek G3' " control mode which is a low active signal to turn on/off 3VA/5VA power source by P MOSFET.

c. Wake Up Event Block:

Power Button	External LAN	PCH Internal LAN	PS2 KB/Mouse	SIO RI#	RTC	GPIO0x/1x
V	V	X	V	X	X	V

Note:

By pressing/triggering any of the above pin, the system could wake up from the sleep (S4/S5) DSW and G3' mode.

V: Supported.

X: does not supported.

6.8.3 Power Saving Controller (Fintek ERP Mode)

The two pins, ERP_CTRL0# and ERP_CTRL1#, which control the standby power rail on/off to fulfill the purpose which decreases the power consumption when the system is in the sleep state or the soft-off state. These two pins connected to the external PMOSs and the defaults are high in the sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, the two pins can be programmable to set which power rail to turn on. The programmable register is powered by the battery. So, the setting is kept even the AC power is lost when the register is set. At the power saving state (FINTEK calls it G3' state), the F81867 consumes 5VSB power rail only to realize a low power consumption system.

The register for setting this mode is at CR0A, index 0xEC [7:6]. When choose Fintek G3' mode, ERP_CTRL0# & ERP_CTRL1# will enter S5. After entering S5 for 6.4s (default, the time is programmable), these two pins would send high level signal and then cut off all the power sources except ATX_5VSB (power consumption is about 15mW). In order to avoid the inrush current from ATX_5VSB, F81867 also provide the soft start circuits at these two pins. See the related register for the soft start circuit (CR0A, index 0xEC [4]).

In sum, there are two blocks in this mode (Please refer to the application circuit for the HW schematic):

a. EUP Control Block:

ERP_CTRL0# and ERP_CTRL1# are low active signals to turn on/off 5VSB power source by P MOSFET.

b. Wake Up Event Block via:

Power Button	External LAN	PCH Internal LAN	PS2 KB/Mouse	SIO RI#	RTC	GPIO0x/1x
V	V	X	V	V	X	V

Note:

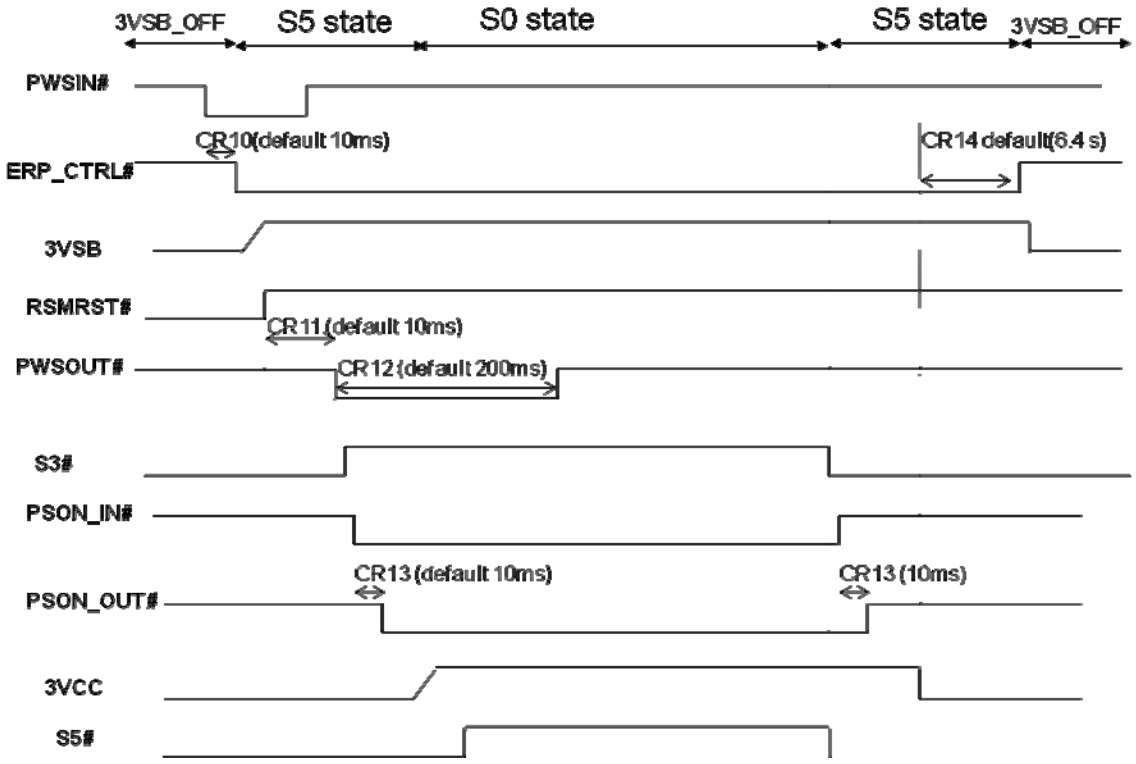
By pressing/triggering any of the above pin, the system could wake up from the sleep (S4/S5) DSW and G3' mode.

V: Supported.

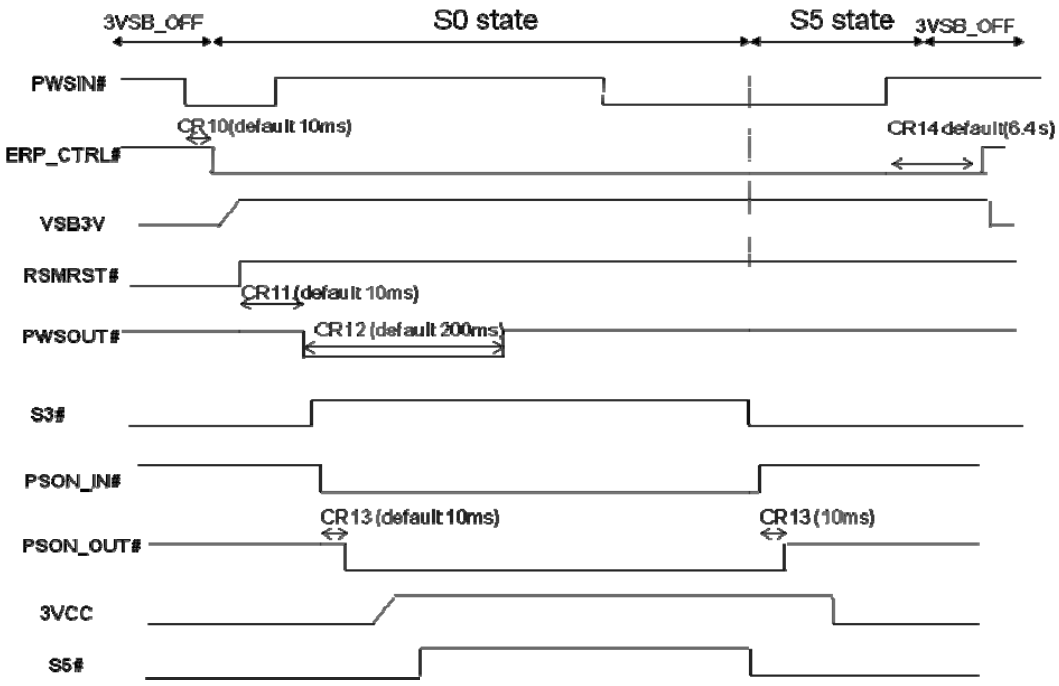
X: Does not supported.

Please see below for Fintek G3' (ERP) timing:

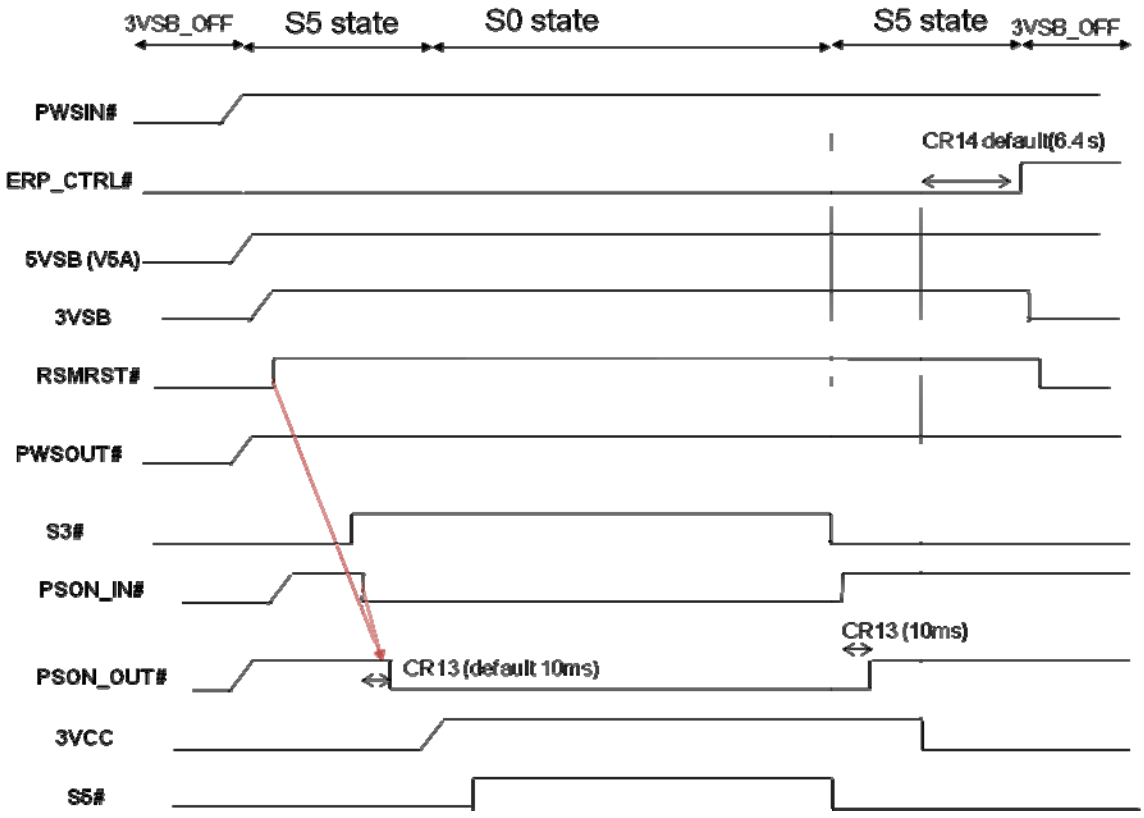
Boot From 3VSB OFF



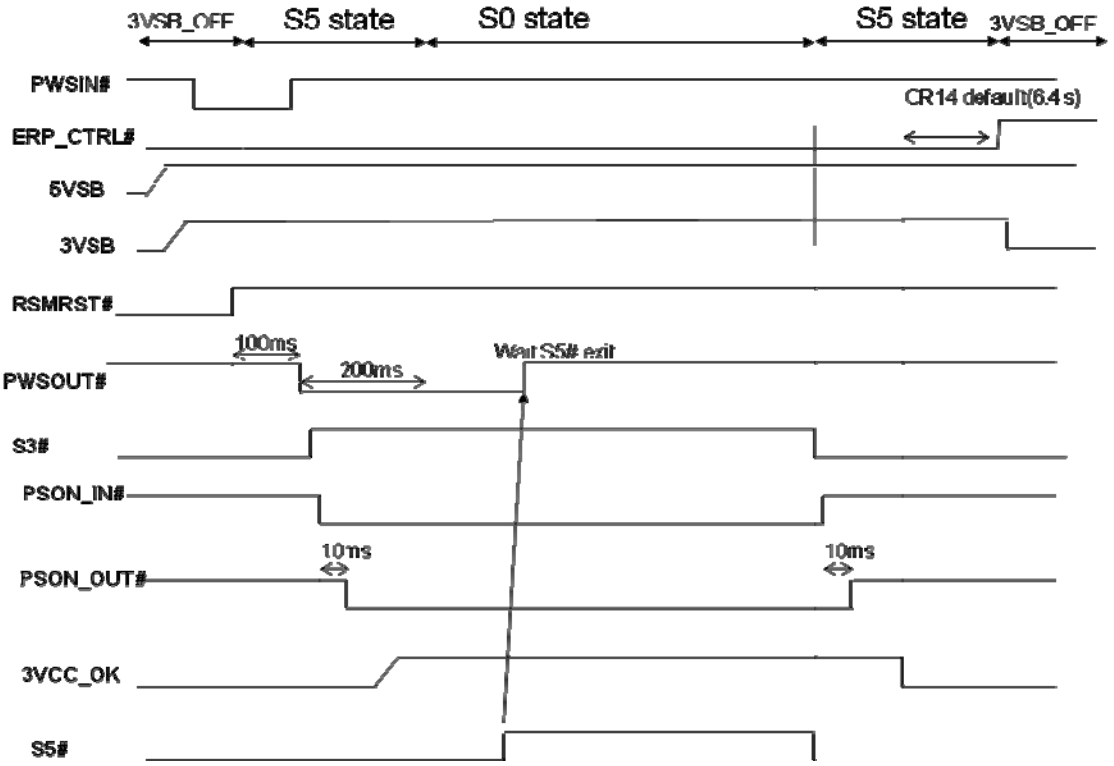
PWSIN# Gating 3VSB OFF



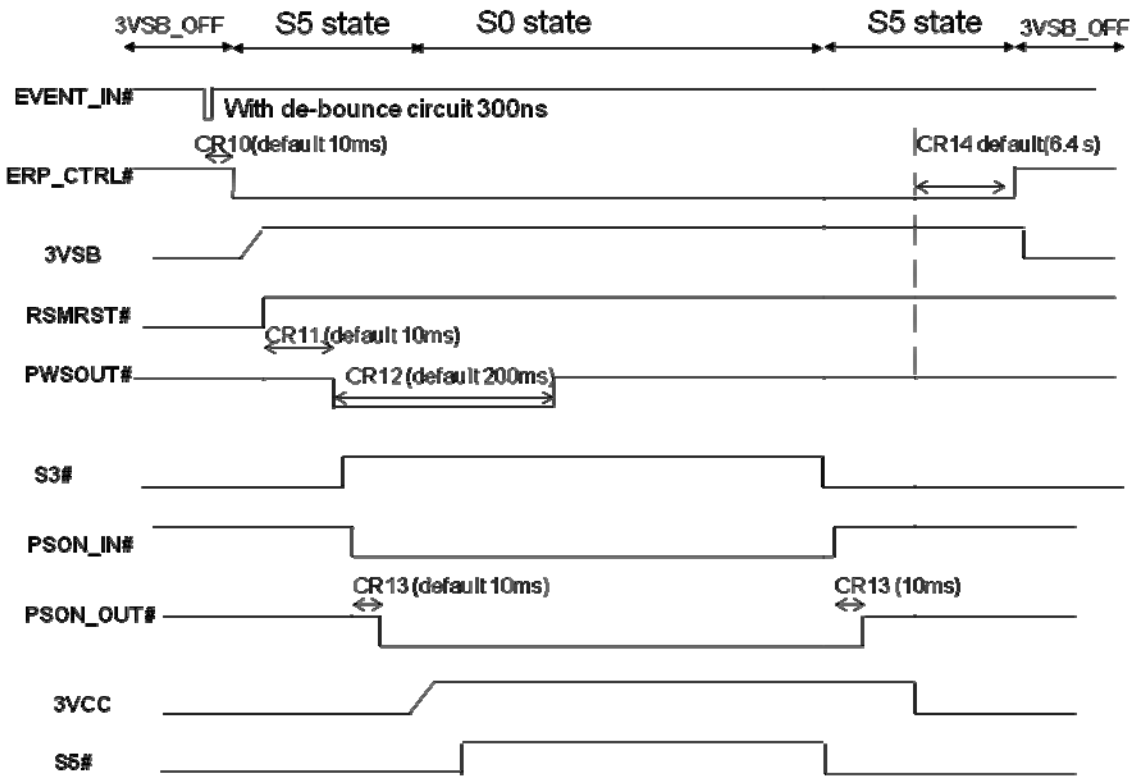
Boot From 5VSB (V5A) AC Lost & Always On



Boot From 5VSB AC Lost & Always Off



Boot From 3VSB OFF By EVENT_IN#



` EVENT_IN# means wake up via GPIO 0x, GPIO 1x, RI#...

6.8.4 ACPI Timing

See below for the related ACPI timing:

6.8.4.1 G3 To S0

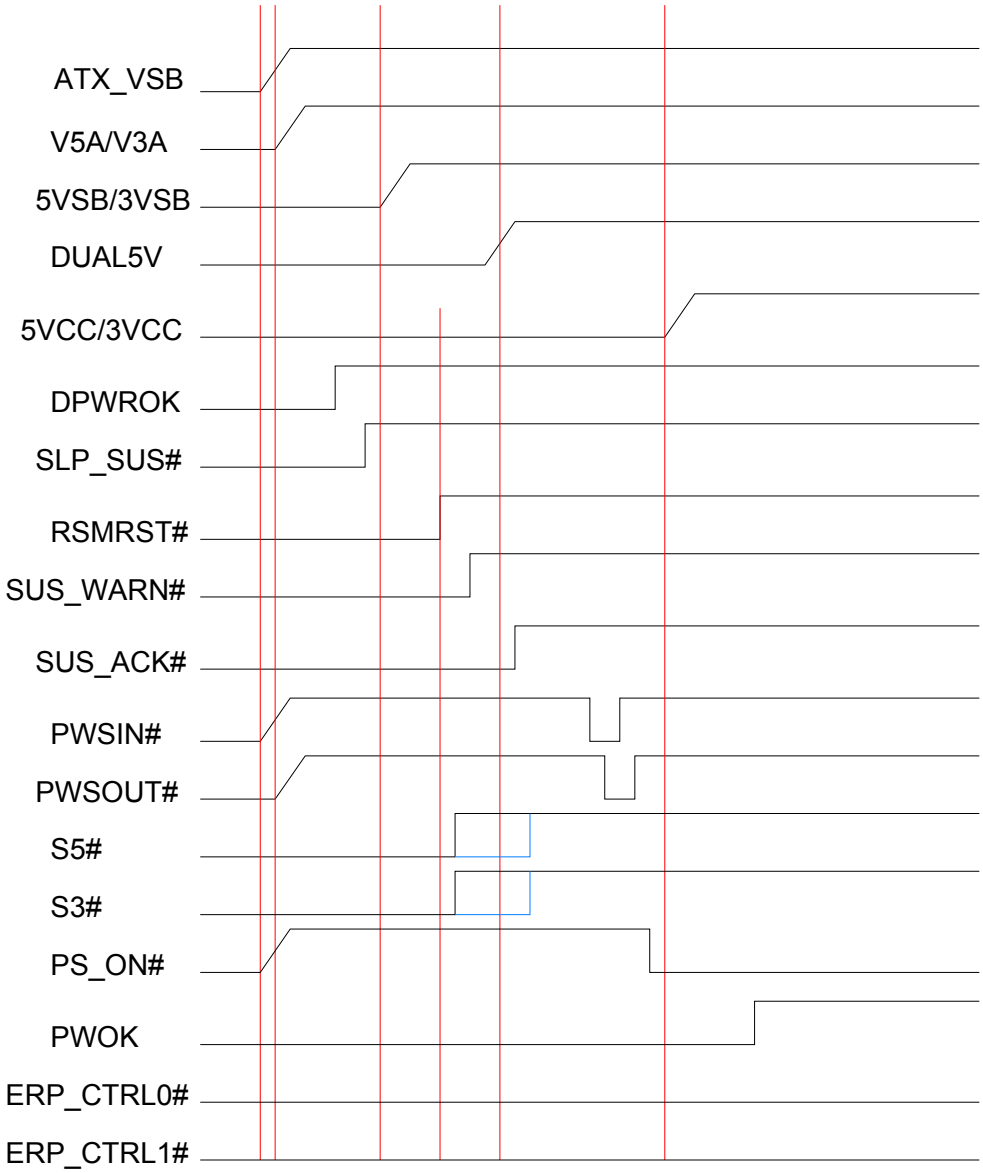


Fig 6-18

6.8.4.2 G3 To S0 (only DSW)

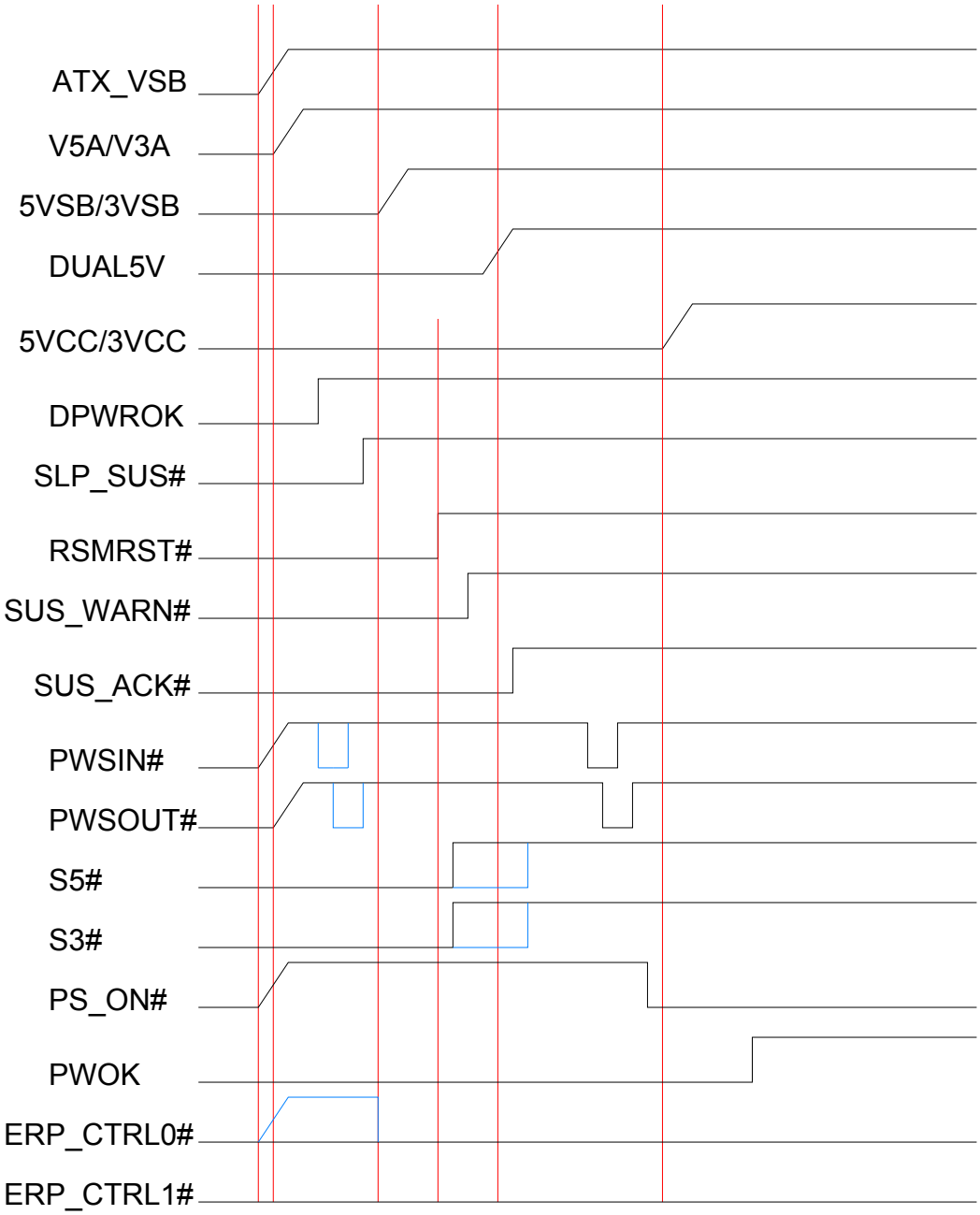


Fig 6-19

6.8.4.3 G3 To S0 (DSW & ERP, AC Resume Green Bold Line)

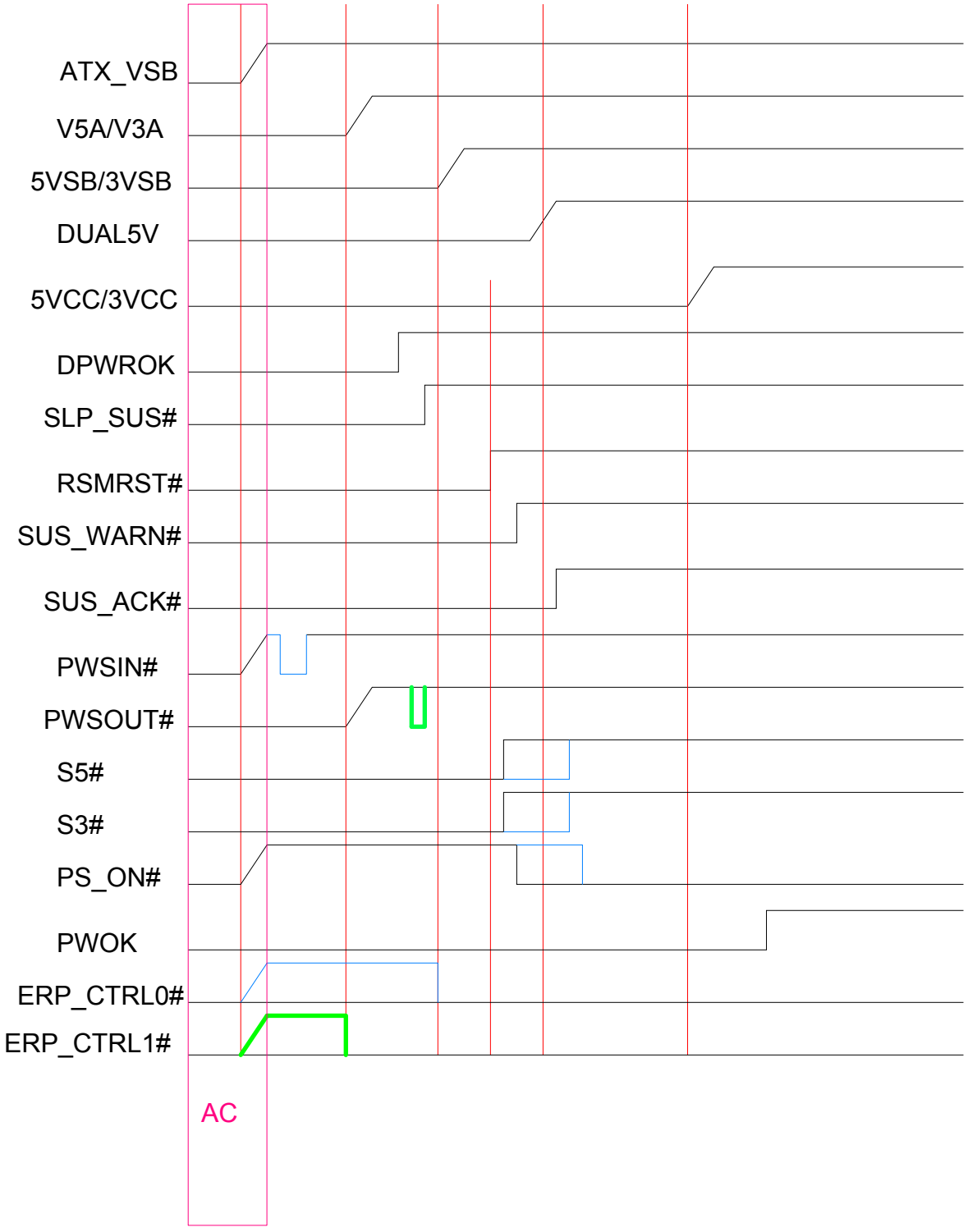


Fig 6-20

6.8.4.4 DSW To S0

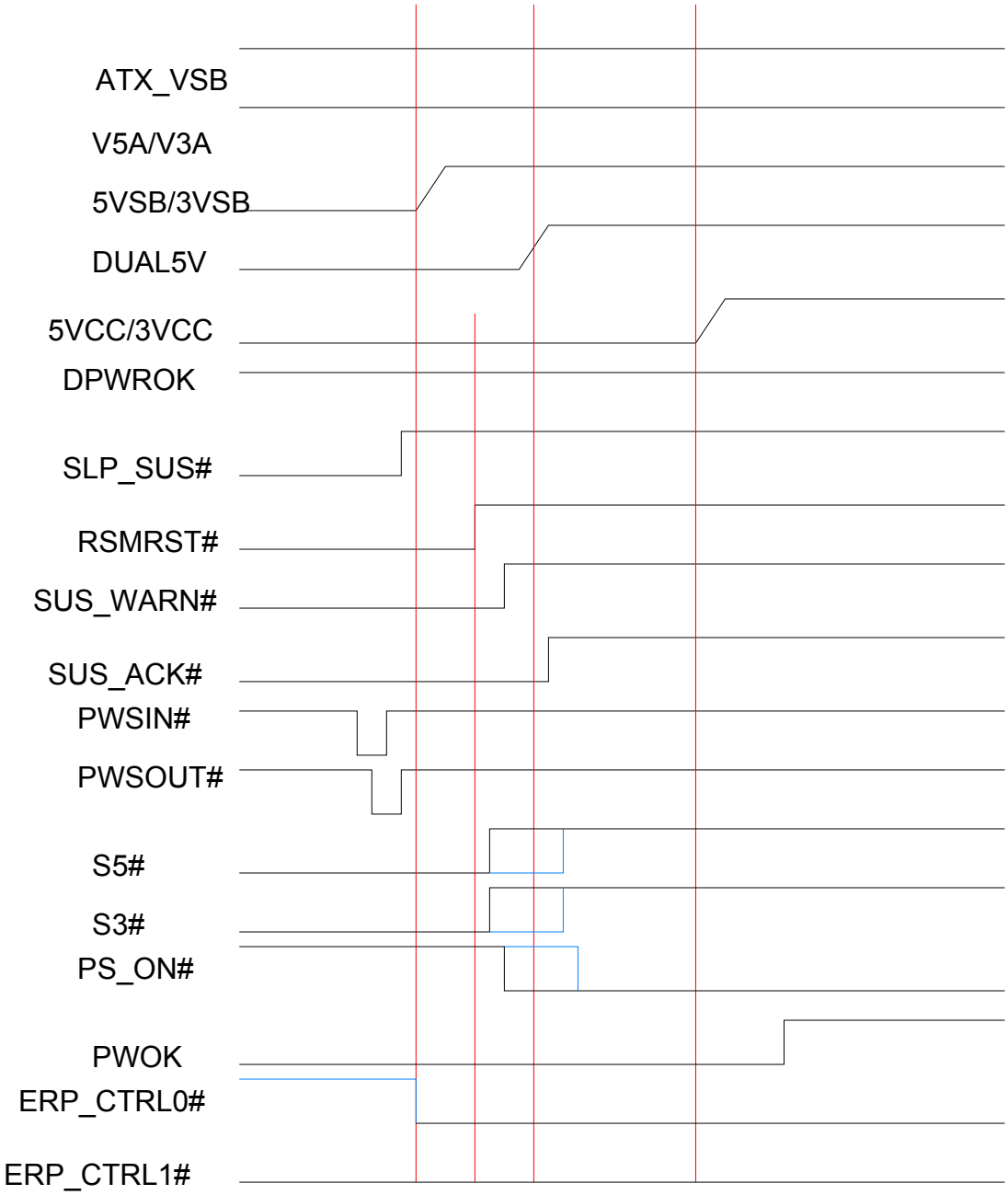


Fig 6-21

6.8.4.5 S0 to DSW

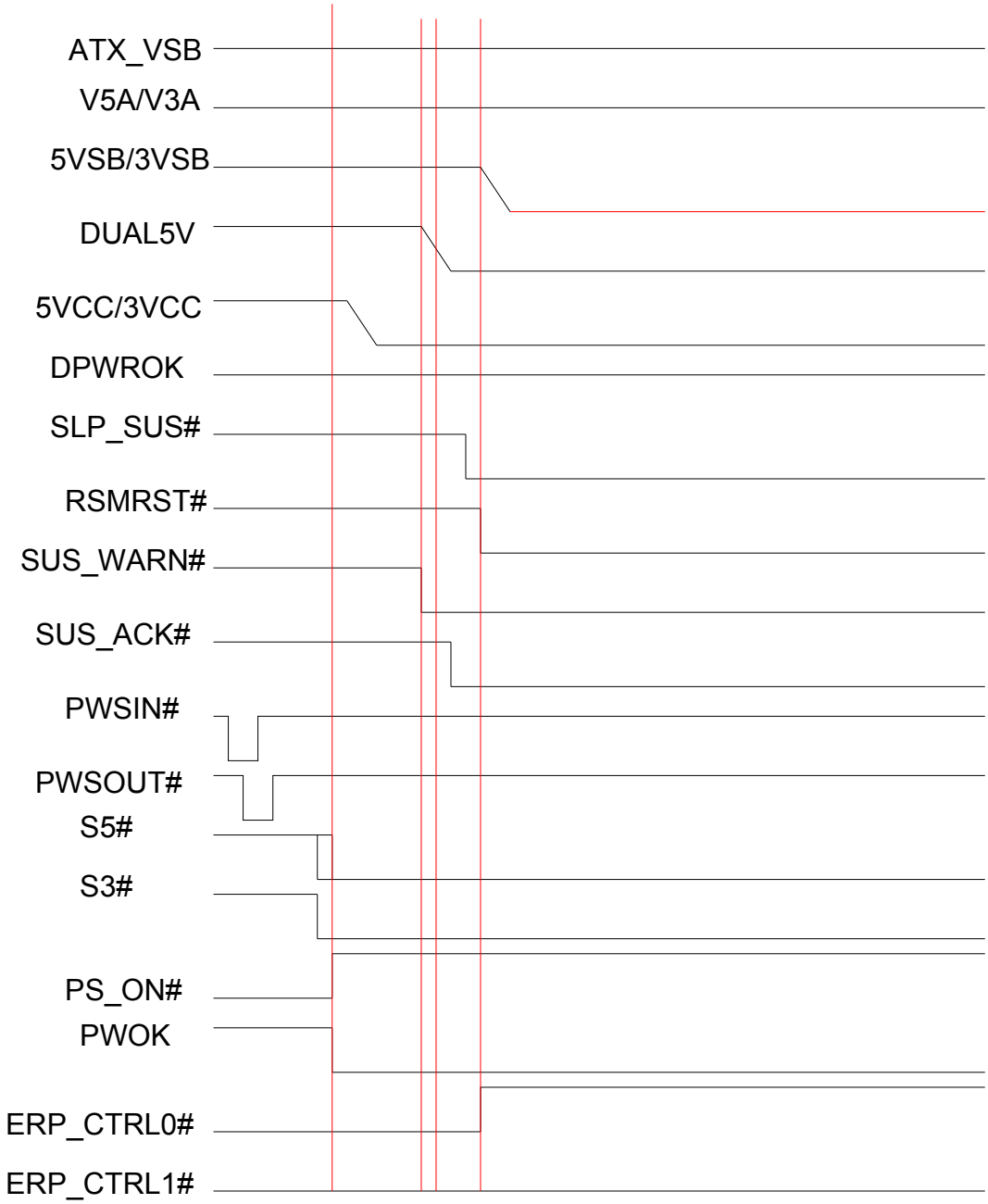


Fig 6-22

6.8.4.6 S0 to G3'

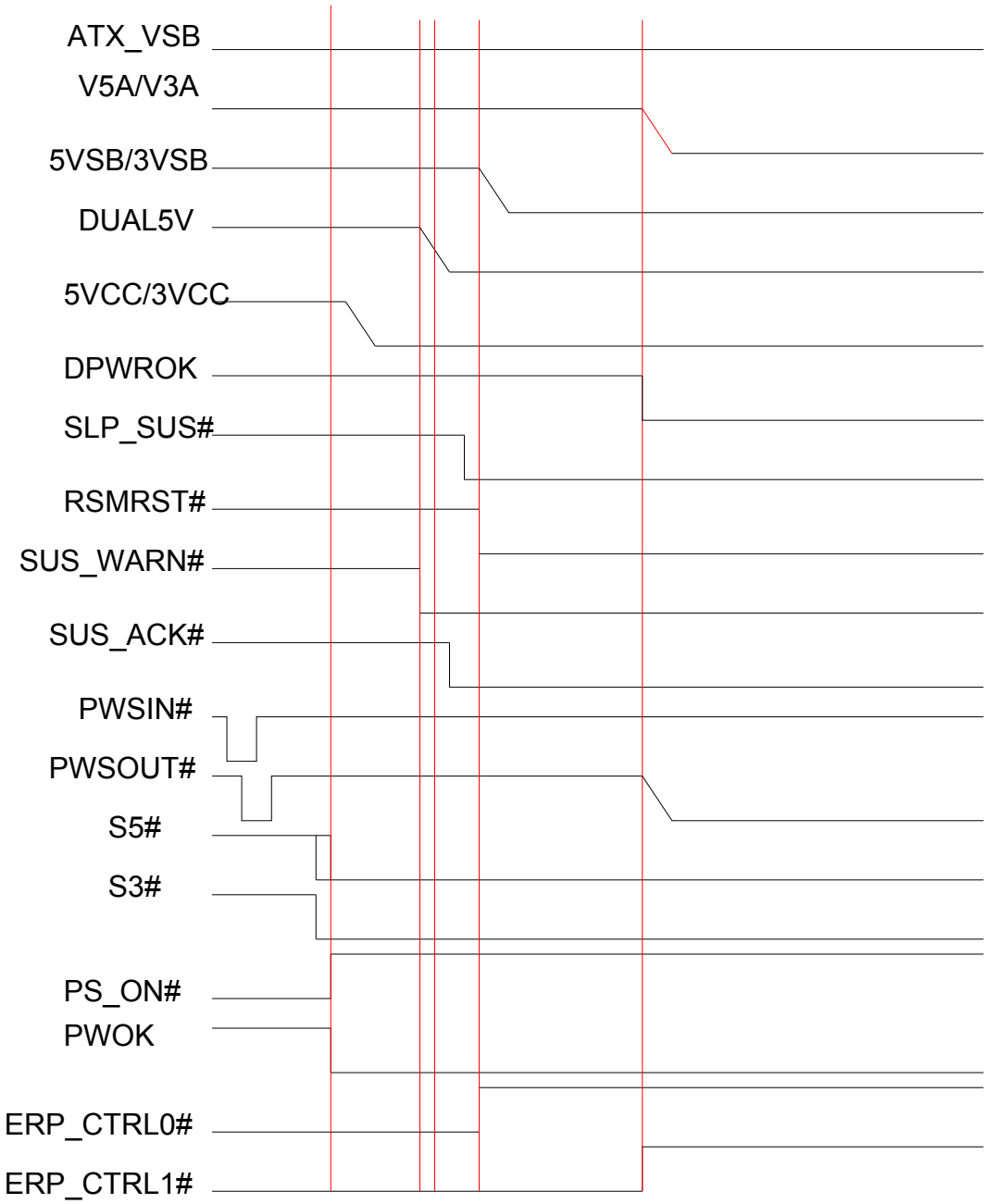


Fig 6-23

- RSMRST# signal: Powered by VBAT sink low.
- DPWROK/PWOK signal: Powered by VBAT sink low.
- 3VSB 2.8V/2.5V and gate SLP_SUS#/DPWROK for Intel mode

PWROK Signals

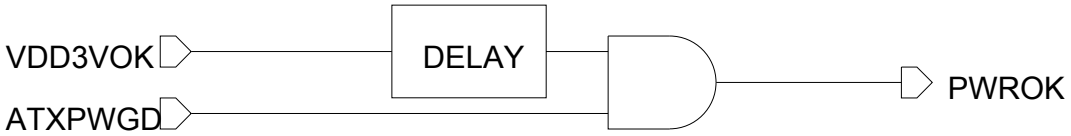


Fig 6-24

PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed via register (100ms ~ 400ms).

6.9 UART

The F81867 provides up to 6 UART ports and supports IRQ sharing for system application. They are compatible with 16C550/16C650/16C750 and 16C850 .The UARTs are used to convert data between parallel format and serial format. They convert parallel data into serial format on transmission and serial format into parallel data on receiver side. The serial format is formed by one start bit, followed by five to eight data bits, a parity bit if programmed and one (1.5 or 2) stop bits. The UARTs include complete modem control capability and an interrupt system that may be software trailed to the computing time required to handle the communication link. They have FIFO mode to reduce the number of interrupts presented to the host. Both receiver and transmitter have a 128-byte FIFO.

The UART control register control & define the asynchronous protocol data communications including data length, stop bit, parity & baud rate selection.

The below content is about the UARTs device register descriptions. All the registers are for software porting reference.

Receiver Buffer Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	RBR	R	LRESET#	00h	The data received. Read only when LCR [7] is 0

Transmitter Holding Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	THR	W	LRESET#	00h	Data to be transmitted. Write only when LCR [7] is 0

Divisor Latch (LSB) — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	DLL	R/W	LRESET#	01h	Baud generator divisor low byte. Access only when LCR [7] is 1.

Divisor Latch (MSB) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-0	DLM	R/W	LRESET#	00h	Baud generator divisor high byte. Access only when LCR [7] is 1.

Interrupt Enable Register (IER) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4	SM2	R/WC	LRESET#	0	This bit is used only in 9-bit mode and always returns “0” when 9-bit mode is disabled. 0: The receiver could receive data byte. 1: The receiver could only receive address byte and issue an interrupt when the address is received.
3	EDSSI	R/W	LRESET#	0	Enable Modem Status Interrupt. Access only when LCR [7] is 0.
2	ELSI	R/W	LRESET#	0	Enable Line Status Error Interrupt. Access only when LCR [7] is 0.
1	ETBFI	R/W	LRESET#	0	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR [7] is 0.
0	ERBFI	R/W	LRESET#	0	Enable Received Data Available Interrupt. Access only when LCR [7] is 0.

Interrupt Identification Register (IIR) — Base + 2

Bit	Name	R/W	Reset	Default	Description
7	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
6	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
5-4	Reserved	-	LRESET#	-	Reserved.
3-1	IRQ_ID	R	LRESET#	00	000: Interrupt is caused by Modem Status 001: Interrupt is caused by Transmitter Holding Register Empty 010: Interrupt is caused by Received Data Available. 110: Interrupt is caused by Character Timeout 011: Interrupt is caused by Line Status.
0	IRQ_PENDN	R	LRESET#	1	1: Interrupt is not pending. 0: Interrupt is pending.

FIFO Control Register — Base + 2

Bit	Name	R/W	Reset	Default	Description
7-6	RCV_TRIG	W	LRESET#	00	00: Receiver FIFO trigger level is 1. 01: Receiver FIFO trigger level is 4. 10: Receiver FIFO trigger level is 8. 11: Receiver FIFO trigger level is 14.
5-3	Reserved	-	LRESET#	-	Reserved.
2	CLRTX	R	LRESET#	0	Reset the transmitter FIFO.
1	CLRRX	R	LRESET#	0	Reset the receiver FIFO.
0	FIFO_EN	R	LRESET#	0	0: Disable FIFO. 1: Enable FIFO.

Line Control Register (LCR) — Base + 3

Bit	Name	R/W	Reset	Default	Description
7	DLAB	R/W	LRESET#	0	0: Divisor Latch can't be accessed. 1: Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	LRESET#	0	0: Transmitter is in normal condition. 1: Transmit a break condition.
5	STKPAR	R/W	LRESET#	0	XX0: Parity Bit is disable 001: Parity Bit is odd. 011: Parity Bit is even 101: Parity Bit is logic 1 111: Parity Bit is logic 0
4	EPS	R/W	LRESET#	0	
3	PEN	R/W	LRESET#	0	
2	STB	R/W	LRESET#	0	0: Stop bit is one bit 1: When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1-0	WLS	R/W	LRESET#	00	00: Word length is 5 bit 01: Word length is 6 bit 10: Word length is 7 bit 11: Word length is 8 bit

MODEM Control Register (MCR) — Base + 4

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	LRESET#	-	Reserved.
4	LOOP	R/W	LRESET#	0	0: UART in normal condition. 1: UART is internal loop back
3	OUT2	R/W	LRESET#	0	0: All interrupt is disabled. 1: Interrupt is enabled (disabled) by IER.
2	OUT1	R/W	LRESET#	0	Read from MSR[6] while in loop back mode
1	RTS	R/W	LRESET#	0	0: RTS# is forced to logic 1 1: RTS# is forced to logic 0
0	DTR	R/W	LRESET#	0	0: DTR# is forced to logic 1 1: DTR# is forced to logic 0

Line Status Register (LSR) — Base + 5

Bit	Name	R/W	Reset	Default	Description
7	RCR_ERR	R	LRESET#	0	0: No error in the FIFO when FIFO is enabled 1: Error in the FIFO when FIFO is enabled.
6	TEMT	R	LRESET#	1	0: Transmitter is in transmitting. 1: Transmitter is empty.
5	THRE	R	LRESET#	1	0: Transmitter Holding Register is not empty. 1: Transmitter Holding Register is empty.
4	BI	R	LRESET#	0	0: No break condition detected. 1: A break condition is detected.
3	FE	R	LRESET#	0	0: Data received has no frame error. 1: Data received has frame error.
2	PE	R	LRESET#	0	0: Data received has no parity error. 1: Data received has parity error.
1	OE	R	LRESET#	0	0: No overrun condition occurred. 1: An overrun condition occurred.
0	DR	R	LRESET#	0	0: No data is ready for read. 1: Data is received.

MODEM Status Register (MSR) — Base + 6

Bit	Name	R/W	Reset	Default	Description
7	DCD	R	-	-	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	-	-	Complement of RI# input. In loop back mode , this bit is equivalent to OUT1 in MCR
5	DSR	R	-	-	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	-	-	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	LRESET#	0	0: No state changed at DCD#. 1: State changed at DCD#.
2	TERI	R	LRESET#	0	0: No Trailing edge at RI#. 1: A low to high transition at RI#.
1	DDSR	R	LRESET#	1	0: No state changed at DSR#. 1: State changed at DSR#.
0	DCTS	R	LRESET#	1	0: No state changed at CTS#. 1: State changed at CTS#.

Scratch Register — Base + 7

Bit	Name	R/W	Reset	Default	Description
7-0	SCR	R/W	LRESET#	00h	Scratch register.

Programmable Baud Rate

The below table shows the use of baud generator with the different frequency 1.8461 MHZ, 14.769 MHZ, 24MHZ:

$$BaudRate = \frac{\text{COM\_CLK}}{\text{Divisor} * 16}$$

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461MHz	PRE-DIV: 1.625 14.769MHz	PRE-DIV: 1.0 24MHz	DECIMAL DIVISOR USED TO GENRATE 16X CLOCK	ERROR PERCENTAGE
50	400	650	2308	0
75	600	975	1538	0
110	880	1430	1049	0
135	1080	1755	855	0
150	1200	1950	769	0
300	2400	3900	385	0
600	4800	7800	192	0
1200	9600	15600	96	0
1800	14400	23400	64	0.01%
2000	16000	26000	58	0.01%
2400	19200	31200	48	0.01%
3600	28800	46800	32	0.01%
4800	38400	62400	24	0.01%
7200	57600	93600	16	0.01%
9600	76800	124800	12	0.01%
19200	153600	249600	6	0.01%
38400	307200	499200	3	0.01%
57600	460800	748800	2	0.01%
115200	921600	1497600	1	0.01%

Fig 6-25

6.10 AMD TSI and Intel PECI 3.0 Functions

The F81867 provides Intel PECI/AMD TSI interfaces for new generational CPU temperature sensing. In AMD TSI interface, there are SIC and SID signals for temperature information reading from AMD CPU. The SIC signal is for clocking use, the other is for data transferring. More detail, please refer register description.

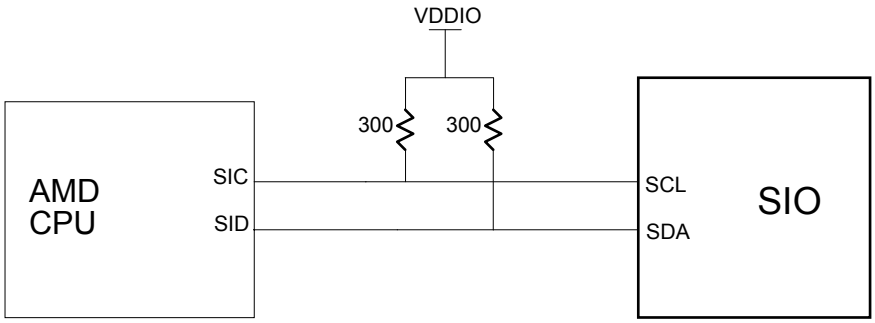


Fig 6-26 AMD TSI

In Intel PECI interface, the F81867 can connect to the CPU directly. The F81867 can read the temperature data from CPU, then the fan control machine of F81867 can implement the Fan to cool down the CPU temperature. The application circuit is as below.

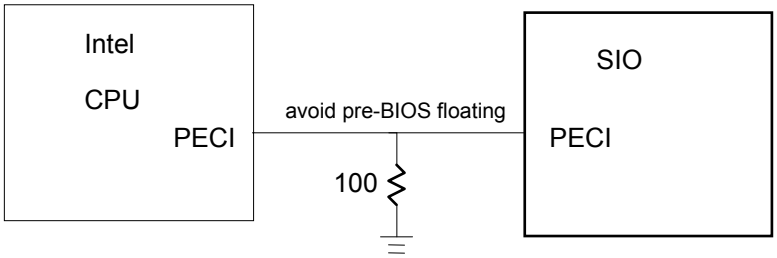


Fig 6-27 Intel PECI

Please see below for the Intel PECI 3.0 Spec. commands. The F81867 integrated most of those commands for the future advantage application. More detail, please refer to the register descriptions.

F81867 Support	PECI 3.0 Command Name	PECI 1.0 Command Name	Status
V	Ping( )	Ping( )	
V	GetTemp( )	GetTemp( )	
V	GetDIB( )		
V	RdIAMSR( )		
-	WrIAMSR( )		
-	RdPCIConfigLocal( )		Not Available in Mobile/DT
-	WrPCIConfigLocal( )		Not Available in Mobile/DT
-	RdPCIConfig( )		Not Available in Mobile/DT
-	WrPCIConfig( )		Not Available in Mobile/DT
V	RdPkgConfig( )		
V	WrPkgConfig( )		

Fig 6-28

6.11 Over Voltage Protection

F81867 over voltage protection function could protect the damage from voltage spikes via over voltage protection (OVP) function. Voltage protection function is enabled via setting the related register. When the force mode occurs, the system would shut down and then can not boot at all. Only re-plugging the power code (cut off VSB) could re-activate or re-boot the system at the force mode.

6.12 Microcontroller

A microcontroller contains a processor core, memory, and programmable input/output peripherals made it economical for designers. Basically Microcontrollers are designed for embedded applications such as automobile engine control systems, medical devices, remote controls, office machines, appliances, power tools, and toys.

F81867 integrates 8 bit 8032 embedded microcontroller which could access GPIO, PWM, hardware monitor, KBC, ACPI & CIR function. See detail for the µC side regeister.

6.13 Debug Port Function

The Debug Port is the interface for host to control the EC side devices. When it is enabled, it replaces EC to control its peripherals and could also access SFR and internal RAM of µC. Please refer to the Debug Port register in EC side to fully control the EC.

Debug Port Data Register — Offset 00h

Bit	Name	R/W	Reset	Default	Description
7-0	DBPORT_DATA	R/W	5VSB	0h	Write data to this byte will change the EC side register which address is set by DBPORT_EC_ADDR. Read data from this byte will return the value of EC side register which address is set by DBPORT_EC_ADDR.

Debug Port Control Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7	BRK_PTR_TRIG	R	5VSB	0	This bit is set when a break point is triggered.
6-1	Reserved	-	-	-	Reserved.
7-0	DBPORT_EN	R/W	5VSB	0	0: Disable debug port. 1: Enable debug port.

Debug Port EC Address Low Byte— Offset 04h

Bit	Name	R/W	Reset	Default	Description
7-0	DBPORT_EC_ADDR	R	5VSB	0	This is the low byte of EC peripheral address.

Debug Port EC Address High Byte— Offset 05h

Bit	Name	R/W	Reset	Default	Description
7-0	DBPORT_EC_ADDR	R	5VSB	0	This is the high byte of EC peripheral address.

6.14 H2E Function

H2E is the interface for host to EC. Host could use this register to notify the EC what to do and can get information return from EC. Some registers are pre-definition. User could change their definition for custom use.

H2E Control Register — Offset 00h

Bit	Name	R/W	Reset	Default	Description
7	P80_DEC_RANGE	R/W	5VSB	0	This bit is used to select the 0x80 port (the address could be set by EC) decode range. 0: Decode 0x80 only. 1: Decode 0x80 and 0x81.
6	E2H_INT_EN	R/W	5VSB	0	0: Disable EC asserts interrupt to Host. 1: Enable EC asserts interrupt to Host.
5	E2H_DATA_AVAIL	R	5VSB	0	This bit is set when EC write data to E2H_DATA (offset + 02h) and is auto clear when host read E2H_DATA.
4	H2E_DATA_AVAIL	R	5VSB	0	This bit is set when hostwrite data to H2E_DATA (offset + 01h) and is auto clear when EC read H2E_DATA.
3-2	E2H_DATA_TYPE	R	5VSB	0	This byte is pre-definition for the type of E2H_DATA. User could change its usage corresponding to their implementation. For the pre-definition function, host read the type to determine the meaning of E2H_DATA.
1-0	H2E_DATA_TYPE	R	5VSB	0	This byte is pre-definition for the type of H2E_DATA. User could change its usage corresponding to their implementation. For the pre-definition function, host read the type to determine the meaning of H2E_DATA.

H2E Data Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7-0	H2E_DATA	R/W	5VSB	0	Host to EC data.

E2H Data Register — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7-0	E2H_DATA	R	5VSB	0	This byte is written by EC. Host could read this byte to get the information return from EC.

WDT Control Port — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7	P80_WDT_TO_ST	R/W	5VSB	0	The bit is pre-defined for Port 80 WDT function. User could change its usage. The WDT is implemented by firmware. When time out occurs, EC set this bit and could assert reset signal from defined pins. Host read this bit to check the status and write "1" to clear status.
6	P80_WDT_EN	R/W	5VSB	0	The bit is pre-defined for Port 80 WDT function. EC read this bit to enable/disable WDT function. 0: Disable WDT function. 1: Enable WDT function.
5-4	P80_WDT_UNIT	R/W	5VSB	0	The bit is pre-defined for Port 80 WDT function. EC read this bit to decide WDT unit. The unit is user defined.
3-0	P80_WDT_PIN	R/W	5VSB	0	The bit is pre-defined for Port 80 WDT function. This is the mask for WDT event pins. The pin to assert WDT event is user defined.

WDT Time Register — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_WDT_TIME	R/W	5VSB	ffh	The byte is pre-defined for Port 80 WDT function. Host writes this byte to inform EC the WDT count down time.

WDT Enable Code — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_WDT_CODE	R/W	5VSB	-	The byte is pre-defined for Port 80 WDT function. EC wait for WDT start until 0x80 port data matches this byte.

80 Port Data — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_DATA	R/W	5VSB	-	The data write to 0x80/0x81(if P80_DEC_RANGE is set) will be latched into this byte. EC could dump the value into internal RAM for further use.

80 Port Data — Offset 07h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_LAST_DATA	R	5VSB	-	This byte is pre-defined for the last 0x80 port last data. EC write 0x80 port data back to this byte.

7. Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the RTS1# pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is an example to enable configuration and disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer to each device chapter if you want more detail information.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20*	Chip ID Register	0	0	0	1	0	0	0	0
21*	Chip ID Register	0	0	0	1	0	0	0	0
23*	Vendor ID Register	0	0	0	1	1	0	0	1
24*	Vendor ID Register	0	0	1	1	0	1	0	0
25*	I2C Address Register	0	0	0	0	0	0	0	0
26*	Clock Select Register	0	0	-	0	0	0	1	1
27*	Port Select Register	1/0	1/0	0	1/0	0	0	-	0
28*	Multi Function Select 1 Register	-	1	1	0	0	0	0	0
28*	Multi Function Select 2 Register	0	0	0	0	0	0	0	0
29*	Multi Function Select 3 Register	0	0	0	0	0	0	1	1
29*	10Hz Clock Divisor High Byte	0	0	0	0	0	0	1	1
2A*	10Hz Clock Divisor Low Byte	1	1	1	0	0	1	1	1
2B*	Multi Function Select 4 Register	0	0	0	-	-	-	1	0
2B*	10Hz Fine Tune Clock Count High Byte	-	-	-	-	-	-	-	-
2C*	10Hz Fine Tune Clock Count Low Byte	-	-	-	-	-	-	-	-
2C*	GPIO0 Enable Register	-	-	-	0	0	0	0	0

2C*	GPIO1 Enable Register	0	0	0	-	1	1	1	1
2C*	GPIO2 Enable Register	0	0	0	0	0	0	0	0
2C*	µC Port Enable Register	1	1	1	0	0	0	0	0
2D*	Wakeup Control Register	-	-	-	-	1	0	0	0

*Aceess by µC and host.

7.1 Global Control Registers

7.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	SOFT_RST	R/W	-	0	Write 1 to reset the register and device powered by VDD (VCC).

7.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET#	00h	00h: Select FDC device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. 0Eh: Select H2E device configuration registers. 10h: Select UART1 device configuration registers. 11h: Select UART2 device configuration registers. 12h: Select UART3 device configuration registers. 13h: Select UART4 device configuration registers. 14h: Select UART5 device configuration registers. 15h: Select UART6 device configuration registers. Otherwise: Reserved.

7.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIP_ID1	R	-	10h	Chip ID 1.

7.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIP_ID2	R	-	10h	Chip ID2.

7.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID1	R	-	19h	Vendor ID 1.

7.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID2	R	-	34h	Vendor ID 2.

7.1.7 I2C Address Select Register — Index 25h

Bit	Name	R/W	Reset	Default	Description
7-1	I2C_ADDR	R/W	5VSB	0	I2C address is used to R/W hardware monitor registers. The default address is determined by I2C_ADDR power on strap pin. It could also be changed by writing this byte with the entry key 0x19, 0x34. The default value is 0x2E which indicates the address is 0x5C.
0	EN_ARA_MODE	R/W	5VSB	0	0: disable I2C ARA. 1: enable I2C ARA.

7.1.8 Clock Select Register — Index 26h

Bit	Name	R/W	Reset	Default	Description
7-6	CLK_SEL	R/W	5VSB	0	The clock source of CLKIN. 00: CLKIN is 48MHz 10: CLKIN is 24MHz 01: CLKIN is 14.318MHz. 10: Reserved.
5	Reserved		-	-	Reserved.
4	MO_PIN_LVL_SEL	R/W	5VSB	0	MCLK/MDATA input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
3	PIN76_LVL_SEL	R/W	5VSB	0	PIN 76 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
2	PIN71_LVL_SEL	R/W	5VSB	0	PIN 71 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
1	PIN68_LVL_SEL	R/W	5VSB	1	PIN 68 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
0	PIN67_LVL_SEL	R/W	5VSB	1	PIN 67 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.

7.1.9 Port Select Register — Index 27h

Bit	Name	R/W	Reset	Default	Description
7	OVP_MODE	R/W	VBAT*	-	0: Enable OVP function. 1: Default is disabled; internal pull high 47kΩ. The default value is determined by power on strap.
6	AT_MODE	R/W	5VSB	-	0: ATX Mode. 1: AT Mode. The default value is determined by power on strap.
5	GPIO_DEC_RANGE	R/W	3VCC	0	0: The GPIO I/O space is 8-byte. 1: The GPIO I/O space is 16-byte.
4	PORT_4E_EN	R/W	5VSB*	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by RTS1#/ Config4E_2E. Pull down to select port 2E/2F. This bit is accessed by the host side only.
3-2	GPIO_PROG_SEL	R/W	5VSB	0	Index 0x2C register select. 00: GPIO0_EN 01: GPIO1_EN 10: GPIO2_EN 11: µC_PORT_EN.
1	HOST_STOP_µC	R/W	-	0	Host set this bit “1” to stop µC. To enter debug mode, host should stop this bit first. This bit is accessed by host side only.
0	CLK_TUNE_PROG_EN	R/W	3VCC	0	Set “1” to enable index 0x29, 0x2A, 0x2B, 0x2C function as clock fine tune register.

7.1.10 Multi-function Select 1 Register — Index 28h (Available when GPIO_PROG_SEL[0] = 0)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	FDC_GP_EN	R/W	5VSB	1	Pin 9 ~ 21 function select. These pins are controlled by FDC_GP_EN, UART5_FUNC_SEL, and UART6_FUNC_SEL. If all these bits are clear to “0”, the function would be FDC.
5	LPT_GP_EN	R/W	5VSB	1	Pin 102 ~ 118 function select. 0: Functions as parallel port. 1: Functions as GPIO7x/GPIO8x.
4	MO_ I2C _EN	R/W	5VSB	0	Pin 61, 62 function select. 0: PS/2 mouse interface MCLK/MDATA. 1: I2C SCL/SDA.
3-2	UART5_FUNC_SEL	R/W	5VSB	0	UART 5 Function Select. 00: No UART 5 pin. 01: Simple UART, only SIN5 and SOUT5 are available. Pin 57 will be function as SOUT5 and Pin 58 will be function as SIN5. 10: Simple UART with RTS#. Pin 59 will be function as RTS5#. 11: Full UART, pin 57 ~ 59, 17 ~ 21 will function as UART 5 pins.

1-0	UART6_FUNC_SEL	R/W	5VSB	0	UART6 Function Select. 00: No UART6 pin. 01: Simple UART, only SIN6 and SOUT6 are available. Pin 10 will be function as SOUT6 and Pin 11 will be function as SIN6. 10: Simple UART with RTS#. Pin 9 will be function as RTS6#. 11: Full UART, pin 9 ~ 16 will function as UART 6 pins.

7.1.11 Multi-function Select 2 Register — Index 28h (Available when GPIO_PROG_SEL[0] = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	µC_P32_PIN59_EN	R/W	VBAT	0	0: Disable µC P32 from pin 59. 1: Enable µC P32 from pin59.
5	µC_P31_PIN57_EN	R/W	VBAT	0	0: Disable µC P31 from pin 57. 1: Enable µC P31 from pin57.
4	µC_P30_PIN58_EN	R/W	VBAT	0	0: Disable µC P30 from pin 58. 1: Enable µC P30 from pin58.
3-2	Reserved	-	-	-	Reserved
1	CIR_PIN76_EN	R/W	VBAT	0	0: Disable CIRRX# from pin76. The pin function is ALERT#/GPIO20/SCL/CIRRX#. 1: Enable CIRRX# from pin76.
0	CIR_PIN71_EN	R/W	VBAT	0	0: Disable CIRRX# from pin71. The pin function is BEEP/GPIO16/SDA/CIRRX#. 1: Enable CIRRX# from pin71.

7.1.12 Multi Function Select 3 Register — Index 29h (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	UART4_FUNC_SEL	R/W	5VSB	0	UART4 Function Select. 00: No UART4 pin. Pin 44 ~ 51 are all GPIOs. 01: Simple UART, only SIN4 and SOUT4 are available. Pin 50 will be function as SOUT4 and Pin 51 will be function as SIN4. 10: Simple UART with RTS# function only. Pin 48 will be function as RTS4#. 11: Full UART, pin 44 ~ 51 will be function as UART pins.
5-4	UART3_FUNC_SEL	R/W	5VSB	0	UART3 Function Select. 00: No UART3 pin. Pin 36 ~ 43 are all GPIOs. 01: Simple UART, only SIN3 and SOUT3 are available. Pin 42 will be function as SOUT3 and Pin 43 will be function as SIN3. 10: Simple UART with RTS# function only. Pin 40 will be function as RTS3#. 11: Full UART, pin 36 ~ 43 will be function as UART pins.
3	SCL3_PIN76_EN	R/W	5VSB	0	0: Disable SCL from pin 76. 1: Enable SCL from pin 76. There is only one slave in the current design, it is recommended to select only one pin for SCL. When multi pins are selected, the priority of these bits is MO_I2C_EN > SCL_PIN76_EN > SCL_PIN67_EN.

2	SDA3_PIN71_EN	R/W	5VSB	0	0: Disable SDA from pin 76. 1: Enable SDA from pin 76. There is only one slave in the current design, it is recommended to select only one pin for SDA. When multi pins are selected, the priority of these bits is MO_I2C_EN > SDA_PIN71_EN > SDA_PIN68_EN.
1	SDA2_PIN68_EN	R/W	5VSB	1	0: Disable SDA from pin 68. 1: Enable SDA from pin 68. There is only one slave in the current design, it is recommended to select only one pin for SDA. When multi pins are selected, the priority of these bits is MO_I2C_EN > SDA_PIN71_EN > SDA_PIN68_EN.
0	SCL2_PIN67_EN	R/W	5VSB	1	0: Disable SCL from pin 67. 1: Enable SCL from pin 67. There is only one slave in the current design, it is recommended to select only one pin for SCL. When multi pins are selected, the priority of these bits is MO_I2C_EN > SCL_PIN76_EN > SCL_PIN67_EN.

7.1.13 10Hz Clock Divisor High Byte — Index 29h (Available when CLK_ TUNE_PROG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7	FINE_TUNE_START	W	-	-	Write “1” to start the fine tune mechanism. The hardware will start to count 10 cycle internal 500KHz clock with 48MHz clock. The count will present in index 0x2A, 0x2B.
6-4	Reserved	-	-	-	Reserved.
3-0	CLK10HZ_DIV	R/W	VBAT	4’h3	The divisor of 10Hz clock. Internal 10Hz clock is used to generate WDT event. It is divided from 10KHz clock and could be fine tune by change its divisor.

7.1.14 10Hz Clock Divisor Low Byte — Index 2Ah (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7	PWM3_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM3 from Pin 110. 1: Enable PWM3 from Pin 110.
6	PWM2_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM2 from Pin 109. 1: Enable PWM2 from Pin 109.
5	PWM1_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM1 from Pin 108. 1: Enable PWM1 from Pin 108.
4	PWM0_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM0 from Pin 107. 1: Enable PWM0 from Pin 107.
3	PWM3_PIN_EN	R/W	5VSB	0	0: Disable PWM3 from Pin 20. 1: Enable PWM3 from Pin 20.
2	PWM2_PIN_EN	R/W	5VSB	0	0: Disable PWM2 from Pin 19. 1: Enable PWM2 from Pin 19.
1	PWM1_PIN_EN	R/W	5VSB	0	0: Disable PWM1 from Pin 18. 1: Enable PWM1 from Pin 18.
0	PWM0_PIN_EN	R/W	5VSB	0	0: Disable PWM0 from Pin 17. 1: Enable PWM0 from Pin 17.

7.1.15 10Hz Clock Divisor Low Byte — Index 2Ah (Available when CLK_TUNE_PROG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	CLK10HZ_DIV	R/W	VBAT	8'hE7	The divisor of 10Hz clock. Internal 10Hz clock is used to generate WDT event. It is divided from 10KHz clock and could be fine tune by change its divisor.

7.1.16 Multi Function Select 4 Register — Index 2Bh (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_EN	R/W	VBAT	0	Pin 87 function select 0: Pin 87 functions as S5#. 1: Pin 87 functions as GPIO67.
6	GPIO66_EN	R/W	VBAT	0	Pin 86 function select 0: Pin 86 functions as DPWROK. 1: Pin 86 functions as GPIO66.
5	GPIO65_EN	R/W	VBAT	0	Pin 74 function select 0: Pin 74 functions as PME#. 1: Pin 74 functions as GPIO65.
4-2	Reserved	-	-	-	Reserved
1	FANIN3_EN	R/W	VBAT	1	Pin 102 function select 0: Pin 102 functions as SCLT. 1: Pin 102 functions as FANIN3.
0	FANCTRL3_EN	R/W	VBAT	0	Pin 103 function select. 0: Pin 103 functions as GPIO70/PE. 1: Pin 103 functions as FANCTRL3.

7.1.17 10Hz Clock Fine Tune Count High Byte — Index 2Bh (Available when CLK_ TUNE_PROG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7	FINE_TUNE_ST	-	5VSB	-	This bit indicates the fine tune mechanism is in process.
6-4	Reserved	-	-	-	Reserved
3-0	FINE_TUNE_CNT	R/W	5VSB	4'h3	This is the count of 10 cycles of internal 500KHz clock with 48MHz clock.

7.1.18 10Hz Clock Fine Tune Count Low Byte — Index 2Ch (Available when CLK_ TUNE_PROG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	FINE_TUNE_CNT	R/W	5VSB	4'h3	This is the count of 10 cycles of internal 500KHz clock with 48MHz clock.

7.1.19 GPIO0 Enable Register — Index 2Ch (Available when CLK_ TUNE_PROG_EN = 0 and GPIO_PROG_SEL = 2'b00)

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO04_EN	R/W	VBAT	0	Pin 56 function select. 0: Pin 56 functions as SLP_SUS#. 1: Pin 56 functions as GPIO04.
3	GPIO03_EN	R/W	VBAT	0	Pin 55 function select. 0: Pin 55 functions as SUS_ACK#. 1: Pin 55 functions as GPIO03.
2	GPIO02_EN	R/W	VBAT	0	Pin 54 function select. 0: Pin 54 functions as SUS_WARN#. 1: Pin 54 functions as GPIO02.
1	GPIO01_EN	R/W	VBAT	0	Pin 53 function select. 0: Pin 53 functions as ERP_CTRL1#. 1: Pin 53 functions as GPIO01.
0	GPIO00_EN	R/W	VBAT	0	Pin 52 function select. 0: Pin 52 functions as ERP_CTRL0#. 1: Pin 52 functions as GPIO00.

7.1.20 GPIO1 Enable Register — Index 2Ch (Available when CLK_ GPIO_PROG_SEL PROG_EN = 0 and GPIO_PROG_SEL = 2'b01)

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_EN	R/W	VBAT	0	Pin 72 function select. 0: Pin 72 functions as PECI. 1: Pin 72 functions as GPIO17.
6	GPIO16_EN	R/W	VBAT	0	Pin 71 function select. 0: Pin 71 functions as BEEP. 1: Pin 71 functions as GPIO16.
5	GPIO15_EN	R/W	VBAT	0	Pin 70 function select. 0: Pin 70 functions as WDTRST#. 1: Pin 70 functions as GPIO15.
4	Reserved	-	-	-	Reserved
3	GPIO13_EN	R/W	VBAT	1	Pin 68 function select. 0: Pin 68 functions as IRRX. 1: Pin 68 functions as GPIO13. If SDA_PIN68_EN is set, pin 68 will be function as SDA.
2	GPIO12_EN	R/W	VBAT	1	Pin 67 function select. 0: Pin 67 functions as IRTX. 1: Pin 67 functions as GPIO12. If SCL_PIN67_EN is set, pin 67 will be function as SCL.

1	GPIO11_EN	R/W	VBAT	1	Pin 66 function select. 0: Pin 66 functions as LED_VCC. 1: Pin 66 functions as GPIO11.
0	GPIO10_EN	R/W	VBAT	1	Pin 65 function select. 0: Pin 65 functions as LED_VSB. 1: Pin 65 functions as GPIO10.

7.1.21 GPIO2 Enable Register — Index 2Ch (Available when CLK_ TUNE_PROG_EN = 0 and GPIO_PROG_SEL = 2'b10)

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_EN	R/W	VBAT	0	Pin 83 function select. 0: Pin 83 functions as RSMRST#. 1: Pin 83 functions as GPIO27.
6	GPIO26_EN	R/W	VBAT	0	Pin 82 function select. 0: Pin 82 functions as PWROK. 1: Pin 82 functions as GPIO26.
5	GPIO25_EN	R/W	VBAT	0	Pin 81 function select. 0: Pin 81 functions as PSON#. 1: Pin 81 functions as GPIO25.
4	GPIO24_EN	R/W	VBAT	0	Pin 80 function select. 0: Pin 81 functions as S3#. 1: Pin 81 functions as GPIO24.
3	GPIO23_EN	R/W	VBAT	0	Pin 79 function select. 0: Pin 68 functions as PWSOUT#. 1: Pin 68 functions as GPIO23.
2	GPIO22_EN	R/W	VBAT	0	Pin 78 function select. 0: Pin 78 functions as PWSIN#. 1: Pin 78 functions as GPIO22.
1	GPIO21_EN	R/W	VBAT	0	Pin 77 function select. 0: Pin 77 functions as ATXPG_IN. 1: Pin 77 functions as GPIO21.
0	GPIO20_EN	R/W	VBAT	0	Pin 76 function select. 0: Pin 76 functions as ALERT#. 1: Pin 76 functions as GPIO20. Pin 76 will be function as SCL: if SCL_PIN76_EN is set.

7.1.22 µC Port Enable Register — Index 2Ch (Available when CLK_TUNE_PROG_EN = 0 and GPIO_PROG_SEL = 2'b11)

Bit	Name	R/W	Reset	Default	Description
7	µC_T2EX_EN	R/W	VBAT	0	Set "1" to enable µC T2EX function from pin 16.
6	µC_T2_EN	R/W	VBAT	0	Set "1" to enable µC T2 function from pin 15.
5	µC_P35_EN	R/W	VBAT	0	Set "1" to enable µC P3.5 (also function as µC T1) function from pin 14.

4	µC_P34_EN	R/W	VBAT	0	Set “1” to enable µC P3.4 (also function as µC T0) function from pin 13.
3	µC_P33_EN	R/W	VBAT	0	Set “1” to enable µC P3.3 (also function as µC INT1#) function from pin 12.
2	µC_P32_EN	R/W	VBAT	0	Set “1” to enable µC P3.2 (also function as µC INT0#) function from pin 9.
1	µC_P31_EN	R/W	VBAT	0	Set “1” to enable µC P3.1 (also function as µC TXD) function from pin 11.
0	µC_P30_EN	R/W	VBAT	0	Set “1” to enable µC P3.0 (also function as µC RXD) function from pin 10.

7.1.23 Wakeup Control Register — Index 2Dh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th>Description</th></tr>
<tr><td>7-4</td><td>Reserved</td><td>-</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>WAKEUP_EN</td><td>R/W</td><td>VBAT</td><td>1</td><td>0: disable KB/Mouse wakeup function.
1: enable KB/Mouse wakeup function.</td></tr>
<tr><td>2-1</td><td>KEY_SEL</td><td>R/W</td><td>VBAT</td><td>00</td><td>Select the keyboard wakeup key. Accompany with KEY_SEL_ADD, there are several key select as list
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wake Key</th></tr>
<tr><td>0</td><td>00</td><td>Ctrl + Esc</td></tr>
<tr><td>0</td><td>01</td><td>Ctrl + F1</td></tr>
<tr><td>0</td><td>10</td><td>Ctrl + Space</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup Key</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power Key</td></tr>
<tr><td>1</td><td>10</td><td>Ctrl + Alt + Backspace</td></tr>
<tr><td>1</td><td>11</td><td>Ctrl + Alt + Delete</td></tr>
</table></td></tr>
<tr><td>0</td><td>MO_SEL</td><td>R/W</td><td>VBAT</td><td>0</td><td>Select the mouse wakeup key.
0: Wakeup by mouse clicking.
1: Wakeup by mouse clicking or movement.</td></tr>
</table>

7.2 Multifunction Function Register Mapping Table

7.2.1 Multi Function Register Mapping For FDC

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN9	GPIO50/DENSEL#/RTS6#	DENSEL	INDEX 27H BIT3-2 = 00 INDEX 28H BIT6 AND BIT3-0 = 0 INDEX 27H BIT0 = 0 INDEX 2AH BIT3-0 = 0
PIN10	GPIO51/MOA#/SIN6	MOA#	
PIN11	GPIO52/DRVA#/SOUT6	DRVA#	
PIN12	GPIO53/WDATA#/DCD6#	WDATA#	
PIN13	GPIO54/DIR#/RI6#	DIR#	
PIN14	GPIO55/STEP#/CTS6#	STEP#	
PIN15	GPIO56/HDSEL#/DTR6	HDSEL#	
PIN16	GPIO57/WGATE#/DSR6#	WGATE#	
PIN17	GPIO60/RDATA#/DCD5#	RDATA#	

PIN18	GPIO61/TRK0#/RI5#	TRK0#	
PIN19	GPIO62/INDEX#/CTS5#	INDEX#	
PIN20	GPIO63/WPT#/DTR5#	WPT#	
PIN21	GPIO64/DSKCHG#/DSR5#	DSKCHG#	

7.2.2 Multi Function Register Mapping For Parallel Port (LPT)

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN102	FANIN3/SLCT	SLCT	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 28H BIT5 = 0 INDEX 2BH BIT1-0 = 00
PIN103	GPIO70/PE/FANCTL3/PWM_DAC3	PE	
PIN104	GPIO71/BUSY	BUSY	
PIN105	GPIO72/ACK#	ACK#	
PIN106	GPIO73/SLIN#	SLIN#	
PIN107	GPIO74/INIT#	INIT#	
PIN108	GPIO75/ERR#	ERR#	
PIN109	GPIO76/AFD#	AFD#	
PIN110	GPIO77/STB#	STB#	
PIN111	GPIO80/PD0	PD0	
PIN112	GPIO81/PD1	PD1	
PIN113	GPIO82/PD2	PD2	
PIN114	GPIO83/PD3	PD3	
PIN115	GPIO84/PD4	PD4	
PIN116	GPIO85/PD5	PD5	
PIN117	GPIO86/PD6	PD6	
PIN118	GPIO87/PD7	PD7	

7.2.3 Multi Function Register Mapping For Hardware Monitor

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN71	BEEP/GPIO16/SDA/CIRRX#	BEEP	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 29H BIT2 = 0 INDEX 2CH BIT6 = 0
PIN76	ALERT#/GPIO20/SCL/CIRRX#	ALERT#	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 29H BIT3 = 0 INDEX 2CH BIT0 = 0
PIN102	FANIN3/SLCT	FANIN3	INDEX 27H BIT0 = 0 INDEX 2BH BIT1 = 1

PIN103	GPIO70/PE/FANCTL3/PWM_DAC3	FANCTL3	INDEX 27H BIT0 = 0 INDEX 2BH BIT0 = 1

7.2.4 Multi Function Register Mapping For KBC (PS/2 Mouse)

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN61	MDATA/SCL	MDATA	INDEX 27H BIT3-2 = 00
PIN62	MCLK/SDA	MCLK	INDEX 28H BIT4 = 0

7.2.5 Multi Function Register Mapping For GPIO0x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN52	ERP_CTRL0#/GPIO00	GPIO00	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 2CH BIT0 = 1
PIN53	ERP_CTRL1#/GPIO01	GPIO01	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 2CH BIT1 = 1
PIN54	SUS_WARN#/GPIO02	GPIO02	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 2CH BIT2 = 1
PIN55	SUS_ACK#/GPIO03	GPIO03	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 2CH BIT3 = 1
PIN56	SLP_SUS#/GPIO04	GPIO04	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 2CH BIT4 = 1
PIN57 PIN58 PIN59	GPIO05/SOUT5 GPIO06/SIN5 GPIO07/RTS5#	GPIO05 GPIO06 GPIO07	INDEX 27H BIT3-2 = 00 INDEX 28H BIT3-2 = 00

7.2.6 Multi Function Register Mapping For GPIO1x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN65	GPIO10/LED_VSB	GPIO10	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 2CH BIT0 = 1
PIN66	GPIO11/LED_VCC	GPIO11	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 2CH BIT1 = 1
PIN67	SCL/GPIO12/IRTX	GPIO12	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 29H BIT0 = 0 INDEX 2CH BIT2 = 1
PIN68	SDA/GPIO13/IRRX	GPIO13	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 29H BIT1 = 0 INDEX 2CH BIT3 = 1
PIN69	GPIO14/ATX_AT_TRAP	GPIO14	SINGLE FUNCTION

PIN70	WDTRST#/GPIO15	GPIO15	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 2CH BIT5 = 1
PIN71	BEEP/GPIO16/SDA/CIRRX#	GPIO16	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 29H BIT2 = 0 INDEX 2CH BIT6 = 1
PIN72	PECI/GPIO17	GPIO17	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 2CH BIT7 = 1

7.2.7 Multi Function Register Mapping For GPIO2x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN76	ALERT#/GPIO20/SCL/CIRRX#	GPIO20	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 29H BIT3 = 0 INDEX 2CH BIT0 = 1
PIN77	ATXPG_IN/GPIO21	GPIO21	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT1 = 1
PIN78	PWSIN#/GPIO22	GPIO22	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT2 = 1
PIN79	PWSOUT#/GPIO23	GPIO23	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT3 = 1
PIN80	S3#/GPIO24	GPIO24	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT4 =1
PIN81	PS_ON#/GPIO25	GPIO25	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT5 = 1
PIN82	PWOK/GPIO26	GPIO26	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT6 = 1
PIN83	RSMRST#/GPIO27	GPIO27	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT7 = 1

7.2.8 Multi Function Register Mapping For GPIO3x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN36	DCD3#/GPIO30	GPIO30	INDEX 27H BIT0 = 0 INDEX 29H BIT5-4 = 00
PIN37	RI3#/GPIO31	GPIO31	
PIN38	CTS3#/GPIO32	GPIO32	
PIN39	DTR3#/GPIO33	GPIO33	
PIN40	RTS3#/GPIO34	GPIO34	
PIN41	DSR3#/GPIO35	GPIO35	
PIN42	SOUT3/GPIO36	GPIO36	

PIN43	SIN3/GPIO37	GPIO37	

7.2.9 Multi Function Register Mapping For GPIO4x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN44	DCD4#/GPIO40	GPIO40	INDEX 27H BIT0 = 0 INDEX 29H BIT7-6 = 00
PIN45	RI4#/GPIO41	GPIO41	
PIN46	CTS4#/GPIO42	GPIO42	
PIN47	DTR4#/GPIO43	GPIO43	
PIN48	RTS4#/GPIO44	GPIO44	
PIN49	DSR4#/GPIO45	GPIO45	
PIN50	SOUT4/GPIO46	GPIO46	
PIN51	SIN4/GPIO47	GPIO47	

7.2.10 Multi Function Register Mapping For GPIO5x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN9	GPIO50/DENSEL#/RTS6#	GPIO50	INDEX 27H BIT3-2 = 00 INDEX 28H BIT6 = 1 AND BIT1-0 = 00
PIN10	GPIO51/MOA#/SIN6	GPIO51	
PIN11	GPIO52/DRVA#/SOUT6	GPIO52	
PIN12	GPIO53/WDATA#/DCD6#	GPIO53	
PIN13	GPIO54/DIR#/RI6#	GPIO54	
PIN14	GPIO55/STEP#/CTS6#	GPIO55	
PIN15	GPIO56/HDSEL#/DTR6	GPIO56	
PIN16	GPIO57/WGATE#/DSR6#	GPIO57	

7.2.11 Multi Function Register Mapping For GPIO6x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN17	GPIO60/RDATA#/DCD5#	GPIO60	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 28H BIT6 = 1 AND BIT3-2 = 00
PIN18	GPIO61/TRK0#/RI5#	GPIO61	
PIN19	GPIO62/INDEX#/CTS5#	GPIO62	
PIN20	GPIO63/WPT#/DTR5#	GPIO63	
PIN21	GPIO64/DSKCHG#/DSR5#	GPIO64	
PIN74	PME#/GPIO65	GPIO65	INDEX 27H BIT0 = 0 INDEX 2BH BIT5 = 1
PIN86	DPWROK/GPIO66	GPIO66	INDEX 27H BIT0 = 0 INDEX 2BH BIT6 = 1
PIN87	S5#/GPIO67	GPIO67	INDEX 27H BIT0 = 0

			INDEX 2BH BIT7 = 1

7.2.12 Multi Function Register Mapping For GPIO7x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN103	GPIO70/PE/FANCTL3/PWM_DAC3	GPIO70	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 28H BIT5 = 1 INDEX 2BH BIT0 =0
PIN104	GPIO71/BUSY	GPIO71	INDEX 27H BIT3-2 = 00 AND BIT0 = 0 INDEX 28H BIT5 = 1
PIN105	GPIO72/ACK#	GPIO72	
PIN106	GPIO73/SLIN#	GPIO73	
PIN107	GPIO74/INIT#	GPIO74	
PIN108	GPIO75/ERR#	GPIO75	
PIN109	GPIO76/AFD#	GPIO76	
PIN110	GPIO77/STB#	GPIO77	

7.2.13 Multi Function Register Mapping For GPIO8x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN111	GPIO80/PD0	GPIO80	INDEX 27H BIT3-2 = 00 INDEX 28H BIT5 = 1
PIN112	GPIO81/PD1	GPIO81	
PIN113	GPIO82/PD2	GPIO82	
PIN114	GPIO83/PD3	GPIO83	
PIN115	GPIO84/PD4	GPIO84	
PIN116	GPIO85/PD5	GPIO85	
PIN117	GPIO86/PD6	GPIO86	
PIN118	GPIO87/PD7	GPIO87	

7.2.14 Multi Function Register Mapping For WDT

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN70	WDTRST#/GPIO15	WDTRST#	INDEX 27H BIT3-2 = 01 AND INDEX BIT0 = 0 INDEX 2CH BIT5 = 0

7.2.15 Multi Function Register Mapping For ERP, LED

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN52	ERP_CTRL0#/GPIO00	ERP_CTRL0#	INDEX 27H BIT3-2 AND BIT0 = 0 INDEX 2CH BIT0 = 0
PIN53	ERP_CTRL1#/GPIO01	ERP_CTRL1#	INDEX 27H BIT3-2 AND BIT0 = 0 INDEX 2CH BIT1 = 0

PIN54	SUS_WARN#/GPIO02	SUS_WARN#	INDEX 27H BIT3-2 AND BIT0 = 0 INDEX 2CH BIT2 = 0
PIN55	SUS_ACK#/GPIO03	SUS_ACK#	INDEX 27H BIT3-2 AND BIT0 = 0 INDEX 2CH BIT3 = 0
PIN56	SLP_SUS#/GPIO04	SLP_SUS#	INDEX 27H BIT3-2 AND BIT0 = 0 INDEX 2CH BIT4 = 0
PIN86	DPWROK/GPIO66	DPWROK	INDEX 27H BIT0 = 0 INDEX 2BH BIT6 = 0
PIN65	GPIO10/LED_VSB	LED_VSB	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 2CH BIT1-0 = 00
PIN66	GPIO11/LED_VCC	LED_VCC	
PIN77	ATXPG_IN/GPIO21	ATXPG_IN	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT1 = 0
PIN78	PWSIN#/GPIO22	PWSIN#	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT2 = 0
PIN79	PWSOUT#/GPIO23	PWSOUT#	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT3 = 0
PIN80	S3#/GPIO24	S3#	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT4 = 0
PIN81	PS_ON#/GPIO25	PS_ON#	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT5 = 0
PIN82	PWOK/GPIO26	PWOK	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT6 = 0
PIN83	RSMRST#/GPIO27	RSMRST#	INDEX 27H BIT3-2 = 10 AND BIT0 = 0 INDEX 2CH BIT7 = 0
PIN87	S5#/GPIO67	S5#	INDEX 27H BIT0 = 0 INDEX 2BH BIT7 =0

7.2.16 Multi Function Register Mapping For IR

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN67 PIN68	SCL/GPIO12/IRTX SDA/GPIO13/IRRX	IRTX IRRX	INDEX 27H BIT3-2 = 01 AND BIT0 = 0 INDEX 29H BIT1-0 = 00 INDEX 2CH BIT3-2 = 00

7.2.17 Multi Function Register Mapping For I2C

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN61	MDATA/SCL	SCL	INDEX 27H BIT3-2 = 00
PIN62	MCLK/SDA	SDA	INDEX 28H BIT4 = 1
PIN71	BEEP/GPIO16/SDA/CIRRX#	SDA	INDEX 27H BIT0 = 0

PIN76	ALERT#/GPIO20/SCL/CIRRX#	SCL	INDEX 29H BIT3-2 = 11

7.2.18 Multi Function Register Mapping For UART 1 & UART 2

UART 1 & 2 are pure pins.

7.2.19 Multi Function Register Mapping For UART 3

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN36	DCD3#/GPIO30	DCD3#	INDEX 27H BIT0 = 0 INDEX 29H BIT5-4 = 01 ONLY SIN3/SOUT3 AVAILABLE INDEX 29H BIT5-4 = 10 ONLY SIN3/SOUT3/RTS3# AVAILABLE INDEX 29H BIT5-4 = 11 FULL UART
PIN37	RI3#/GPIO31	RI3#	
PIN38	CTS3#/GPIO32	CTS3#	
PIN39	DTR3#/GPIO33	DTR3#	
PIN40	RTS3#/GPIO34	RTS3#	
PIN41	DSR3#/GPIO35	DSR3#	
PIN42	SOUT3/GPIO36	SOUT3	
PIN43	SIN3/GPIO37	SIN3	

7.2.20 Multi Function Register Mapping For UART 4

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN44	DCD4#/GPIO40	DCD4#	INDEX 27H BIT0 = 0 INDEX 29H BIT7-6 = 01 ONLY SIN4/SOUT4 AVAILABLE INDEX 29H BIT7-6 = 10 ONLY SIN4/SOUT4/RTS4# AVAILABLE INDEX 29H BIT7-6 = 11 FULL UART
PIN45	RI4#/GPIO41	RI4#	
PIN46	CTS4#/GPIO42	CTS4#	
PIN47	DTR4#/GPIO43	DTR4#	
PIN48	RTS4#/GPIO44	RTS4#	
PIN49	DSR4#/GPIO45	DSR4#	
PIN50	SOUT4/GPIO46	SOUT4	
PIN51	SIN4/GPIO47	SIN4	

7.2.21 Multi Function Register Mapping For UART 5

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN17	GPIO60/RDATA#/DCD5#	DCD5#	INDEX 27H BIT3-2 = 00 INDEX 28H BIT3-2 = 01 ONLY SIN5/SOUT5 AVAILABLE INDEX 28H BIT3-2 = 10 ONLY SIN5/SOUT5/RTS5# AVAILABLE INDEX 28H BIT3-2 = 11 FULL UART
PIN18	GPIO61/TRK0#/RI5#	RI5#	
PIN19	GPIO62/INDEX#/CTS5#	CTS5#	
PIN20	GPIO63/WPT#/DTR5#	DTR5#	
PIN21	GPIO64/DSKCHG#/DSR5#	DSR5#	
PIN57	GPIO05/SOUT5	SOUT5	
PIN58	GPIO06/SIN5	SIN5	
PIN59	GPIO07/RTS5#	RTS5#	

7.2.22 Multi Function Register Mapping For UART 6

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER
PIN9	GPIO50/DENSEL#/RTS6#	RTS6#	INDEX 27H BIT3-2 = 00 INDEX 28H BIT1-0 = 01 ONLY SIN6/SOUT6 AVAILABLE INDEX 28H BIT1-0 = 10 ONLY SIN6/SOUT6/RTS6# AVAILABLE INDEX 28H BIT1-0 = 11 FULL UART
PIN10	GPIO51/MOA#/SIN6	SIN6	
PIN11	GPIO52/DRVA#/SOUT6	SOUT6	
PIN12	GPIO53/WDATA#/DCD6#	DCD6#	
PIN13	GPIO54/DIR#/RI6#	RI6#	
PIN14	GPIO55/STEP#/CTS6#	CTS6#	
PIN15	GPIO56/HDSEL#/DTR6#	DTR6#	
PIN16	GPIO57/WGATE#/DSR6#	DSR6#	

7.3 FDC Registers (CR00)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	FDC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	0
74	DMA Channel Select Register	-	-	-	-	-	0	1	0
F0	FDD Mode Register	-	-	-	0	1	1	1	0
F2	FDD Drive Type Register	-	-	-	-	-	-	1	1
F4	FDD Selection Register	-	-	-	0	0	-	0	0

FDC Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	FDC_EN	R/W	LRESET#	1	0: disable FDC. 1: enable FDC.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of FDC base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	F0h	The LSB of FDC base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELFDCIRQ	R/W	LRESET#	06h	Select the IRQ channel for FDC.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved.
2-0	SELFDCDMA	R/W	LRESET#	010	Select the DMA channel for FDC.

FDD Mode Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4	FDC_SW_WP	R/W	LRESET#	0	FDC Software Write Protect. 0: Write protect is determined by WPT# pin. 1: Enable Write Protect.
3-2	IF_MODE	R/W	LRESET#	11	00: Model 30 mode. 01: PS/2 mode. 10: Reserved. 11: AT mode (default).
1	FDMAMODE	R/W	LRESET#	1	0: enable burst mode. 1: non-busrt mode (default).
0	Reserved	R/W	-	0	Reserved.

FDD Drive Type Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	FDD_TYPE	R/W	LRESET#	11	FDD drive type.

FDD Selection Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4-3	FDD_DRT	R/W	LRESET#	00	Data rate table select, refer to table A. 00: select regular drives and 2.88 format. 01: reserved. 10: 2 mega tape. 11: reserved.
2	Reserved	-	-	-	Reserved.
1-0	FDD_DT	R/W	LRESET#	00	Drive type select, refer to table B.

TABLE A

Data Rate Table Select		Data Rate		Selected Data Rate		DENSEL
FDD_DRT[1]	FDD_DRT[0]	DATARATE1	DATARATE0	MFM	FM	

0	0	0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
0	1	0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
1	0	0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0
		1	1	1Meg	---	1

TABLE B

Drive Type		DRVDEN0	Remark
FDD_DT1	FDD_DT0		
0	0	DENSEL	4/2/1 MB 3.5” 2/1 MB 5.25” 1/1.6/1 MB 3.5” (3-Mode)
0	1	DATARATE1	
1	0	DENSEL#	
1	1	DATARATE0	

7.4 Parallel Port Registers (CR03)

“-“ Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Parallel Port Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	0	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	1
74	DMA Channel Select Register	-	-	-	0	-	0	1	1
F0	PRT Mode Select Register	0	1	0	0	0	0	1	0

Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	PRT_EN	R/W	LRESET#	1	0: disable Parallel Port. 1: enable Parallel Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of Parallel Port base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	78h	The LSB of Parallel Port base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELPRTIRQ	R/W	LRESET#	7h	Select the IRQ channel for Parallel Port.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4	ECP_DMA_MODE	R/W	LRESET#	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	-	Reserved.
2-0	SELPRTDMA	R/W	LRESET#	011	Select the DMA channel for Parallel Port.

PRT Mode Select Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	SPP_IRQ_MODE	R/W	LRESET#	0	Interrupt mode in non-ECP mode. 0: Level mode. 1: Pulse mode.
6-3	ECP_FIFO_THR	R/W	LRESET#	1000	ECP FIFO threshold.
2-0	PRT_MODE	R/W	LRESET#	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

7.5 Hardware Monitor Registers (CR04)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	HM_EN	R/W	LRESET#	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	02h	The MSB of Hardware Monitor base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	95h	The LSB of Hardware Monitor base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELHMIRQ	R/W	LRESET#	0000	Select the IRQ channel for Hardware Monitor.

7.6 KBC Registers (CR05)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0
FE	PS/2 Swap Register	0	-	-	0	0	0	0	1

KBC Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	KBC_EN	R/W	3VCC	1	0: disable KBC. 1: enable KBC.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of KBC command port address. The address of data port is command port address + 4

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELKIRQ	R/W	LRESET#	0h	Select the IRQ channel for keyboard interrupt.

Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELMIRQ	R/W	LRESET#	0h	Select the IRQ channel for PS/2 mouse interrupt.

PS/2 Swap Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	KB_MO_SWAP	R/W	VBAT	0	Keyboard Mouse Swap. 0: Keyboard/Mouse is not swapped. 1: Keyboard/Mouse is swapped. This bit could be programmed by user. If AUTO_DET_EN is set, this bit is also updated by hardware.
3-0	KBC_TEST_BIT	R/W	VBAT	3h	Fintek test mode bits.

7.7 GPIO Registers (CR06)

7.7.1 GPIO Configuration Registers

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	GPIO Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0

GPIO Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	GPIO_EN	R/W	LRESET#	0	0: disable GPIO I/O port. 1: enable GPIO I/O port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of GPIO I/O port address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	60h	The LSB of KBC data port address. When GPIO_DEC_RANGE is "0", only 8 bytes are decoded: Base + 0: index port. Base + 1: data port. Base + 2: GPIO8 data register. Base + 3: GPIO7 data register. Base + 4: GPIO6 data register. Base + 5: GPIO5 data register. Base + 6: GPIO0 data register. Base + 7: GPIO1 data register. If GPIO_DEC_RANGE is set to "1", more 8 bytes are decoded: Base + 8: GPIO2 data register. Base + 9: GPIO3 data register. Base + 10: GPIO4 data register. Otherwise: Reserved. There are three ways to access the GPIO registers. 1. Use configuration register port 0x4E/0x4F (or 0x2E/0x2F), the LDN for GPIO is 0x06. 2. Use GPIO index/data port. Write index to index port first and then read/write the register. 3. Use digital I/O port. The way only access GPIO data register. Write data to this port will control the data output register. And read this port will read the pin status register.

7.7.2 GPIO IRQ Channel Select Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
70	GPIO0 IRQ Channel Select Register	-	-	-	-	0	0	0	1
71	GPIO1 IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	GPIO5 IRQ Channel Select Register	-	-	-	-	0	0	0	1
73	GPIO8 IRQ Channel Select Register	-	-	-	-	0	0	0	1

GPIO0 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGP0IRQ	R/W	LRESET#	1h	Select the IRQ channel for GPIO0 interrupt.

GPIO1 IRQ Channel Select Register — Index 71h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGP1IRQ	R/W	LRESET#	1h	Select the IRQ channel for GPIO1 interrupt.

GPIO5 IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGP5IRQ	R/W	LRESET#	1h	Select the IRQ channel for GPIO5 interrupt.

GPIO8 IRQ Channel Select Register — Index 73h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGP8IRQ	R/W	LRESET#	1h	Select the IRQ channel for GPIO8 interrupt.

7.7.3 GPIO IRQ Sharing Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
7E	GPIO IRQ Share Enable Register	-	-	-	-	0	0	0	0
7F	GPIO IRQ Share Mode Register	0	0	0	0	0	0	0	0

GPIO IRQ Sharing Enable Register Index 7Eh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	GP8_IRQ_SHARE	R/W	LRESET#	0	0: GPIO8 IRQ is not sharing with other devices. 1: GPIO8 IRQ is sharing with other devices.

2	GP5_IRQ_SHARE	R/W	LRESET#	0	0: GPIO5 IRQ is not sharing with other devices.. 1: GPIO5 IRQ is sharing with other devices.
1	GP1_IRQ_SHARE	R/W	LRESET#	0	0: GPIO1 IRQ is not sharing with other devices. 1: GPIO1 IRQ is sharing with other devices.
0	GP0_IRQ_SHARE	R/W	LRESET#	0	0: GPIO0 IRQ is not sharing with other devices. 1: GPIO0 IRQ is sharing with other devices.

GPIO IRQ Sharing Mode Register Index 7Fh

Bit	Name	R/W	Reset	Default	Description
7-6	GP8_IRQ_MODE	R/W	LRESET#	0	GPIO8 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge. 10 : Sharing IRQ active high Level. 11 : Reserved. This bit is effective when IRQ is sharing with other device (GP8_IRQ_SHARE is “1”).
5-4	GP5_IRQ_MODE	R/W	LRESET#	0	GPIO5 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge. 10 : Sharing IRQ active high Level. 11 : Reserved. This bit is effective when IRQ is sharing with other device (GP5_IRQ_SHARE is “1”).
3-2	GP1_IRQ_MODE	R/W	LRESET#	0	GPIO1 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge. 10 : Sharing IRQ active high Level. 11 : Reserved. This bit is effective when IRQ is sharing with other device (GP1_IRQ_SHARE is “1”).

1-0	GP0_IRQ_MODE	R/W	LRESET#	0	GPIO0 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge. 10 : Sharing IRQ active high Level. 11 : Reserved. This bit is effective when IRQ is sharing with other device (GP0_IRQ_SHARE is "1").

7.7.4 GPIO0x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
F0	GPIO0 Output Enable Register	0	0	0	0	0	0	0	0
F1	GPIO0 Output Data Register	0	0	0	0	1	1	1	1
F2	GPIO0 Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO0 Drive Enable Register	0	0	0	0	0	0	0	0
F4	GPIO0 Output Mode 1 Register	0	0	0	0	0	0	0	0
F5	GPIO0 Output Mode 2 Register	0	0	0	0	0	0	0	0
F6	GPIO0 Pulse Width Select 1 Register	0	0	0	0	0	0	0	0
F7	GPIO0 Pulse Width Select 2 Register	0	0	0	0	0	0	0	0
F8	GPIO0 SMI Enable Register	0	0	0	0	0	0	0	0
F9	GPIO0 SMI Status Register	0	0	0	0	0	0	0	0

GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_OE	R/W	5VSB	0	0: GPIO07 is input. 1: GPIO07 is output.
6	GPIO06_OE	R/W	5VSB	0	0: GPIO06 is input. 1: GPIO06 is output.
5	GPIO05_OE	R/W	5VSB	0	0: GPIO05 is input. 1: GPIO05 is output.
4	GPIO04_OE	R/W	5VSB	0	0: GPIO04 is input. 1: GPIO04 is output.
3	GPIO03_OE	R/W	5VSB	0	0: GPIO03 is input. 1: GPIO03 is output.
2	GPIO02_OE	R/W	5VSB	0	0: GPIO02 is input. 1: GPIO02 is output.
1	GPIO01_OE	R/W	5VSB	0	0: GPIO01 is input. 1: GPIO01 is output.

0	GPIO00_OE	R/W	5VSB	0	0: GPIO00 is input. 1: GPIO00 is output.

GPIO0 Output Data Register — Index F1h (This byte could be also written by base address + 6)

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_VAL	R/W	5VSB	0	GPIO07 supports pulse mode. When pulse mode is selected, write "1" to this bit will assert a pulse from GPIO07. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO07. 0: outputs 0 when in output mode. 1: outputs 1 when in output mode. GPIO07 will be tri-state if GPIO07_DRV is clear to "0".
6	GPIO06_VAL	R/W	5VSB	0	GPIO06 supports pulse mode. When pulse mode is selected, write "1" to this bit will assert a pulse from GPIO06. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO06. 0: outputs 0 when in output mode. 1: outputs 1 when in output mode. GPIO06 will be tri-state if GPIO06_DRV is clear to "0".
5	GPIO05_VAL	R/W	5VSB	0	GPIO05 supports pulse mode. When pulse mode is selected, write "1" to this bit will assert a pulse from GPIO05. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO05. 0: outputs 0 when in output mode. 1: outputs 1 when in output mode. GPIO05 will be tri-state if GPIO05_DRV is clear to "0".
4	GPIO04_VAL	R/W	5VSB	0	GPIO04 supports pulse mode. When pulse mode is selected, write "1" to this bit will assert a pulse from GPIO04. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO04. 0: outputs 0 when in output mode. 1: outputs 1 when in output mode. GPIO04 will be tri-state if GPIO04_DRV is clear to "0".1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	5VSB	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	5VSB	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	5VSB	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_VAL	R/W	5VSB	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

GPIO0 Pin Status Register — Index F2h (This byte could be also read by base address + 6)

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_IN	R	-	-	The pin status of GPIO07/RTS5#.
6	GPIO06_IN	R	-	-	The pin status of GPIO06/SIN5.
5	GPIO05_IN	R	-	-	The pin status of GPIO05/SOUT5.
4	GPIO04_IN	R	-	-	The pin status of SLP_SUS#/GPIO04.

3	GPIO03_IN	R	-	-	The pin status of SUS_ACK#/GPIO03.
2	GPIO02_IN	R	-	-	The pin status of SUS_WARN#/GPIO02.
1	GPIO01_IN	R	-	-	The pin status of ERP_CTRL1#/GPIO01.
0	GPIO00_IN	R	-	-	The pin status of ERP_CTRL0#/GPIO00.

GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DRV_EN	R/W	5VSB	0	GPIO07 Drive Enable. 0: GPIO07 is open drain. 1: GPIO07 is push pull.
6	GPIO06_DRV_EN	R/W	5VSB	0	GPIO06 Drive Enable. 0: GPIO06 is open drain. 1: GPIO06 is push pull.
5	GPIO05_DRV_EN	R/w	5VSB	0	GPIO05 Drive Enable. 0: GPIO05 is open drain. 1: GPIO05 is push pull.
4	GPIO04_DRV_EN	R/W	5VSB	0	GPIO04 Drive Enable. 0: GPIO04 is open drain. 1: GPIO04 is push pull.
3	GPIO03_DRV_EN	R/W	5VSB	0	GPIO03 Drive Enable. 0: GPIO03 is open drain. 1: GPIO03 is push pull.
2	GPIO02_DRV_EN	R/W	5VSB	0	GPIO02 Drive Enable. 0: GPIO02 is open drain. 1: GPIO02 is push pull.
1	GPIO01_DRV_EN	R/W	5VSB	0	GPIO01 Drive Enable. 0: GPIO01 is open drain. 1: GPIO01 is push pull.
0	GPIO00_DRV_EN	R/W	5VSB	0	GPIO00 Drive Enable. 0: GPIO00 is open drain. 1: GPIO00 is push pull.

GPIO0 Output Mode 1 Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO03_MODE	R/W	5VSB	00b	GPIO03 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO03_PW_SEL.
5-4	GPIO02_MODE	R/w	5VSB	00b	GPIO02 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO02_PW_SEL.

3-2	GPIO01_MODE	R/W	5VSB	00b	GPIO01 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO01_PW_SEL.
1-0	GPIO00_MODE	R/W	5VSB	00b	GPIO00 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO00_PW_SEL.

GPIO0 Output Mode 2 Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_MODE	R/W	5VSB	00b	GPIO07 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO07_PW_SEL.
5-4	GPIO06_MODE	R/w	5VSB	00b	GPIO06 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO06_PW_SEL.
3-2	GPIO05_MODE	R/W	5VSB	00b	GPIO05 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO05_PW_SEL.
1-0	GPIO04_MODE	R/W	5VSB	00b	GPIO04 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO04_PW_SEL.

GPIO0 Pulse Width Select 1 Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO03_PW_SEL	R/W	5VSB	00b	GPIO03 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
5-4	GPIO02_PW_SEL	R/w	5VSB	00b	GPIO02 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
3-2	GPIO01_PW_SEL	R/W	5VSB	00b	GPIO01 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO00_PW_SEL	R/W	5VSB	00b	GPIO00 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.

GPIO0 Pulse Width Select 2 Register — Index F7h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_PW_SEL	R/W	5VSB	00b	GPIO07 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
5-4	GPIO06_PW_SEL	R/w	5VSB	00b	GPIO06 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
3-2	GPIO05_PW_SEL	R/W	5VSB	00b	GPIO05 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO04_PW_SEL	R/W	5VSB	00b	GPIO04 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.

GPIO0 SMI Enable Register — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO07_SMI_ST is set.
6	GPIO06_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO06_SMI_ST is set.
5	GPIO05_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO05_SMI_ST is set.
4	GPIO04_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO04_SMI_ST is set.
3	GPIO03_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO03_SMI_ST is set.
2	GPIO02_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO02_SMI_ST is set.
1	GPIO01_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO01_SMI_ST is set.
0	GPIO00_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO00_SMI_ST is set.

GPIO0 SMI Status Register — Index F9h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO07 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO06_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO06 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO05_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO05 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO04_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO04 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO03_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO03 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO02_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO02 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO01_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO01 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO00_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO00 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

7.7.5 GPIO1x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
E0	GPIO1 Output Enable Register	0	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	1	1	1	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	0	0	0	0	0	0	0	0
E8	GPIO1 SMI Enable Register	0	0	0	0	0	0	0	0
E9	GPIO1 SMI Status Register	0	0	0	0	0	0	0	0

GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_OE	R/W	5VSB	0	0: GPIO17 is in input mode. 1: GPIO17 is in output mode.
6	GPIO16_OE	R/W	5VSB	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	5VSB	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	5VSB	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	5VSB	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	5VSB	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	5VSB	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	5VSB	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

GPIO1 Output Data Register — Index E1h (This byte could be also written by base address + 7)

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_VAL	R/W	5VSB	1	0: GPIO17 outputs 0 when in output mode. 1: GPIO17 outputs1 when in output mode.
6	GPIO16_VAL	R/W	5VSB	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_VAL	R/W	5VSB	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	5VSB	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	5VSB	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.

2	GPIO12_VAL	R/W	5VSB	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	5VSB	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	5VSB	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

GPIO1 Pin Status Register — Index E2h (This byte could be also read by base address + 7)

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_IN	R	-	-	The pin status of PECI/GPIO17.
6	GPIO16_IN	R	-	-	The pin status of BEEP/GPIO16/SDA/CIRRX#.
5	GPIO15_IN	R	-	-	The pin status of WDTRST#/GPIO15.
4	GPIO14_IN	R	-	-	The pin status of GPIO14/AT_ATX_TRAP.
3	GPIO13_IN	R	-	-	The pin status of SDA/GPIO13/IRRX.
2	GPIO12_IN	R	-	-	The pin status of SCL/GPIO12/IRTX
1	GPIO11_IN	R	-	-	The pin status of GPIO11/LED_VCC.
0	GPIO10_IN	R	-	-	The pin status of GPIO10/LED_VSB.

GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_DRV_EN	R/W	5VSB	0	0: GPIO17 is open drain in output mode. 1: GPIO17 is push pull in output mode.
6	GPIO16_DRV_EN	R/W	5VSB	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	5VSB	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	5VSB	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	5VSB	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	5VSB	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	VBAT	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode. This bit is powered by VBAT.
0	GPIO10_DRV_EN	R/W	VBAT	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode. This bit is powered by VBAT.

GPIO1 SMI Enable Register — Index E8h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO17_SMI_ST is set.
6	GPIO16_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO16_SMI_ST is set.

5	GPIO15_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO15_SMI_ST is set.
4	GPIO14_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO14_SMI_ST is set.
3	GPIO13_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO13_SMI_ST is set.
2	GPIO12_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO12_SMI_ST is set.
1	GPIO11_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO11_SMI_ST is set.
0	GPIO10_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO10_SMI_ST is set.

GPIO1 SMI Status Register — Index E9h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO17 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO16_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO16 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO15_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO15 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO14_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO14 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO13_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO13 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO12_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO12 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO11_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO11 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO10_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO10 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

7.7.6 GPIO2x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
D0	GPIO2 Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2 Output Data Register	1	1	1	1	1	1	1	1
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0

GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_OE	R/W	5VSB	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	5VSB	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	5VSB	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	5VSB	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	5VSB	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	5VSB	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	5VSB	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	5VSB	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

GPIO2 Output Data Register — Index D1h (This byte could be also written by base address + 8 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_VAL	R/W	5VSB	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs1 when in output mode.
6	GPIO26_VAL	R/W	5VSB	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs1 when in output mode.
5	GPIO25_VAL	R/W	5VSB	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	5VSB	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	5VSB	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	5VSB	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	5VSB	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.

0	GPIO20_VAL	R/W	5VSB	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

GPIO2 Pin Status Register — Index D2h (This byte could be also read by base address + 8 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_IN	R	-	-	The pin status of RSMRST#/GPIO27.
6	GPIO26_IN	R	-	-	The pin status of PWOK/GPIO26.
5	GPIO25_IN	R	-	-	The pin status of PS_ON#/GPIO25.
4	GPIO24_IN	R	-	-	The pin status of S3#/GPIO24.
3	GPIO23_IN	R	-	-	The pin status of PWSOUT#/GPIO23.
2	GPIO22_IN	R	-	-	The pin status of PWSIN#/GPIO22.
1	GPIO21_IN	R	-	-	The pin status of ATXPG_IN#/GPIO21.
0	GPIO20_IN	R	-	-	The pin status of ALERT#/GPIO20/SCL/CIRRX#.

GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_DRV_EN	R/W	5VSB	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	5VSB	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	5VSB	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	5VSB	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	5VSB	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	5VSB	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	5VSB	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	5VSB	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

7.7.7 GPIO3x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
C0	GPIO3 Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3 Output Data Register	1	1	1	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register	0	0	0	0	0	0	0	0

GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_OE	R/W	LRESET#	0	0: GPIO37 is input. 1: GPIO37 is output.
6	GPIO36_OE	R/W	LRESET#	0	0: GPIO36 is input. 1: GPIO36 is output.
5	GPIO35_OE	R/W	LRESET#	0	0: GPIO35 is input. 1: GPIO35 is output.
4	GPIO34_OE	R/W	LRESET#	0	0: GPIO34 is input. 1: GPIO34 is output.
3	GPIO33_OE	R/W	LRESET#	0	0: GPIO33 is input. 1: GPIO33 is output.
2	GPIO32_OE	R/W	LRESET#	0	0: GPIO32 is input. 1: GPIO32 is output.
1	GPIO31_OE	R/W	LRESET#	0	0: GPIO31 is input. 1: GPIO31 is output.
0	GPIO30_OE	R/W	LRESET#	0	0: GPIO30 is input. 1: GPIO30 is output.

GPIO3 Output Data Register — Index C1h (This byte could be also written by base address + 9 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_VAL	R/W	LRESET#	1	0: GPIO37 outputs 0 when in output mode. 1: GPIO37 outputs 1 when in output mode.
6	GPIO36_VAL	R/W	LRESET#	1	0: GPIO36 outputs 0 when in output mode. 1: GPIO36 outputs 1 when in output mode.
5	GPIO35_VAL	R/W	LRESET#	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_VAL	R/W	LRESET#	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	LRESET#	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	LRESET#	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	LRESET#	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	LRESET#	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

GPIO3 Pin Status Register — Index C2h (This byte could be also read by base address + 9 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_IN	R	-	-	The pin status of SIN3/GPIO37.
6	GPIO36_IN	R	-	-	The pin status of SOUT3/GPIO36.

5	GPIO35_IN	R	-	-	The pin status of DSR3#/GPIO35.
4	GPIO34_IN	R	-	-	The pin status of RTS3#/GPIO34.
3	GPIO33_IN	R	-	-	The pin status of DTR3#/GPIO33.
2	GPIO32_IN	R	-	-	The pin status of CTS3#/GPIO32.
1	GPIO31_IN	R	-	-	The pin status of RI3#/GPIO31.
0	GPIO30_IN	R	-	-	The pin status of DCD3#/GPIO30.

GPIO3 Drive Enable Register — Index C3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DRV_EN	R/W	LRESET#	0	GPIO37 Drive Enable. 0: GPIO37 is open drain. 1: GPIO37 is push pull.
6	GPIO36_DRV_EN	R/W	LRESET#	0	GPIO36 Drive Enable. 0: GPIO36 is open drain. 1: GPIO36 is push pull.
5	GPIO35_DRV_EN	R/w	LRESET#	0	GPIO35 Drive Enable. 0: GPIO35 is open drain. 1: GPIO35 is push pull.
4	GPIO34_DRV_EN	R/W	LRESET#	0	GPIO34 Drive Enable. 0: GPIO34 is open drain. 1: GPIO34 is push pull.
3	GPIO33_DRV_EN	R/W	LRESET#	0	GPIO33 Drive Enable. 0: GPIO33 is open drain. 1: GPIO33 is push pull.
2	GPIO32_DRV_EN	R/W	LRESET#	0	GPIO32 Drive Enable. 0: GPIO32 is open drain. 1: GPIO32 is push pull.
1	GPIO31_DRV_EN	R/W	LRESET#	0	GPIO31 Drive Enable. 0: GPIO31 is open drain. 1: GPIO31 is push pull.
0	GPIO30_DRV_EN	R/W	LRESET#	0	GPIO30 Drive Enable. 0: GPIO30 is open drain. 1: GPIO30 is push pull.

7.7.8 GPIO4x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
B0	GPIO4 Output Enable Register	0	0	0	0	0	0	0	0
B1	GPIO4 Output Data Register	1	1	1	1	1	1	1	1
B2	GPIO4 Pin Status Register	-	-	-	-	-	-	-	-
B3	GPIO4 Driver Enable Register	0	0	0	0	0	0	0	0

GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_OE	R/W	LRESET#	0	0: GPIO47 is input. 1: GPIO47 is output.
6	GPIO46_OE	R/W	LRESET#	0	0: GPIO46 is input. 1: GPIO46 is output.
5	GPIO45_OE	R/W	LRESET#	0	0: GPIO45 is input. 1: GPIO45 is output.
4	GPIO44_OE	R/W	LRESET#	0	0: GPIO44 is input. 1: GPIO44 is output.
3	GPIO43_OE	R/W	LRESET#	0	0: GPIO43 is input. 1: GPIO43 is output.
2	GPIO42_OE	R/W	LRESET#	0	0: GPIO42 is input. 1: GPIO42 is output.
1	GPIO41_OE	R/W	LRESET#	0	0: GPIO41 is input. 1: GPIO41 is output.
0	GPIO40_OE	R/W	LRESET#	0	0: GPIO40 is input. 1: GPIO40 is output.

GPIO4 Output Data Register — Index B1h (This byte could be also written by base address + 10 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DATA	R/W	LRESET#	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_DATA	R/W	LRESET#	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_DATA	R/W	LRESET#	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_DATA	R/W	LRESET#	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3	GPIO43_DATA	R/W	LRESET#	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs 1 when in output mode.
2	GPIO42_DATA	R/W	LRESET#	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs 1 when in output mode.
1	GPIO41_DATA	R/W	LRESET#	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs 1 when in output mode.
0	GPIO40_DATA	R/W	LRESET#	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs 1 when in output mode.

GPIO4 Pin Status Register — Index B2h (This byte could be also read by base address + 10 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_ST	R	-	-	The pin status of SIN4/GPIO47.
6	GPIO46_ST	R	-	-	The pin status of SOUT4/GPIO46.
5	GPIO45_ST	R	-	-	The pin status of DSR4#/GPIO45.

4	GPIO44_ST	R	-	-	The pin status of RTS4#/GPIO44.
3	GPIO43_ST	R	-	-	The pin status of DTR4#/GPIO43.
2	GPIO42_ST	R	-	-	The pin status of CTS4#/GPIO42.
1	GPIO41_ST	R	-	-	The pin status of RI4#/GPIO41.
0	GPIO40_ST	R	-	-	The pin status of DCD4#/GPIO40.

GPIO4 Drive Enable Register — Index B3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DRV_EN	R/W	LRESET#	0	GPIO47 Drive Enable. 0: GPIO47 is open drain. 1: GPIO47 is push pull.
6	GPIO46_DRV_EN	R/W	LRESET#	0	GPIO46 Drive Enable. 0: GPIO46 is open drain. 1: GPIO46 is push pull.
5	GPIO45_DRV_EN	R/w	LRESET#	0	GPIO45 Drive Enable. 0: GPIO45 is open drain. 1: GPIO45 is push pull.
4	GPIO44_DRV_EN	R/W	LRESET#	0	GPIO44 Drive Enable. 0: GPIO44 is open drain. 1: GPIO44 is push pull.
3	GPIO43_DRV_EN	R/W	LRESET#	0	GPIO43 Drive Enable. 0: GPIO43 is open drain. 1: GPIO43 is push pull.
2	GPIO42_DRV_EN	R/W	LRESET#	0	GPIO42 Drive Enable. 0: GPIO42 is open drain. 1: GPIO42 is push pull.
1	GPIO41_DRV_EN	R/W	LRESET#	0	GPIO41 Drive Enable. 0: GPIO41 is open drain. 1: GPIO41 is push pull.
0	GPIO40_DRV_EN	R/W	LRESET#	0	GPIO40 Drive Enable. 0: GPIO40 is open drain. 1: GPIO40 is push pull.

7.7.9 GPIO5x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
A0	GPIO5 Output Enable Register	0	0	0	0	0	0	0	0
A1	GPIO5 Output Data Register	1	1	1	1	1	1	1	1
A2	GPIO5 Pin Status Register	-	-	-	-	-	-	-	-
A3	GPIO5 Drive Enable Register	0	0	0	0	0	0	0	0
A8	GPIO5 SMI Enable Register	0	0	0	0	0	0	0	0
A9	GPIO5 SMI Status Register	0	0	0	0	0	0	0	0

GPIO5 Output Enable Register — Index A0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_OE	R/W	LRESET#	0	0: GPIO57 is in input mode. 1: GPIO57 is in output mode.
6	GPIO56_OE	R/W	LRESET#	0	0: GPIO56 is in input mode. 1: GPIO56 is in output mode.
5	GPIO55_OE	R/W	LRESET#	0	0: GPIO55 is in input mode. 1: GPIO55 is in output mode.
4	GPIO54_OE	R/W	LRESET#	0	0: GPIO54 is in input mode. 1: GPIO54 is in output mode.
3	GPIO53_OE	R/W	LRESET#	0	0: GPIO53 is in input mode. 1: GPIO53 is in output mode.
2	GPIO52_OE	R/W	LRESET#	0	0: GPIO52 is in input mode. 1: GPIO52 is in output mode.
1	GPIO51_OE	R/W	LRESET#	0	0: GPIO51 is in input mode. 1: GPIO51 is in output mode.
0	GPIO50_OE	R/W	LRESET#	0	0: GPIO50 is in input mode. 1: GPIO50 is in output mode.

GPIO5 Output Data Register — Index A1h (This byte could be also written by base address + 5)

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_DATA	R/W	LRESET#	1	0: GPIO57 outputs 0 when in output mode. 1: GPIO57 outputs 1 when in output mode.
6	GPIO56_DATA	R/W	LRESET#	1	0: GPIO56 outputs 0 when in output mode. 1: GPIO56 outputs 1 when in output mode.
5	GPIO55_DATA	R/W	LRESET#	1	0: GPIO55 outputs 0 when in output mode. 1: GPIO55 outputs 1 when in output mode.
4	GPIO54_DATA	R/W	LRESET#	1	0: GPIO54 outputs 0 when in output mode. 1: GPIO54 outputs 1 when in output mode.
3	GPIO53_DATA	R/W	LRESET#	1	0: GPIO53 outputs 0 when in output mode. 1: GPIO53 outputs 1 when in output mode.
2	GPIO52_DATA	R/W	LRESET#	1	0: GPIO52 outputs 0 when in output mode. 1: GPIO52 outputs 1 when in output mode.
1	GPIO51_DATA	R/W	LRESET#	1	0: GPIO51 outputs 0 when in output mode. 1: GPIO51 outputs 1 when in output mode.
0	GPIO50_DATA	R/W	LRESET#	1	0: GPIO50 outputs 0 when in output mode. 1: GPIO50 outputs 1 when in output mode.

GPIO5 Pin Status Register — Index A2h (This byte could be also read by base address + 5)

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_ST	R	-	-	The pin status of GPIO57/WGATE#/DSR6#/T2EX.
6	GPIO56_ST	R	-	-	The pin status of GPIO56/HDSEL#/DTR6#/T2.
5	GPIO55_ST	R	-	-	The pin status of GPIO55/STEP#/CTS6#/P35.
4	GPIO54_ST	R	-	-	The pin status of GPIO54/DIR#/RI6#/P34.
3	GPIO53_ST	R	-	-	The pin status of GPIO53/WDATA#/DCD6#/P33.

2	GPIO52_ST	R	-	-	The pin status of GPIO52/DRVA#/SOUT6/P32.
1	GPIO51_ST	R	-	-	The pin status of GPIO51/MOA#/SIN6/P31.
0	GPIO50_ST	R	-	-	The pin status of GPIO50/DENSEL#/RTS6#/P30.

GPIO5 Drive Enable Register — Index A3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_DRV_EN	R/W	LRESET#	0	GPIO57 Drive Enable. 0: GPIO57 is open drain. 1: GPIO57 is push pull.
6	GPIO56_DRV_EN	R/W	LRESET#	0	GPIO56 Drive Enable. 0: GPIO56 is open drain. 1: GPIO56 is push pull.
5	GPIO55_DRV_EN	R/w	LRESET#	0	GPIO55 Drive Enable. 0: GPIO55 is open drain. 1: GPIO55 is push pull.
4	GPIO54_DRV_EN	R/W	LRESET#	0	GPIO54 Drive Enable. 0: GPIO54 is open drain. 1: GPIO54 is push pull.
3	GPIO53_DRV_EN	R/W	LRESET#	0	GPIO53 Drive Enable. 0: GPIO53 is open drain. 1: GPIO53 is push pull.
2	GPIO52_DRV_EN	R/W	LRESET#	0	GPIO52 Drive Enable. 0: GPIO52 is open drain. 1: GPIO52 is push pull.
1	GPIO51_DRV_EN	R/W	LRESET#	0	GPIO51 Drive Enable. 0: GPIO51 is open drain. 1: GPIO51 is push pull.
0	GPIO50_DRV_EN	R/W	LRESET#	0	GPIO50 Drive Enable. 0: GPIO50 is open drain. 1: GPIO50 is push pull.

GPIO5 SMI Enable Register — Index A8h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO57_SMI_ST is set.
6	GPIO56_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO56_SMI_ST is set.
5	GPIO55_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO55_SMI_ST is set.
4	GPIO54_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO54_SMI_ST is set.
3	GPIO53_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO53_SMI_ST is set.
2	GPIO52_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO52_SMI_ST is set.

1	GPIO51_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO51_SMI_ST is set.
0	GPIO50_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO50_SMI_ST is set.

GPIO5 SMI Status Register — Index A9h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO57 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO56_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO56 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO55_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO55 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO54_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO54 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO53_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO53 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO52_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO52 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO51_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO51 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO50_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO50 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

7.7.10 GPIO6x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
90	GPIO6 Output Enable Register	0	0	0	0	0	0	0	0
91	GPIO6 Output Data Register	1	1	1	1	1	1	1	1
92	GPIO6 Pin Status Register	-	-	-	-	-	-	-	-
93	GPIO6 Drive Enable Register	0	0	0	0	0	0	0	0

GPIO6 Output Enable Register — Index 90h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_OE	R/W	LRESET#	0	0: GPIO67 is in input mode. 1: GPIO67 is in output mode.
6	GPIO66_OE	R/W	LRESET#	0	0: GPIO66 is in input mode. 1: GPIO65 is in output mode.
5	GPIO65_OE	R/W	LRESET#	0	0: GPIO65 is in input mode. 1: GPIO65 is in output mode.
4	GPIO64_OE	R/W	LRESET#	0	0: GPIO64 is in input mode. 1: GPIO64 is in output mode.
3	GPIO63_OE	R/W	LRESET#	0	0: GPIO63 is in input mode. 1: GPIO63 is in output mode.
2	GPIO62_OE	R/W	LRESET#	0	0: GPIO62 is in input mode. 1: GPIO62 is in output mode.
1	GPIO61_OE	R/W	LRESET#	0	0: GPIO61 is in input mode. 1: GPIO61 is in output mode.
0	GPIO60_OE	R/W	LRESET#	0	0: GPIO60 is in input mode. 1: GPIO60 is in output mode.

GPIO6 Output Data Register — Index 91h (This byte could be also written by base address + 4)

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_VAL	R/W	LRESET#	1	0: GPIO67 outputs 0 when in output mode. 1: GPIO67 outputs 1 when in output mode.
6	GPIO66_VAL	R/W	LRESET#	1	0: GPIO66 outputs 0 when in output mode. 1: GPIO66 outputs 1 when in output mode.
5	GPIO65_VAL	R/W	LRESET#	1	0: GPIO65 outputs 0 when in output mode. 1: GPIO65 outputs 1 when in output mode.
4	GPIO64_VAL	R/W	LRESET#	1	0: GPIO64 outputs 0 when in output mode. 1: GPIO64 outputs 1 when in output mode.
3	GPIO63_VAL	R/W	LRESET#	1	0: GPIO63 outputs 0 when in output mode. 1: GPIO63 outputs 1 when in output mode.
2	GPIO62_VAL	R/W	LRESET#	1	0: GPIO62 outputs 0 when in output mode. 1: GPIO62 outputs 1 when in output mode.
1	GPIO61_VAL	R/W	LRESET#	1	0: GPIO61 outputs 0 when in output mode. 1: GPIO61 outputs 1 when in output mode.
0	GPIO60_VAL	R/W	LRESET#	1	0: GPIO60 outputs 0 when in output mode. 1: GPIO60 outputs 1 when in output mode.

GPIO6 Pin Status Register — Index 92h (This byte could be also read by base address + 4)

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_IN	R	-	-	The pin status of S5#/GPIO67.
6	GPIO66_IN	R	-	-	The pin status of DPWROK/GPIO66.
5	GPIO65_IN	R	-	-	The pin status of PME#/GPIO65.
4	GPIO64_IN	R	-	-	The pin status of GPIO64/DSKCHG#/DSR5#.
3	GPIO63_IN	R	-	-	The pin status of GPIO63/WPT#/DTR5#/PWM3.

2	GPIO62_IN	R	-	-	The pin status of GPIO62/INDEX#/CTS5#/PWM2.
1	GPIO61_IN	R	-	-	The pin status of GPIO61/TRK0#/RI5#/PWM1.
0	GPIO60_IN	R	-	-	The pin status of GPIO60/RDATA#/DCD5#/PWM0.

GPIO6 Drive Enable Register — Index 93h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_DRV_EN	R/W	LRESET#	0	0: GPIO67 is open drain in output mode. 1: Reserved.
6	GPIO66_DRV_EN	R/W	LRESET#	0	0: GPIO66 is open drain in output mode. 1: GPIO66 is push pull in output mode.
5	GPIO65_DRV_EN	R/W	LRESET#	0	0: GPIO65 is open drain in output mode. 1: GPIO65 is push pull in output mode.
4	GPIO64_DRV_EN	R/W	LRESET#	0	0: GPIO64 is open drain in output mode. 1: GPIO64 is push pull in output mode.
3	GPIO63_DRV_EN	R/W	LRESET#	0	0: GPIO63 is open drain in output mode. 1: GPIO63 is push pull in output mode.
2	GPIO62_DRV_EN	R/W	LRESET#	0	0: GPIO62 is open drain in output mode. 1: GPIO62 is push pull in output mode.
1	GPIO61_DRV_EN	R/W	LRESET#	0	0: GPIO61 is open drain in output mode. 1: GPIO61 is push pull in output mode.
0	GPIO60_DRV_EN	R/W	LRESET#	0	0: GPIO60 is open drain in output mode. 1: GPIO60 is push pull in output mode.

7.7.11 GPIO7x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
80	GPIO7 Output Enable Register	0	0	0	0	0	0	0	0
81	GPIO7 Output Data Register	1	1	1	1	1	1	1	1
82	GPIO7 Pin Status Register	-	-	-	-	-	-	-	-
83	GPIO7 Drive Enable Register	0	0	0	0	0	0	0	0

GPIO7 Output Enable Register — Index 80h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_OE	R/W	LRESET#	0	0: GPIO77 is in input mode. 1: GPIO77 is in output mode.
6	GPIO76_OE	R/W	LRESET#	0	0: GPIO76 is in input mode. 1: GPIO75 is in output mode.
5	GPIO75_OE	R/W	LRESET#	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.
4	GPIO74_OE	R/W	LRESET#	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	LRESET#	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.

2	GPIO72_OE	R/W	LRESET#	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.
1	GPIO71_OE	R/W	LRESET#	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	LRESET#	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

GPIO7 Output Data Register — Index 81h (This byte could be also written by base address + 3)

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_VAL	R/W	LRESET#	1	0: GPIO77 outputs 0 when in output mode. 1: GPIO77 outputs 1 when in output mode.
6	GPIO76_VAL	R/W	LRESET#	1	0: GPIO76 outputs 0 when in output mode. 1: GPIO76 outputs 1 when in output mode.
5	GPIO75_VAL	R/W	LRESET#	1	0: GPIO75 outputs 0 when in output mode. 1: GPIO75 outputs 1 when in output mode.
4	GPIO74_VAL	R/W	LRESET#	1	0: GPIO74 outputs 0 when in output mode. 1: GPIO74 outputs 1 when in output mode.
3	GPIO73_VAL	R/W	LRESET#	1	0: GPIO73 outputs 0 when in output mode. 1: GPIO73 outputs 1 when in output mode.
2	GPIO72_VAL	R/W	LRESET#	1	0: GPIO72 outputs 0 when in output mode. 1: GPIO72 outputs 1 when in output mode.
1	GPIO71_VAL	R/W	LRESET#	1	0: GPIO71 outputs 0 when in output mode. 1: GPIO71 outputs 1 when in output mode.
0	GPIO70_VAL	R/W	LRESET#	1	0: GPIO70 outputs 0 when in output mode. 1: GPIO70 outputs 1 when in output mode.

GPIO7 Pin Status Register — Index 82h (This byte could be also read by base address + 3)

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_IN	R	-	-	The pin status of GPIO77/STB#.
6	GPIO76_IN	R	-	-	The pin status of GPIO76/AFD#.
5	GPIO75_IN	R	-	-	The pin status of GPIO75/ERR#.
4	GPIO74_IN	R	-	-	The pin status of GPIO74/INIT#.
3	GPIO73_IN	R	-	-	The pin status of GPIO73/SLIN#.
2	GPIO72_IN	R	-	-	The pin status of GPIO72/ACK#.
1	GPIO71_IN	R	-	-	The pin status of GPIO71/BUSY.
0	GPIO70_IN	R	-	-	The pin status of GPIO70/PE/FANCTRL3/PWM_DC3.

GPIO7 Drive Enable Register — Index 83h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_DRV_EN	R/W	LRESET#	0	0: GPIO77 is open drain in output mode. 1: GPIO77 is push pull in output mode.
6	GPIO76_DRV_EN	R/W	LRESET#	0	0: GPIO76 is open drain in output mode. 1: GPIO76 is push pull in output mode.

5	GPIO75_DRV_EN	R/W	LRESET#	0	0: GPIO75 is open drain in output mode. 1: GPIO75 is push pull in output mode.
4	GPIO74_DRV_EN	R/W	LRESET#	0	0: GPIO74 is open drain in output mode. 1: GPIO74 is push pull in output mode.
3	GPIO73_DRV_EN	R/W	LRESET#	0	0: GPIO73 is open drain in output mode. 1: GPIO73 is push pull in output mode.
2	GPIO72_DRV_EN	R/W	LRESET#	0	0: GPIO72 is open drain in output mode. 1: GPIO72 is push pull in output mode.
1	GPIO71_DRV_EN	R/W	LRESET#	0	0: GPIO71 is open drain in output mode. 1: GPIO71 is push pull in output mode.
0	GPIO70_DRV_EN	R/W	LRESET#	0	0: GPIO70 is open drain in output mode. 1: GPIO70 is push pull in output mode.

7.7.12 GPIO8x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
88	GPIO8 Output Enable Register	0	0	0	0	0	0	0	0
89	GPIO8 Output Data Register	1	1	1	1	1	1	1	1
8A	GPIO8 Pin Status Register	-	-	-	-	-	-	-	-
8B	GPIO8 Drive Enable Register	0	0	0	0	0	0	0	0
8E	GPIO8 SMI Enable Register	0	0	0	0	0	0	0	0
8F	GPIO8 SMI Status Register	0	0	0	0	0	0	0	0

GPIO8 Output Enable Register — Index 88h

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_OE	R/W	LRESET#	0	0: GPIO87 is in input mode. 1: GPIO87 is in output mode.
6	GPIO86_OE	R/W	LRESET#	0	0: GPIO86 is in input mode. 1: GPIO85 is in output mode.
5	GPIO85_OE	R/W	LRESET#	0	0: GPIO85 is in input mode. 1: GPIO85 is in output mode.
4	GPIO84_OE	R/W	LRESET#	0	0: GPIO84 is in input mode. 1: GPIO84 is in output mode.
3	GPIO83_OE	R/W	LRESET#	0	0: GPIO83 is in input mode. 1: GPIO83 is in output mode.
2	GPIO82_OE	R/W	LRESET#	0	0: GPIO82 is in input mode. 1: GPIO82 is in output mode.
1	GPIO81_OE	R/W	LRESET#	0	0: GPIO81 is in input mode. 1: GPIO81 is in output mode.
0	GPIO80_OE	R/W	LRESET#	0	0: GPIO80 is in input mode. 1: GPIO80 is in output mode.

GPIO8 Output Data Register — Index 89h (This byte could be also written by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_VAL	R/W	LRESET#	1	0: GPIO87 outputs 0 when in output mode. 1: GPIO87 outputs 1 when in output mode.
6	GPIO86_VAL	R/W	LRESET#	1	0: GPIO86 outputs 0 when in output mode. 1: GPIO86 outputs 1 when in output mode.
5	GPIO85_VAL	R/W	LRESET#	1	0: GPIO85 outputs 0 when in output mode. 1: GPIO85 outputs 1 when in output mode.
4	GPIO84_VAL	R/W	LRESET#	1	0: GPIO84 outputs 0 when in output mode. 1: GPIO84 outputs 1 when in output mode.
3	GPIO83_VAL	R/W	LRESET#	1	0: GPIO83 outputs 0 when in output mode. 1: GPIO83 outputs 1 when in output mode.
2	GPIO82_VAL	R/W	LRESET#	1	0: GPIO82 outputs 0 when in output mode. 1: GPIO82 outputs 1 when in output mode.
1	GPIO81_VAL	R/W	LRESET#	1	0: GPIO81 outputs 0 when in output mode. 1: GPIO81 outputs 1 when in output mode.
0	GPIO80_VAL	R/W	LRESET#	1	0: GPIO80 outputs 0 when in output mode. 1: GPIO80 outputs 1 when in output mode.

GPIO8 Pin Status Register — Index 8Ah (This byte could be also read by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_IN	R	-	-	The pin status of GPIO87/PD7.
6	GPIO86_IN	R	-	-	The pin status of GPIO86/PD6.
5	GPIO85_IN	R	-	-	The pin status of GPIO85/PD5.
4	GPIO84_IN	R	-	-	The pin status of GPIO84/PD4.
3	GPIO83_IN	R	-	-	The pin status of GPIO83/PD3.
2	GPIO82_IN	R	-	-	The pin status of GPIO82/PD2.
1	GPIO81_IN	R	-	-	The pin status of GPIO81/PD1.
0	GPIO80_IN	R	-	-	The pin status of GPIO80/PD0.

GPIO8 Drive Enable Register — Index 8Bh

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_DRV_EN	R/W	LRESET#	0	0: GPIO87 is open drain in output mode. 1: GPIO87 is push pull in output mode.
6	GPIO86_DRV_EN	R/W	LRESET#	0	0: GPIO86 is open drain in output mode. 1: GPIO86 is push pull in output mode.
5	GPIO85_DRV_EN	R/W	LRESET#	0	0: GPIO85 is open drain in output mode. 1: GPIO85 is push pull in output mode.
4	GPIO84_DRV_EN	R/W	LRESET#	0	0: GPIO84 is open drain in output mode. 1: GPIO84 is push pull in output mode.
3	GPIO83_DRV_EN	R/W	LRESET#	0	0: GPIO83 is open drain in output mode. 1: GPIO83 is push pull in output mode.
2	GPIO82_DRV_EN	R/W	LRESET#	0	0: GPIO82 is open drain in output mode. 1: GPIO82 is push pull in output mode.

1	GPIO81_DRV_EN	R/W	LRESET#	0	0: GPIO81 is open drain in output mode. 1: GPIO81 is push pull in output mode.
0	GPIO80_DRV_EN	R/W	LRESET#	0	0: GPIO80 is open drain in output mode. 1: GPIO80 is push pull in output mode.

GPIO8 SMI Enable Register — Index 8Eh

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO87_SMI_ST is set.
6	GPIO86_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO86_SMI_ST is set.
5	GPIO85_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO85_SMI_ST is set.
4	GPIO84_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO84_SMI_ST is set.
3	GPIO83_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO83_SMI_ST is set.
2	GPIO82_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO82_SMI_ST is set.
1	GPIO81_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO81_SMI_ST is set.
0	GPIO80_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO80_SMI_ST is set.

GPIO8 SMI Status Register — Index 8Fh

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO87 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO86_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO86 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO85_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO85 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO84_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO84 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO83_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO83 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO82_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO82 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

1	GPIO81_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO81 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO80_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO80 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

7.8 GPIO8x Scan Code Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
D8	GPIO8 Make Code 0 Register	0	0	0	0	0	0	0	0
D9	GPIO8 Make Code 1 Register	0	0	0	0	0	0	0	0
DA	GPIO8 Make Code 2 Register	0	0	0	0	0	0	0	0
DB	GPIO8 Make Code 3 Register	0	0	0	0	0	0	0	0
DC	GPIO8 Make Code 4 Register	0	0	0	0	0	0	0	0
DD	GPIO8 Make Code 5 Register	0	0	0	0	0	0	0	0
DE	GPIO8 Make Code 6 Register	0	0	0	0	0	0	0	0
DF	GPIO8 Make Code 7 Register	0	0	0	0	0	0	0	0
C8	GPIO8 Pre Code 0 Register	1	1	1	0	0	0	0	0
C9	GPIO8 Pre Code 1 Register	1	1	1	0	0	0	0	0
CA	GPIO8 Pre Code 2 Register	1	1	1	0	0	0	0	0
CB	GPIO8 Pre Code 3 Register	1	1	1	0	0	0	0	0
CC	GPIO8 Pre Code 4 Register	1	1	1	0	0	0	0	0
CD	GPIO8 Pre Code 5 Register	1	1	1	0	0	0	0	0
CE	GPIO8 Pre Code 6 Register	1	1	1	0	0	0	0	0
CF	GPIO8 Pre Code 7 Register	1	1	1	0	0	0	0	0
B8	GPIO8 Scan Code 0 Control Register	0	0	0	0	0	0	0	0
B9	GPIO8 Scan Code 1 Control Register	0	0	0	0	0	0	0	0
BA	GPIO8 Scan Code 2 Control Register	0	0	0	0	0	0	0	0
BB	GPIO8 Scan Code 3 Control Register	0	0	0	0	0	0	0	0
BC	GPIO8 Scan Code 4 Control Register	0	0	0	0	0	0	0	0
BD	GPIO8 Scan Code 5 Control Register	0	0	0	0	0	0	0	0
BE	GPIO8 Scan Code 6 Control Register	0	0	0	0	0	0	0	0
BF	GPIO8 Scan Code 7 Control Register	0	0	0	0	0	0	0	0
AC-AD	Reserved for Fintek.	0	0	0	0	0	0	0	0
AE	GPIO8 Function Select 1 Register	0	0	0	0	0	0	0	0
AF	GPIO8 Function Select 2 Register	0	0	0	0	0	0	0	0

GPIO8 Make Code 0 Register — Index D8h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE0	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO80.

GPIO8 Make Code 1 Register — Index D9h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE1	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µCThe source of event is GPIO81.

GPIO8 Make Code 2 Register — Index DAh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE2	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC The source of event is GPIO82.

GPI8O Make Code 3 Register — Index DBh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE3	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO83.

GPIO8 Make Code 4 Register — Index DCh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE4	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO84.

GPIO8 Make Code 5 Register — Index DDh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE5	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO85.

GPIO Make Code 6 Register — Index DEh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE6	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO86.

GPIO8 Make Code 7 Register — Index DFh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE7	R/W	5VSB	0	This byte is used to assert the make code when the scan code event 0 is occurred. The scan code events will set KBC OBF and put their make/break code into the KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO87.

GPIO8 Pre-Code 0 Register — Index C8h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE0	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 1 Register — Index C9h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE1	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 2 Register — Index CAh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE2	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 3 Register — Index CBh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE3	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 4 Register — Index CCh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE4	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 5 Register — Index CDh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE5	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 6 Register — Index CEh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE6	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 7 Register — Index CFh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE7	R/W	5VSB	0xE0	This byte is used to assert the pre-code before the make/break code when it is enabled.

GPIO8 Scan Code 0 Control Register — Index B8h

Bit	Name	R/W	Reset	Default	Description
7	GP0_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when the scan code event is occurred.
6	GP0_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when the scan code event is occurred.
5	GP0_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when the scan code event is occurred.
4	GP0_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event is occurred. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP0_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP0_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Scan Code 1 Control Register — Index B9h

Bit	Name	R/W	Reset	Default	Description
7	GP1_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurred.
6	GP1_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurred.
5	GP1_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurred.
4	GP1_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurred. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP1_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP1_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Scan Code 2 Control Register — Index BAh

Bit	Name	R/W	Reset	Default	Description
7	GP2_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurred.
6	GP2_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurred.
5	GP2_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurred.
4	GP2_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurred. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP2_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP2_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Scan Code 3 Control Register — Index BBh

Bit	Name	R/W	Reset	Default	Description
7	GP3_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurred.
6	GP3_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurred.
5	GP3_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurred.

4	GP3_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurred. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP3_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP3_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Scan Code 4 Control Register — Index BCh

Bit	Name	R/W	Reset	Default	Description
7	GP4_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurred.
6	GP4_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurred.
5	GP4_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurred.
4	GP4_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurred. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP4_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP4_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Scan Code 5 Control Register — Index BDh

Bit	Name	R/W	Reset	Default	Description
7	GP5_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurred.
6	GP5_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurred.
5	GP5_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurred.
4	GP5_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurred. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP5_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP5_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Scan Code 6 Control Register — Index BEh

Bit	Name	R/W	Reset	Default	Description
7	GP6_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurred.
6	GP6_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurred.
5	GP6_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurred.
4	GP6_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurred. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP6_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP6_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Scan Code 7 Control Register — Index BFh

Bit	Name	R/W	Reset	Default	Description
7	GP7_CTRL_EN	R/W	5VSB	0	Set "1" will assert a left "Ctrl" key code first when scan code event occurred.
6	GP7_ALT_EN	R/W	5VSB	0	Set "1" will assert a left "Alt" key code first when scan code event occurred.
5	GP7_SHIFT_EN	R/W	5VSB	0	Set "1" will assert a left "Shift" key code first when scan code event occurred.
4	GP7_PRE_EN	R/W	5VSB	0	Set "1" will assert a left pre-code first when scan code 0 event occurred. When multiple keys are enabled, the sequence is "Ctrl" → "Alt" → "Shift" → Pre-code → Make/Break code.
3-2	GP7_DELAY_TIME	R/W	5VSB	0	The delay time for repeating the make code could be user defined. µC read this register to determine the delay time.
0	GP7_REP_TIME	R/W	5VSB	0	The repeat time for repeating the make code could be user defined. µC read this register to determine the delay time.

GPIO8 Function Select 1 Register — Index AEh

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO83_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO83 is.
5-4	GPIO82_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO82 is.
3-2	GPIO81_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO81 is.
1-0	GPIO80_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO80 is.

GPIO8 Function Select 2 Register — Index AFh

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO87_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO87 is.
5-4	GPIO86_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO86 is.
3-2	GPIO85_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO85 is.
1-0	GPIO84_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO84 is.

Remark:

GPIO also provides index/data port to access the whole GPIO registers. The index port is base address + 0 and data port is base address + 1. The index for each register is the same as the one for configuration register. For example, to write GPIO0 output enable register 0xAA, below is the procedure:

1. **Write index port 0xF0.**
2. **Write data port 0xAA.**

7.9 WDT Registers (CR07)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	WDT Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F5	WDT Control Register	0	0	0	0	0	0	0	0
F6	WDT Timer Register	0	0	0	0	0	0	0	0
FA	WDT PME Enable Register	0	0	0	1	-	-	-	0

WDT Device Base Address Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	0	Reserved
0	WDT_EN	R/W	5VSB	0	0: disable WDT base address. 1: enable WDT base address.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	5VSB	00h	The MSB of WDT base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	5VSB	00h	The LSB of WDT base address.

Watchdog Control Configuration Register 1 — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R	-	0	Reserved
6	WDTMOUT_STS	R/W	5VSB	0	If watchdog timeout event occurred, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	5VSB	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	5VSB	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	5VSB	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	5VSB	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	5VSB	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

Watchdog Timer Configuration Register 2 — Index F6h

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME	R/W	5VSB	0	Time of watchdog timer (0~255)

Watchdog PME Enable Configuration Register 2 — Index FAh

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME	R	5VSB	0	0: No WDT PME occurred. 1: WDT PME occurred. The WDT PME is occurred one unit before WDT timeout.
6	WDT_PME_EN	R/W	5VSB	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5	Reserved	R	-	0	Reserved
4	WDT_CLK_SEL	R/W	5VSB	1	WDT Clock Source Select 0: Internal 1KHz clock. 1: 1KHZ clock driven by CLKIN.
3-1	Reserved	R	-	0	Reserved
0	WDOUT_EN	R/W	5VSB	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.

7.10 PME, ACPI and EUP Registers (LDN 0x0A)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0
F0	PME Event Enable 1 Register	0	0	0	0	0	0	0	0
F1	PME Event Status 1 Register	-	-	-	-	-	-	-	-
F2	PME Event Enable 2 Register	0	0	0	0	0	0	0	0
F3	PME Event Status 2 Register	-	-	-	-	-	-	-	-
F4	ACPI Control Register 1	-	-	0	0	0	1	1	1
F5	ACPI Control Register 2	-	0	0	1	1	1	-	-
F6	ACPI Control Register 3	0	-	-	0	0	-	-	-
F8	LED Control Register 1	-	0	0	0	0	0	0	0
F9	LED Control Register 2	-	0	0	0	-	0	0	0
FA	LED Control Register 3	-	-	-	-	0	1	1	1
FC	DSW Delay Register	-	-	-	-	-	-	0	0
FE	RI De-bounce Select Register	0	0-	-	-	-	-	0	0
E0	ERP Enable Register	-	-	0	0	1	1	0	0
E1	ERP Control Register 1	1	0	0	0	0	0	0	-
E2	ERP Control Register 2	-	0	0	0	0	0	0	0
E3	ERP PWSIN De-bounce Register	0	0	0	1	0	0	1	1
E4	ERP RSMRST De-bounce Register	0	0	0	0	1	0	0	1
E5	ERP PWSOUT Pulse Register	1	1	0	0	0	1	1	1
E6	ERP PSON De-bounce Register	0	0	0	1	0	0	1	1
E7	ERP Deep S5 Delay Register	0	1	1	0	0	0	1	1
E8	ERP Wakeup Enable Register	0	-	0	1	0	0	0	0

E9	ERP Deep S3 Delay Register	0	0	0	0	1	1	1	1
EC	ERP Mode Select Register	0	0	0	1	0	1	-	-
ED	ERP WDT Control Register	-	-	-	-	-	-	0	0
EE	ERP WDT Time Register	0	0	0	0	0	0	0	0

PME Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	PME_EN	R/W	5VSB	0	PME global enable register. 0: disable PME. 1: enable PME.

PME Event Enable 1 Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	WDT_PME_EN	R/W	5VSB	0	WDT PME event enable. 0: disable WDT PME event. 1: enable WDT PME event.
5	GP_PME_EN	R/W	5VSB	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.
4	MO_PME_EN	R/W	5VSB	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
3	KB_PME_EN	R/W	5VSB	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
2	HM_PME_EN	R/W	5VSB	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
1	PRT_PME_EN	R/W	5VSB	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
0	FDC_PME_EN	R/W	5VSB	0	FDC PME event enable. 0: disable FDC PME event. 1: enable FDC PME event.

PME Event Status 1 Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7	ERP_PME_ST	R/WC	5VSB	-	ERP PME event status. 0: ERP has no PME event. 1: ERP has a PME event to assert. Write 1 to clear to be ready for next PME event.

6	WDT_PME_ST	R/WC	5VSB	-	WDT PME event status. 0: WDT has no PME event. 1: WDT has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	GP_PME_ST	R/WC	5VSB	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	MO_PME_ST	R/WC	5VSB	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	KB_PME_ST	R/WC	5VSB	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	HM_PME_ST	R/WC	5VSB	-	Hardware monitors PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	PRT_PME_ST	R/WC	5VSB	-	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	FDC_PME_ST	R/WC	5VSB	-	FDC PME event status. 0: FDC has no PME event. 1: FDC has a PME event to assert. Write 1 to clear to be ready for next PME event.

PME Event Enable 2 Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7	RI2_PME_EN	R/W	5VSB	0	RI2# PME event enable. 0: disable RI2# PME event. 1: enable RI2# PME event.
6	RI1_PME_EN	R/W	5VSB	0	RI1# PME event enable. 0: disable RI1# PME event. 1: enable RI1# PME event.
5	UART6_PME_EN	R/W	5VSB	0	UART 6 PME event enable. 0: disable UART 6 PME event. 1: enable UART 6 PME event.
4	UART5_PME_EN	R/W	5VSB	0	UART 5 PME event enable. 0: disable UART 5 PME event. 1: enable UART 5 PME event.

3	UART4_PME_EN	R/W	5VSB	0	UART 4 PME event enable. 0: disable UART 4 PME event. 1: enable UART 4 PME event.
2	UART3_PME_EN	R/W	5VSB	0	UART 3 PME event enable. 0: disable UART 3 PME event. 1: enable UART 3 PME event.
1	UART2_PME_EN	R/W	5VSB	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
0	UART1_PME_EN	R/W	5VSB	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.

PME Event Status 2 Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	RI2_PME_ST	R/WC	5VSB	-	RI2# PME event status. 0: RI2# has no PME event. 1: RI2# has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	RI1_PME_ST	R/WC	5VSB	-	RI1# PME event status. 0: RI1# has no PME event. 1: RI1# has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	UART6_PME_ST	R/WC	5VSB	-	UART 6 PME event status. 0: UART 6 has no PME event. 1: UART 6 has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	UART5_PME_ST	R/WC	5VSB	-	UART 5 PME event status. 0: UART 5 has no PME event. 1: UART 5 has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	UART4_PME_ST	R/WC	5VSB	-	UART 4 PME event status. 0: UART 4 has no PME event. 1: UART 4 has a PME event to assert. Write 1 to clear to be ready for next PME event.

2	UART3_PME_ST	R/WC	5VSB	-	UART 3 PME event status. 0: UART 3 has no PME event. 1: UART 3 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UART2_PME_ST	R/WC	5VSB	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	UART1_PME_ST	R/WC	5VSB	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.

ACPI Control Register 1 — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5	EN_GPWAKEUP	R/W	VBAT	0	Set one to enable GPIO SMI event asserted via PWSOUT#.
4	EN_KBWAKEUP	R/W	VBAT	0	Set one to enable keyboard wakeup event asserted via PWSOUT#.
3	EN_MOWAKEUP	R/W	VBAT	0	Set one to enable mouse wakeup event asserted via PWSOUT#.
2-1	PWRCTRL	R/W	VBAT	11	The ACPI Control the PSON_N to always on or always off or keep last state 00 : keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/W	5VSB	1	When 5VSB power lose, it will set to 1, and write 1 to clear it

ACPI Control Register 2 — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6-5	PWROK_DELAY	R/W	5VSB	0	The additional PWROK delay. 00: no delay (default) 01: 100ms. 10: 200ms 11: 400ms.
4-3	VDD_DELAY	R/W	5VSB	11	The PWROK delay timing from VDD3VOK by followed setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms (default)
2	VINDB_EN	R/W	5VSB	1	Enable the ATXPG de-bounce. (10us)
1-0	Reserved	-	-	-	Reserved.

ACPI Control Register 3 — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	S3_SEL	R/W	5VSB	0	Select the KBC S3 condition source. 0: Enter S3 state when internal VDD3VOK signal de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6-5	Reserved	-	5VSB	-	Reserved.
4	PSON_DEL_EN	R/W	5VSB	0	0: PSON# is the inverted of S3# signal. 1: PSON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
3	WDT_PWROK_EN	R/W	5VSB	0	Set “1” to this bit will enable WDT timeout event asset from PWROK pin.
2-0	Reserved	-		-	Reserved.

LED Control Register 1 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	LED_VCC_INV_DIS	R/W	VBAT	0	0: LED_VCC clock output is inverted. 1: LED_VCC clock output is not inverted.
6	LED_VCC_DS3	R/W	VBAT	0	0: Disable LED_VCC deep S3 mode. 1: Enable LED_VCC deep S3 mode. Output 75% duty 0.25HZ clock.
5-4	LED_VCC_S5_MODE	R/W	VBAT	00	The three bits {LED_VCC_S5_MODE_ADD, LED_VCC_S5_MODE [1:0]} select the LED_VCC mode in S5 state. 000: Sink low. 001: Tri-state or drive high control by GPIO11_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.* *When LED_VCC_INV_DIS is set to “1” the duty is 25%, otherwise, the duty is 75%.
3-2	LED_VCC_S3_MODE	R/W	VBAT	00	The three bits {LED_VCC_S3_MODE_ADD, LED_VCC_S3_MODE [1:0]} select the LED_VCC mode in S3 state. 000: Sink low. 001: Tri-state or drive high control by GPIO11_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.* *When LED_VCC_INV_DIS is set to “1” the duty is 25%, otherwise, the duty is 75%.

1-0	LED_VCC_S0_MODE	R/W	VBAT	00	The three bits {LED_VCC_S0_MODE_ADD, LED_VCC_S0_MODE [1:0]} select the LED_VCC mode in S0 state. 000: Sink low. 001: Tri-state or drive high control by GPIO11_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.* *When LED_VCC_INV_DIS is set to "1" the duty is 25%, otherwise, the duty is 75%.

LED Control Register 2 — Index F9h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	LED_VSB_S5_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S5_MODE.
5	LED_VSB_S3_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S3_MODE.
4	LED_VSB_S0_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S0_MODE.
3	Reserved	-	-	-	Reserved
2	LED_VCC_S5_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S5_MODE.
1	LED_VCC_S3_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S3_MODE.
0	LED_VCC_S0_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S0_MODE.

LED Control Register 3 — Index FAh

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	LED_VSB_DS3	R/W	VBAT	0	0: Disable LED_VSB deep S3 mode. 1: Enable LED_VSB deep S3 mode. Output 0.25HZ clock with 25% duty.
5-4	LED_VSB_S5_MODE	R/W	VBAT	00	The three bits {LED_VSB_S5_MODE_ADD, LED_VSB_S5_MODE [1:0]} select the LED_VSB mode in S5 state. 000: Sink low. 001: Tri-state or drive high control by GPIO10_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.*

3-2	LED_VSB_S3_MODE	R/W	VBAT	00	The three bits {LED_VSB_S3_MODE_ADD, LED_VSB_S3_MODE [1:0]} select the LED_VSB mode in S3 state. 000: Sink low. 001: Tri-state or drive high control by GPIO10_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.*
1-0	LED_VSB_S0_MODE	R/W	VBAT	00	The three bits {LED_VSB_S0_MODE_ADD, LED_VSB_S0_MODE [1:0]} select the LED_VSB mode in S0 state. 000: Sink low. 001: Tri-state or drive high control by GPIO10_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.*

DSW Delay Register — Index FCh

Bit	Name	R/W	Reset	Default	Description
7	E2H_PME_ST	R/WC	-	-	EC to Host PME event status. 0: EC to Host has no PME event. 1: EC to Host has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	CIR_PME_ST	R/WC	5VSB	-	CIR wakeup PME event status. 0: CIR wakeup has no PME event. 1: CIR wakeup a PME event to assert. Write 1 to clear to be ready for next PME event.
5	E2H_PME_EN	R/WC	-	-	EC to Host PME event enable. 0: Disable EC to Host PME event. 1: Enable EC to Host PME event.
4	CIR_PME_EN	R/WC	5VSB	-	CIR event enable. 0: Disable CIR PME event. 1: Enable CIR PME event.
3-0	DSW_DELAY	R/W	5VSB	7	This is the delay time between SUS_WARN# and SUS_ACK#. The unit is 0.5 sec. Default time is 3.5s ~ 4s. The default could be trimmed to 0s ~ 0.5s.

RI De-bounce Select Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved
1-0	RI_DB_SEL	R/W	5VSB	0	Select RI# de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

ERP Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	ERP_EN	R/W	VBAT	0	0 : disable ERP function 1: enable ERP function
6	S3_BACK	R/W	VBAT	0	This bit will set “1” when system is back from S3 state.
5-2	Reserved	-	-	-	Reserved
1	RING_PME_EN	R/W	VBAT	0	RING1 PME event enable. 0: disable RING1 PME event. 1: enable RING1 PME event, when RING1 falling edge detect
0	RING_PWSOUT_EN	R/W	VBAT	0	RING1 PWSOUT event enable. 0: disable RING1 PWSOUT event. 1: enable RING1 PWSOUT event, when RING1 falling edge detect

ERP Control Register 1 — Index E1h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved
5	S3_ ERP_CTRL1#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL1# will output Low when S3 state. Else If set to “1” ERP_CTRL1# will output High when S3 state.
4	S3 _ ERP_CTRL0#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL0# will output Low when S3 state. Else If set to “1” ERP_CTRL0# will output High when S3 state.
3	S5 _ ERP_CTRL1#_DIS	R/W	VBAT	1	If clear to “0” ERP_CTRL1# will output Low when S5 state. Else If set to “1” ERP_CTRL1# will output High when S5 state.
2	S5 _ ERP_CTRL0#_DIS	R/W	VBAT	1	If clear to “0” ERP_CTRL0# will output Low when S5 state. Else If set to “1” ERP_CTRL0# will output High when S5 state.
1	AC_ ERP_CTRL1#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL1# will output Low when after AC lost. Else If set to “1” ERP_CTRL1# will output High when after AC lost.
0	AC_ ERP_CTRL0#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL0# will output Low when after AC lost. Else If set to “1” ERP_CTRL0# will output High when after AC lost.

ERP Control Register 2 — Index E2h

Bit	Name	R/W	Reset	Default	Description
7	AC_LOST	R	5VSB	1	This bit is AC lost status and writes 1 to this bit will clear it.
6	Reserved	R/W	VBAT	0	Reserved

5	VSB_CTRL_EN[1]	R/W	VBAT	1'b0	0: Disable ERP_CTRL1# assert RSMRST low 1: Enable ERP_CTRL1# assert RSMRST low
4	VSB_CTRL_EN[0]	R/W	VBAT	1'b0	0: Disable ERP_CTRL0# assert RSMRST low 1: Enable ERP_CTRL0# assert RSMRST low
3-2	Reserved	R/W	VBAT	0	Reserved
1	RSMRST_DET_5V_N	R/W	VBAT	0	Device detects 5VSB power ok (4.4V) and VSB3V_IN become high, and after ~50ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check 5VSB power ok.
0	Reserved	R	-	-	Reserved

ERP PWSIN De-bounce Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7-0	PWSIN_DEB_TIME	R/W	VBAT	13h	PWSIN# pin input de-bounce time. The unit is 1ms, default is 20ms.

ERP RSMRST De-bounce Register — Index E4h

Bit	Name	R/W	Reset	Default	Description
7-0	RSMRST_DEB_TIME	R/W	VBAT	9h	RSMRST internal de-bounce time. The unit is 1ms and default is 10ms.

ERP PWSOUT Pulse Width Register — Index E5h

Bit	Name	R/W	Reset	Default	Description
7-0	PWSOUT_PW	R/W	VBAT	C7h	PWSOUT output pulse width. The unit is 1ms and default is 200ms.

ERP PWSIN De-bounce Register — Index E6h

Bit	Name	R/W	Reset	Default	Description
7-0	PSON_DEB_TIME	R/W	VBAT	13h	PSON# pin input de-bounce time. The unit is 1ms, default is 10ms.

ERP Deep S5 Delay Register — Index E7h

Bit	Name	R/W	Reset	Default	Description
7-0	DS5_DELAY_TIME	R/W	VBAT	63h	The delay time from S5 state to deep S5 state. The unit is 64ms and default is 6.4 sec.

ERP Wakeup Enable Register — Index E8h

Bit	Name	R/W	Reset	Default	Description
7	RI2_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable RI2# event to wakeup system.
6	Reserved	-	-	-	Reserved
5	RI1_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable RI1# event to wakeup system.
4	Reserved	R/W	VBAT	0	Reserved
3	GP_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable GPIO event to wakeup system.
2	TMOUT_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Timeout event to wakeup system.
1	MO_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Mouse event to wakeup system.
0	KB_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Keyboard event to wakeup system.

ERP Deep S3 Delay Register — Index E9h

Bit	Name	R/W	Reset	Default	Description
7-0	DS3_DELAY_TIME	R/W	VBAT	Fh	The delay time from S3 state to deep S3 state. The unit is 64ms and default is 1.024 sec.

ERP Mode Select Register — Index ECh

Bit	Name	R/W	Reset	Default	Description
7-6	ERP_MODE	R/W	VBAT	0	00: Fintek G3' mode. 01: Intel DSW + Fintek G3` mode. 10: Reserved. 11: Intel DSW mode.
5	DPWROK_CTRL_EN	R/W	VBAT	0	Set "1" to enable DPWROK reset by ERP_CTRL1#.
4	SOFT_START_EN	R/W	VBAT	1	0: disable ERP soft start. 1: enable ERP soft start.
3-2	SOFT_START_RATE	R/W	VBAT	1h	The soft start rate. 00: 5ms. 01: 10ms. 10: 27ms. 11: 54ms.
1-0	Reserved	-	-	-	Reserved

ERP WDT Control Register — Index EDh

Bit	Name	R/W	Reset	Default	Description
7-6	ERP_WD_TIME[11:10]	R/W	VBAT	-	Time of ERP watchdog timer. Write index EEh will load watchdog time.
7-5	Reserved	R	-	-	Reserved
4	ERP_WDTMOUT_STATUS	R	VBAT	-	Watchdog timeout status.
3-2	ERP_WD_TIME[9:8]	R/W	VBAT	-	Reserved
1	WD_UNIT	R/W	VBAT	0	ERP WDT unit. It is the time unit of ERP_WD_TIME. 0: 1sec. 1: 60 sec.
0	WD_EN	R/W	VBAT	0	Set "1" to enable ERP WDT. Auto clear if timeout occurred.

ERP WDT Time Register — Index EEh

Bit	Name	R/W	Reset	Default	Description
7-0	ERP_WD_TIME	R/W	VBAT	0	Time of ERP watchdog timer.

7.11 RTC RAM Registers (LDN 0x0B)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	RTC RAM Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	1
61	Base Address Low Register	1	0	0	1	0	1	0	1

RTC RAM Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	RTC_RAM_EN	R/W	VBAT	1	0: disable RTC RAM. 1: enable RTC RAM.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	VBAT	02h	The MSB of RTC RAM base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	VBAT	95h	The LSB of RTC RAM base address. The RTC RAM is accessed by index/data port. The index port is {BASE_ADDR_HI, BASE_ADDR_LO[7:1],1'b0} and the data port is {BASE_ADDR_HI, BASE_ADDR_LO[7:1], 1'b1}. Write the index first to select the RAM address and then read/write data port to access the context of RAM.

7.12 H2E Configuration Registers (LDN 0x0E)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H2E I/O Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	H2E IRQ Channel Select Register	-	-	-	-	0	0	0	0

FDC Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	H2E_EN	R/W	5VSB	1	0: disable H2E. 1: enable H2E.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	5VSB	00h	The MSB of H2E base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	5VSB	00h	The LSB of H2E base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELH2EIRQ	R/W	5VSB	00h	Select the IRQ channel for H2E.

7.13 Debug Port Host Side Registers (LDN 0x0F)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Debug Port I/O Port Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0

Debug Port I/O Port Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	DBPORT_IO_EN	R/W	5VSB	0	0: disable Debug Port I/O port. 1: enable Debug Port I/O port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	5VSB	00h	The MSB of Debug Port base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	5VSB	00h	The LSB of Debug Port base address.

Debug Port Read Data Register — Offset + 0x00

Bit	Name	R/W	Reset	Default	Description
7-0	DBPORT_DATA	R	5VSB	00h	The reading of µC side register from the debug port.

Debug Port Control Register — Offset + 0x01

Bit	Name	R/W	Reset	Default	Description
7	BRK_PRT_TRIG	R	-	0	Status of breakpoint trigger.

6-1	Reserved	-	5VSB	-	Reserved
0	DBPORT_EN	R/W	5VSB	0	Set "!" to enable debug port. Debug port register could be accessed by set address to 0x3200 + offset. To access the µC side register including SFR and RAM data. Entry key should be entered via the debug port µC side register.

Debug Port Control Register — Offset + 0x01

Bit	Name	R/W	Reset	Default	Description
7	BRK_PRT_TRIG	R	5VSB	0	Status of breakpoint trigger.
6-1	Reserved	-	-	-	Reserved
0	DBPORT_EN	R/W	5VSB	0	Set "!" to enable debug port. Debug port register could be accessed by set address to 0x3200 + offset. To access the µC side register including SFR and RAM data. Entry key should be entered via debug port µC side register.

Debug Port Address Low Byte Register — Offset + 0x04

Bit	Name	R/W	Reset	Default	Description
7-0	DBPORT_L_ADDR	R/W	5VSB	0	Address low byte for µC side register address.

Debug Port Address High Byte Register — Offset + 0x05

Bit	Name	R/W	Reset	Default	Description
7-0	DBPORT_H_ADDR	R/W	5VSB	0	Address high byte for µC side register address.

7.14 UART1 Registers (CR10)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	IRQ Share Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	9bit-mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9bit-mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Register	0	0	0	0	0	-	0	0

UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UART 1_EN	R/W	LRESET#	1	0: disable UART 1 I/O Port. 1: enable UART 1 I/O Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of UART 1 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	F8h	The LSB of UART 1 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUR1IRQ	R/W	LRESET#	4h	Select the IRQ channel for UART 1.

IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LREST#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART1_CLK_SEL	R/W	LRESET#	0	Select the clock source for UART1. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 1. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 2. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR 0101_1100b SADEN 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 3. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 4. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR 0101_1100b SADEN 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LREST#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LREST#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).

2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

7.15 UART2 Registers (CR11)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	1	1	0	0	0
F0	IRQ Share Register	-	-	-	-	0	0	1	1
F2	Clock Select Register	0	0	0	0	-	-	0	0
F4	9bit-mode Slave Address Register	-	-	-	-	-	-	0	0
F5	9bit-mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F0	IRQ Share Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Register	0	0	0	0	0	-	0	0

UART 2 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UART2_EN	R/W	LRESET#	1	0: disable UART 2 I/O Port. 1: enable UART 2 I/O Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	02h	The MSB of UART 2 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-1	BASE_ADDR_LO	R/W	LRESET#	F8h	The LSB of UART 2 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUR12RQ	R/W	LRESET#	3h	Select the IRQ channel for UART 2.

IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART2 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART2_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART2. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 5. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 6. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 7. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 8. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR: 0101_1100b SADEN: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART2 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
2	Reserved	-	LRESET#	-	Reserved.
1-0	FIFO_MODE	R/W	LREST#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

7.16 UART3 Registers (CR12)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	0	1	0	0	0
F0	IRQ Share Register	-	-	-	-	0	0	1	1
F2	Clock Select Register	0	0	0	0	-	-	0	0
F4	9bit-mode Slave Address Register	-	-	-	-	-	-	0	0
F5	9bit-mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F0	IRQ Share Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Register	0	0	0	0	0	-	0	0

UART 3 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UART3_EN	R/W	LRESET#	1	0: disable UART 3 I/O Port. 1: enable UART 3 I/O Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of UART 3 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	E8h	The LSB of UART 3 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART3IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 3.

IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)

5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART3 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART3_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART3. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 9. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 10. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 11. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 12. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR 0101_1100b SADEN 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART3 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

7.17 UART4 Registers (CR13)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	0	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	IRQ Share Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	9bit-mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9bit-mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Register	0	0	0	0	0	-	0	0

UART 4 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UART4_EN	R/W	LRESET#	1	0: disable UART 4 I/O Port. 1: enable UART 4 I/O Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of UART 4 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	E8h	The LSB of UART 4 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART4IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 4.

IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)

5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	LRESET#	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART4 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART4_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART4. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 13. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 14. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 15. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 16. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART4 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

7.18 UART5 Registers (CR14)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	IRQ Share Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	0	0	0	0	-	-	0	0
F4	9bit-mode Slave Address Register	-	-	-	-	-	-	0	0
F5	9bit-mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F0	IRQ Share Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Register	0	0	0	0	0	-	0	0

UART 5 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UART5_EN	R/W	LRESET#	0	0: disable UART 5 I/O Port. 1: enable UART 5 I/O Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of UART 5 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	The LSB of UART 5 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART5IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 5.

IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.

6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	LRESET#	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART5 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART5_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART5. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 17. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 18. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 19. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 20. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR: 0101_1100b SADEN: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART5 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

7.19 UART6 Registers (CR15)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	IRQ Share Register	0	0	0	0	0	0	0	0
F1	IR Mode Register	-	-	-	0	0	1	0	0
F2	Clock Select Register	-	-	-	0	0	0	0	0
F4	9bit-mode Slave Address Register	-	-	-	-	-	-	0	0
F5	9bit-mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F0	IRQ Share Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Register	0	0	0	0	0	-	0	0

UART 6 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UART6_EN	R/W	LRESET#	0	0: disable UART 6 I/O Port. 1: enable UART 6 I/O Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of UART 6 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	The LSB of UART 6 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART6IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 6.

IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.

6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3	RXW4C_IR	R/W	LRESET#	0	0 : No reception delay when SIR is changed from TX to RX. 1 : Reception delay 4 character-time when SIR is changed from TX to RX.
2	TXW4C_IR	R/W	LRESET#	0	0 : No transmission delay when SIR is changed from RX to TX. 1 : Transmission delay 4 character-time when SIR is changed from RX to TX.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART5 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

IR Mode Select Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved. Return 010b when read.
4-3	IRMODE1 IRMODE0	R/W	LRESET#	00b	0X: Disable IR1 function. 10 : Enable IR1 function, active pulse is 1.6uS. 11 : Enable IR1 function, active pulse is 3/16 bit time.
2	HDUPLX	R/W	LRESET#	1	0 : Full Duplex function for IR self test. 1 : Half Duplex function. Return 1 when read.
1	TXINV_IR	R/W	LRESET#	0	0 : IRTX is not inversed. 1 : Inverse the IRTX.
0	RXINV_IR	R/W	LRESET#	0	0 : IRRX is not inversed. 1 : Inverse the IRRX.

Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART6_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART6. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 21. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 22. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 23. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 24. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.

3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 will select the UART5 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

7.20 µC Side Registers

The µC side registers are basically accessed by µC with the MOVX instruction. Every device (peripheral) has its own base address. The address mapping is list as following table.

Device	Base Address	Range	Remark
INTC	0x1000	256 bytes	Interrupt Control
GCTRL	0x1100	256 bytes	General Control
PWM	0x1200	256 bytes	
SRAM1	0x1300	256 bytes	
SRAM2	0x1400	256 bytes	
E2H	0x1500	256 bytes	EC to host
Embedded Flash	0x1F00	256 bytes	
HWM	0x2000	256 bytes	Could accessed by host side
GPIO	0x2100	256 bytes	Could accessed by host side
KBC	0x2200	256 bytes	
ACPI	0x2300	256 bytes	
CFG	0x2400	256 bytes	Configuration; Could be accessed by host side
RAM	0x2500	256 bytes	Could be accessed by host side
CIR	0x2600	256 bytes	
µC_SFR	0x3000	256 bytes	For Debug Port only
µC_RAM	0x3100	256 bytes	For Debug Port only
DBPORT	0x3200	256 bytes	For Debug Port only

7.20.1 Interrupt Control µC Side Register (Base Address 0x1000, 256 bytes)

Interrupt Status Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	CIR_INT_ST	R/WC	5VSB	0	0: No CIR interrupt event. 1: A CIR interrupt event occurs. Write “1” to clear this bit.
5	P80_INT_ST	R/WC	5VSB	0	0: No 0x80 port interrupt event. 1: A 0x80 port interrupt event occurs. Write “1” to clear this bit.
4	H2E_INT_ST	R/WC	5VSB	0	0: No H2E interrupt event. 1: A H2E interrupt event occurs. Write “1” to clear this bit.
3	ACPI_INT_ST	R/WC	5VSB	0	0: No ACPI interrupt event. 1: An ACPI interrupt event occurs. Write “1” to clear this bit.
2	KBC_INT_ST	R/WC	5VSB	0	0: No KBC interrupt event. 1: A KBC interrupt event occurs. Write “1” to clear this bit.
1	GPIO_INT_ST	R/WC	5VSB	0	0: No GPIO interrupt event. 1: A GPIO interrupt event occurs. Write “1” to clear this bit.
0	HM_INT_ST	R/WC	5VSB	0	0: No hardware monitor interrupt event. 1: A hardware monitor interrupt event occurs. Write “1” to clear this bit.

Interrupt Enable Register — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	CIR_INT_EN	R/WC	5VSB	0	0: Disable CIR interrupt. 1: Enable CIR interrupt.
5	P80_INT_EN	R/WC	5VSB	0	0: Disable 0x80 Port interrupt. 1: Enable 0x80 Port interrupt.
4	H2E_INT_EN	R/WC	5VSB	0	0: Disable Host to EC interrupt. 1: Enable Host to EC interrupt.
3	ACPI_INT_EN	R/WC	5VSB	0	0: Disable ACPI interrupt. 1: Enable ACPI interrupt.
2	KBC_INT_EN	R/WC	5VSB	0	0: Disable KBC interrupt. 1: Enable KBC interrupt.
1	GPIO_INT_EN	R/WC	5VSB	0	0: Disable GPIO interrupt. 1: Enable GPIO interrupt.
0	HM_INT_EN	R/WC	5VSB	0	0: Disable HM interrupt. 1: Enable HM interrupt. The peripheral interrupt is asserted to INT1# of µC.

Interrupt Polarity Register — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	CIR_INT_POL	R/WC	5VSB	0	0: Rising edge of event will trigger an interrupt. 1: Falling edge of event will trigger an interrupt.

5	P80_INT_POL	R/WC	5VSB	0	0: Rising edge of event will trigger an interrupt. 1: Falling edge of event will trigger an interrupt.
4	H2E_INT_POL	R/WC	5VSB	0	0: Rising edge of event will trigger an interrupt. 1: Falling edge of event will trigger an interrupt.
3	ACPI_INT_POL	R/WC	5VSB	0	0: Rising edge of event will trigger an interrupt. 1: Falling edge of event will trigger an interrupt.
2	KBC_INT_POL	R/WC	5VSB	0	0: Rising edge of event will trigger an interrupt. 1: Falling edge of event will trigger an interrupt.
1	GPIO_INT_POL	R/WC	5VSB	0	0: Rising edge of event will trigger an interrupt. 1: Falling edge of event will trigger an interrupt.
0	HM_INT_POL	R/WC	5VSB	0	0: Rising edge of event will trigger an interrupt. 1: Falling edge of event will trigger an interrupt.

Interrupt Status 3 Register — Offset 10h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	PD_INT_ST	R/WC	5VSB	0	0: No power down event 1: A power down event occurs. It is set by falling edge of PWROK. It is cleared by read this bit.
0	DBPORT_INT_ST	R/WC	5VSB	0	0: No debug port event. 1: A debug port interrupt event occurs. Clear by reading this bit.

Power Fail Register — Offset 11h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	PWROK	R	5VSB	0	Status of PWROK.
0	PD_INT_EN	R/WC	5VSB	0	Set “1” to enable power fail interrupt.

7.20.2 General Control µC Side Register (Base Address 0x1100, 256 bytes)

Chip ID 1 Register — Offset 00h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIPID1	R	-	0x00	Chip ID 1

Chip ID 2 Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIPID2	R	-	0x95	Chip ID 2

µC Reset Select Register — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved.

0	EC_GRST	R/W	5VSB	0	0: µC and peripherals are reset by 5VSB power on reset, µC watchdog timerout reset and Debug port exit reset. 1: µC and peripherals are reset by 5VSB power on reset and Debug port exit reset.

WDT Reset Gate 1 Register — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7	SMFI_WD_RST_DIS	R/W	5VSB	1	0: SMFI will reset by µC watchdog timeout. 1: SMFI won't be reset by µC watchdog timeout.
6-5	Reserved	-	-	-	Reserved.
4	INTC_WD_RST_DIS	R/W	5VSB	1	0: INTC will reset by µC watchdog timeout. 1: INTC won't be reset by µC watchdog timeout.
3-2	Reserved	-	-	-	Reserved.
1	CIR_WD_RST_DIS	R/W	5VSB	1	0: CIR will reset by µC watchdog timeout. 1: CIR won't be reset by µC watchdog timeout.
0	PWM_WD_RST_DIS	R/W	5VSB	1	0: PWM will reset by µC watchdog timeout. 1: PWM won't be reset by C watchdog timeout.

WDT Reset Gate 2 Register — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	ACPI_WD_RST_DIS	R/W	5VSB	1	0: ACPI will reset by µC watchdog timeout. 1: ACPI won't be reset by µC watchdog timeout.
2	KBC_WD_RST_DIS	R/W	5VSB	1	0: KBC will reset by µC watchdog timeout. 1: KBC won't be reset by µC watchdog timeout.
1	GPIO_WD_RST_DIS	R/W	5VSB	1	0: GPIO will reset by µC watchdog timeout. 1: GPIO won't be reset by µC watchdog timeout.
0	CFG_WD_RST_DIS	R/W	5VSB	1	0: CFG will reset by µC watchdog timeout. 1: CFG won't be reset by µC watchdog timeout

RTC RAM Write Protect Register — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7	RTC_WR_DIS_7	R/W	5VSB	0	Set "1" to enable write protect for RTC RAM index 0xF0 ~ 0xFF.
6	RTC_WR_DIS_6	R/W	5VSB	0	Set "1" to enable write protect for RTC RAM index 0xE0 ~ 0xEF.
5	RTC_WR_DIS_5	R/W	5VSB	0	Set "1" to enable write protect for RTC RAM index 0xD0 ~ 0xDF.

4	RTC_WR_DIS_4	R/W	5VSB	0	Set “1” to enable write protect for RTC RAM index 0xC0 ~ 0xCF.
3	RTC_WR_DIS_3	R/W	5VSB	0	Set “1” to enable write protect for RTC RAM index 0xB0 ~ 0xBF.
2	RTC_WR_DIS_2	R/W	5VSB	0	Set “1” to enable write protect for RTC RAM index 0xA0 ~ 0xAF.
1	RTC_WR_DIS_1	R/W	5VSB	0	Set “1” to enable write protect for RTC RAM index 0x90 ~ 0x9F.
0	RTC_WR_DIS_0	R/W	5VSB	0	Set “1” to enable write protect for RTC RAM index 0x80 ~ 0x8F.

Software Reset 1 Register — Offset 10h

Bit	Name	R/W	Reset	Default	Description
7	RSMFI	W	-	-	Write “1” to assert a software reset to SPI block.
6-5	Reserved	-	-	-	Reserved.
4	RINTC	W	-	-	Write “1” to assert a software reset to INTC block.
3-2	Reserved	-	-	-	Reserved.
1	RCIR	W	-	-	Write “1” to assert a software reset to CIR block.
0	RPWM	W	-	-	Write “1” to assert a software reset to PWM block.

Software Reset 2 Register — Offset 11h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	ACPI_WD_RST_DIS	R/W	5VSB	1	0: ACPI will reset by µC watchdog timeout. 1: ACPI won’t be reset by µC watchdog timeout.
2	KBC_WD_RST_DIS	R/W	5VSB	1	0: KBC will reset by µC watchdog timeout. 1: KBC won’t be reset by µC watchdog timeout.
1	GPIO_WD_RST_DIS	R/W	5VSB	1	0: GPIO will reset by µC watchdog timeout. 1: GPIO won’t be reset by µC watchdog timeout.
0	CFG_WD_RST_DIS	R/W	5VSB	1	0: CFG will reset by µC watchdog timeout. 1: CFG won’t be reset by µC watchdog timeout.

Software Reset 2 Register — Offset 11h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	RACPI	W	5VSB	-	Write “1” to assert a software reset to ACPI block.
2	RKBC	W	5VSB	-	Write “1” to assert a software reset to KBC block.
1	RGPIO	W	5VSB	-	Write “1” to assert a software reset to GPIO block.
0	RCFG	W	5VSB	-	Write “1” to assert a software reset to CFG block.

7.20.3 PWM Control µC Side Register (Base Address 0x1200, 256 bytes)

Clock Group 0 Divisor Register — Offset 00h

Bit	Name	R/W	Reset	Default	Description
7-0	GR0_DIV	R/W	5VSB	0x00	Clock group 0 divisor. The group 0 clock will be 12MHz/(GR0_DIV +1)*256.

Clock Group 1 Divisor Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7-0	GR1_DIV	R/W	5VSB	0x00	Clock group 1 divisor. The group 2 clock will be 12MHz/(GR0_DIV +1)*256.

Clock Group 2 Divisor Register — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7-0	GR2_DIV	R/W	5VSB	0x00	Clock group 2 divisor. The group 2 clock will be 12MHz/(GR0_DIV +1)*256.

Clock Group 3 Divisor Register — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7-0	GR3_DIV	R/W	5VSB	0x00	Clock group 3 divisor. The group 3 clock will be 12MHz/(GR0_DIV +1)*256. The PWM clock source could be select among these four group clock.

PWM Polarity Register — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	PWM3_POL	R/W	5VSB	0	0: Normal PWM output. 1: PWM output is inverted.
2	PWM2_POL	R/W	5VSB	0	0: Normal PWM output. 1: PWM output is inverted.
1	PWM1_POL	R/W	5VSB	0	0: Normal PWM output. 1: PWM output is inverted.
0	PWM0_POL	R/W	5VSB	0	0: Normal PWM output. 1: PWM output is inverted.

PWM Group Select Register — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7-6	PCS3	R/W	5VSB	00	00: PWM3 clock source is group 0 clock. 01: PWM3 clock source is group 1 clock. 10: PWM3 clock source is group 2 clock. 11: PWM3 clock source is group 3 clock.
5-4	PCS2	R/W	5VSB	00	00: PWM2 clock source is group 0 clock. 01: PWM2 clock source is group 1 clock. 10: PWM2 clock source is group 2 clock. 11: PWM2 clock source is group 3 clock.

3-2	PCS1	R/W	5VSB	00	00: PWM1 clock source is group 0 clock. 01: PWM1 clock source is group 1 clock. 10: PWM1 clock source is group 2 clock. 11: PWM1 clock source is group 3 clock.
1-0	PCS0	R/W	5VSB	00	00: PWM0 clock source is group 0 clock. 01: PWM0 clock source is group 1 clock. 10: PWM0 clock source is group 2 clock. 11: PWM0 clock source is group 3 clock.

PWM Clock Gate Register — Offset 08h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	PCSGR3	R/W	5VSB	0	0: Enable PWM3 clock. 1: Disable PWM3 clock.
2	PCSGR2	R/W	5VSB	0	0: Enable PWM2 clock. 1: Disable PWM2 clock.
1	PCSGR1	R/W	5VSB	0	0: Enable PWM1 clock. 1: Disable PWM1 clock.
0	PCSGR0	R/W	5VSB	0	0: Enable PWM0 clock. 1: Disable PWM0 clock.

PWM Type Register — Offset 09h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	PWM3_TYPE	R/W	5VSB	0	0: Open drain. 1: Push pull.
2	PWM2_TYPE	R/W	5VSB	0	0: Open drain. 1: Push pull.
1	PWM1_TYPE	R/W	5VSB	0	0: Open drain. 1: Push pull.
0	PWM0_TYPE	R/W	5VSB	0	0: Open drain. 1: Push pull.

PWM Enable Register — Offset 0Ah

Bit	Name	R/W	Reset	Default	Description
7	SOFT_RST	W	5VSB	0	Write “1” to software reset PWM block.
6-1	Reserved	-	-	-	Reserved.
0	PCCE	R/W	5VSB	0	0: Disable PWM. All clocks will be disabled. 1: Enable PWM.

PWM0 Duty Control Register — Offset 10h

Bit	Name	R/W	Reset	Default	Description
7-0	DCR0	R/W	5VSB	0	The duty cycle of PWM0 will be (DCR0/255)*100%. Set 0 to force stop and 0xFF to force 100% duty.

PWM1 Duty Control Register — Offset 11h

Bit	Name	R/W	Reset	Default	Description
7-0	DCR1	R/W	5VSB	0	The duty cycle of PWM1 will be (DCR1/255)*100%. Set 0 to force stop and 0xFF to force 100% duty.

PWM2 Duty Control Register — Offset 12h

Bit	Name	R/W	Reset	Default	Description
7-0	DCR2	R/W	5VSB	0	The duty cycle of PWM2 will be (DCR2/255)*100%. Set 0 to force stop and 0xFF to force 100% duty.

PWM3 Duty Control Register — Offset 13h

Bit	Name	R/W	Reset	Default	Description
7-0	DCR3	R/W	5VSB	0	The duty cycle of PWM3 will be (DCR3/255)*100%. Set 0 to force stop and 0xFF to force 100% duty.

7.20.4 µC Side SRAM1 Register (Base Address 0x1300, 256 bytes)

Offset 00h ~ FFh, 256 bytes SRAM accssed by µC, SRAM Powered by I_VSB3V

7.20.5 µC Side SRAM2 Register (Base Address 0x1400, 256 bytes)

Offset 00h ~ FFh, 256 bytes SRAM accssed by µC, SRAM powered by I_VSB3V

7.20.6 Host to EC Control µC Side Register (Base Address 0x1500, 256 bytes)

Host to EC Control Register — Offset 00h

Bit	Name	R/W	Reset	Default	Description
7	P80_DEC_RANGE	R/W	5VSB	0	0: 0x80 port will decode all 16-bit address. 1: 0x80 port will decode 15-bit address, ignore LSB.
6	E2H_INT_EN	R/W	5VSB	0	0: Disable EC to Host interrupt. 1: Assert to Host (if SIRQ channel is enabled) when EC to Host data available which is set by writing E2C_DATA register (offset 02h). Also assert SMI event to PME block when this bit is enabled.
5	E2H_DATA_AVAIL	R/W	5VSB	0	This bit is set when µC write data to offset 02h and is clear by host reading the corresponding data. (H2E bass + 02h)
4	H2E_DATA_AVAIL	R	5VSB	0	This bit is set when host write data to offset 01h and is clear by µC reading the corresponding data. (E2H bass + 01h)
3-2	E2H_DATA_TYPE	R/W	5VSB	0	User defined register to define the type of EC to host data (offset + 02h)
1-0	H2E_DATA_TYPE	R	5VSB	0	User defined register to define the type of host to EC data (offset + 01h)

Host to EC Data Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7-0	H2E_DATA	R	5VSB	0x00	This is the data written by host to communicate with µC. The type of this byte is determined by H2E_DATA_TYPE. µC reads this byte and check the H2E_DATA_TYPE to decide what action should be done.

EC to Host Data Register — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7-0	E2H_DATA	R/W	5VSB	0x00	This is the data written by µC to communicate with host. The type of this byte is determined by E2H_DATA_TYPE. Host reads this byte and check the E2H_DATA_TYPE to decide what action should be done.

Port 80 WDT Control Register — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7	P80_WDT_TO_ST	R/W	5VSB	0	This bit is written by µC to indicate a timeout status. Host could write “1” to this bit to clear status.
6	P80_WDT_EN	R	5VSB	0	Host write “1” to this bit to inform µC to enable Port 80 WDT function.
5-4	P80_WDT_UNIT	R	5VSB	0	Written by host to define the time unit. Ex. 00: 100ms. 01: 1 second. 10: 1 minute. 11: 1 hour.
3-0	P80_WDT_PIN	R	5VSB	0	Written by host to define the pins to assert WDT reset signal.

Port 80 WDT Time Register — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_WDT_TIME	R	5VSB	0xff	Written by host to define the time count of WDT.

Port 80 WDT Code Register — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_WDT_CODE	R	5VSB	0xff	Written by host to define the code to start WDT.

Port 80 Code Register — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_CODE	R	5VSB	0xff	This byte record the data write to Port 80 address (default 0x0080).

Port 80 Last Code Register — Offset 07h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_LAST_CODE	R/W	5VSB	0xff	µC could write the last data of 80 port into this byte to record the last code during current boot up.

Port 80 Base Address High Byte Register — Offset 10h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_BASE_H	R/W	5VSB	0x00	The 80 port base address high byte.

Port 80 Base Address Low Byte Register — Offset 11h

Bit	Name	R/W	Reset	Default	Description
7-0	P80_BASE_L	R/W	5VSB	0x00	The 80 port base address low byte.

7.20.7 Embedded Flash Control (base address 0x1F00, 256 byte)

Control Register1 — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7	START_CMD	W	-	-	Write 1 to this bit will start a single byte read or single byte write command
6-2	Reserved	-	-	-	Reserved
1	IFREN	R/W	5VSB	0	Reserved.
0	FLASH_CMD	R/W	5VSB	0	0: Read , 1:Write

Status Register — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved
1	TIMEOUT_STS	R	5VSB	0	This bit indicates that a single byte write command is timeout and failed.
0	CMD_BUSY	R	5VSB	0	This bit indicates the command is still progressing.

Control Register2 — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7-0	ADR_L	R/W	5VSB	0	{ADR_H, ADR_L} is 13-bits address for embedded flash

Control Register3 — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4-0	ADR_H	R/W	5VSB	0	{ADR_H, ADR_L} is 13-bits address for embedded flash

Control Register4 — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7-0	WR_DATA	R/W	5VSB	0	This byte is data for single byte write command.

Control Register5 — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7-0	RD_DATA	R	5VSB	0	This byte is stores data read by a single byte read command.

Fintek Used Only Register 1 — Offset 07h

Bit	Name	R/W	Reset	Default	Description
7-0	Reserved	R/W	5VSB	1	This byte is fintek used only, don't change the default value

Fintek Used Only Register 2 — Offset 0Fh

Bit	Name	R/W	Reset	Default	Description
7-0	Reserved	-	-	-	This byte is fintek used only, don't write to this byte.

7.20.8 Hardware Monitor µC Side Register (base address 0x2000, 256 byte)

7.18.8.1 Temperature Setting

Configuration Register 1 — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	0h	-	0	Reserved
2	POWER_DOWN	R/W	5VSB	0	Hardware monitor function power down.
1	FAN_START	R/W	5VSB	1	Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	5VSB	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

Protection Mode Configuration Register — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Dummy register.
6	CASE_BEEP_EN	R/W	5VSB	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.
5-4	OVT_MODE	R/W	5VSB	0	00: The OVT# will be low active level mode. 01: The OVT# will be low pulse mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	Reserved	R/W	-	0	Dummy register.
2	CASE_SMI_EN	R/W	5VSB	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	5VSB	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

Case Open Status Register — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	R/W	-	0	Reserved
0	CASE_STS	R/W	VBAT	0	Case open event status, write 1 to clear if case open event cleared. (This bit is powered by VBAT.)

Configuration Register 2— Offset 04h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	BIAS_EN	R/W	5VSB	0	Reserved for Fintek use only
5-1	Reserved	R/W	-	-	Reserved
0	S3_HM_EN	R/W	5VSB	0	Set 1 to enable monitoring at S3 state.

TSI Control Register1 — Offset 08h

Bit	Name	R/W	Reset	Default	Description
7-1	TSI_ADDR	R/W	5VSB	26h	AMD TSI or Intel IBex slave address
0	Reserved	-	-	-	Reserved

TSI Control Register2 — Offset 09h

Bit	Name	R/W	Reset	Default	Description
7-1	SMB_ADDR	R/W	5VSB	0	Address for I2C master to use a block write command
0	Reserved	-	-	-	Reserved

Configuration Register 3 — Offset 0Ah

Bit	Name	R/W	Reset	Default	Description
7	BETA_EN2	R/W	5VSB	0	0: disable the T2 beta compensation. 1: enable the T2 beta compensation.
6	BETA_EN1	R/W	5VSB	0	0: disable the T1 beta compensation. 1: enable the T1 beta compensation.
5	INTEL_SEL	R/W	5VSB	1	This bit is used to select AMD TSI or Intel IBEX when TSI_EN is set to 1. 0: Select AMD 1: Select Intel
4	MXM_MODE	R/W	LRESET#	0	Reserved.
3-2	VTT_SEL	R/W	5VSB	0	PECI (VTT) voltage selection. 00: VTT is 1.23V 01: VTT is 1.13V 10: VTT is 1.00V 11: VTT is 1.00V
1	TSI_EN	R/W	5VSB	0	Set this bit 1 to enable AMD TSI or Intel IBEX function
0	PECI_EN	R/W	LRESET#	0	Set this bit 1 to enable Intel PECI function

PECI Address Register — Offset 0Bh

Bit	Name	R/W	Reset	Default	Description
7-4	CPU_SEL	R/W	5VSB	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping () command to find the CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 0, i.e. PECI address is 0x31. 0100: CPU is in socket 0, i.e. PECI address is 0x32. 1000: CPU is in socket 0, i.e. PECI address is 0x33. Others are reserved.
3-1	Reserved	-	-	0	Reserved.
0	DOMAIN1_EN	R/W	5VSB	0	If the CPU is selected as dual core. Set this register 1 to read the temperature of domain1.

TCC TEMP Register — Offset 0Ch

Bit	Name	R/W	Reset	Default	Description
7-0	TCC_TEMP	R/W	5VSB	8'h55	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127.

TSI_OFFSET Register — Offset 0Dh

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_OFFSET	R/W	5VSB	8'h00	This byte is used as the offset to be added to the CPU temperature reading of AMD_TSI. The range of this register is -128 ~ 127.

Configuration Register 4 — Offset 0Fh

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	0	Reserved.
5	Reserved	R/W	-	1	Dummy Register
4-2	Reserved	-	-	0	Reserved.
1-0	DIG_RATE_SEL	R/W	5VSB	0	Reserved for Fintek use only

TSI Temperature 0 – Offset E0h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP0	R/W	5VSB	-	This is the AMD TSI reading if AMD TSI enable. And will be highest temperature among CPU, MCH and PCH if Intel temperature interface enable. The range is 0~255°C. To access this byte, MCH_BANK_SEL must set to "0".
	I2C_DATA0	R/W	5VSB	8'h00	This byte is used as multi-purpose: 7. The received data of receive protocol. 8. The first received byte of read word protocol. 9. The 10th received byte of read block protocol. 10. The sent data for send byte protocol and write byte protocol. 11. The first send byte for write word protocol. 12. The first send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 1 – Offset E1h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP1	R	5VSB	-	This is the high byte of Intel temperature interface PCH reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA1	R/W	5VSB	8'h00	This byte is used as multi-purpose: 5. The second received byte of read word protocol. 6. The 11th received byte of read block protocol. 7. The second send byte for write word protocol. 8. The second send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 2 Low Byte – Offset E2h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP2_LO	R	5VSB	-	This is the low byte of Intel temperature interface CPU reading. The reading is the fraction part of CPU temperature. Bit 0 indicates the error status. 0: No error. 1: Error code. To access this byte, MCH_BANK_SEL should be set to "0".

	I2C_DATA2	R/W	5VSB	8'h00	This is the 12th byte of the block read protocol. This byte is also used as the 3rd byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 2 High Byte – Offset E3h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP2_HI	R	5VSB	-	This is the high byte of Intel temperature interface CPU reading. The reading is the decimal part of CPU temperature. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA3	R/W	5VSB	8'h00	This is the 13th byte of the block read protocol. This byte is also used as the 4th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 3 – Offset E4h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP3	R	5VSB	-	This is the high byte of Intel temperature interface MCH reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA4	R/W	5VSB	8'h00	This is the 14th byte of the block read protocol. This byte is also used as the 5th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 4 – Offset E5h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP4	R	5VSB	-	This is the high byte of Intel temperature interface DIMM0 reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA5	R/W	5VSB	8'h00	This is the 15th byte of the block read protocol. This byte is also used as the 6th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 5 – Offset E6h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP5	R	5VSB	-	This is the high byte of Intel temperature interface DIMM1 reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".

	I2C_DATA6	R/W	5VSB	8'h00	This is the 16th byte of the block read protocol. This byte is also used as the 7th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 6 – Offset E7h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP6	R	5VSB	-	This is the high byte of Intel temperature interface DIMM2 reading. The range is 0~255°C. To access this byte, MCH_BANK_SEL should be set to "0".
	I2C_DATA7	R/W	5VSB	8'h00	This is the 17th byte of the block read protocol. This byte is also used as the 8th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 7 – Offset E8h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP7	R	5VSB	-	This is the high byte of Intel temperature interface DIMM3 reading. The range is 0~255°C. The above 9 bytes could also be used as the read data of block read protocol if the TSI is disable or pending.
	I2C_DATA8	R/W	5VSB	8'h00	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

I2C Data Buffer 9 – Offset E9h

Bit	Name	R/W	Reset	Default	Description
7-0	I2C_DATA9	R/W	5VSB	FFh	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

Block Write Count Register – Offset ECh

Bit	Name	R/W	Reset	Default	Description
7	MCH_BANK_SEL	R/W	5VSB	0	This bit is used to select the register in Offset E0h to E9h. Set "0" to read the temperature bank and "1" to access the data bank.
6	Reserved	-	-	0	Reserved
5-0	BLOCK_WR_CNT	R/W	5VSB	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

I2C Command Byte/TSI Command Byte – Offset EDh

Bit	Name	R/W	Reset	Default	Description
7-0	I2C_CMD/TSI_CMD	R/W	5VSB	0/1	There are actual two bytes for this Offset. TSI_CMD_PROG select which byte to be programmed: 0: I2C_CMD, which is the command code for write byte/word, read byte/word, block write/read and process call protocol. 1: TSI_CMD, which is the command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

I2C Status – Offset EEh

Bit	Name	R/W	Reset	Default	Description
7	TSI_PENDING	R/W	LRESET#	0	Set 1 to pending auto TSI accessing. (In AMD model, auto accessing will issue a send-byte followed a receive-byte; In Intel model, auto accessing will issue a block read). To use the SCL/ SDA as a I2C master, set this bit to “1” first.
6	TSI_CMD_PROG	R/W	5VSB	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	5VSB	0	Kill the current I2C transfer and return the state machine to idle. It will set an fail status if the current transfer is not completed.
4	FAIL_STS	R	5VSB	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next I2C transfer.
3	I2C_ABT_ERR	R	5VSB	0	This is the arbitration lost status if a I2C command is issued. Auto cleared by next I2C command.
2	I2C_TO_ERR	R	5VSB	0	This is the timeout status if a I2C command is issued. Auto cleared by next I2C command.
1	I2C_NAC_ERR	R	5VSB	0	This is the NACK error status if a I2C command is issued. Auto cleared by next I2C command.
0	I2C_READY	R	5VSB	1	0: a I2C transfer is in process. 1: Ready for next I2C command.

I2C Protocol Select – Offset EFh

Bit	Name	R/W	Reset	Default	Description
7	I2C_START	W	-	0	Write “1” to trigger a I2C transfer with the protocol specified by SMB_PROTOCOL.
6-4	Reserved	-	-	-	Reserved.

3-0	I2C_PROTOCOL	R/W	5VSB	0	Select what protocol if a I2C transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: Reserved. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: Reserved 1101b: block read. 1111b: Reserved Otherwise: reserved.

7.18.8.2 PECI 3.0 & Temperature Setting

PECI 3.0 Command and Register

PECI Configuration Register — Offset 40h

Bit	Name	R/W	Reset	Default	Description
7	RDIAMSR_CMD_EN	R/W	5VSB	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR() command before a GetTemp() command.
6	C3_UPDATE_EN	R/W	5VSB	0	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR() is 0x82.
5-4	Reserved	R	-	-	Reserved
3	C3_PTEMP_EN	R/W	5VSB	0	Set this bit 1 to enable updateing positive value of temperature if the completion code of RdIAMSR() is 0x82.
2	C0_PTEMP_EN	R/W	5VSB	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	5VSB	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is 0x82.
0	C0_ALL0_EN	R/W	5VSB	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.

PECI Master Control Register — Offset 41h

Bit	Name	R/W	Reset	Default	Description
7	PECI_CMD_START	W	5VSB	-	Write 1 to this bit to start a PECI command when using as a PECI master. (PECI_PENDING must be set to 1)
6-5	Reserved	R	-	-	Reserved
4	PECI_PENDING	R/W	5VSB	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	-	Reserved

2-0	PECI_CMD	R/W	5VSB	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

PECI Master Status Register — Offset 42h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	-	Reserved
2	ABORT_FCS	R/WC	5VSB	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	5VSB	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
0	PECI_FINISH	R/WC	5VSB	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

PECI Master DATA0 Register — Offset 43h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA0	R/W	5VSB	0	For RdIAMSR(), RdPkgConfig() and WrPkgConfig() command, this byte represents "Host ID[7:1] & Retry[0]". Please refer to PECI interface specification for more detail.

PECI Master DATA1 Register — Offset 44h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA1	R/W	5VSB	0	For RdIAMSR() , this byte represents "Processor ID". For RdPkgConfig() and WrPkgConfig() , this byte represents "Offset". Please refer to PECI interface specification for more detail.

PECI Master DATA2 Register — Offset 45h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA2	R/W	5VSB	0	For RdIAMSR(), this byte is the least significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the least significant byte of "Parameter". Please refer to PECI interface specification for more detail.

PECI Master DATA3 Register — Offset 46h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA3	R/W	5VSB	0	For RdIAMSR(), this byte is the most significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the most significant byte of "Parameter". Please refer to PECI interface specification for more detail.

PECI Master DATA4 Register — Offset 47h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA4	R/W	5VSB	0	For GetDIB() , this byte represents "Device Info" For GetTemp(), this byte represents the least significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte is "Completion Code". For WrPkgConfig(), this byte represents "DATA[7:0]"

PECI Master DATA5 Register — Offset 48h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA5	R/W	5VSB	0	For GetDIB() , this byte represents "Revision Number" For GetTemp(), this byte represents the most significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[7:0]" For WrPkgConfig(), this byte represents "DATA[15:8]"

PECI Master DATA6 Register — Offset 49h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA6	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[15:8]". For WrPkgConfig(), this byte represents "DATA[23:16]"

PECI Master DATA7 Register — Offset 4Ah

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA7	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[23:16]". For WrPkgConfig(), this byte represents "DATA[31:24]"

PECI Master DATA8 Register — Offset 4Bh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA8	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[31:24]". For WrPkgConfig(), this byte represents "AW FCS"

PECI Master DATA9 Register — Offset 4Ch

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA9	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[39:32]". For WrPkgConfig(), this byte represents "Completion Code"

PECI Master DATA10 Register — Offset 4Dh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA10	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[47:40]".

PECI Master DATA11 Register — Offset 4Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA11	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[55:48]".

PECI Master DATA12 Register — Offset 4Fh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA12	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[63:56]".

HM Manual Control Register1 — Offset 50h

Bit	Name	R/W	Reset	Default	Description
7	LOAD_CH	W	-	-	Write 1 to load a temperature or voltage channel to be converted
6	STOP_CH	R/W	5VSB	0	Set to 1 when load a channel will generate a one-shot conversion.
5	HOLD_CH	R/W	5VSB	0	Set to 1 when load a channel will keep converting this channel.
4:0	CHANNEL	R/W	5VSB	0	First channel to be converted when LOAD_CH is set to 1. 00000: VCC 00001: VIN1 00010: VIN2 00011: VIN3 00100: VIN4 00101: VSB3V 00110: VBAT 00111: VSB5V 10000: Intel PECI 10001: T1 10010: T2 11000: AMD TSI/Intel IBex

HM Manual Control Status Register 1— Offset 51h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	V_CONV_STS	R	5VSB	-	At least one of the voltage channels had finish converting.
5	PECI_CONV_STS	WC	5VSB	-	PECI channel had finish converting
4	TSI_CONV_STS	WC	5VSB	-	TSI channel had finish converting
3	Reserved	-		-	Reserved
2	T2_CONV_STS	WC	5VSB	-	T2 channel had finish converting
1	T1_CONV_STS	WC	5VSB	-	T1 channel had finish converting
0	Reserved	-		-	Reserved

HM Manual Control Status Register 2— Offset 52h

Bit	Name	R/W	Reset	Default	Description
7	VSB5V_CONV_STS	WC	5VSB	-	VSB5V voltage channel had finish converting
6	VBAT_CONV_STS	WC	5VSB	-	VBAT voltage channel had finish converting
5	VSB3V_CONV_STS	WC	5VSB	-	VSB3V voltage channel had finish converting

4	VIN4_CONV_STS	WC	5VSB	-	VIN4 voltage channel had finish converting
3	VIN3_CONV_STS	WC	5VSB	-	VIN3 voltage channel had finish converting
2	VIN2_CONV_STS	WC	5VSB	-	VIN2 voltage channel had finish converting
1	VIN1_CONV_STS	WC	5VSB	-	VIN1 voltage channel had finish converting
0	VCC_CONV_STS	WC	5VSB	-	VCC voltage channel had finish converting

HM µC Interrupt Enable Register 1— Offset 53h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved
5	PECI_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and PECI _CONV_STS is 1.
4	TSI_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and TSI_CONV_STS is 1.
3	Reserved	-	-	-	Reserved
2	T2_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and T2_CONV_STS is 1.
1	T1_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and T1_CONV_STS is 1.
0	T0_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and T0_CONV_STS is 1.

HM µC Interrupt Enable Register 2— Offset 54h

Bit	Name	R/W	Reset	Default	Description
7	VSB5V_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VSB5V _CONV_STS is 1.
6	VBAT_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VBAT _CONV_STS is 1.
5	VSB3V_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VSB 3V_CONV_STS is 1.
4	VIN4_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VIN4 _CONV_STS is 1.
3	VIN3_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VIN3 _CONV_STS is 1.
2	VIN2_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VIN2 _CONV_STS is 1.
1	VIN1_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VIN1 _CONV_STS is 1.
0	VCC_INT_EN	R/W	5VSB	0	Generate an interrupt for µC when this bit is set to 1 and VCC _CONV_STS is 1.

HM RAW Data Register 1— Offset 55h

Bit	Name	R/W	Reset	Default	Description
7-0	RAW_DATA_L	R	5VSB	0	Low byte of HM converting raw data

HM RAW Data Register 2— Offset 56h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved

1-0	RAW_DATA_H	R	5VSB	0	The highest two bits of HM converting raw data

Temperature Register

Temperature PME# Enable Register — Offset 60h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	EN_ T2_OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	EN_ T0_ OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP0 exceeds OVT setting.
3	Reserved	R/W	-	0	Reserved
2	EN_ T2_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	EN_ T0_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP0 exceeds high limit setting.

Temperature Interrupt Status Register — Offset 61h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	T2_OVT _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
5	T1_OVT _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
4	T0_OVT _STS	R/W	3VCC	0	A one indicates TEMP0 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
3	Reserved	R/W	-	0	Reserved
2	T2_EXC _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
1	T1_EXC _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
0	T0_EXC _STS	R/W	3VCC	0	A one indicates TEMP0 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.

Temperature Real Time Status Register — Offset 62h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	T2_OVT	R/W	3VCC	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the "OVT limit –hysteresis" temperature.
5	T1_OVT	R/W	3VCC	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the "OVT limit –hysteresis" temperature.
4	T0_OVT	R/W	3VCC	0	Set when the TEMP0 exceeds the OVT limit. Clear when the TEMP0 is below the "OVT limit –hysteresis" temperature.
3	Reserved	R/W	-	0	Reserved
2	T2_EXC	R/W	3VCC	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the "high limit –hysteresis" temperature.
1	T1_EXC	R/W	3VCC	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the "high limit –hysteresis" temperature.
0	T0_EXC	R/W	3VCC	0	Set when the TEMP0 exceeds the high limit. Clear when the TEMP0 is below the "high limit –hysteresis" temperature.

Temperature BEEP Enable Register — Offset 63h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	EN_ T2_ OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	EN_ T0_ OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP0 exceeds OVT limit setting.
3	Reserved	R/W	-	0	Reserved
2	EN_ T2_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	EN_ T0_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP0 exceeds high limit setting.

T1 OVT and High Limit Temperature Select Register — Offset 64h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R/W	-	0	Reserved

5-4	OVT_TEMP_SEL	R/W	5VSB	0	Select the source temperature for T1 OVT Limit. 0: Select T1 to be compared to Temperature 1 OVT Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 OVT Limit. 2: Select CPU temperature from AMD TSI or Intel PCH I2C to be compared to Temperature 1 OVT Limit. 3: Select the MAX temperature from Intel PCH I2C to be compared to Temperature 1 OVT Limit.
3-2	Reserved	R/W	-	0	Reserved
1-0	HIGH_ TEMP_SEL	R/W	5VSB	0	Select the source temperature for T1 High Limit. 0: Select T1 to be compared to Temperature 1 High Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 High Limit. 2: Select CPU temperature from AMD TSI or Intel PCH I2C to be compared to Temperature 1 High Limit. 3: Select the MAX temperature from Intel PCH I2C to be compared to Temperature 1 High Limit.

OVT and Alert Output Enable Register 1 — Offset 66h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	0	Reserved
6	EN_T2_ALERT	R/W	5VSB	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R/W	5VSB	0	Enable temperature 1 alert event (asserted when temperature over high limit)
4	EN_T0_ALERT	R/W	5VSB	0	Enable temperature 0 alert event (asserted when temperature over high limit)
3	Reserved	-	-	0	Reserved
2	EN_T2_OVT	R/W	5VSB	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	5VSB	1	Enable over temperature (OVT) mechanism of temperature1.
0	EN_T0_OVT	R/W	5VSB	0	Enable over temperature (OVT) mechanism of temperature0.

Reserved —Offset 67~69h

Bit	Name	R/W	Reset	Default	Description
7-0	Reserved	-	-	-	Reserved

Temperature Sensor Type Register — Offset 6Bh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	RO	-	0	Reserved
3	Reserved	RO	-	0	Reserved
2	T2_MODE	R/W	5VSB	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	5VSB	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	R	-	0	Reserved

TEMP1 Limit Hystersis Select Register — Offset 6Ch

Bit	Name	R/W	Reset	Default	Description
7-4	TEMP1_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	TEMP0_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

TEMP2 and TEMP3 Limit Hystersis Select Register — Offset 6Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	R	-	0	Reserved
3-0	TEMP2_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).

DIODE OPEN Status Register — Offset 6Fh

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R	-	-	Reserved
5	PECI_OPEN	R	3VCC	-	When PECI interface is enabled, “1” indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4	TSI_OPEN	R	3VCC	-	When TSI interface is enabled, “1” indicates the error of not receiving NACK bit or a timeout occurred.
3	Reserved	R	-	-	Reserved
2	T2_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 2 is open or short
1	T1_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 1 is open or short
0	T0_DIODE_OPEN	RO	3VCC	-	This register indicates the abnormality of temperature 0 measurement.

Temperature — Offset 70h- 8Dh

Address	Attribute	Reset	Default Value	Description
70h	RO	3VCC	--	Temperature 0 reading. The unit of reading is 1°C.At the moment of reading this register.
71h	Reserved	3VCC	FFh	Reserved
72h	R	3VCC	--	Temperature 1 reading. The unit of reading is 1ºC.At the moment of reading this register.
73h	R	3VCC	--	Reserved
74h	R	3VCC	--	Temperature 2 reading. The unit of reading is 1ºC.At the moment of reading this register.
75-79h	R	3VCC	--	Reserved
7Ah	R	3VCC	--	The data of CPU temperature from digital interface after IIR filter. (Available if Intel IBX or AMD TSI interface is enabled)
7Bh	R	3VCC	--	The raw data of PCH temperature from digital interface. (Only available if Intel IBX interface is enabled)
7Ch	R	3VCC	--	The raw data of MCH read from digital interface. (Only available if Intel IBX interface is enabled)
7Dh	R	3VCC	--	The raw data of maximum temperature between CPU/PCH/MCH from digital interface. (Only available if Intel IBX interface is enabled)
7Eh	R	3VCC	--	The data of CPU temperature from digital interface after IIR filter. (Only available if PECI interface is enabled)
80h	R/W	5VSB	64h	Temperature sensor 0 OVT limit. The unit is 1°C.
81h	R/W	5VSB	55h	Temperature sensor 0 high limit. The unit is 1°C.
82h	R/W	5VSB	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	5VSB	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	5VSB	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	5VSB	55h	Temperature sensor 2 high limit. The unit is 1°C.
86-8Bh	R	--	--	Reserved
8C~8Dh	R	--	FFH	Reserved

T1 Slope Adjust Register — Offset 7Fh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	T1_ADD	R/W	5VSB	0h	This bit is the sign bit for T1 reading slope adjustment. See T1_SCALE below for detail.

2-0	T1_SCALE	R/W	-	0h	T1_ADD	T1_SCALE	Slope
					X	00	No adjustment
					0	01	15/16
					0	10	31/32
					0	11	63/64
					1	01	17/16
					1	10	33/32
					1	11	65/64

Temperature Filter Select Register —Offset 8Eh

Bit	Name	R/W	Reset	Default	Description
7-6	IIR-QUEUR0	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. 00: 8 times. 01: 12 times. 10: 16 times. (default) 11: 24 times.
5-4	IIR-QUEUR2	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. 00: 8 times. 01: 12 times. 10: 16 times. (default) 11: 24 times.
3-2	IIR-QUEUR1	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.
1-0	IIR-QUEUR_DIG	R/W	5VSB	2'b10	The queue time for second filter to quickly update values. (for CPU temperature from PECI or TSI interface) 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.

7.18.8.3 Voltage Setting

Voltage-Protect Shut Down Enable Register — Offset 10h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	0	Reserved.
6	V3_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for VIN3
5	V2_VP_EN	R/W	VBAT*	0	Voltage-Protect enable for VIN2

4-1	Reserved	-	-	0	Reserved
0	V0_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for 3VCC

Voltage-Protect Status Register (Powered by VBAT) — Offset 11h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved.
0	V_EXC_VP	R/WC	VBAT/ 5VSB*	0	This bit is voltage-protect status. Once one of the monitored voltages (3VCC, VIN5, VIN6) over its related over-voltage limits or under its related under-voltage limits and if the related voltage-protect shut down enable bit is set, this bit will be set to 1. Write a 1 to this bit will clear it to 0. (This bit is powered by VBAT)

*Reset by VBAT when OVP_MODE is “0”, Reset by 5VSB when OVP_MODE is “1”

Voltage-Protect Configuration Register — Offset 12h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-2	PU_TIME	R/W	VBAT	2’h1	PSON# de-active time select for voltage protection. 00: PSON# tri-state 0.5 sec and then inverted of S3# when over voltage or under voltage occurs. 01: PSON# tri-state 1 sec and then inverted of S3# when over voltage or under voltage occurs. 10: PSON# tri-state 2 sec and then inverted of S3# when over voltage or under voltage occurs. 11: PSON# tri-state 4 sec and then inverted of S3# when over voltage or under voltage occurs.
1-0	VP_EN_DELAY	R/W	VBAT	2’h2	VP_EN_DELAY could set the delay time to start voltage protecting after VDD power is ok when OVP_MODE is 1. (OVP_MODE is strapped by RTS1# pin) 00: bypass 01: 50ms 10: 100ms 11: 200ms

Voltage1 PME# Enable Register — Offset 14h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved

1	EN_V1_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for VIN1.
0	Reserved	-	-	-	Reserved

Voltage1 Interrupt Status Register — Offset 15h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	0	Reserved
1	V1_ EXC _STS	R/W	5VSB	0	This bit is set when the VIN1 is over the high limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	-	-	-	Reserved

Voltage1 Exceeds Real Time Status Register 1 — Offset 16h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	0	Reserved
1	V1_EXC	RO	5VSB	0	A one indicates VIN1 exceeds the high or low limit. A zero indicates VIN1 is in the safe region.
0	Reserved	--	-	0	Reserved

Voltage1 BEEP Enable Register — Offset 17h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	0	Reserved
1	EN_V1_BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP output of VIN1.
0	Reserved	--	-	0	Reserved

Voltage Protection Power Good Select Register — Offset 3Fh

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	--	-	0	Reserved
0	OVP_RST_SEL	R/W	VBAT	0	0: OVP/UVP power good signal is 3VCCOK (3VCC > 2.8V) 1: OVP/UVP power good signal is PWROK. OVP/UVP function wont' start detecting until power good.

Voltage reading and limit— Offset 20h- 4Fh

Address	Attribute	Reset	Default Value	Description
20h	R	3VCC	--	3VCC reading. The unit of reading is 8mV.
21h	R	3VCC	--	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	R	3VCC	--	VIN2 reading. The unit of reading is 8mV.
23h	R	3VCC	--	VIN3 reading. The unit of reading is 8mV.
24h	R	3VCC	--	VIN4 reading. The unit of reading is 8mV.

25h	R	3VCC	--	VSB3V reading. The unit of reading is 8mV.
26h	R	3VCC	--	VBAT reading. The unit of reading is 8mV.
27h	R	3VCC	--	VSB5V reading. The unit of reading is 8 mV. The VSB5V voltage to be monitored is internally divided by 3.
28h-2Ch	R	--	FF	Reserved
2Dh	RO	3VCC	--	FAN1 present fan duty reading
2Eh	RO	3VCC	--	FAN2 present fan duty reading
2Fh	RO	3VCC	--	FAN3 present fan duty reading
30	RO	VBAT	89	3VCC under-voltage protection limit. The unit is 8mV
31	R/W	VBAT	F2	3VCC over-voltage protection limit. The unit is 8 mV
32~35h	R		FF	Reserved
36h	R/W	VBAT	E2	VIN2 over-voltage limit (V2_OVV_LIMIT). The unit is 8mv. (This byte is powered by VBAT.)
37h	R/W	VBAT	E1	VIN3 over-voltage limit (V3_OVV_LIMIT). The unit is 8mv. (This byte is powered by VBAT.)
38h	R/W	VBAT	83	VIN2 under-voltage limit (V2_UVV_LIMIT). The unit is 8mv (This byte is powered by VBAT)
39h	R/W	VBAT	96	VIN3 under-voltage limit (V3_UVV_LIMIT). The unit is 8mv (This byte is powered by VBAT)
3A	R/W	5VSB	FF	V1 High Limit setting register. The unit is 8mV.
3B~3F	RO		FF	Reserved.

7.18.8.4 Fan Control Setting

FAN PME# Enable Register — Offset 90h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	0	Reserved
2	EN_FAN3_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt Set this bit 1 to enable PME# function for Fan3.
1	EN_FAN2_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

FAN Interrupt Status Register — Offset 91h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	0	Reserved
2	FAN3_STS	R/W	3VCC	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	3VCC	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	3VCC	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

FAN Real Time Status Register — Offset 92h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	--	-	0	Reserved
2	FAN3_EXC	R	3VCC	--	This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	R	3VCC	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	R	3VCC	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

FAN BEEP# Enable Register — Offset 93h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	FULL_WITH_ T2_EN	R/W	5VSB	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_ T1_EN	R/W	5VSB	0	Set one will enable FAN to force full speed when T1 over high limit.
4	Reserved	-	-	-	Reserved
3	Reserved	-	-	-	Reserved.
2	EN_FAN3_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.
1	EN_FAN2_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.

FAN Type Select Register — Offset 94h FAN_PROG_SEL = 0

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5-4	FAN3_TYPE	R/W	3VCC	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL3 0: FANCTRL3 is pull up by external resistor. 1: FANCTRL3 is pull down by internal 100KΩ resistor.
3-2	FAN2_TYPE	R/W	3VCC	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL2 0: FANCTRL2 is pull up by external resistor. 1: FANCTRL2 is pull down by internal 100KΩ resistor.
1-0	FAN1_TYPE	R/W	3VCC	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL1 0: FANCTRL1 is pull up by external resistor. 1: FANCTRL1is pull down by internal 100KΩ resistor.

S: Register default values are decided by trapping.

Fan1 Base Temperature Register – Offset 94h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	FAN1_BASE _TEMP	R/W	5VSB	0	This register is used to set the base temperature for FAN1 temperature adjustment. The FAN1 temperature is calculated according to the equation: Tfan1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG and FAN1_TEMP_SEL. Tb is this register, Ta is selected by TFAN1_ADJ_SEL and Ct is selected by TFAN1_ADJ_UP_RATE/TFAN1_ADJ_DN_RATE. To access this register, FAN_PROG_SEL(CR9F[7]) must set to “1”.

FAN1 Temperature Adjust Rate Register — Offset 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6-4	TFAN1_ADJ_UP _RATE		5VSB	3’h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.
3	Reserved	-		-	Reserved
2-0	TFAN1_ADJ_DN _RATE	R/W	5VSB	3’h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.

FAN mode Select Register — Offset 96h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved
5-4	FAN3_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xC6-0xCE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xC6-0xCE. 10: Manual mode fan control. User can write expected **RPM** count to 0xC2-0xC3, and F81867 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control. User can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xC3, and F81867 will output this desired duty or voltage to control fan speed.
3-2	FAN2_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xB6-0xBE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** (voltage) defined in 0xB6-0xBE. 10: Manual mode fan control. User can write expected **RPM** count to 0xB2-0xB3, and F81867 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F81867 will output this desired duty or voltage to control fan speed.

1-0	FAN1_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xA6-0xAE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expected **RPM** count to 0xA2-0xA3, and F81867 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F81867 will output this desired duty or voltage to control fan speed.

Fan1 Adjustment Temperature Select Register – Offset 96h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved
2-0	TFAN1_ADJ_SEL	R/W	5VSB	0h	This selects which temperature to be used as Ta for Fan1 temperature adjustment. 000: PECI (CR7Eh) 001: T1 (CR72h) 010: T2 (CR74h) 011: T0 (CR70h) 100: IBX/TSI CPU temperature (CR7Ah) 101:IBX PCH temperature (CR7Bh). 110: IBX MCH temperature (CR7Ch). 111: IBX maximum temperature (CR7Dh). To access this register FAN_PROG_SEL must set to “1”.

Faster Fan Filter Control Register — Offset 97h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved.
2	FLT_FAST3	R/W	5VSB	0	Set this bit 1 if FAN3 is using a faster fan.
1	FLT_FAST2	R/W	5VSB	0	Set this bit 1 if FAN2 is using a faster fan.
0	FLT_FAST1	R/W	5VSB	0	Set this bit 1 if FAN1 is using a faster fan.

Auto FAN1 and FAN2 Boundary Hystersis Select Register — Offset 98h

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_HYS	R/W	5VSB	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	5VSB	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Auto FAN3 Boundary Hystersis Select Register — Offset 99h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	FAN3_HYS	R/W	5VSB	2h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Fan3 Control Register — Offset 9Ah

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	FREQ_SEL_ADD3	R/W	5VSB	0	This bit and FAN3_PWM_FREQ_SEL are used to select FAN3 PWM frequency. NEW_FREQ_SEL3 = { FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FREQ_SEL_ADD2	R/W	5VSB	0	This bit and FAN2_PWM_FREQ_SEL are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz

4	FREQ_SEL_ADD1	R/W	5VSB	0	This bit and FAN1_PWM_FREQ_SEL are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
3-2	Reserved	R/W	-	0	Reserved (Keep the value of these two bits “0”)
1-0	Reserved	-	-	-	Reserved

Auto Fan Up Speed Update Rate Select Register— Offset 9Bh

FAN_PROG_SEL = 0

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5-4	FAN3_UP_RATE	R/W	5VSB	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_UP_RATE	R/W	5VSB	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_UP_RATE	R/W	5VSB	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

Auto Fan Down Speed update Rate Select Register -- Offset 9Bh FAN_PROG_SEL = 1

Bit	Name	R/W	Reset	Default	Description
7	UP_DN_RATE_EN	R/W	5VSB	0	0: Fan down rate disable 1: Fan down rate enable
6	DIRECT_LOAD_EN	R/W	5VSB	0	0: Direct load disable 1: Direct load enable for manual duty mode

5-4	FAN3_DN_RATE	R/W	5VSB	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_DN_RATE	R/W	5VSB	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DN_RATE	R/W	5VSB	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Offset 9Ch

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_STOP _DUTY	R/W	5VSB	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP _DUTY	R/W	5VSB	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN3 START UP DUTY-CYCLE/VOLTAGE — Offset 9Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	FAN3_STOP_ DUTY	R/W	5VSB	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN PROGRAMMABLE DUTY-CYCLE/VOLTAGE LOADED AFTER POWER-ON — Offset 9Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PROG_DUTY_VAL	R/W	5VSB	66h	This byte will be immediately loaded as Fan duty value after VDD is powered on if it has been programmed before shut down.

Fan Fault Time Register — Offset 9Fh

Bit	Name	R/W	Reset	Default	Description
7	FAN_PROG_SEL	R/W	5VSB	0	Set this bit to "1" will enable accessing registers of other bank.
6	FAN_MNT_SEL	R/W	5VSB	0	Set this bit to monitor a slower fan.
5	Reserved	-	-	-	Reserved
4	FULL_DUTY_SEL	R/W	3VCC	-	0: The Fan Duty is 100% and will be loaded immediately after VDD is powered on if CR9E is not been programmed before shut down. (pull down by external resistor) 1: The Fan Duty is 40% and will be loaded immediately after VDD is powered on if CR9E is not been programmed before shut down. (pull up by internal 47KΩ resistor). This register is power on trap by DTR1#.
3-0	F_FAULT_TIME	R/W	5VSB	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0 , means 1 seconds. ; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register Offset 9C-9Dh.

D. FAN1 Offset A0h~AFh

Address	Attribute	Reset	Default Value	Description
A0h	RO	3VCC	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	3VCC	8'hff	FAN1 count reading (LSB).
A2h	R/W	VBAT	8'h00	RPM mode(CR96 bit0=0): FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1(0) this register is auto updated by hardware. Duty mode(CR96 bit0=1): This byte is reserved byte.
A3h	R/W	VBAT	8'h01	RPM mode(CR96 bit0=0): FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit0=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit1(0) this register is updated by hardware. Ex: 5(5*100/255 % 255 (100%
A4h	R/W	5VSB	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	5VSB	8'hff	FAN1 full speed count reading (LSB).

VT1 BOUNDARY 1 TEMPERATURE – Offset A6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP1	R/W	5VSB	3Ch (60oC)	The first boundary temperature for VT1 in temperature mode. When VT1 temperature exceeds this boundary, expected FAN1 value will be loaded from segment 1 register (Offset AAh). When VT1 temperature is under this boundary – hysteresis, expected FAN1 value will be loaded from segment 2 register (Offset ABh). This byte is a 2's complement value ranged from -128'C ~ 127'C.

VT1 BOUNDARY 2 TEMPERATURE – Offset A7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP1	R/W	5VSB	32 (50ºC)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 2 register (Offset ABh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 3 register (Offset ACh). This byte is a 2's complement value ranging from -128ºC ~ 127ºC.

VT1 BOUNDARY 3 TEMPERATURE – Offset A8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP1	R/W	5VSB	28h (40ºC)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 3 register (Offset ACh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 4 register (Offset ADh). This byte is a 2's complement value ranging from -128ºC ~ 127ºC.

VT1 BOUNDARY 4 TEMPERATURE – Offset A9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP1	R/W	5VSB	1Eh (30ºC)	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 4 register (Offset ADh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 5 register (Offset AEh). This byte is a 2's complement value ranging from -128ºC ~ 127ºC.

FAN1 SEGMENT 1 SPEED COUNT – Offset AAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED1	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 2 SPEED COUNT – Offset ABh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED1	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 3 SPEED COUNT Register – Offset ACh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED1	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 4 SPEED COUNT Register – Offset ADh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED1	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 5 SPEED COUNT Register – Offset AEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED1	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 Temperature Mapping Select – Offset AFh

Bit	Name	R/W	Reset	Default	Description
7	FAN1_TEMP _SEL_DIG	R/W	5VSB	0	This bit companies with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	FAN1_PWM _FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD1 are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN1_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_ INTERPOLATION_ EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP _HIGH_EN	R/W	5VSB	1	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.
2	FAN1_JUMP _LOW_EN	R/W	5VSB	1	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.

1-0	FAN1_TEMP_SEL	R/W	5VSB	01	This registers company with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 0 (CR70h). 100: fan1 follows IBX/TSI CPU temperature (CR7Ah) 101: fan1 follows IBX PCH temperature (CR7Bh). 110: fan1 follows IBX MCH temperature (CR7Ch). 111: fan1 follows IBX maximum temperature (CR7Dh). Others are reserved.

E. FAN2 Offset B0h~BFh

Address	Attribute	Reset	Default Value	Description
B0h	RO	3VCC	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	3VCC	8'hff	FAN2 count reading (LSB).
B2h	R/W	VBAT	8'h00	RPM mode(CR96 bit2=0): FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. Duty mode(CR96 bit2=1): This byte is reserved byte.
B3h	R/W	VBAT	8'h01	RPM mode(CR96 bit2=0): FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit2=1): The Value programming in this byte is duty value. In auto fan mode(CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 (100%

B4h	R/W	5VSB	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	5VSB	8'hff	FAN2 full speed count reading (LSB).

VT2 BOUNDARY 1 TEMPERATURE – Offset B6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP2	R/W	5VSB	3Ch (60oC)	The first boundary temperature for VT2 in temperature mode. When VT2 temperature exceeds this boundary, FAN2 expect value will load from segment 1 register (Offset Bah). When VT2 temperature is under this boundary – hysteresis, FAN2 expect value will load from segment 2 register (Offset BAh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

VT2 BOUNDARY 2 TEMPERATURE – Offset B7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP2	R/W	5VSB	32 (50ºC)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 2 register (Offset BBh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 3 register (Offset BCh). This byte is a 2's complement value ranging from -128ºC ~ 127ºC.

VT2 BOUNDARY 3 TEMPERATURE – Offset B8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP2	R/W	5VSB	28h (40ºC)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 3 register (Offset BCh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 4 register (Offset BDh). This byte is a 2's complement value ranging from -128ºC ~ 127ºC.

VT2 BOUNDARY 4 TEMPERATURE – Offset B9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP2	R/W	5VSB	1Eh (30ºC)	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 4 register (Offset BDh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 5 register (Offset BEh). This byte is a 2's complement value ranging from -128ºC ~ 127ºC.

FAN2 SEGMENT 1 SPEED COUNT – Offset BAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED2	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 2 SPEED COUNT – Offset BBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED2	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 3 SPEED COUNT Register – Offset BCh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED2	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 4 SPEED COUNT Register – Offset BDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED2	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 5 SPEED COUNT Register – Offset BEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED2	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 Temperature Mapping Select – Offset BFh

Bit	Name	R/W	Reset	Default	Description
7	FAN2_TEMP_ SEL_DIG	R/W	5VSB	0	This bit companies with FAN2_TEMP_SEL to select the temperature source for controlling FAN2.
6	FAN2_PWM_ FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD2 are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN2_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.

4	FAN2_ INTERPOLATION_EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_ HIGH_EN	R/W	5VSB	1	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.
2	FAN2_JUMP_ LOW_EN	R/W	5VSB	1	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.
1-0	FAN2_TEMP_SEL	R/W	5VSB	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR7Eh) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011: fan2 follows temperature 0 (CR70h). 100: fan2 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan2 follows IBEX PCH temperature (CR7Bh). 110: fan2 follows IBEX MCH temperature (CR7Ch). 111: fan2 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

F. FAN3 Offset C0h- CFh

Address	Attribute	Reset	Default Value	Description
C0h	RO	3VCC	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	3VCC	8'hff	FAN3 count reading (LSB).

C2h	R/W	VBAT	8'h00	RPM mode(CR96 bit4=0): FAN3 expect speed count value (MSB), in auto fan mode(CR96 bit5➔0) this register is auto updated by hardware. Duty mode(CR96 bit4=1): This byte is reserved byte.
C3h	R/W	VBAT	8'h01	RPM mode(CR96 bit4=0): FAN3 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit4=1): The Value programming in this byte is duty value. In auto fan mode(CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	5VSB	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	5VSB	8'hff	FAN3 full speed count reading (LSB).

VT3 BOUNDARY 1 TEMPERATURE – Offset C6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP3	R/W	5VSB	3Ch ($60^{o}C$)	The first boundary temperature for VT3 in temperature mode. When VT3 temperature **exceeds** this boundary, FAN3 expect value will load from segment **1** register (Offset CA)h. When VT3 temperature is **under** this boundary – hysteresis, FAN3 expect value will load from segment **2** register (Offset CAh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

VT3 BOUNDARY 2 TEMPERATURE – Offset C7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP3	R/W	5VSB	32 ($50^{o}C$)	The 2nd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 2 register (Offset CBh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 3 register (Offset CCh). This byte is a 2's complement value ranging from -128 ^{o}C ~ 127 ^{o}C.

VT3 BOUNDARY 3 TEMPERATURE – Offset C8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP3	R/W	5VSB	28h (40°C)	The 3rd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 3 register (Offset CCh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 4 register (Offset CDh). This byte is a 2's complement value ranging from -128 °C ~ 127 °C.

VT3 BOUNDARY 4 TEMPERATURE – Offset C9h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP3	R/W	5VSB	1Eh (30°C)	The 4th BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 4 register (Offset CDh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 5 register (Offset CEh). This byte is a 2's complement value ranging from -128 °C ~ 127 °C.

FAN3 SEGMENT 1 SPEED COUNT – Offset CAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED3	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 2 SPEED COUNT – Offset CBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED3	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN3_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 3 SPEED COUNT – Offset CCh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED3	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN3_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 4 SPEED COUNT – Offset CDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED3	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN3_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 5 SPEED COUNT – Offset CEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5SPEED3	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN3_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 Temperature Mapping Select – Offset CFh

Bit	Name	R/W	Reset	Default	Description
7	FAN3_TEMP_ SEL_DIG	R/W	5VSB	0	This bit companies with FAN3_TEMP_SEL select the temperature source for controlling FAN3.

6	FAN3_PWM_ FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD3 are used to select FAN3 PWM frequency. NEW_FREQ_SEL3 = { FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN3_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_ INTERPOLATION_EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN3_JUMP_ HIGH_EN	R/W	5VSB	1	This register controls the FAN3 duty movement when temperature over highest boundary. 0: The FAN3 duty will increases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register. This bit only activates in duty mode.
2	FAN3_JUMP_ LOW_EN	R/W	5VSB	1	This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN3 duty will decreases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC2SPEED3 register. This bit only activates in duty mode.
1-0	FAN3_TEMP_SEL	R/W	5VSB	11	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 000: fan3 follows PECI temperature (CR7Eh) 001: fan3 follows temperature 1 (CR72h). 010: fan3 follows temperature 2 (CR74h). 011: fan3 follows temperature 0 (CR70h). 100: fan3 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan3 follows IBEX PCH temperature (CR7Bh). 110: fan3 follows IBEX MCH temperature (CR7Ch). 111: fan3 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

7.20.9 GPIO µC Side Register (Base Address 0x2100, 256 bytes)

GPIO0 Output Enable Register — offset F0h.

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_OE	R/W	5VSB	0	0: GPIO07 is in input mode. 1: GPIO07 is in output mode.
6	GPIO06_OE	R/W	5VSB	0	0: GPIO06 is in input mode. 1: GPIO06 is in output mode.
5	GPIO05_OE	R/W	5VSB	0	0: GPIO05 is in input mode. 1: GPIO05 is in output mode.
4	GPIO04_OE	R/W	5VSB	0	0: GPIO04 is in input mode. 1: GPIO04 is in output mode.
3	GPIO03_OE	R/W	5VSB	0	0: GPIO03 is in input mode. 1: GPIO03 is in output mode.
2	GPIO02_OE	R/W	5VSB	0	0: GPIO02 is in input mode. 1: GPIO02 is in output mode.
1	GPIO01_OE	R/W	5VSB	0	0: GPIO01 is in input mode. 1: GPIO01 is in output mode.
0	GPIO00_OE	R/W	5VSB	0	0: GPIO00 is in input mode. 1: GPIO00 is in output mode.

GPIO0 Output Data Register — offset F1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_VAL	R/W	5VSB	0	GPIO07 supports pulse mode. When pulse mode is selected, write “1” to this bit will assert a pulse from GPIO07. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO07. 0: outputs 0 when in output mode. 1: outputs1 when in output mode. GPIO07 will be tri-state if GPIO07_DRV is clear to “0”.
6	GPIO06_VAL	R/W	5VSB	0	GPIO06 supports pulse mode. When pulse mode is selected, write “1” to this bit will assert a pulse from GPIO06. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO06. 0: outputs 0 when in output mode. 1: outputs1 when in output mode. GPIO06 will be tri-state if GPIO06_DRV is clear to “0”.
5	GPIO05_VAL	R/W	5VSB	0	GPIO05 supports pulse mode. When pulse mode is selected, write “1” to this bit will assert a pulse from GPIO05. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO05. 0: outputs 0 when in output mode. 1: outputs1 when in output mode. GPIO05 will be tri-state if GPIO05_DRV is clear to “0”.

4	GPIO04_VAL	R/W	5VSB	0	GPIO04 supports pulse mode. When pulse mode is selected, write “1” to this bit will assert a pulse from GPIO04. Auto clear when pulse is finished. When level mode is selected, write 0/1 to this bit will set the level of GPIO04. 0: outputs 0 when in output mode. 1: outputs1 when in output mode. GPIO04 will be tri-state if GPIO04_DRV is clear to “0”.1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	5VSB	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	5VSB	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	5VSB	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_VAL	R/W	5VSB	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

GPIO0 Pin Status Register — offset F2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_IN	R	-	-	The pin status of GPIO07/RTS5#.
6	GPIO06_IN	R	-	-	The pin status of GPIO06/SIN5.
5	GPIO05_IN	R	-	-	The pin status of GPIO05/SOUT5.
4	GPIO04_IN	R	-	-	The pin status of SLP_SUS#/GPIO04.
3	GPIO03_IN	R	-	-	The pin status of SUS_ACK#/GPIO03/SPI_MOSI.
2	GPIO02_IN	R	-	-	The pin status of SUS_WARN#/GPIO02/SPI_MISO.
1	GPIO01_IN	R	-	-	The pin status of ERP_CTRL1#/GPIO01/SPI_CS#.
0	GPIO00_IN	R	-	-	The pin status of ERP_CTRL0#/GPIO00/SPI_CLK.

GPIO0 Drive Enable Register — offset F3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DRV_EN	R/W	5VSB	0	0: GPIO07 is open drain in output mode. 1: GPIO07 is push pull in output mode.
6	GPIO06_DRV_EN	R/W	5VSB	0	0: GPIO06 is open drain in output mode. 1: GPIO06 is push pull in output mode.
5	GPIO05_DRV_EN	R/W	5VSB	0	0: GPIO05 is open drain in output mode. 1: GPIO05 is push pull in output mode.
4	GPIO04_DRV_EN	R/W	5VSB	0	0: GPIO04 is open drain in output mode. 1: GPIO04 is push pull in output mode.
3	GPIO03_DRV_EN	R/W	5VSB	0	0: GPIO03 is open drain in output mode. 1: GPIO03 is push pull in output mode.
2	GPIO02_DRV_EN	R/W	5VSB	0	0: GPIO02 is open drain in output mode. 1: GPIO02 is push pull in output mode.
1	GPIO01_DRV_EN	R/W	5VSB	0	0: GPIO01 is open drain in output mode. 1: GPIO01 is push pull in output mode.
0	GPIO00_DRV_EN	R/W	5VSB	0	0: GPIO00 is open drain in output mode. 1: GPIO00 is push pull in output mode.

GPIO0 Mode Register — offset F5h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_MODE	R/W	5VSB	0	The output mode of GPIO07. 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
5-4	GPIO06_MODE	R/W	5VSB	0	The output mode of GPIO06. 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
3-2	GPIO05_MODE	R/W	5VSB	0	The output mode of GPIO05. 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
1-0	GPIO04_MODE	R/W	5VSB	0	The output mode of GPIO04. 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.

GPIO0 Pulse Select Register — offset F7h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_PW_SEL	R/W	5VSB	0	The pulse width of GPIO07 in pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
5-4	GPIO06_PW_SEL	R/W	5VSB	0	The pulse width of GPIO06 in pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
3-2	GPIO05_PW_SEL	R/W	5VSB	0	The pulse width of GPIO05 in pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO04_PW_SEL	R/W	5VSB	0	The pulse width of GPIO04 in pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.

GPIO0 SMI Enable Register — offset F8h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO07_SMI_ST is set.
6	GPIO06_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO06_SMI_ST is set.
5	GPIO05_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO05_SMI_ST is set.
4	GPIO04_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO04_SMI_ST is set.
3	GPIO03_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO03_SMI_ST is set.
2	GPIO02_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO02_SMI_ST is set.
1	GPIO01_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO01_SMI_ST is set.
0	GPIO00_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO00_SMI_ST is set.

GPIO0 SMI Status Register — offset F9h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO07 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO06_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO06 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO05_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO05 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO04_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO04 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO03_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO03 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO02_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO02 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO01_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO01 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO00_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO00 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

GPIO1 Output Enable Register — offset E0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_OE	R/W	5VSB	0	0: GPIO17 is in input mode. 1: GPIO17 is in output mode.
6	GPIO16_OE	R/W	5VSB	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	5VSB	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	5VSB	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	5VSB	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	5VSB	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	5VSB	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	5VSB	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

GPIO1 Output Data Register — offset E1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_VAL	R/W	5VSB	1	0: GPIO17 outputs 0 when in output mode. 1: GPIO17 outputs1 when in output mode.
6	GPIO16_VAL	R/W	5VSB	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_VAL	R/W	5VSB	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	5VSB	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	5VSB	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	5VSB	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	5VSB	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	5VSB	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

GPIO1 Pin Status Register — offset E2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_IN	R	-	-	The pin status of PECI/GPIO17.
6	GPIO16_IN	R	-	-	The pin status of BEEP/GPIO16/SDA/CIRRX#.
5	GPIO15_IN	R	-	-	The pin status of WDTRST#/GPIO15.
4	GPIO14_IN	R	-	-	The pin status of GPIO14/AT_ATX_TRAP.
3	GPIO13_IN	R	-	-	The pin status of SDA/GPIO13/IRRX.

2	GPIO12_IN	R	-	-	The pin status of SCL/GPIO12/IRTX
1	GPIO11_IN	R	-	-	The pin status of GPIO11/LED_VCC.
0	GPIO10_IN	R	-	-	The pin status of GPIO10/LED_VSB.

GPIO1 Drive Enable Register — offset E3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_DRV_EN	R/W	5VSB	0	0: GPIO17 is open drain in output mode. 1: GPIO17 is push pull in output mode.
6	GPIO16_DRV_EN	R/W	5VSB	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	5VSB	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	5VSB	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	5VSB	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	5VSB	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	VBAT	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode. This bit is powered by VBAT.
0	GPIO10_DRV_EN	R/W	VBAT	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode. This bit is powered by VBAT.

GPIO1 SMI Enable Register — offset E8h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO17_SMI_ST is set.
6	GPIO16_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO16_SMI_ST is set.
5	GPIO15_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO15_SMI_ST is set.
4	GPIO14_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO14_SMI_ST is set.
3	GPIO13_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO13_SMI_ST is set.
2	GPIO12_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO12_SMI_ST is set.
1	GPIO11_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO11_SMI_ST is set.
0	GPIO10_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO10_SMI_ST is set.

GPIO1 SMI Status Register — offset E9h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO17 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO16_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO16 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO15_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO15 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO14_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO14 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO13_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO13 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO12_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO12 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO11_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO11 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO10_SMI_ST	R/W	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO10 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

GPIO2 Output Enable Register — offset D0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_OE	R/W	5VSB	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	5VSB	0	0: GPIO26 is in input mode. 1: GPIO25 is in output mode.
5	GPIO25_OE	R/W	5VSB	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	5VSB	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	5VSB	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	5VSB	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	5VSB	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	5VSB	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

GPIO2 Output Data Register — offset D1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_VAL	R/W	5VSB	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs 1 when in output mode.
6	GPIO26_VAL	R/W	5VSB	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs 1 when in output mode.
5	GPIO25_VAL	R/W	5VSB	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	5VSB	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	5VSB	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	5VSB	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	5VSB	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	5VSB	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

GPIO2 Pin Status Register — offset D2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_IN	R	-	-	The pin status of RSMRST#/GPIO27.
6	GPIO26_IN	R	-	-	The pin status of PWROK/GPIO26.
5	GPIO25_IN	R	-	-	The pin status of PSON#/GPIO25.
4	GPIO24_IN	R	-	-	The pin status of S3#/GPIO24.
3	GPIO23_IN	R	-	-	The pin status of PWSOUT#/GPIO23.
2	GPIO22_IN	R	-	-	The pin status of PWSIN#/GPIO22.
1	GPIO21_IN	R	-	-	The pin status of ATXPG/GPIO21.
0	GPIO20_IN	R	-	-	The pin status of ALERT#/GPIO20/SCL/CIRRX#.

GPIO2 Drive Enable Register — offset D3h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	5VSB	-	Reserved.
5	GPIO25_DRV_EN	R/W	5VSB	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	5VSB	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	5VSB	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	5VSB	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	5VSB	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	5VSB	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

			5VSB		

GPIO3 Output Enable Register — offset C0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_OE	R/W	LRESET#	0	0: GPIO37 is in input mode. 1: GPIO37 is in output mode.
6	GPIO36_OE	R/W	LRESET#	0	0: GPIO36 is in input mode. 1: GPIO35 is in output mode.
5	GPIO35_OE	R/W	LRESET#	0	0: GPIO35 is in input mode. 1: GPIO35 is in output mode.
4	GPIO34_OE	R/W	LRESET#	0	0: GPIO34 is in input mode. 1: GPIO34 is in output mode.
3	GPIO33_OE	R/W	LRESET#	0	0: GPIO33 is in input mode. 1: GPIO33 is in output mode.
2	GPIO32_OE	R/W	LRESET#	0	0: GPIO32 is in input mode. 1: GPIO32 is in output mode.
1	GPIO31_OE	R/W	LRESET#	0	0: GPIO31 is in input mode. 1: GPIO31 is in output mode.
0	GPIO30_OE	R/W	LRESET#	0	0: GPIO30 is in input mode. 1: GPIO30 is in output mode.

GPIO3 Output Data Register — offset C1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_VAL	R/W	LRESET#	1	0: GPIO37 outputs 0 when in output mode. 1: GPIO37 outputs 1 when in output mode.
6	GPIO36_VAL	R/W	LRESET#	1	0: GPIO36 outputs 0 when in output mode. 1: GPIO36 outputs 1 when in output mode.
5	GPIO35_VAL	R/W	LRESET#	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_VAL	R/W	LRESET#	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	LRESET#	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	LRESET#	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	LRESET#	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	LRESET#	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

GPIO3 Pin Status Register — offset C2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_IN	R	-	-	The pin status of SIN3/GPIO37.
6	GPIO36_IN	R	-	-	The pin status of SOUT3/GPIO36.
5	GPIO35_IN	R	-	-	The pin status of DSR3#/GPIO35.

4	GPIO34_IN	R	-	-	The pin status of RTS3#/GPIO34.
3	GPIO33_IN	R	-	-	The pin status of DTR3#/GPIO33.
2	GPIO32_IN	R	-	-	The pin status of CTS3#/GPIO32.
1	GPIO31_IN	R	-	-	The pin status of RI3#/GPIO31.
0	GPIO30_IN	R	-	-	The pin status of DCD3#/GPIO30.

GPIO3 Drive Enable Register — offset C3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DRV_EN	R/W	LRESET#	0	0: GPIO37 is open drain in output mode. 1: GPIO37 is push pull in output mode.
6	GPIO36_DRV_EN	R/W	LRESET#	0	0: GPIO36 is open drain in output mode. 1: GPIO36 is push pull in output mode.
5	GPIO35_DRV_EN	R/W	LRESET#	0	0: GPIO35 is open drain in output mode. 1: GPIO35 is push pull in output mode.
4	GPIO34_DRV_EN	R/W	LRESET#	0	0: GPIO34 is open drain in output mode. 1: GPIO34 is push pull in output mode.
3	GPIO33_DRV_EN	R/W	LRESET#	0	0: GPIO33 is open drain in output mode. 1: GPIO33 is push pull in output mode.
2	GPIO32_DRV_EN	R/W	LRESET#	0	0: GPIO32 is open drain in output mode. 1: GPIO32 is push pull in output mode.
1	GPIO31_DRV_EN	R/W	LRESET#	0	0: GPIO31 is open drain in output mode. 1: GPIO31 is push pull in output mode.
0	GPIO30_DRV_EN	R/W	LRESET#	0	0: GPIO30 is open drain in output mode. 1: GPIO30 is push pull in output mode.

GPIO4 Output Enable Register — offset B0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_OE	R/W	LRESET#	0	0: GPIO47 is in input mode. 1: GPIO47 is in output mode.
6	GPIO46_OE	R/W	LRESET#	0	0: GPIO46 is in input mode. 1: GPIO45 is in output mode.
5	GPIO45_OE	R/W	LRESET#	0	0: GPIO45 is in input mode. 1: GPIO45 is in output mode.
4	GPIO44_OE	R/W	LRESET#	0	0: GPIO44 is in input mode. 1: GPIO44 is in output mode.
3	GPIO43_OE	R/W	LRESET#	0	0: GPIO43 is in input mode. 1: GPIO43 is in output mode.
2	GPIO42_OE	R/W	LRESET#	0	0: GPIO42 is in input mode. 1: GPIO42 is in output mode.
1	GPIO41_OE	R/W	LRESET#	0	0: GPIO41 is in input mode. 1: GPIO41 is in output mode.
0	GPIO40_OE	R/W	LRESET#	0	0: GPIO40 is in input mode. 1: GPIO40 is in output mode.

GPIO4 Output Data Register — offset B1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_VAL	R/W	LRESET#	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_VAL	R/W	LRESET#	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_VAL	R/W	LRESET#	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_VAL	R/W	LRESET#	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3	GPIO43_VAL	R/W	LRESET#	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs 1 when in output mode.
2	GPIO42_VAL	R/W	LRESET#	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs 1 when in output mode.
1	GPIO41_VAL	R/W	LRESET#	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs 1 when in output mode.
0	GPIO40_VAL	R/W	LRESET#	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs 1 when in output mode.

GPIO4 Pin Status Register — offset B2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_IN	R	-	-	The pin status of SIN4/GPIO47.
6	GPIO46_IN	R	-	-	The pin status of SOUT4/GPIO46.
5	GPIO45_IN	R	-	-	The pin status of DSR4#/GPIO45.
4	GPIO44_IN	R	-	-	The pin status of RTS4#/GPIO44.
3	GPIO43_IN	R	-	-	The pin status of DTR4#/GPIO43.
2	GPIO42_IN	R	-	-	The pin status of CTS4#/GPIO42.
1	GPIO41_IN	R	-	-	The pin status of RI4#/GPIO41.
0	GPIO40_IN	R	-	-	The pin status of DCD4#/GPIO40.

GPIO4 Drive Enable Register — offset B3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DRV_EN	R/W	LRESET#	0	0: GPIO47 is open drain in output mode. 1: GPIO47 is push pull in output mode.
6	GPIO46_DRV_EN	R/W	LRESET#	0	0: GPIO46 is open drain in output mode. 1: GPIO46 is push pull in output mode.
5	GPIO45_DRV_EN	R/W	LRESET#	0	0: GPIO45 is open drain in output mode. 1: GPIO45 is push pull in output mode.
4	GPIO44_DRV_EN	R/W	LRESET#	0	0: GPIO44 is open drain in output mode. 1: GPIO44 is push pull in output mode.
3	GPIO43_DRV_EN	R/W	LRESET#	0	0: GPIO43 is open drain in output mode. 1: GPIO43 is push pull in output mode.
2	GPIO42_DRV_EN	R/W	LRESET#	0	0: GPIO42 is open drain in output mode. 1: GPIO42 is push pull in output mode.

1	GPIO41_DRV_EN	R/W	LRESET#	0	0: GPIO41 is open drain in output mode. 1: GPIO41 is push pull in output mode.
0	GPIO40_DRV_EN	R/W	LRESET#	0	0: GPIO40 is open drain in output mode. 1: GPIO40 is push pull in output mode.

GPIO5 Output Enable Register — offset A0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_OE	R/W	LRESET#	0	0: GPIO57 is in input mode. 1: GPIO57 is in output mode.
6	GPIO56_OE	R/W	LRESET#	0	0: GPIO56 is in input mode. 1: GPIO56 is in output mode.
5	GPIO55_OE	R/W	LRESET#	0	0: GPIO55 is in input mode. 1: GPIO55 is in output mode.
4	GPIO54_OE	R/W	LRESET#	0	0: GPIO54 is in input mode. 1: GPIO54 is in output mode.
3	GPIO53_OE	R/W	LRESET#	0	0: GPIO53 is in input mode. 1: GPIO53 is in output mode.
2	GPIO52_OE	R/W	LRESET#	0	0: GPIO52 is in input mode. 1: GPIO52 is in output mode.
1	GPIO51_OE	R/W	LRESET#	0	0: GPIO51 is in input mode. 1: GPIO51 is in output mode.
0	GPIO50_OE	R/W	LRESET#	0	0: GPIO50 is in input mode. 1: GPIO50 is in output mode.

GPIO5 Output Data Register — offset A1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_VAL	R/W	LRESET#	1	0: GPIO57 outputs 0 when in output mode. 1: GPIO57 outputs 1 when in output mode.
6	GPIO56_VAL	R/W	LRESET#	1	0: GPIO56 outputs 0 when in output mode. 1: GPIO56 outputs 1 when in output mode.
5	GPIO55_VAL	R/W	LRESET#	1	0: GPIO55 outputs 0 when in output mode. 1: GPIO55 outputs 1 when in output mode.
4	GPIO54_VAL	R/W	LRESET#	1	0: GPIO54 outputs 0 when in output mode. 1: GPIO54 outputs 1 when in output mode.
3	GPIO53_VAL	R/W	LRESET#	1	0: GPIO53 outputs 0 when in output mode. 1: GPIO53 outputs 1 when in output mode.
2	GPIO52_VAL	R/W	LRESET#	1	0: GPIO52 outputs 0 when in output mode. 1: GPIO52 outputs 1 when in output mode.
1	GPIO51_VAL	R/W	LRESET#	1	0: GPIO51 outputs 0 when in output mode. 1: GPIO51 outputs 1 when in output mode.
0	GPIO50_VAL	R/W	LRESET#	1	0: GPIO50 outputs 0 when in output mode. 1: GPIO50 outputs 1 when in output mode.

GPIO5 Pin Status Register — offset A2h

Bit	Name	R/W	Reset	Default	Description
4	GPIO57_IN	R	-	-	The pin status of GPIO57/WGATE#/DSR6#/T2EX.
4	GPIO56_IN	R	-	-	The pin status of GPIO56/HDSEL#/DTR6#/T2.
4	GPIO55_IN	R	-	-	The pin status of GPIO55/STEP#/CTS6#/P35.
4	GPIO54_IN	R	-	-	The pin status of GPIO54/DIR#/RI6#/P34.
3	GPIO53_IN	R	-	-	The pin status of GPIO53/WDATA#/DCD6#/P33.
2	GPIO52_IN	R	-	-	The pin status of GPIO52/DRVA#/SOUT6/P32.
1	GPIO51_IN	R	-	-	The pin status of GPIO51/MOA#/SIN6/P31.
0	GPIO50_IN	R	-	-	The pin status of GPIO50/DENSEL#/RTS6#/P30.

GPIO5 Drive Enable Register — offset A3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_DRV_EN	R/W	LRESET#	0	0: GPIO57 is open drain in output mode. 1: GPIO57 is push pull in output mode.
6	GPIO56_DRV_EN	R/W	LRESET#	0	0: GPIO56 is open drain in output mode. 1: GPIO56 is push pull in output mode.
5	GPIO55_DRV_EN	R/W	LRESET#	0	0: GPIO55 is open drain in output mode. 1: GPIO55 is push pull in output mode.
4	GPIO54_DRV_EN	R/W	LRESET#	0	0: GPIO54 is open drain in output mode. 1: GPIO54 is push pull in output mode.
3	GPIO53_DRV_EN	R/W	LRESET#	0	0: GPIO53 is open drain in output mode. 1: GPIO53 is push pull in output mode.
2	GPIO52_DRV_EN	R/W	LRESET#	0	0: GPIO52 is open drain in output mode. 1: GPIO52 is push pull in output mode.
1	GPIO51_DRV_EN	R/W	LRESET#	0	0: GPIO51 is open drain in output mode. 1: GPIO51 is push pull in output mode.
0	GPIO50_DRV_EN	R/W	LRESET#	0	0: GPIO50 is open drain in output mode. 1: GPIO50 is push pull in output mode.

GPIO5 SMI Enable Register — offset A8h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO57_SMI_ST is set.
6	GPIO56_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO56_SMI_ST is set.
5	GPIO55_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO55_SMI_ST is set.
4	GPIO54_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO54_SMI_ST is set.
3	GPIO53_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO53_SMI_ST is set.
2	GPIO52_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO52_SMI_ST is set.

1	GPIO51_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO51_SMI_ST is set.
0	GPIO50_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO50_SMI_ST is set.

GPIO5 SMI Status Register — offset A9h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO57 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO56_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO56 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO55_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO55 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO54_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO54 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO53_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO53 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO52_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO52 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO51_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO51 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO50_SMI_ST	R/W	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO50 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

GPIO6 Output Enable Register — offset 90h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_OE	R/W	LRESET#	0	0: GPIO67 is in input mode. 1: GPIO67 is in output mode.
6	GPIO66_OE	R/W	LRESET#	0	0: GPIO66 is in input mode. 1: GPIO65 is in output mode.
5	GPIO65_OE	R/W	LRESET#	0	0: GPIO65 is in input mode. 1: GPIO65 is in output mode.
4	GPIO64_OE	R/W	LRESET#	0	0: GPIO64 is in input mode. 1: GPIO64 is in output mode.
3	GPIO63_OE	R/W	LRESET#	0	0: GPIO63 is in input mode. 1: GPIO63 is in output mode.
2	GPIO62_OE	R/W	LRESET#	0	0: GPIO62 is in input mode. 1: GPIO62 is in output mode.

1	GPIO61_OE	R/W	LRESET#	0	0: GPIO61 is in input mode. 1: GPIO61 is in output mode.
0	GPIO60_OE	R/W	LRESET#	0	0: GPIO60 is in input mode. 1: GPIO60 is in output mode.

GPIO6 Output Data Register — offset 91h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_VAL	R/W	LRESET#	1	0: GPIO67 outputs 0 when in output mode. 1: GPIO67 outputs 1 when in output mode.
6	GPIO66_VAL	R/W	LRESET#	1	0: GPIO66 outputs 0 when in output mode. 1: GPIO66 outputs 1 when in output mode.
5	GPIO65_VAL	R/W	LRESET#	1	0: GPIO65 outputs 0 when in output mode. 1: GPIO65 outputs 1 when in output mode.
4	GPIO64_VAL	R/W	LRESET#	1	0: GPIO64 outputs 0 when in output mode. 1: GPIO64 outputs 1 when in output mode.
3	GPIO63_VAL	R/W	LRESET#	1	0: GPIO63 outputs 0 when in output mode. 1: GPIO63 outputs 1 when in output mode.
2	GPIO62_VAL	R/W	LRESET#	1	0: GPIO62 outputs 0 when in output mode. 1: GPIO62 outputs 1 when in output mode.
1	GPIO61_VAL	R/W	LRESET#	1	0: GPIO61 outputs 0 when in output mode. 1: GPIO61 outputs 1 when in output mode.
0	GPIO60_VAL	R/W	LRESET#	1	0: GPIO60 outputs 0 when in output mode. 1: GPIO60 outputs 1 when in output mode.

GPIO6 Pin Status Register — offset 92h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_IN	R	-	-	The pin status of S5#/GPIO67.
6	GPIO66_IN	R	-	-	The pin status of DPWROK/GPIO66.
5	GPIO65_IN	R	-	-	The pin status of PME#/GPIO65.
4	GPIO64_IN	R	-	-	The pin status of GPIO64DSKCHG#/DSR5#.
3	GPIO63_IN	R	-	-	The pin status of GPIO63/WPT#/DTR5#/PWM3.
2	GPIO62_IN	R	-	-	The pin status of GPIO62/INDEX#/CTS5#/PWM2.
1	GPIO61_IN	R	-	-	The pin status of GPIO61/TRK0#/RI5#/PWM1.
0	GPIO60_IN	R	-	-	The pin status of GPIO60/RDATA#/DCD5#/PWM0.

GPIO6 Drive Enable Register — offset 93h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_DRV_EN	R/W	LRESET#	0	0: GPIO67 is open drain in output mode. 1: GPIO67 is push pull in output mode.
6	GPIO66_DRV_EN	R/W	LRESET#	0	0: GPIO66 is open drain in output mode. 1: GPIO66 is push pull in output mode.
5	GPIO65_DRV_EN	R/W	LRESET#	0	0: GPIO65 is open drain in output mode. 1: GPIO65 is push pull in output mode.
4	GPIO64_DRV_EN	R/W	LRESET#	0	0: GPIO64 is open drain in output mode. 1: GPIO64 is push pull in output mode.

3	GPIO63_DRV_EN	R/W	LRESET#	0	0: GPIO63 is open drain in output mode. 1: GPIO63 is push pull in output mode.
2	GPIO62_DRV_EN	R/W	LRESET#	0	0: GPIO62 is open drain in output mode. 1: GPIO62 is push pull in output mode.
1	GPIO61_DRV_EN	R/W	LRESET#	0	0: GPIO61 is open drain in output mode. 1: GPIO61 is push pull in output mode.
0	GPIO60_DRV_EN	R/W	LRESET#	0	0: GPIO60 is open drain in output mode. 1: GPIO60 is push pull in output mode.

GPIO7 Output Enable Register — offset 80h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_OE	R/W	LRESET#	0	0: GPIO77 is in input mode. 1: GPIO77 is in output mode.
6	GPIO76_OE	R/W	LRESET#	0	0: GPIO76 is in input mode. 1: GPIO75 is in output mode.
5	GPIO75_OE	R/W	LRESET#	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.
4	GPIO74_OE	R/W	LRESET#	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	LRESET#	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.
2	GPIO72_OE	R/W	LRESET#	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.
1	GPIO71_OE	R/W	LRESET#	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	LRESET#	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

GPIO7 Output Data Register — offset 81h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_VAL	R/W	LRESET#	1	0: GPIO77 outputs 0 when in output mode. 1: GPIO77 outputs 1 when in output mode.
6	GPIO76_VAL	R/W	LRESET#	1	0: GPIO76 outputs 0 when in output mode. 1: GPIO76 outputs 1 when in output mode.
5	GPIO75_VAL	R/W	LRESET#	1	0: GPIO75 outputs 0 when in output mode. 1: GPIO75 outputs 1 when in output mode.
4	GPIO74_VAL	R/W	LRESET#	1	0: GPIO74 outputs 0 when in output mode. 1: GPIO74 outputs 1 when in output mode.
3	GPIO73_VAL	R/W	LRESET#	1	0: GPIO73 outputs 0 when in output mode. 1: GPIO73 outputs 1 when in output mode.
2	GPIO72_VAL	R/W	LRESET#	1	0: GPIO72 outputs 0 when in output mode. 1: GPIO72 outputs 1 when in output mode.
1	GPIO71_VAL	R/W	LRESET#	1	0: GPIO71 outputs 0 when in output mode. 1: GPIO71 outputs 1 when in output mode.
0	GPIO70_VAL	R/W	LRESET#	1	0: GPIO70 outputs 0 when in output mode. 1: GPIO70 outputs 1 when in output mode.

GPIO7 Pin Status Register — offset 82h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_IN	R	-	-	The pin status of GPIO77/STB#.
6	GPIO76_IN	R	-	-	The pin status of GPIO76/AFD#.
5	GPIO75_IN	R	-	-	The pin status of GPIO75/ERR#.
4	GPIO74_IN	R	-	-	The pin status of GPIO74/INIT#.
3	GPIO73_IN	R	-	-	The pin status of GPIO73/SLIN#.
2	GPIO72_IN	R	-	-	The pin status of GPIO72/ACK#.
1	GPIO71_IN	R	-	-	The pin status of GPIO71/BUSY.
0	GPIO70_IN	R	-	-	The pin status of GPIO70/PE/FANCTRL3.

GPIO7 Drive Enable Register — offset 83h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_DRV_EN	R/W	LRESET#	0	0: GPIO77 is open drain in output mode. 1: GPIO77 is push pull in output mode.
6	GPIO76_DRV_EN	R/W	LRESET#	0	0: GPIO76 is open drain in output mode. 1: GPIO76 is push pull in output mode.
5	GPIO75_DRV_EN	R/W	LRESET#	0	0: GPIO75 is open drain in output mode. 1: GPIO75 is push pull in output mode.
4	GPIO74_DRV_EN	R/W	LRESET#	0	0: GPIO74 is open drain in output mode. 1: GPIO74 is push pull in output mode.
3	GPIO73_DRV_EN	R/W	LRESET#	0	0: GPIO73 is open drain in output mode. 1: GPIO73 is push pull in output mode.
2	GPIO72_DRV_EN	R/W	LRESET#	0	0: GPIO72 is open drain in output mode. 1: GPIO72 is push pull in output mode.
1	GPIO71_DRV_EN	R/W	LRESET#	0	0: GPIO71 is open drain in output mode. 1: GPIO71 is push pull in output mode.
0	GPIO70_DRV_EN	R/W	LRESET#	0	0: GPIO70 is open drain in output mode. 1: GPIO70 is push pull in output mode.

GPIO8 Output Enable Register — offset 88h

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_OE	R/W	LRESET#	0	0: GPIO87 is in input mode. 1: GPIO87 is in output mode.
6	GPIO86_OE	R/W	LRESET#	0	0: GPIO86 is in input mode. 1: GPIO85 is in output mode.
5	GPIO85_OE	R/W	LRESET#	0	0: GPIO85 is in input mode. 1: GPIO85 is in output mode.
4	GPIO84_OE	R/W	LRESET#	0	0: GPIO84 is in input mode. 1: GPIO84 is in output mode.
3	GPIO83_OE	R/W	LRESET#	0	0: GPIO83 is in input mode. 1: GPIO83 is in output mode.
2	GPIO82_OE	R/W	LRESET#	0	0: GPIO82 is in input mode. 1: GPIO82 is in output mode.

1	GPIO81_OE	R/W	LRESET#	0	0: GPIO81 is in input mode. 1: GPIO81 is in output mode.
0	GPIO80_OE	R/W	LRESET#	0	0: GPIO80 is in input mode. 1: GPIO80 is in output mode.

GPIO8 Output Data Register — offset 89h

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_VAL	R/W	LRESET#	1	0: GPIO87 outputs 0 when in output mode. 1: GPIO87 outputs 1 when in output mode.
6	GPIO86_VAL	R/W	LRESET#	1	0: GPIO86 outputs 0 when in output mode. 1: GPIO86 outputs 1 when in output mode.
5	GPIO85_VAL	R/W	LRESET#	1	0: GPIO85 outputs 0 when in output mode. 1: GPIO85 outputs 1 when in output mode.
4	GPIO84_VAL	R/W	LRESET#	1	0: GPIO84 outputs 0 when in output mode. 1: GPIO84 outputs 1 when in output mode.
3	GPIO83_VAL	R/W	LRESET#	1	0: GPIO83 outputs 0 when in output mode. 1: GPIO83 outputs 1 when in output mode.
2	GPIO82_VAL	R/W	LRESET#	1	0: GPIO82 outputs 0 when in output mode. 1: GPIO82 outputs 1 when in output mode.
1	GPIO81_VAL	R/W	LRESET#	1	0: GPIO81 outputs 0 when in output mode. 1: GPIO81 outputs 1 when in output mode.
0	GPIO80_VAL	R/W	LRESET#	1	0: GPIO80 outputs 0 when in output mode. 1: GPIO80 outputs 1 when in output mode.

GPIO8 Pin Status Register — offset 8Ah

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_IN	R	-	-	The pin status of GPIO87/PD7.
6	GPIO86_IN	R	-	-	The pin status of GPIO86/PD6.
5	GPIO85_IN	R	-	-	The pin status of GPIO85/PD5.
4	GPIO84_IN	R	-	-	The pin status of GPIO84/PD4.
3	GPIO83_IN	R	-	-	The pin status of GPIO83/PD3.
2	GPIO82_IN	R	-	-	The pin status of GPIO82/PD2.
1	GPIO81_IN	R	-	-	The pin status of GPIO81/PD1.
0	GPIO80_IN	R	-	-	The pin status of GPIO80/PD0.

GPIO8 Drive Enable Register — offset 8Bh

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_DRV_EN	R/W	LRESET#	0	0: GPIO87 is open drain in output mode. 1: GPIO87 is push pull in output mode.
6	GPIO86_DRV_EN	R/W	LRESET#	0	0: GPIO86 is open drain in output mode. 1: GPIO86 is push pull in output mode.
5	GPIO85_DRV_EN	R/W	LRESET#	0	0: GPIO85 is open drain in output mode. 1: GPIO85 is push pull in output mode.

4	GPIO84_DRV_EN	R/W	LRESET#	0	0: GPIO84 is open drain in output mode. 1: GPIO84 is push pull in output mode.
3	GPIO83_DRV_EN	R/W	LRESET#	0	0: GPIO83 is open drain in output mode. 1: GPIO83 is push pull in output mode.
2	GPIO82_DRV_EN	R/W	LRESET#	0	0: GPIO82 is open drain in output mode. 1: GPIO82 is push pull in output mode.
1	GPIO81_DRV_EN	R/W	LRESET#	0	0: GPIO81 is open drain in output mode. 1: GPIO81 is push pull in output mode.
0	GPIO80_DRV_EN	R/W	LRESET#	0	0: GPIO80 is open drain in output mode. 1: GPIO80 is push pull in output mode.

7.20.10 GPIO8x Scan Code Registers

GPIO8 Make Code 0 Register — offset D8h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE0	R/W	5VSB	0	This byte is used to assert make code when scan code event 0 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO80.

GPIO8 Make Code 1 Register — offset D9h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE1	R/W	5VSB	0	This byte is used to assert make code when scan code event 1 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO81.

GPIO8 Make Code 2 Register — offset DAh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE2	R/W	5VSB	0	This byte is used to assert make code when scan code event 2 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO82.

GPIO8 Make Code 3 Register — offset DBh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE3	R/W	5VSB	0	This byte is used to assert make code when scan code event 3 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO83.

GPIO8 Make Code 4 Register — offset DCh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE4	R/W	5VSB	0	This byte is used to assert make code when scan code event 4 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO84.

GPIO8 Make Code 5 Register — offset DDh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE5	R/W	5VSB	0	This byte is used to assert make code when scan code event 5 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO85.

GPIO8 Make Code 6 Register — offset DEh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE6	R/W	5VSB	0	This byte is used to assert make code when scan code event 6 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO86.

GPIO8 Make Code 7 Register — offset DFh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_MAKE_CODE7	R/W	5VSB	0	This byte is used to assert make code when scan code event 7 occur. The scan code events will set KBC OBF and put their make/break code into KBC output buffer. The break code is make code + 0x80 and this function is implemented by µC. The source of event is GPIO87.

GPIO8 Pre-Code 0 Register — offset C8h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE0	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 1 Register — offset C9h

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE1	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 2 Register — offset CAh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE2	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 3 Register — offset CBh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE3	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 4 Register — offset CCh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE4	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 5 Register — offset CDh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE5	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 6 Register — offset CEh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE6	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Pre-Code 7 Register — offset CFh

Bit	Name	R/W	Reset	Default	Description
7-0	GP_PRE_CODE7	R/W	5VSB	0xE0	This byte is used to assert a pre-code before the make/break code when it is enabled.

GPIO8 Scan Code 0 Control Register — offset B8h

Bit	Name	R/W	Reset	Default	Description
7	GP0_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurs.
6	GP0_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurs.
5	GP0_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurs.
4	GP0_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP0_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP0_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO8 Scan Code 1 Control Register — offset B9h

Bit	Name	R/W	Reset	Default	Description
7	GP1_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurs.
6	GP1_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurs.
5	GP1_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurs.
4	GP1_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP1_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP1_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO8 Scan Code 2 Control Register — offset BAh

Bit	Name	R/W	Reset	Default	Description
7	GP2_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurs.
6	GP2_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurs.
5	GP2_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurs.
4	GP2_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP2_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP2_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO8 Scan Code 3 Control Register — offset BBh

Bit	Name	R/W	Reset	Default	Description
7	GP3_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurs.
6	GP3_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurs.
5	GP3_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurs.
4	GP3_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP3_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP3_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO8 Scan Code 4 Control Register — offset BCh

Bit	Name	R/W	Reset	Default	Description
7	GP4_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurs.
6	GP4_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurs.
5	GP4_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurs.
4	GP4_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.
3-2	GP4_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP4_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO8 Scan Code 5 Control Register — offset BDh

Bit	Name	R/W	Reset	Default	Description
7	GP5_CTRL_EN	R/W	5VSB	0	Set “1” will assert a left “Ctrl” key code first when scan code event occurs.
6	GP5_ALT_EN	R/W	5VSB	0	Set “1” will assert a left “Alt” key code first when scan code event occurs.
5	GP5_SHIFT_EN	R/W	5VSB	0	Set “1” will assert a left “Shift” key code first when scan code event occurs.
4	GP5_PRE_EN	R/W	5VSB	0	Set “1” will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is “Ctrl” → “Alt” → “Shift” → Pre-code → Make/Break code.

3-2	GP5_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP5_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO8 Scan Code 6 Control Register — offset BEh

Bit	Name	R/W	Reset	Default	Description
7	GP6_CTRL_EN	R/W	5VSB	0	Set "1" will assert a left "Ctrl" key code first when scan code event occurs.
6	GP6_ALT_EN	R/W	5VSB	0	Set "1" will assert a left "Alt" key code first when scan code event occurs.
5	GP6_SHIFT_EN	R/W	5VSB	0	Set "1" will assert a left "Shift" key code first when scan code event occurs.
4	GP6_PRE_EN	R/W	5VSB	0	Set "1" will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is "Ctrl" → "Alt" → "Shift" → Pre-code → Make/Break code.
3-2	GP6_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP6_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO8 Scan Code 7 Control Register — offset BFh

Bit	Name	R/W	Reset	Default	Description
7	GP7_CTRL_EN	R/W	5VSB	0	Set "1" will assert a left "Ctrl" key code first when scan code event occurs.
6	GP7_ALT_EN	R/W	5VSB	0	Set "1" will assert a left "Alt" key code first when scan code event occurs.
5	GP7_SHIFT_EN	R/W	5VSB	0	Set "1" will assert a left "Shift" key code first when scan code event occurs.
4	GP7_PRE_EN	R/W	5VSB	0	Set "1" will assert a left pre-code first when scan code 0 event occurs. When multiple keys are enabled, the sequence is "Ctrl" → "Alt" → "Shift" → Pre-code → Make/Break code.
3-2	GP7_DELAY_TIME	R/W	5VSB	0	The delay time for repeat make code could be user defined. µC reads this register to determine the delay time.
0	GP7_REP_TIME	R/W	5VSB	0	The repeat time for repeat make code could be user defined. µC reads this register to determine the delay time.

GPIO7 Function Select 1 Register — offset ACh

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO73_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO73 is.
5-4	GPIO72_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO72 is.
3-2	GPIO71_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO71 is.
1-0	GPIO70_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO70 is.

GPIO7 Function Select Register — offset ADh

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO77_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO77 is.

5-4	GPIO76_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO76 is.
3-2	GPIO75_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO75 is.
1-0	GPIO74_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO74 is.

GPIO8 Function Select 1 Register — offset AEh

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO83_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO83 is.
5-4	GPIO82_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO82 is.
3-2	GPIO81_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO81 is.
1-0	GPIO80_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO80 is.

GPIO8 Function Select Register — offset AFh

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO87_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO87 is.
5-4	GPIO86_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO86 is.
3-2	GPIO85_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO85 is.
1-0	GPIO84_FUNC_SEL	R/W	5VSB	0	These two bits are used for host and µC communication. µC could used these two bits to decide which function GOPIO84 is.

7.20.11 KBC µC Side Register (Base Address 0x2200, 256 bytes)

Output Buffer Register — Offset 00h

Bit	Name	R/W	Reset	Default	Description
7-0	µC_OUTPUT_BUF	R/W	5VSB	0	The code µC write to KBC. After write this byte, KBC OBF will be set.

KBC Control Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7	µC_KB_OBF	R/W	5VSB	0	This bit is set by writing µC_OUTPUT_BUF when MO_DATE_EN is disabled. It will auto cleared when the host read 0x60 port.
6	µC_MO_OBF	R/W	5VSB	0	This bit is set by write µC_OUTPUT_BUF when MO_DATE_EN is enabled. It will auto cleared when the host read 0x60 port.
5	µC_DIS_OBF	R/W	5VSB	0	Set “1” to disable PS/2 to set OBF flag.
4	MO_DATA_EN	R/W	5VSB	0	0: µC_OUTPUT_BUF is the keyboard data. 1: µC_OUTPUT_BUF is the mouse data.

3	HOST_DIS_MO_CLK	R	5VSB	0	This bit represents the status of host disable mouse clock signal.
2	HOST_DIS_KB_CLK	R	5VSB	0	This bit represents the status of host disable keyboard clock signal.
1	µC_DIS_MO_CLK	R/W	5VSB	0	Set "1" to disable PS/2 mouse interface. PS2_CTRL_EN switch the disable signal between HOST_DIS_MO_CLK and µC_DIS_MO_CLK.
0	µC_DIS_KB_CLK	R/W	5VSB	0	Set "1" to disable PS/2 keyboard interface. PS2_CTRL_EN switch the disable signal between HOST_DIS_KB_CLK and µC_DIS_KB_CLK.

KBC Status Register — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7-0	KBC_STS	R	5VSB	-	The status of KBC. Same as 0x64 port of host side.

PS/2 Interrupt Enable Register — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7	KBC_ST_INT_EN	R/W	5VSB	0	0: Disable KBC status interrupt. 1: Enable KBC status interrupt. KBC_STS change will assert interrupt to µC.
6	Reserved	-	-	-	Reserved.
5	MO_RD_IN_EN	R/W	5VSB	0	0: Disable read mouse data interrupt. 1: Enable read mouse data interrupt. Host read mouse data will assert interrupt to µC.
4	KB_RD_IN_EN	R/W	5VSB	0	0: Disable read keyboard data interrupt. 1: Enable read keyboard data interrupt. Host read mouse data will assert interrupt to µC.
3	MO_WR_INT_EN	R/W	5VSB	0	0: Disable PS/2 mouse write command interrupt. 1: Enable PS/2 mouse interface interrupt. An interrupt will be asserted to µC when the host write command to PS/2 mouse which will set MO_WR_BYTE_ST.
2	KB_WR_INT_EN	R/W	5VSB	0	0: Disable PS/2 keyboard write command interrupt. 1: Enable PS/2 keyboard interface interrupt. An interrupt will be asserted to µC when host write command to PS/2 keyboard which will set KB_WR_BYTE_ST.
1	MO_RCV_INT_EN	R/W	5VSB	0	0: Disable PS/2 mouse interface receiving interrupt. 1: Enable PS/2 mouse interface receiving interrupt. An interrupt will be asserted to µC when a byte is received which will set MO_RCV_BYTE_ST.
0	KB_RCV_INT_EN	R/W	5VSB	0	0: Disable PS/2 keyboard interface receiving interrupt. 1: Enable PS/2 keyboard interface receiving interrupt. An interrupt will be asserted to µC when a byte is received which will set KB_RCV_BYTE_ST.

PS/2 Receiving Status Register — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7	KBC_ST_CHG_ST	R/WC	5VSB	0	This bit will be set when KBC_STS changes.
6	Reserved	-	-	-	Reserved.
5	MO_RD_ST	R/WC	5VSB	0	This bit will be set when host read mouse data.
4	KB_RD_ST	R/WC	5VSB	0	This bit will be set when host read keyboard data.
3	MO_WR_BYTE_ST	R/WC	5VSB	0	This bit will be set when host write data to mouse. Write "1" to clear.
2	KB_WR_BYTE_ST	R/WC	5VSB	0	This bit will be set when host write data to keyboard. Write "1" to clear.

1	MO_RCV_BYTE_ST	R/WC	5VSB	0	This bit will be set when PS/2 mouse interface receive a byte. Write “1” to clear.
0	KB_RCV_BYTE_ST	R/WC	5VSB	0	This bit will be set when PS/2 keyboard interface receive a byte. Write “1” to clear.

PS/2 Keyboard Unmapped Code Register — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7-0	KB_UNMAPPED_CODE	R	5VSB	0	This is the raw data received from keyboard. Not translated into scan code set 1.

PS/2 Keyboard Data Register — Offset 06h

Bit	Name	R/W	Reset	Default	Description
7-0	KB_CODE	R	5VSB	0	The keyboard data after translated into scan code set 1.

PS/2 Mouse Data Register — Offset 07h

Bit	Name	R/W	Reset	Default	Description
7-0	MO_CODE	R	5VSB	0	The mouse data receive from a mouse.

PS/2 Host Output Register — Offset 08h

Bit	Name	R/W	Reset	Default	Description
7-0	PS2_HOST_DOUT	R	5VSB	0	This is the output data host write to PS/2 keyboard/mouse. Check MO_WR_BYTE_ST/KB_WR_BYTE_ST to determine the data is for keyboard or mouse.

PS/2 µC Output Register — Offset 09h

Bit	Name	R/W	Reset	Default	Description
7-0	PS2_µC_DOUT	R/W	5VSB	0	This is the output data µC wants to write to PS/2 keyboard/mouse.

PS/2 Control Register — Offset 0Ah

Bit	Name	R/W	Reset	Default	Description
7	µC_CMD_RST	W	5VSB	-	Write “1” to assert a KBC command reset to PS/2.
6	µC_CLR_IBF	W	5VSB	-	Write “1” to clear IBF.
5	µC_CLR_SWAP	W	5VSB	-	Write “1” to disable keyboard/mouse swap.
4	µC_SET_SWAP	R/W	5VSB	-	Write “1” to enable keyboard/mouse swap. This bit will return the status of swap enable.
3	µC_MO_RD	W	5VSB	-	When PS2_CTRL_EN is set to “1”, write “1” to this bit will assert a mouse read signal to PS/2 block to reset the PS/2 state machine.
2	µC_KB_RD	W	5VSB	-	When PS2_CTRL_EN is set to “1”, write “1” to this bit will assert a keyboard read signal to PS/2 block to reset the PS/2 state machine.
1	µC_MO_WR	W	5VSB	-	When PS2_CTRL_EN is set to “1”, write “1” to this bit will assert a mouse write signal to PS/2 block and the data is the PS2_µC_DOUT.
0	µC_KB_WR	W	5VSB	-	When PS2_CTRL_EN is set to “1”, write “1” to this bit will assert a keyboard write signal to PS/2 block and the data is the PS2_µC_DOUT.

PS/2 Reset Control Register — Offset 0Bh

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5	LRESET_ST	R	5VSB	0	The status of LRESET#.
4	KBC_S3	R	5VSB	0	The S3 condition status for PS/2.
3-2	Reserved	-	-	-	Reserved.
1	µC_LRESET_N	R/W	5VSB	1	When PS2_CTRL_EN is set, µC could use the bit to reset KBC block.
0	µC_KBC_S3	R/W	5VSB	0	When PS2_CTRL_EN is set, µC could use the bit to emulate a S3 condition for wakeup function.

PS/2 Reset Control Register — Offset 0Ch

Bit	Name	R/W	Reset	Default	Description
7	P_MDATA_IN	R	-	-	Pin status of MDATA.
6	P_MCLK_IN	R	-	-	Pin status of MCLK.
5	P_KDATA_IN	R	-	-	Pin status of KDATA.
4	P_KCLK_IN	R	-	-	Pin status of KCLK.
3	µC_MDATA_OUT	R/W	5VSB	1	When µC_MO_PIN_EN is set, µC uses this bit to control the MDATA.
2	µC_MCLK_OUT	R/W	5VSB	1	When µC_MO_PIN_EN is set, µC uses this bit to control the MCLK.
1	µC_KDATA_OUT	R/W	5VSB	1	When µC_KB_PIN_EN is set, µC uses this bit to control the KDATA.
0	µC_KCLK_OUT	R/W	5VSB	1	When µC_KB_PIN_EN is set, µC uses this bit to control the KCLK.

PS/2 Control Register — Offset 0Fh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	µC_KB_PIN_EN	R/W	5VSB	0	Set “1” to control KCLK/KDATA by µC_KCLK_OUT and µC_KDATA_OUT.
2	µC_MO_PIN_EN	R/W	5VSB	0	Set “1” to control MCLK/MDATA by µC_MCLK_OUT and µC_MDATA_OUT.
1	PS2_CTRL_EN	R/W	5VSB	0	0: Disable µC to control PS/2 interface. 1: Enable µC to control PS/2 interface. µC could assert read/write signal to PS/2 block if PSEUDO_8048_EN is “0”.
0	PSEUDO_8048_EN	R/W	5VSB	0	Set “1” to emulate 8048 to response KBC command. When this bit is set, any read/write signal for PS/2 is block. µC is responsible to return the data to keyboard controller.

7.20.12 ACPI µC Side Register (Base Address 0x2300, 256 bytes)

ACPI Pin Status 1 Register — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	RSMRST_N_IN	R	-	0	Pin status of RSMRST#.
5	PWROK_IN	R	-	0	Pin status of PWROK.
4	PSON_N_IN	R	-	0	Pin status of PS_ON#.
3	PWSOUT_N_IN	R	-	0	Pin status of PWSOUT#.

2	PME_N_IN	R	-	0	Pin status of PME#.
1	ERP_CTRL1_IN	R	-	0	Pin status of ERP_CTRL1#.
0	ERP_CTRL0_IN	R	-	0	Pin status of ERP_CTRL0#.

ACPI Pin Status 2 Register — Offset 04h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	LRESET_N_IN	R	-	-	Pin status of LRESET#.
5	VSB3VOK	R	-	0	The VSB3V power is ready.
4	VDD3VOK	R	-	0	The VDD3V power is ready.
3	S5_N_IN	R	-	0	Pin status of S5#.
2	S3_N_IN	R	-	0	Pin status of S3#.
1	PWSIN_N_IN	R	-	0	Pin status of PWSIN#.
0	ATXPG_IN	R	-	0	Pin status of ATXPG.

ACPI Pin Status 3 Register — Offset 05h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	DPWROK_IN	R	-	0	Pin status of DPWROK.
2	SUS_ACK_N_IN	R	-	0	Pin status of SUS_ACK#.
1	SUS_WARN_N_IN	R	-	0	Pin status of SUS_WARN#.
0	SLP_SUS_N_IN	R	-	0	Pin status of SLP_SUS.

ACPI Input Pin Control 1 Register — Offset 07h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	µC_ATXPG	R/W	5VSB	1	µC control this bit to and-ed with ATXPG pin for internal ATXPG signal.
2	µC_S3_N	R/W	5VSB	1	µC control this bit to and-ed with S3# pin for internal S3# signal.
1	µC_S5_N	R/W	5VSB	1	µC control this bit to and-ed with S5# pin for internal S5# signal.
0	µC_PWSIN_N	R/W	5VSB	1	µC control this bit to and-ed with PWSIN# pin for internal PWSIN# signal.

ACPI Input Pin Control 2 Register — Offset 08h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	µC_SUS_WARN_N	R/W	5VSB	1	µC control this bit to and-ed with SUS_WARN# pin for internal SUS_WARN# signal.
0	µC_SLP_SUS_N	R/W	5VSB	1	µC control this bit to and-ed with SLP_SUS# pin for internal SLP_SUS# signal.

KB PME Control Register — Offset 0Eh

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	5VSB	-	Reserved.
5	MS_PME_ST	R/WC	5VSB	-	This bit is the status of mouse PME event. It is the same as the PME configuration register in host side. Write “1” will clear the status.
4	KB_PME_ST	R/WC	5VSB	-	This bit is the status of keyboard PME event. It is the same as the PME configuration register in host side. Write “1” will clear the status.
3-2	Reserved	-	5VSB	-	Reserved.
1	MS_PME_EN	R/W	5VSB	0	0: Disable mouse PME event. 1: Enable mouse PME event.
0	KB_PME_EN	R/W	5VSB	0	0: Disable keyboard PME event. 1: Enable keyboard PME event.

ERP State Control Register — Offset 0Fh

Bit	Name	R/W	Reset	Default	Description
7	S3_BACK	R/W	5VSB	0	µC set this bit to inform host that the system is return from deep S3 state.
6-2	Reserved	-	-	-	Reserved.
0	DS3_STATE	R/W	5VSB	0	µC set this bit to make ACPI control signals entering deep S3 state. For example, LED will output 0.25Hz clock in deep S3 state.

ACPI Deep S3 Control Register — Offset 0Fh

Bit	Name	R/W	Reset	Default	Description
7	S3_BACK	R/W	5VSB	0	Set “1” to inform host the system is back from S3 state.
6-1	Reserved	-	-	-	Reserved.
0	DS3_STATE	R/W	5VSB	0	Set “1” to enter deep S3 state.

ACPI Interrupt Enable Register 1— Offset 10h

Bit	Name	R/W	Reset	Default	Description
7	LRESET_ST_INT_EN	R/W	5VSB	0	0: Disable LRESET# pin status interrupt. 1: Enable LRESET# pin status interrupt. An interrupt will assert to µC if LRESET# pin status change.
6	S5_ST_INT_EN	R/W	5VSB	0	0: Disable S5 state interrupt. 1: Enable S5 state interrupt. An interrupt will assert to µC if system enter S5 state.
5	S3_ST_INT_EN	R/W	5VSB	0	0: Disable S3 state interrupt. 1: Enable S3 state interrupt. An interrupt will assert to µC if system enter S3 state.
4	S0_ST_INT_EN	R/W	5VSB	0	0: Disable S0 state interrupt. 1: Enable S0 state interrupt. An interrupt will assert to µC if system enter S0 state.
3	S5_INT_EN	R/W	5VSB	0	0: Disable S5# pin status interrupt. 1: Enable S5# pin status interrupt. An interrupt will assert to µC if S5# pin status change.
2	S3_INT_EN	R/W	5VSB	0	0: Disable S3# pin status interrupt. 1: Enable S3# pin status interrupt. An interrupt will assert to µC if S3# pin status change.

1	PWSIN_INT_EN	R/W	5VSB	0	0: Disable PWSIN# pin status interrupt. 1: Enable PWSIN# pin status interrupt. An interrupt will assert to µC if PWSIN# pin status change.
0	ATXPG_INT_EN	R/W	5VSB	0	0: Disable ATXPG pin status interrupt. 1: Enable ATXPG pin status interrupt. An interrupt will assert to µC if ATXPG pin status change.

ACPI Interrupt Status Register 1 — Offset 11h

Bit	Name	R/W	Reset	Default	Description
7	LRESET_INT_ST	R/WC	5VSB	0	This bit will be set “1” if LRESET# pin status changes. Write “1” to clear.
6	S5_ST_INT_ST	R/WC	5VSB	0	This bit will be set “1” if system enters S5 state. Write “1” to clear.
5	S3_ST_INT_ST	R/WC	5VSB	0	This bit will be set “1” if system enters S3 state. Write “1” to clear.
4	S0_ST_INT_EN	R/WC	5VSB	0	This bit will be set “1” if system enters S0 state. Write “1” to clear.
3	S5_INT_ST	R/WC	5VSB	0	This bit will be set “1” if S5# pin status changes. Write “1” to clear.
2	S3_INT_ST	R/WC	5VSB	0	This bit will be set “1” if S3# pin status changes. Write “1” to clear.
1	PWSIN_INT_ST	R/WC	5VSB	0	This bit will be set “1” if PWSIN# pin status changes. Write “1” to clear.
0	ATXPG_INT_ST	R/WC	5VSB	0	This bit will be set “1” if ATXPG pin status changes. Write “1” to clear.

ACPI Interrupt Enable Register 2— Offset 12h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	SUS_WARN_INT_EN	R/W	5VSB	0	0: Disable SUS_WARN# pin status interrupt. 1: Enable SUS_WARN## pin status interrupt. An interrupt will assert to µC if SUS_WARN# pin status change.
0	SLP_SUS_INT_EN	R/W	5VSB	0	0: Disable SLP_SUS# pin status interrupt. 1: Enable SLP_SUS# pin status interrupt. An interrupt will assert to µC if SLP_SUS# pin status change.

ACPI Interrupt Status Register 2 — Offset 13h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	SUS_WARN_INT_ST	R/WC	5VSB	0	This bit will be set “1” if SUS_WARN# pin status changes. Write “1” to clear.
0	SLP_SUS_INT_ST	R/WC	5VSB	0	This bit will be set “1” if SLP_SUS# pin status changes. Write “1” to clear.

7.20.13 Configuration Register (Base Address 0x2400, 256 bytes)

Chip ID 1 Register — offset 20h (Powered by I_VSB3V)

Bit	Name	R/W	Reset	Default	Description
7-0	CHIP_ID1	R	-	0x10	Chip ID 1.

Chip ID 2 Register — offset 21h (Powered by I_VSB3V)

Bit	Name	R/W	Reset	Default	Description

7-0	CHIP_ID2	R	-	0x10	Chip ID 2.

Vendor ID 1 Register — offset 23h (Powered by I_VSB3V)

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID1	R	-	0x19	Vendor ID 1.

Vendor ID 2 Register — offset 24h (Powered by I_VSB3V)

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID2	R	-	0x34	Vendor ID 2.

I2C Address Register — offset 25h

Bit	Name	R/W	Reset	Default	Description
7-1	I2C_ADDR	R/W	5VSB	0	I2C address is used to R/W hardware monitor registers. The default address is determined by I2C_ADDR_TRAP power on strap pin. It could also be changed by write this byte with entry key 0x19, 0x34. The default value is 0x2E which indicates the address is 0x5C.
0	EN_ARA_MODE	R/W	5VSB	0	0: Disable ARA. 1: Enable ARA.

Clock Select Register — offset 26h

Bit	Name	R/W	Reset	Default	Description
7-6	CLK_SEL	R/W	5VSB	0	The clock source of CLKIN. 00: CLKIN is 48MHz 10: CLKIN is 24MHz 01: CLKIN is 14.318MHz. 10: Reserved.
5	Reserved		-		Reserved.
4	MO_PIN_LVL_SEL	R/W	5VSB	0	MCLK/MDATA input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
3	PIN76_LVL_SEL	R/W	5VSB	0	PIN 76 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
2	PIN71_LVL_SEL	R/W	5VSB	0	PIN 71 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
1	PIN68_LVL_SEL	R/W	5VSB	1	PIN 68 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
0	PIN67_LVL_SEL	R/W	5VSB	1	PIN 67 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.

Port Select Register — offset 27h

Bit	Name	R/W	Reset	Default	Description
7	OVP_MODE	R/W	VBAT*	-	0: Enable OVP function. 1: Default is disabled; internal pull high 47kΩ. The default value is determined by power on strap.
6	AT_MODE	R/W	5VSB	-	0: ATX Mode. 1: AT Mode. The default value is determined by power on strap.
5	GPIO_DEC_RANGE	R/W	3VCC	0	0: The GPIO I/O space is 8-byte. 1: The GPIO I/O space is 16-byte.
4	PORT_4E_EN	R/W	5VSB*	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by RTS1#/ Config4E_2E. Pull down to select port 2E/2F. This bit is accessed by host side only.
3-2	GPIO_PROG_SEL	R/W	5VSB	0	Offset 2Ch register select. 00: GPIO0_EN 01: GPIO1_EN 10: GPIO2_EN 11: µC_PORT_EN. Bit 0 also select the offset 28h register: 0: Multi-function Select 1 Register 1: Multi-function Select 2 Register.
1	Reserved	-	-	-	Reserved
0	CLK_TUNE_PROG_EN	R/W	3VCC	0	Set “1” to enable index 0x29, 0x2a, 0x2b, 0x2c function as clock fine tune register.

Multi-function Select 1 Register — offset 28h (Available when GPIO_PROG_SEL[0] = 0)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	FDC_GP_EN	R/W	5VSB	1	Pin 9 ~ 21 function select. These pins are controlled by FDC_GP_EN, UART5_FUNC_SEL, UART6_FUNC_SEL and PWM_PIN_EN. To function as FDC, all these bits should be clear to “0”.
5	LPT_GP_EN	R/W	5VSB	1	Pin 102 ~ 118 function select. 0: Functions as parallel port. 1: Functions as GPIO7/GPIO8.
4	MO_I2C_EN	R/W	5VSB	0	Pin 61, 62 function select. 0: PS/2 mouse interface MCLK/MDATA. 1: I2C SCL/SDA.

3-2	UART5_FUNC_SEL	R/W	5VSB	0	UART5 Function Select. 00: No UART5 pin. 01: Simple UART: only SIN5 and SOUT5 are available. Pin 57 will be function as SOUT5 and Pin 58 will function as SIN5. 10: Simple UART with RTS#. In addition to simple UART, pin 59 will be function as RTS5#. 11: Full UART: pin 57 ~ 59, 17 ~ 21 will be function as UART pins.
1-0	UART6_FUNC_SEL	R/W	5VSB	0	UART6 Function Select. 00: No UART6 pin. 01: Simple UART: only SIN6 and SOUT6 are available. Pin 10 will be function as SOUT6 and Pin 11 will be function as SIN6. 10: Simple UART with RTS#. In addition to simple UART, pin 9 will be function as RTS6#. 11: Full UART: pin 9 ~ 16 will be function as UART pins.

Multi-function Select 2 Register — offset 28h (Available when GPIO_PROG_SEL[0] = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	µC_P32_PIN59_EN	R/W	5VSB	0	0: Disable µC P32 from pin 59. 1: Enable µC P32 from pin59.
5	µC_P31_PIN57_EN	R/W	5VSB	0	0: Disable µC P31 from pin 57. 1: Enable µC P31 from pin57.
4	µC_P30_PIN58_EN	R/W	5VSB	0	0: Disable µC P30 from pin 58. 1: Enable µC P30 from pin58.
3-2	Reserved	-	-	-	Reserved
1	CIR_PIN76_EN	R/W	VBAT	0	0: Disable CIRRX# from pin76. The pin function is ALERT#/GPIO20/SCL. 1: Enable CIRRX# from pin76.
0	CIR_PIN71_EN	R/W	VBAT	0	0: Disable CIRRX# from pin71. The pin function is BEEP/GPIO16/SDA. 1: Enable CIRRX# from pin71.

Multi Function Select 3 Register — offset 29h (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	UART4_FUNC_SEL	R/W	5VSB	0	UART4 Function Select. 00: No UART4 pin. Pin 44 ~ 51 are all GPIOs. 01: Simple UART: only SIN4 and SOUT4 are available. Pin 50 will be function as SOUT4 and Pin 51 will be function as SIN4. 10: Simple UART with RTS#. In addition to the simple UART, pin 48 will be function as RTS4#. 11: Full UART: pin 44 ~ 51 will be function as UART pins.

5-4	UR3_FUNC_SEL	R/W	5VSB	0	UART3 Function Select. 00: No UART3 pin. Pin 36 ~ 43 are all GPIOs. 01: Simple UART: only SIN3 & SOUT3 are available. Pin 42 will be function as SOUT3 and Pin 43 will be function as SIN3. 10: Simple UART with RTS#. In addition to simple UART, pin 40 will be function as RTS3#. 11: Full UART: pin 36 ~ 43 will be function as UART pins.
3	SCL3_PIN76_EN	R/W	5VSB	0	0: Disable SCL from pin 76. 1: Enable SCL from pin 76. There is only one slave in the current design, it is recommended to select only one pin for SCL. When multi pins are selected, the priority of these bits is MO_I2C_EN > SCL_PIN76_EN > SCL_PIN67_EN.
2	SDA3_PIN71_EN	R/W	5VSB	0	0: Disable SDA from pin 76. 1: Enable SDA from pin 76. There is only one slave in the current design, it is recommended to select only one pin for SDA. When multi pins are selected, the priority of these bits is MO_I2C_EN > SDA_PIN71_EN > SDA_PIN68_EN.
1	SDA2_PIN68_EN	R/W	5VSB	1	0: Disable SDA from pin 68. 1: Enable SDA from pin 68. There is only one slave in current design, it is recommended to select only one pin for SDA. When multi pins are selected, the priority of these bits is MO_I2C_EN > SDA_PIN71_EN > SDA_PIN68_EN.
0	SCL2_PIN67_EN	R/W	5VSB	1	0: Disable SCL from pin 67. 1: Enable SCL from pin 67. There is only one slave in current design, it is recommended to select only one pin for SCL. When multi pins are selected, the priority of these bits is MO_I2C_EN > SCL_PIN76_EN > SCL_PIN67_EN.

10Hz Clock Divisor High Byte — offset 29h (Available when CLK_ TUNE_PROG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7	FINE_TUNE_START	W	-	-	Write “1” to start fine tune mechanism. The hardware will start to count 10 cycle internal 500KHz clock with 48MHz clock. The count will present in index 0x2A, 0x2B.
6-4	Reserved	-	-	-	Reserved
3-0	CLK10HZ_DIV	R/W	VBAT	4’h3	The divisor of 10Hz clock. Internal 10Hz clock is used to generate WDT event. It is divided from 10KHz clock and could be fine tune by change its divisor.

Multi Function Select 2 Register — offset 2Ah (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7	PWM3_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM3 from Pin 110. 1: Enable PWM3 from Pin 110.
6	PWM2_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM2 from Pin 109. 1: Enable PWM2 from Pin 109.
5	PWM1_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM1 from Pin 108. 1: Enable PWM1 from Pin 108.

4	PWM0_LPT_PIN_EN	R/W	5VSB	0	0: Disable PWM0 from Pin 107. 1: Enable PWM0 from Pin 107.
3	PWM3_PIN_EN	R/W	5VSB	0	0: Disable PWM3 from Pin 20. 1: Enable PWM3 from Pin 20.
2	PWM2_PIN_EN	R/W	5VSB	0	0: Disable PWM2 from Pin 19. 1: Enable PWM2 from Pin 19.
1	PWM1_PIN_EN	R/W	5VSB	0	0: Disable PWM1 from Pin 18. 1: Enable PWM1 from Pin 18.
0	PWM0_PIN_EN	R/W	5VSB	0	0: Disable PWM0 from Pin 17. 1: Enable PWM0 from Pin 17.

10Hz Clock Divisor Low Byte — offset 2Ah (Available when CLK_TUNE_PROG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	CLK10HZ_DIV	R/W	VBAT	8'hE7	The divisor of 10Hz clock. Internal 10Hz clock is used to generate WDT event. It is divided from 10KHz clock and could be fine tune by change its divisor.

Multi Function Select 3 Register — offset 2Bh (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_EN	R/W	VBAT	0	Pin 87 function select 0: Pin 87 functions as S5#. 1: Pin 87 functions as GPIO67.
6	GPIO66_EN	R/W	VBAT	0	Pin 86 function select 0: Pin 86 functions as DPWROK. 1: Pin 86 functions as GPIO66.
5	GPIO65_EN	R/W	VBAT	0	Pin 74 function select 0: Pin 74 functions as PME#. 1: Pin 74 functions as GPIO65.
4-2	Reserved	-	-	-	Reserved
1	FANIN3_EN	R/W	VBAT	1	Pin 102 function select 0: Pin 102 functions as SCLT. 1: Pin 102 functions as FANIN3.
0	FANCTRL3_EN	R/W	VBAT	0	Pin 103 function select. 0: Pin 103 functions as GPIO70/PE. 1: Pin 103 functions as FANCTRL3.

10Hz Clock Fine Tune Count High Byte — offset 2Bh (Available when CLK_ TUNE_PROG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7	FINE_TUNE_ST	-	5VSB	-	This bit indicates the fine tune mechanism is in process.
6-4	Reserved	-	-	-	Reserved
3-0	FINE_TUNE_CNT	R/W	5VSB	4'h3	This is the count of 10 cycles of internal 500KHz clock with 48MHz clock.

10Hz Clock Fine Tune Count Low Byte — offset 2Ch (Available when CLK_ TUNE_PROG_EN = 1

Bit	Name	R/W	Reset	Default	Description
7-0	FINE_TUNE_CNT	R/W	5VSB	4'h3	This is the count of 10 cycles of internal 500KHz clock with 48MHz clock.

GPIO0 Enable Register — offset 2Ch (Available when CLK_PROG_EN = 0 and GPIO_PROG_SEL = 2'b00)

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO04_EN	R/W	VBAT	0	Pin 56 function select. 0: Pin 56 functions as SLP_SUS#. 1: Pin 56 functions as GPIO04.
3	GPIO03_EN	R/W	VBAT	0	Pin 55 function select. 0: Pin 55 functions as SUS_ACK#. 1: Pin 55 functions as GPIO03.
2	GPIO02_EN	R/W	VBAT	0	Pin 54 function select. 0: Pin 54 functions as SUS_WARN#. 1: Pin 54 functions as GPIO02.
1	GPIO01_EN	R/W	VBAT	0	Pin 53 function select. 0: Pin 53 functions as ERP_CTRL1#. 1: Pin 53 functions as GPIO01.
0	GPIO00_EN	R/W	VBAT	0	Pin 52 function select. 0: Pin 52 functions as ERP_CTRL0#. 1: Pin 52 functions as GPIO00.

GPIO1 Enable Register — offset 2Ch (Available when CLK_PROG_EN = 0 and GPIO_PROG_SEL = 2'b01)

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_EN	R/W	VBAT	0	Pin 72 function select. 0: Pin 72 functions as PECI. 1: Pin 72 functions as GPIO17.
6	GPIO16_EN	R/W	VBAT	0	Pin 71 function select. 0: Pin 71 functions as BEEP. 1: Pin 71 functions as GPIO16.
5	GPIO15_EN	R/W	VBAT	0	Pin 70 function select. 0: Pin 70 functions as WDTRST#. 1: Pin 70 functions as GPIO15.
4	Reserved	-	-	-	Reserved
3	GPIO13_EN	R/W	VBAT	1	Pin 68 function select. 0: Pin 68 functions as IRRX. 1: Pin 68 functions as GPIO13. If SDA_PIN68_EN is set, pin 68 will function as SDA.

2	GPIO12_EN	R/W	VBAT	1	Pin 67 function select. 0: Pin 67 functions as IRTX. 1: Pin 67 functions as GPIO12. If SCL_PIN67_EN is set, pin 67 will function as SCL.
1	GPIO11_EN	R/W	VBAT	1	Pin 66 function select. 0: Pin 66 functions as LED_VCC. 1: Pin 66 functions as GPIO11.
0	GPIO10_EN	R/W	VBAT	1	Pin 65 function select. 0: Pin 65 functions as LED_VSB. 1: Pin 65 functions as GPIO10.

GPIO2 Enable Register — offset 2Ch (Available when CLK_PROG_EN = 0 and GPIO_PROG_SEL = 2'b10)

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_EN	R/W	VBAT	0	Pin 83 function select. 0: Pin 83 functions as RSMRST#. 1: Pin 83 functions as GPIO27.
6	GPIO26_EN	R/W	VBAT	0	Pin 82 function select. 0: Pin 82 functions as PWROK. 1: Pin 82 functions as GPIO26.
5	GPIO25_EN	R/W	VBAT	0	Pin 81 function select. 0: Pin 81 functions as PSON#. 1: Pin 81 functions as GPIO25.
4	GPIO24_EN	R/W	VBAT	0	Pin 80 function select. 0: Pin 81 functions as S3#. 1: Pin 81 functions as GPIO24.
3	GPIO23_EN	R/W	VBAT	0	Pin 79 function select. 0: Pin 68 functions as PWSOUT#. 1: Pin 68 functions as GPIO23.
2	GPIO22_EN	R/W	VBAT	0	Pin 78 function select. 0: Pin 78 functions as PWSIN#. 1: Pin 78 functions as GPIO22.
1	GPIO21_EN	R/W	VBAT	0	Pin 77 function select. 0: Pin 77 functions as ATXPG_IN. 1: Pin 77 functions as GPIO21.
0	GPIO20_EN	R/W	VBAT	0	Pin 76 function select. 0: Pin 76 functions as ALERT#. 1: Pin 76 functions as GPIO20. Pin 76 will function as SC: if SCL_PIN76_EN is set.

µC Port Enable Register — offset 2Ch (Available when CLK_PROG_EN = 0 and GPIO_PROG_SEL = 2'b11)

Bit	Name	R/W	Reset	Default	Description
7	µC_T2EX_EN	R/W	VBAT	0	Set "1" to enable µC T2EX function from pin 16.
6	µC_T2_EN	R/W	VBAT	0	Set "1" to enable µC T2 function from pin 15.

5	µC_P35_EN	R/W	VBAT	0	Set “1” to enable µC P3.5 (also function as µC T1) function from pin 14.
4	µC_P34_EN	R/W	VBAT	0	Set “1” to enable µC P3.4 (also function as µC T0) function from pin 13.
3	µC_P33_EN	R/W	VBAT	0	Set “1” to enable µC P3.3 (also function as µC INT1#) function from pin 12.
2	µC_P32_EN	R/W	VBAT	0	Set “1” to enable µC P3.2 (also function as µC INT0#) function from pin 9.
1	µC_P31_EN	R/W	VBAT	0	Set “1” to enable µC P3.1 (also function as µC TXD) function from pin 11.
0	µC_P30_EN	R/W	VBAT	0	Set “1” to enable µC P3.0 (also function as µC RXD) function from pin 10.

Wakeup Control Register — offset 2Dh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th>Description</th></tr>
<tr><td>7-5</td><td>Reserved</td><td>R/W</td><td>-</td><td>0</td><td>Reserved</td></tr>
<tr><td>4</td><td>KEY_SEL_ADD</td><td>R/W</td><td>VBAT</td><td>0</td><td>This bit is added to add more wakeup key function.</td></tr>
<tr><td>3</td><td>WAKEUP_EN</td><td>R/W</td><td>VBAT</td><td>1</td><td>0: disable keyboard/mouse wake up.
1: enable keyboard/mouse wake up.</td></tr>
<tr><td>2-1</td><td>KEY_SEL</td><td>R/W</td><td>VBAT</td><td>00</td><td>This registers select the keyboard wake up key. Accompanying with KEY_SEL_ADD, there are eight wakeup keys:
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wakeup Key</th></tr>
<tr><td>0</td><td>00</td><td>Ctrl + Esc</td></tr>
<tr><td>0</td><td>01</td><td>Ctrl + F1</td></tr>
<tr><td>0</td><td>10</td><td>Ctrl + Space</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power</td></tr>
<tr><td>1</td><td>10</td><td>Ctrl + Alt + Space</td></tr>
<tr><td>1</td><td>11</td><td>Space</td></tr>
</table></td></tr>
<tr><td>0</td><td>MO_SEL</td><td>R/W</td><td>VBAT</td><td>0</td><td>This register selects the mouse wake up key.
0: Wake up by clicking.
1: Wake up by clicking and movement.</td></tr>
</table>

7.20.14 RAM µC Side Register (Base Address 0x2500, 8 bytes)

The 256 byte RAM is accessed by Base Address + RAM address.

7.20.15 CIR µC Side Register (Base Address 0x2600, 256 bytes)

CIR – CIR FIFO Register – Index 2300h

Bit	Name	R/W	Reset	Default	Description
7-0	CIR_FIFO	R	5VSB	00h	Receiver Buffer is read only register. When the CIR pulse train has been detected and passed by the internal signal filter, the data sampled and shifted into shifter register will be written into Receiver Buffer Register

CIR – Interrupt Enable Register – Index 2301h

Bit	Name	R/W	Reset	Default	Description
7	Interrupt_EN	R/W	5VSB	0b	Write 1 to enable CIR interrupt.
6-0	Reserved	-	-	00h	Reserved

CIR – Interrupt Status Register – Index 2302h

Bit	Name	R/W	Reset	Default	Description
7-4	FIFO_CNT	R	5VSB	0h	This nibble indicates the number of byte that RX data receive.
3	FIFO_RST	R/W	5VSB	0b	Write 1 to reset CIR FIFO.
2	Reserved	-	-	0b	Reserved
1	Data_Lost	R	5VSB	0b	This bit indicates FIFO data lost, and write 1 to clear this bit.
0	Ready	R	5VSB	0b	This bit indicates RX data ready, and write 1 to clear this bit.

CIR – Baud Rate Low Byte Register – Index 2303h

Bit	Name	R/W	Reset	Default	Description
7-0	Baud_Lo	R/W	5VSB	A5h	The registers of BLL are baud rate divisor latch.

CIR – Baud Rate High Byte Register – Index 2304h

Bit	Name	R/W	Reset	Default	Description
7-0	Baud_Hi	R/W	5VSB	01h	The registers of BHL are baud rate divisor latch.

CIR – Waveform Logic 1 Data Register – Index 2305h

Bit	Name	R/W	Reset	Default	Description
7-0	WaveH	R/W	5VSB	80h	The registers of WaveH indicate RX logic 1 waveform

CIR – Waveform Logic 0 Data Register – Index 2306h

Bit	Name	R/W	Reset	Default	Description
7-0	WaveL	R/W	5VSB	80h	The registers of WaveL indicate RX logic 0 count number

CIR – Waveform Logic 1 Count Register – Index 2307h

Bit	Name	R/W	Reset	Default	Description
7-0	WaveH_Count	R/W	5VSB	04h	The registers of WaveH_Count indicate RX logic 1 count number

CIR – Waveform Logic 0 Count Register – Index 2308h

Bit	Name	R/W	Reset	Default	Description
7-0	WaveL_Count	R/W	5VSB	02h	The registers of WaveL_Count indicate RX logic 0 count number

CIR – Rx Protocol Register – Index 2309h

Bit	Name	R/W	Reset	Default	Description
7	Low_Frequency	R/W	5VSB	1b	Write 1 to indicate RX carry frequency from 20k to 100k, and write 0 to indicate RX carry frequency from 400k to 500k.
6-5	Reserved	-	-	0h	Reserved
4	RXINV	R/W	5VSB	1b	Write 1 to indicate invert RX input, or to indicate by pass RX.
3	Bypass	R/W	5VSB	1b	Write 1 to indicate RX input is demodulation , or to indicate RX is un-demodulation.
2-0	Protocol	R/W	5VSB	1h	000 : ITT 001 : NEC 010 : NOKIA 011 : SHARP 100 : SONY 101 : PHILIPS RC5

7.20.16 Debug Port µC Side Register (Base Address 0x3200, 256 bytes)

These registers are accessed by the host debug port interface, µC can't access these register.

Debug Port Control Register — Offset 00h

Bit	Name	R/W	Reset	Default	Description
7	SOFT_RST	W	5VSB	0	Debug Port asserts a software reset to µC.
6-4	Reserved	-	-	-	Reserved
3	DBPORT_EXIT_RST_EN	R/W	5VSB	0	Set "!" to enable reset µC after exit debug mode.
2	DBPORT_STEP	W	5VSB	0	Write "1" to trigger a single step.
1	DBPORT_NEXT_BRK	W	5VSB	0	Write "1" to force µC run to next break point.
0	DBPORT_FREE_RUN	R/W	5VSB	0	0: µC will stop when entering into the debug mode. 1: µC is free run.

Break Point Select Register — Offset 01h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved
1-0	BRK_PTR_SEL	R/W	-5VSB	00h	00: Select break point 0 to access. 01: Select break point 1 to access. 10: Select break point 2 to access. 11: Select break point 3 to access.

Break Point Low Register — Offset 02h

Bit	Name	R/W	Reset	Default	Description
7-0	BRK_PTR_LO	R/W	5VSB	00h	The low byte address of break point.

Break Point High Register — Offset 03h

Bit	Name	R/W	Reset	Default	Description
7-0	BRK_PTR_HI	R/W	5VSB	00h	The high byte address of break point.

Break Point Enable Register — Offset + 05h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	BRK_PTR3_EN	R/W	5VSB	0	Set “1” to enable break point 3. µC will stop when program counter match the programmed break points.
2	BRK_PTR2_EN	R/W	5VSB	0	Set “1” to enable break point 2. µC will stop when program counter match the programmed break points.
1	BRK_PTR1_EN	R/W	5VSB	0	Set “1” to enable break point 1. µC will stop when program counter match the programmed break points.
0	BRK_PTR0_EN	R/W	5VSB	0	Set “1” to enable break point 0. µC will stop when program counter match the programmed break points.

Debug Port Status Register — Offset + 06h

Bit	Name	R/W	Reset	Default	Description
7	DBPORT_ENTRY	R	5VSB	-	This bit will set “1” when enter debug mode.
6	DBPORT_STOP_µC	R	5VSB	-	This bit will set “1” when µC stops.
5-3	Reserved	-	-	-	Reserved
2	DBPORT_STEP_STS	R/W	5VSB	0	This bit will set after a single step operation. Write “1” to clear.
1	DBPORT_BRK_STS	R/W	5VSB	0	This bit will set when a break point matches. Write “1” to clear.
0	Reserved	-	-	-	Reserved

Debug Port Interrupt Enable Register — Offset + 07h

Bit	Name	R/W	Reset	Default	Description
7	DBPORT_TEST_MODE	R/W	5VSB	0	Write “1” to enable Fintek test mode.
6-3	Reserved	-	-	-	Reserved
2	DBPORT_STEP_INT_EN	R/W	5VSB	0	0: Disable single step interrupt. 1: Enable single step interrupt.
1	DBPORT_BRK_INT_EN	R/W	5VSB	0	0: Disalbe break point match interrupt. 1: Enable break point match interrupt. BRK_PTR_TRIG will be set when single step is end and DBPORT_STEP_INT_EN is set. Or DBPORT_BRK_INT_EN is set and a break point matches.
0	Reserved	-	-	-	Reserved

Debug Port Program Count Low Register — Offset + 0Ah

Bit	Name	R/W	Reset	Default	Description
7-0	PC_LO	R/W	5VSB	0	For write, this is the low byte of program counter written to µC. It returns the current program counter low byte of µC when read.

Debug Port Program Count High Register — Offset + 0Ah

Bit	Name	R/W	Reset	Default	Description
7-0	PC_HI	R/W	5VSB	0	For write, this is the high byte of program counter written to µC. It returns the current program counter high byte of µC when read. The PC_HI and PC_LO will write to µC's program counter after writing this byte.

Debug Port Entry Data Register — Offset + 0Fh

Bit	Name	R/W	Reset	Default	Description
7-0	ENTRY_DATA	R/W	5VSB	0	To enter or exit debug mode, a sequence of data is needed to write to this byte. To enter the debug mode, the sequence is 0x19, 0x34, x010, 0x03. To exit the debug mode, the sequence is 0x30, 0x01, 0x43, 0x91.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	-40 to +85 (F81867-I) 0 to +70 (F81867)	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

8.2 DC Characteristics

(T_A = 70° C, 3VCC = 3.3V ± 10%, GND = 0V)

Parameter	Conditions	MIN	TYP	MAX	Unit
Temperature Error, Remote Diode	60 °C < T_D < 100 °C, 3VCC = 3.0V to 3.6V 0 °C <T_D < 60°C 100 °C <T_D < 127°C		± 1 ± 2	± 3 ± 5	°C
3VCC Voltage range		3.0	3.3	3.6	V
5VSB Voltage range		4.5	5.0	5.5	V
3VSB Voltage range		3.0	3.3	3.6	V
VBAT Voltage range		2.4	3.0	3.6	V
3VCC average operating current			20		mA
5VSB average operating current			10		mA
5VSB standby current			3		mA
3VSB average operating current			3		mA
3VSB standby current			1		mA
VBAT standby current			1		uA
Resolution			1		°C
3VCC Power on reset threshold			2.6	3.0	V
5VSB Power on reset threshold			4.3	4.5	V
3VSB Power on reset threshold			2.6	3.0	V
Diode source current	High Level		95		uA
	Low Level		10		uA

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{st}-TTL level input pin with schmitt trigger.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$IN_{st,\ lv}$-Low volgate, TTL level input pin with schmitt trigger.						
Input Low Voltage	VIL			0.4	V	
Input High Voltage	VIH	1.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$IN_{t,5V}$-TTL level input pin, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	

Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$IN_{st,5V}$-TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$IN_{t,\ u47,\ 5V}$-TTL level input pin, pull up 47kΩ, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
O_8-Output pin with 8 mA sink/source capability.						
Output High Current	IOL		-8		mA	VOH = 2.4V
Output Low Current	IOL		+8		mA	VOL = 0.4V
O_{12} -Output pin with 12 mA sink/source capability.						
Output High Current	IOL		-12		mA	VOH = 2.4V
Output Low Current	IOL		+12		mA	VOL = 0.4V
O_{14} -Output pin with 14 mA sink/source capability.						
Output High Current	IOL		-14		mA	VOH = 2.4V
Output Low Current	IOL		+14		mA	VOL = 0.4V
O_{16} -Output pin with 16 mA sink/source capability.						
Output High Current	IOL		-16		mA	VOH = 2.4V
Output Low Current	IOL		+16		mA	VOL = 0.4V
$OD_{14,5v}$-Open drain output pin with 14 mA sink capability, 5V tolerance.						
Output Low Current	IOL		+14		mA	VOL = 0.4V
$OD_{16,u10}$-Open drain output pin with 16 mA sink capability, internal 10KΩ pull-up.						
Output Low Current	IOL		+16		mA	VOL = 0.4V
$OD_{12,5V}$-Open drain output pin with 12 mA sink capability 5V tolerance.						
Output Low Current	IOL		+12		mA	VOL = 0.4V
$OD_{24t,5v}$-Open drain output pin with 24 mA sink capability, 5V tolerance.						
Output Low Current	IOL		+24		mA	VOL = 0.4V
$OOD_{12,\ 5v}$- Open drain or push pull by the register, with 12 mA sink/source capability, 5V tolerance.						
Output High Current	IOL		-12		mA	VOH = 0.4V
Output Low Current	IOL		+12		mA	VOL = 0.4V
$I/O_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, with 12 mA sink/source capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-12		mA	VOH = 2.4V
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/O_{8st,\ 5v}$-TTL level bi-directional pin with schmitt trigger, with 8 mA sink/source capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-8		mA	VOH = 2.4V
Output Low Current	IOL		+8		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{12st,\ 5v}$-TTL level bi-directional pin with schmitt trigger, output with 12 mA sink/source capability or open drain with 12mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	

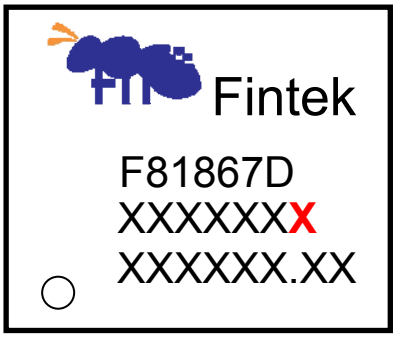
Output High Current	IOL		-12		mA	VOH = 2.4V
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD$_{14st, 5v}$-TTL level bi-directional pin with schmitt trigger, output with 14 mA sink/source capability or open drain with 14mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-14		mA	VOH = 2.4V
Output Low Current	IOL		+14		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD$_{8st, 5v}$ -TTL level bi-directional pin with schmitt trigger, output with 8 mA sink/source capability or open drain with 8mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-8		mA	VOH = 2.4V
Output Low Current	IOL		+8		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OD$_{16st,5v}$-TTL level bi-directional pin with schmitt trigger, open drain output with16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OD$_{12st, 5v}$- TTL level bi-directional pin with schmitt trigger, open drain output with 12mA source-sink capability, 5V tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	
Input High Threshold Voltage	Vt+	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/O$_{16st}$- TTL level bi-directional pin and schmitt trigger, 16 mA sink capability.						
Input Low Threshold Voltage	Vt-			0.8	V	
Input High Threshold Voltage	Vt+	2.0			V	
Output High Current	IOH		-16		mA	VOH = 2.4V
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V

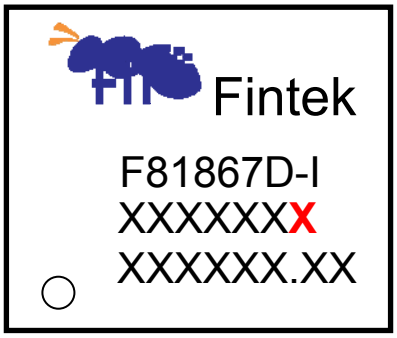
9. Ordering Information

Part Number	Package Type	Production Flow
F81867D-I	128-LQFP Green Package	Industrial, -40°C to +85°C
F81867D	128-LQFP Green Package	Commercial, 0°C to +70°C

10. Top Marking Specification

The version identification is shown as the bold red characters. Please refer to below for detail:





1st Line: Fintek Logo

2nd Line: **F81867D/F81867D-I** where D means the package code & -I means industrial spec.

3rd Line: Assembly Plant Code (X) + Assembled Year Code (X) + Week Code (XX) + Fintek Internal Code (XX) + **IC Version (X)** where A means version A, B means version B, …

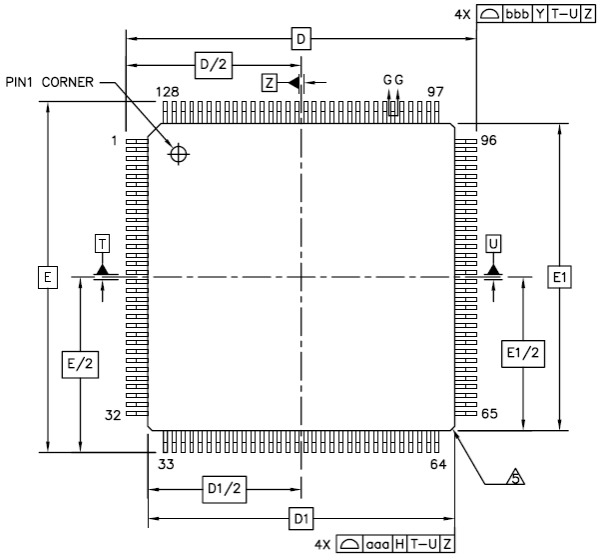
4th Line: Wafer Fab Code (XXXX…XX)

◯ : Pin 1 Identifier

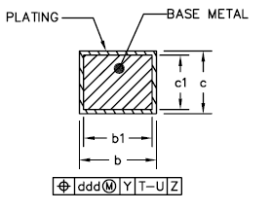
11. Package Dimensions

128 LQFP (14*14)

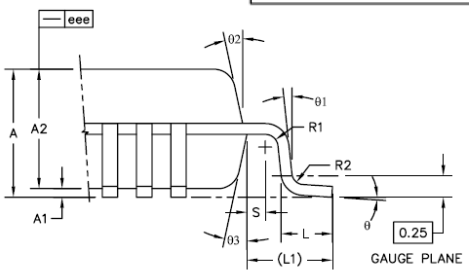
Unit: mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



SECTION G–G
SCALE: 100/1



DETAIL F
SCALE: 20/1

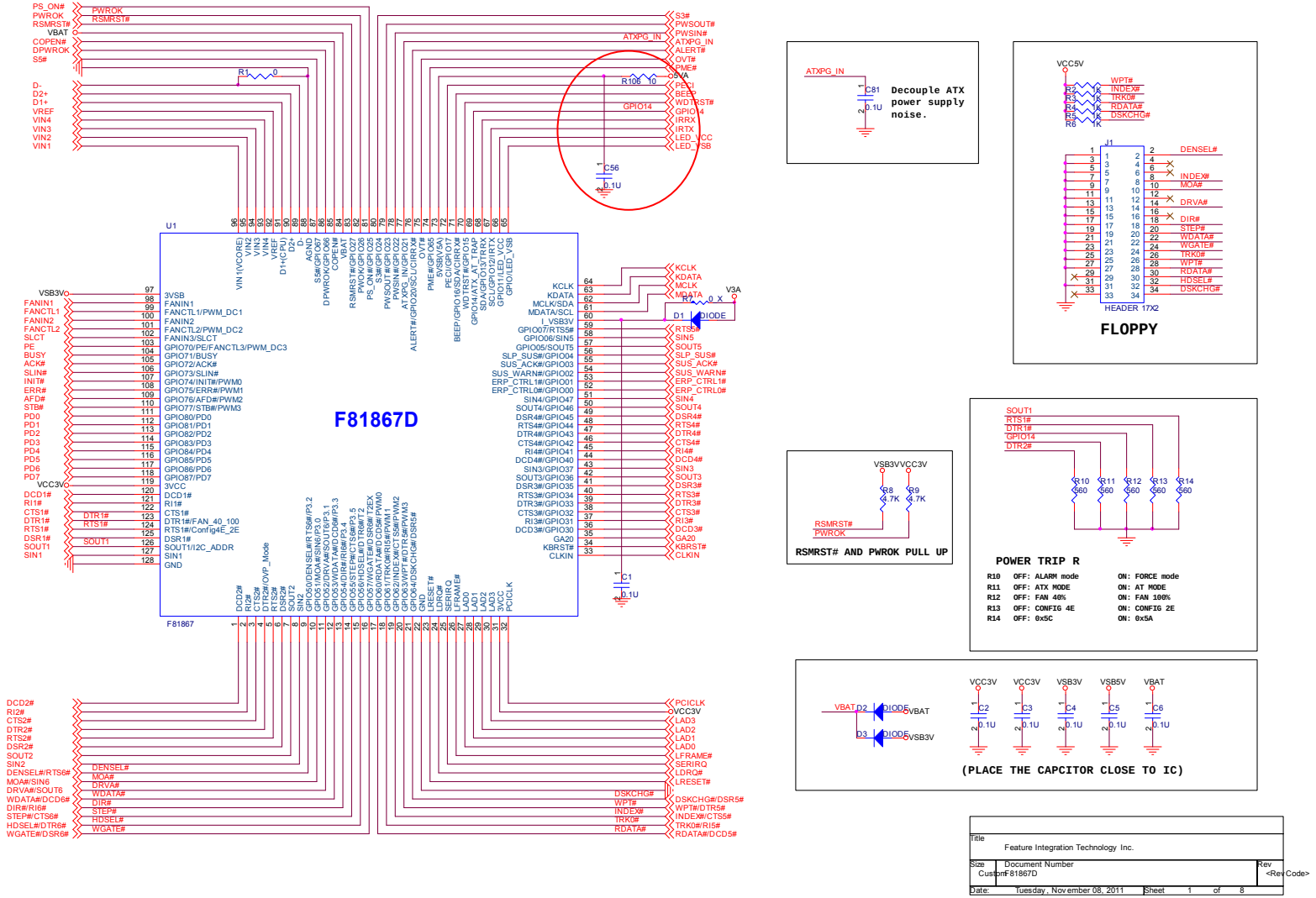
NOTES:
1. JEDEC NO. : N/A.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

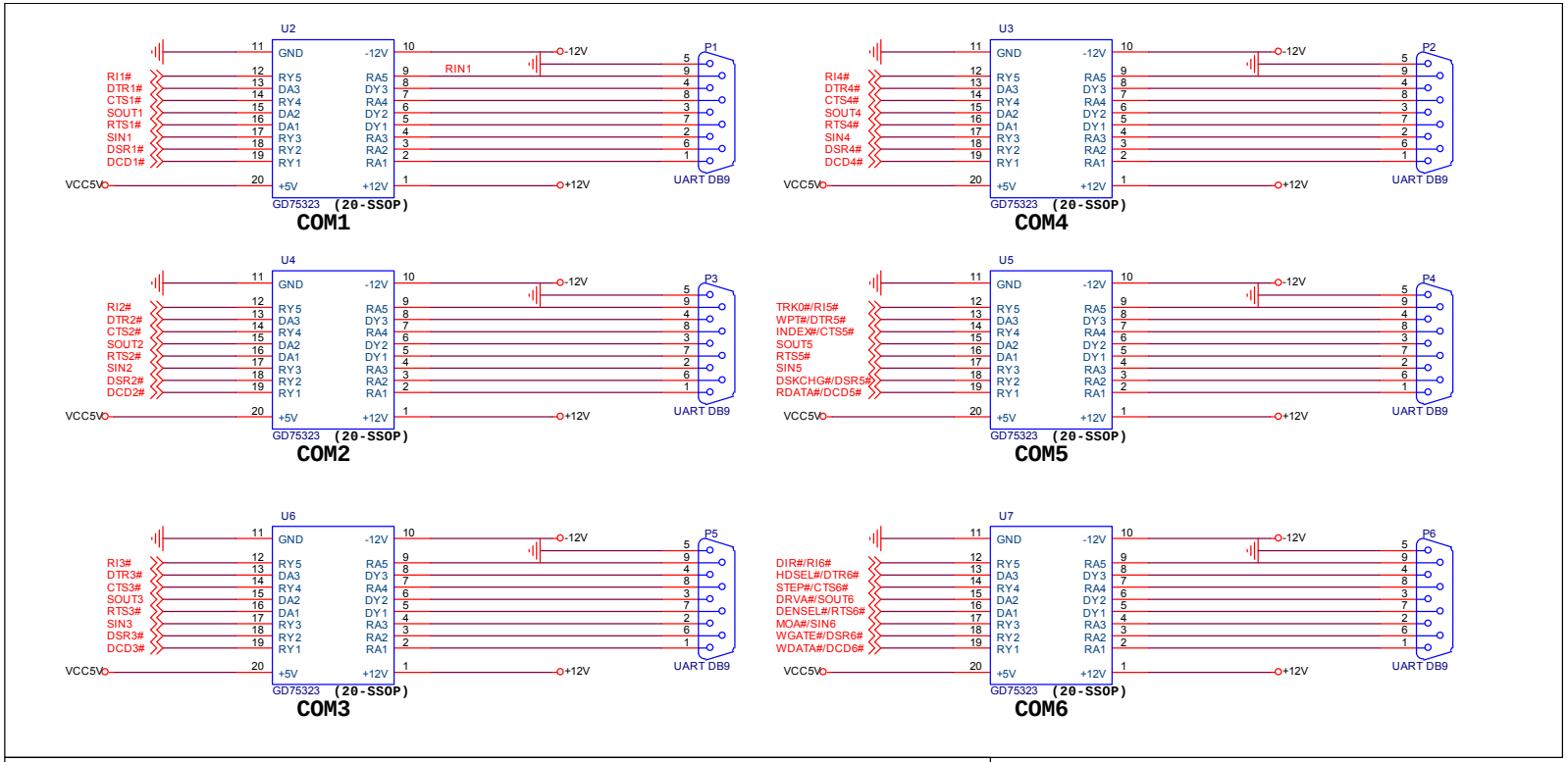
Feature Integration Technology Inc.

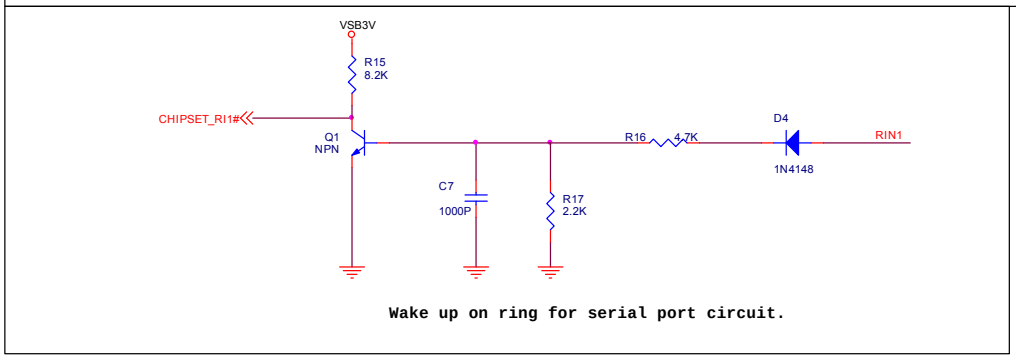
Headquarters
3F-7, No 36, Tai Yuan St.,
Chupei City, Hsinchu, Taiwan 302, R.O.C.
TEL : 886-3-5600168
FAX : 886-3-5600166
www: http://www.fintek.com.tw

Taipei Office
Bldg. K4, 7F, No.700, Chung Cheng Rd.,
Chungho City, Taipei, Taiwan 235, R.O.C.
TEL : 866-2-8227-8027
FAX : 866-2-8227-8037

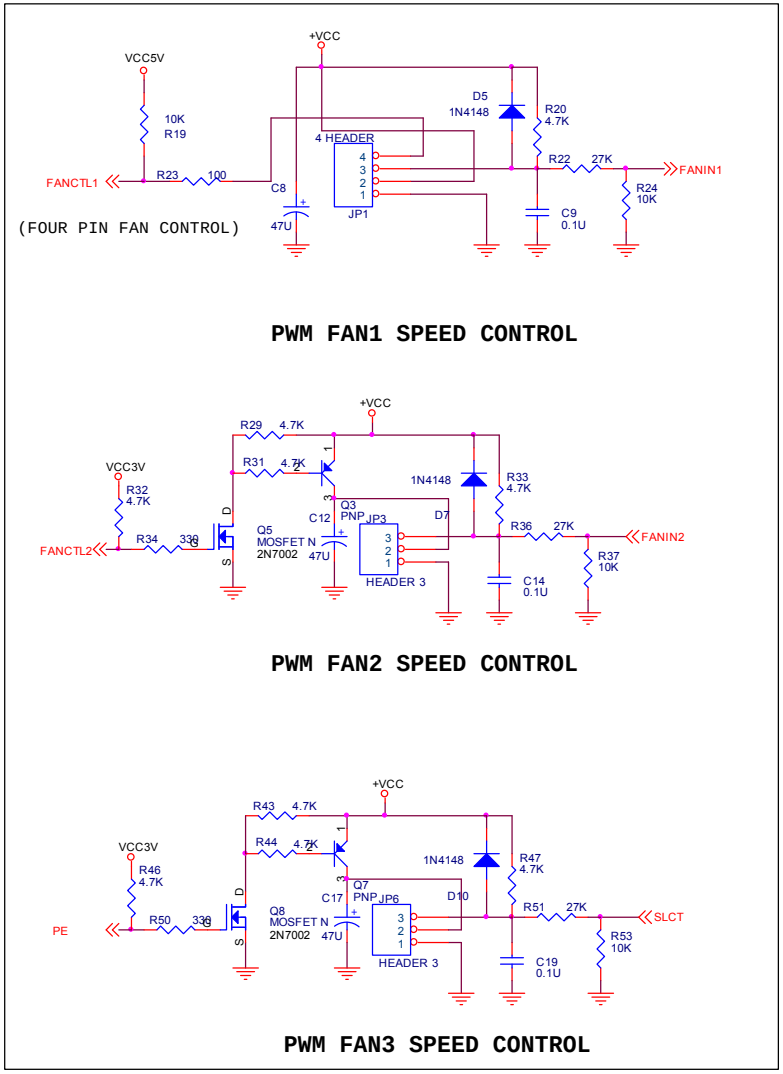
12.Application Circuit

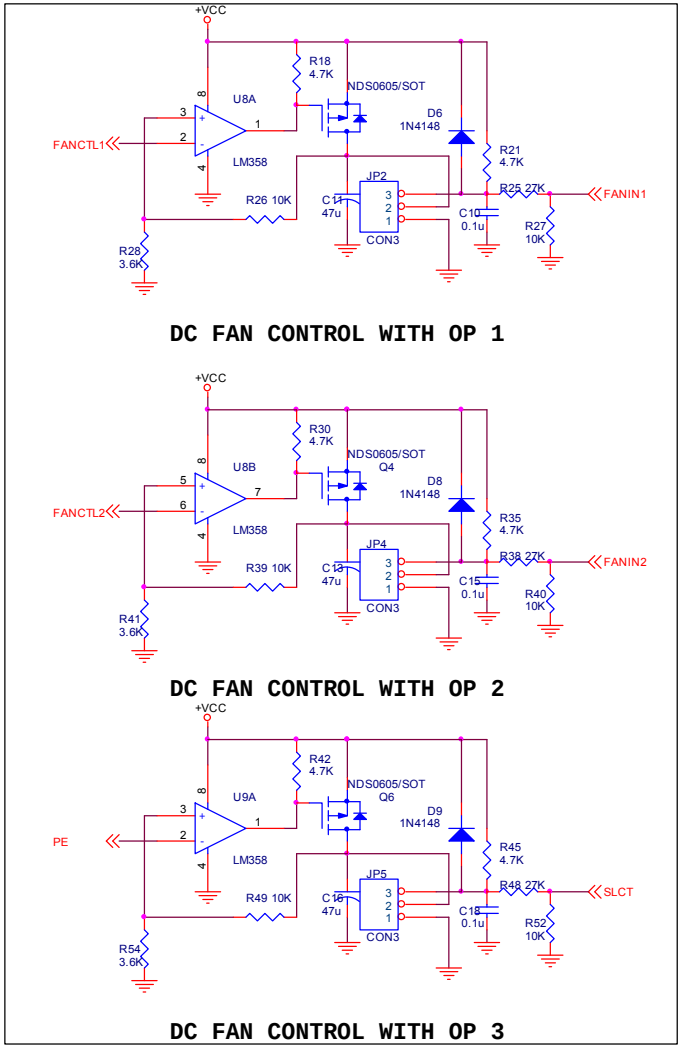






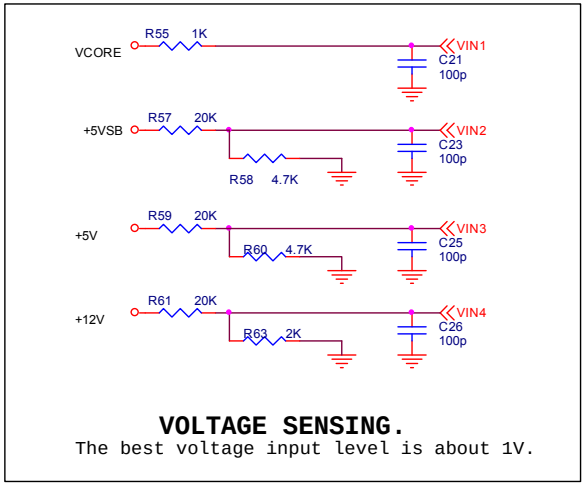
Title	Feature Integration Technology Inc.	
Size B	Document Number F81867	Rev <RevCode>
Date: Thursday, June 23, 2011	Sheet 2 of 8	



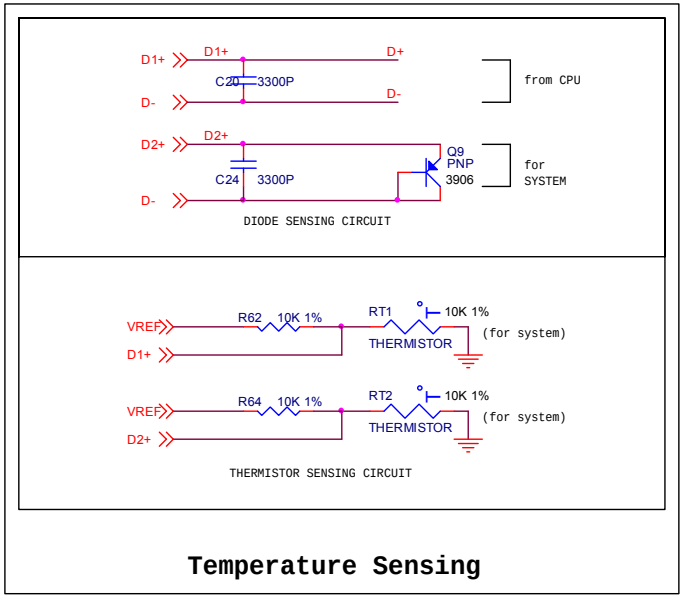


FAN CONTROL FOR PWM OR DC

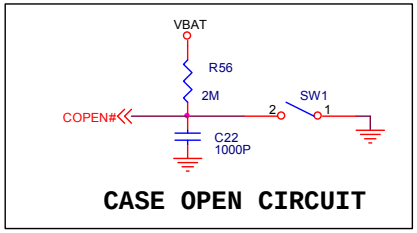
Title: Feature Integration Technology Inc.			
Size: B	Document Number: F81867		Rev: <Rev Code>
Date: Thursday, June 23, 2011	Sheet 3 of 8		



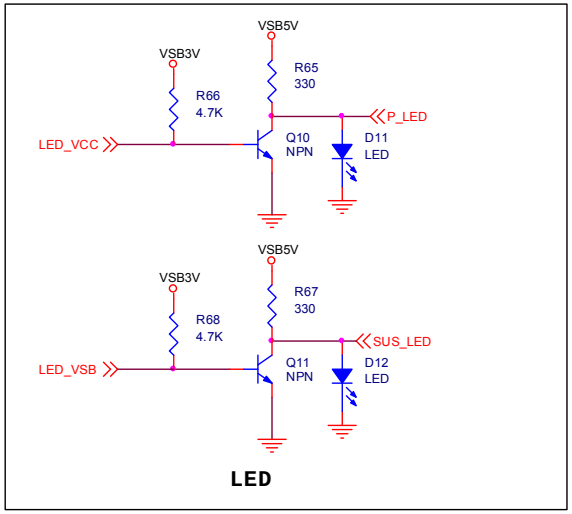
VOLTAGE SENSING.
The best voltage input level is about 1V.



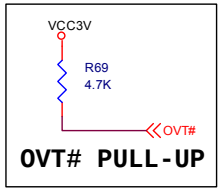
Temperature Sensing



CASE OPEN CIRCUIT

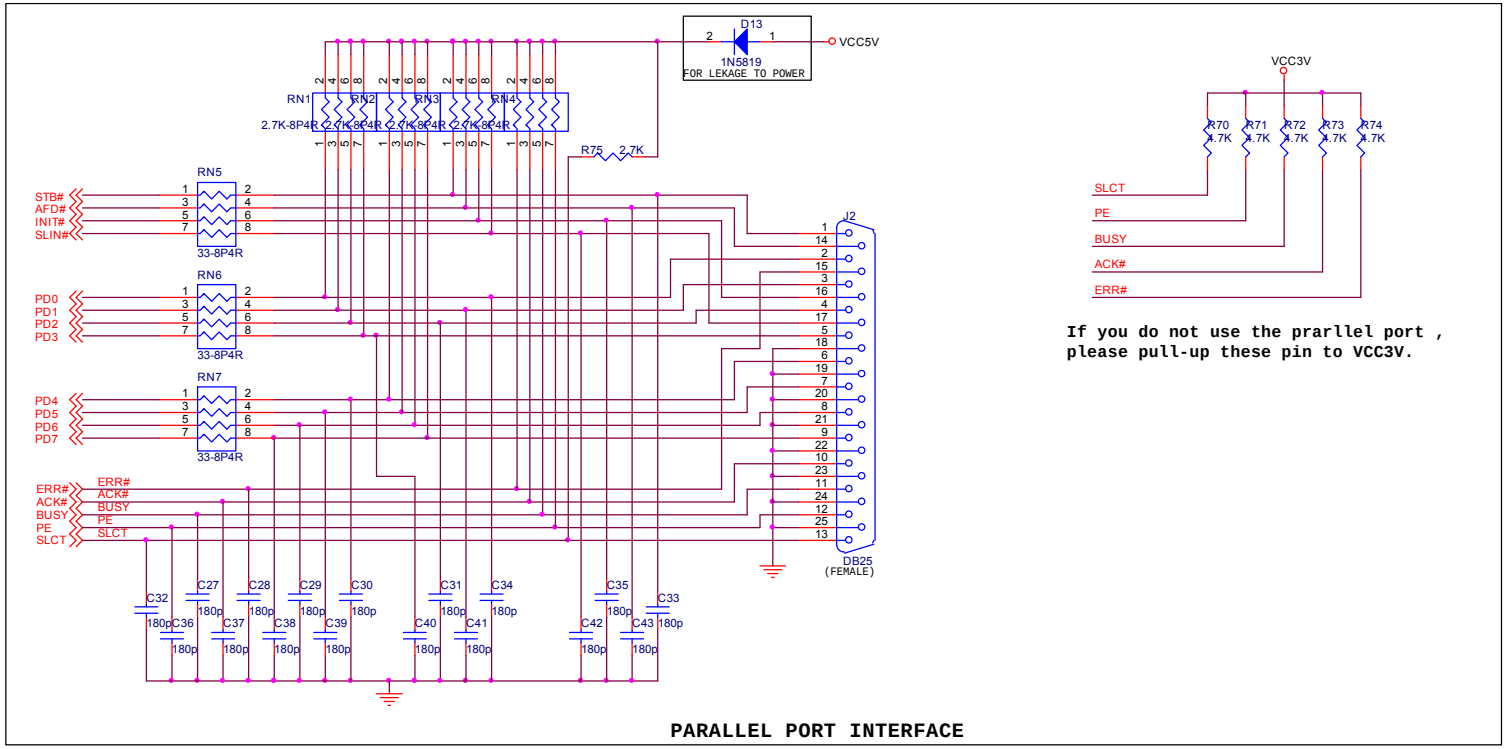


LED



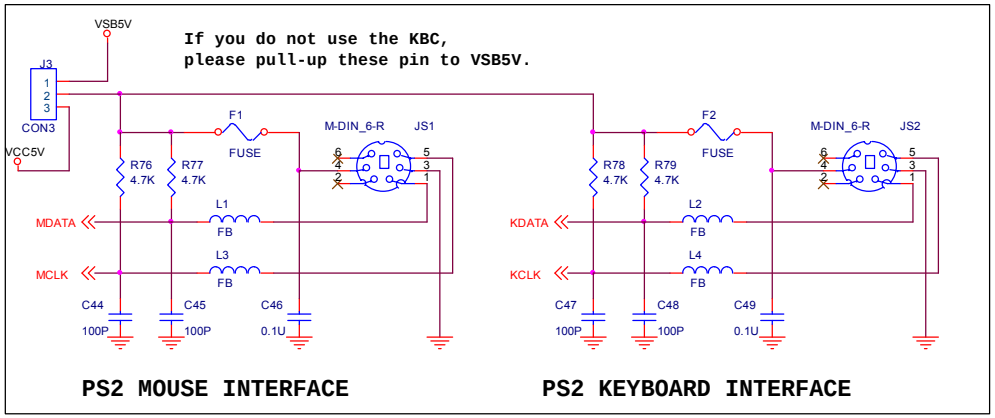
OVT# PULL-UP

Title	Feature Integration Technology Inc.	
Size B	Document Number F81867	Rev <Rev Cod
Date: Thursday, June 23, 2011	Sheet 4 of 8	



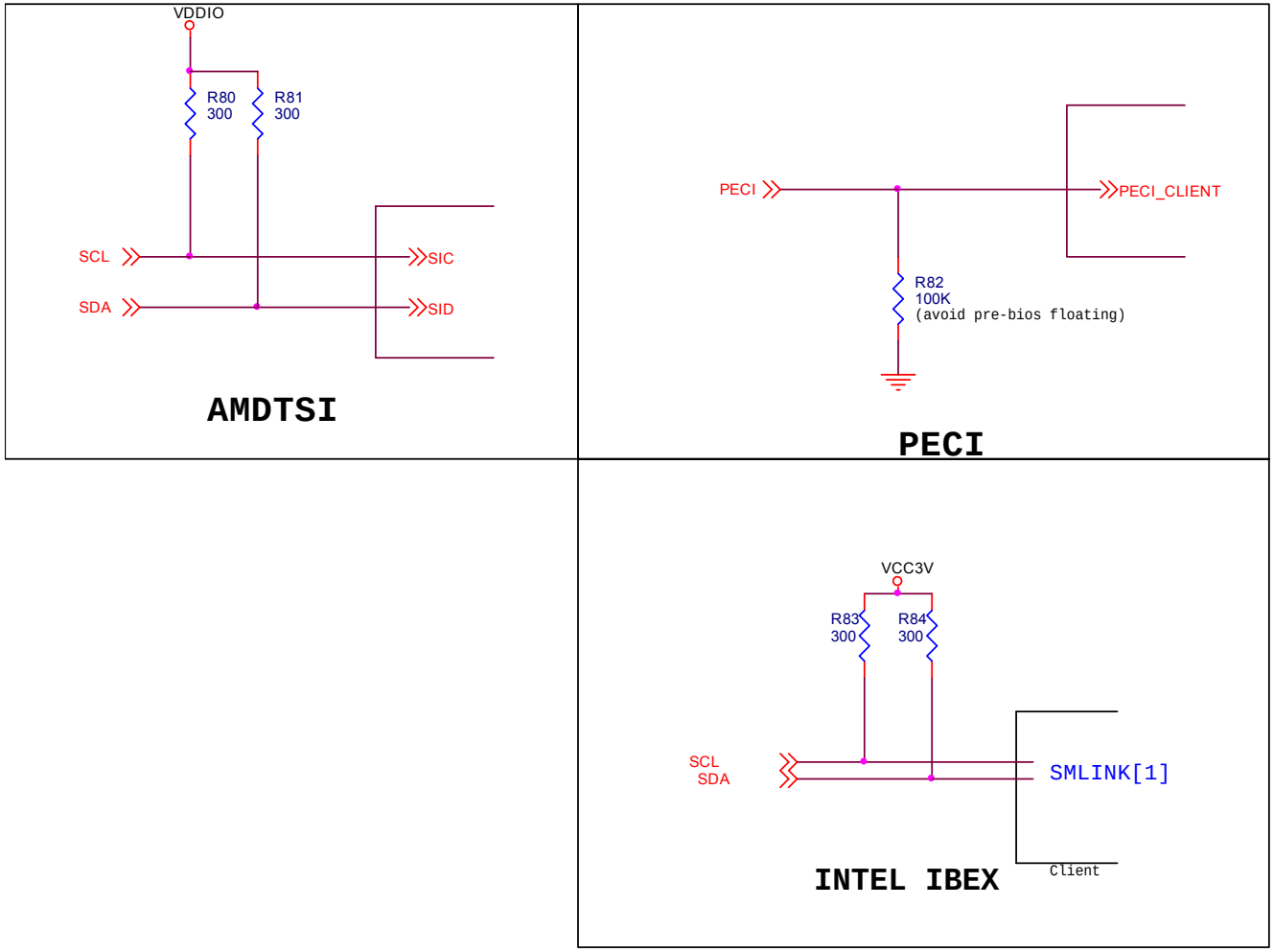
If you do not use the prarllel port , please pull-up these pin to VCC3V.

PARALLEL PORT INTERFACE

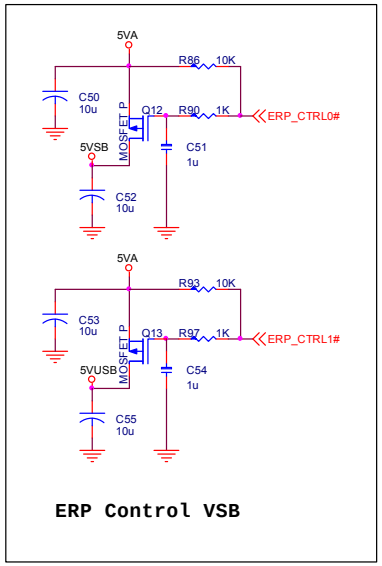


PS2 MOUSE INTERFACE **PS2 KEYBOARD INTERFACE**

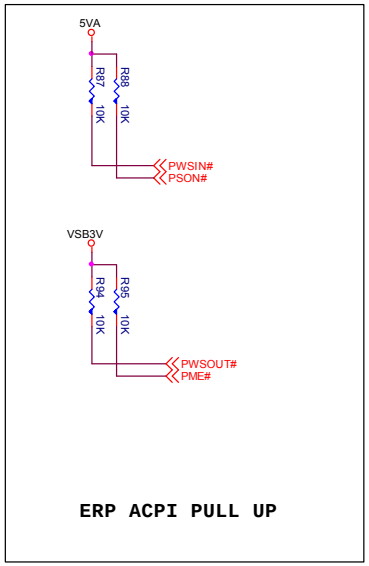
Title	Feature Integration Technology Inc.		
Size B	Document Number F81867		Rev <Rev Code>
Date: Thursday , June 23, 2011		Sheet 5 of 8	



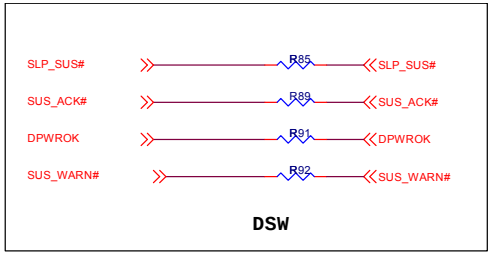
Title: Feature Integration Technology Inc.			
Size: A	Document Number: F81867		Rev: <Rev Code>
Date: Thursday, June 23, 2011	Sheet 6 of 8		



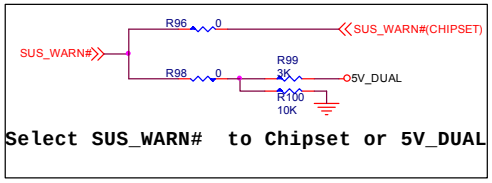
ERP Control VSB



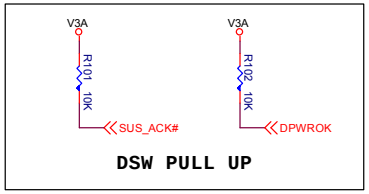
ERP ACPI PULL UP



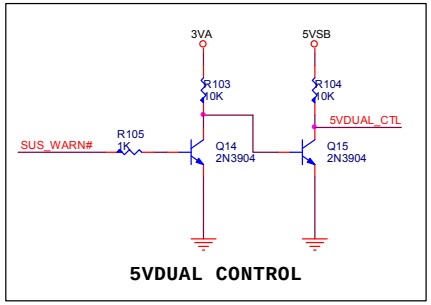
DSW



Select SUS_WARN# to Chipset or 5V_DUAL



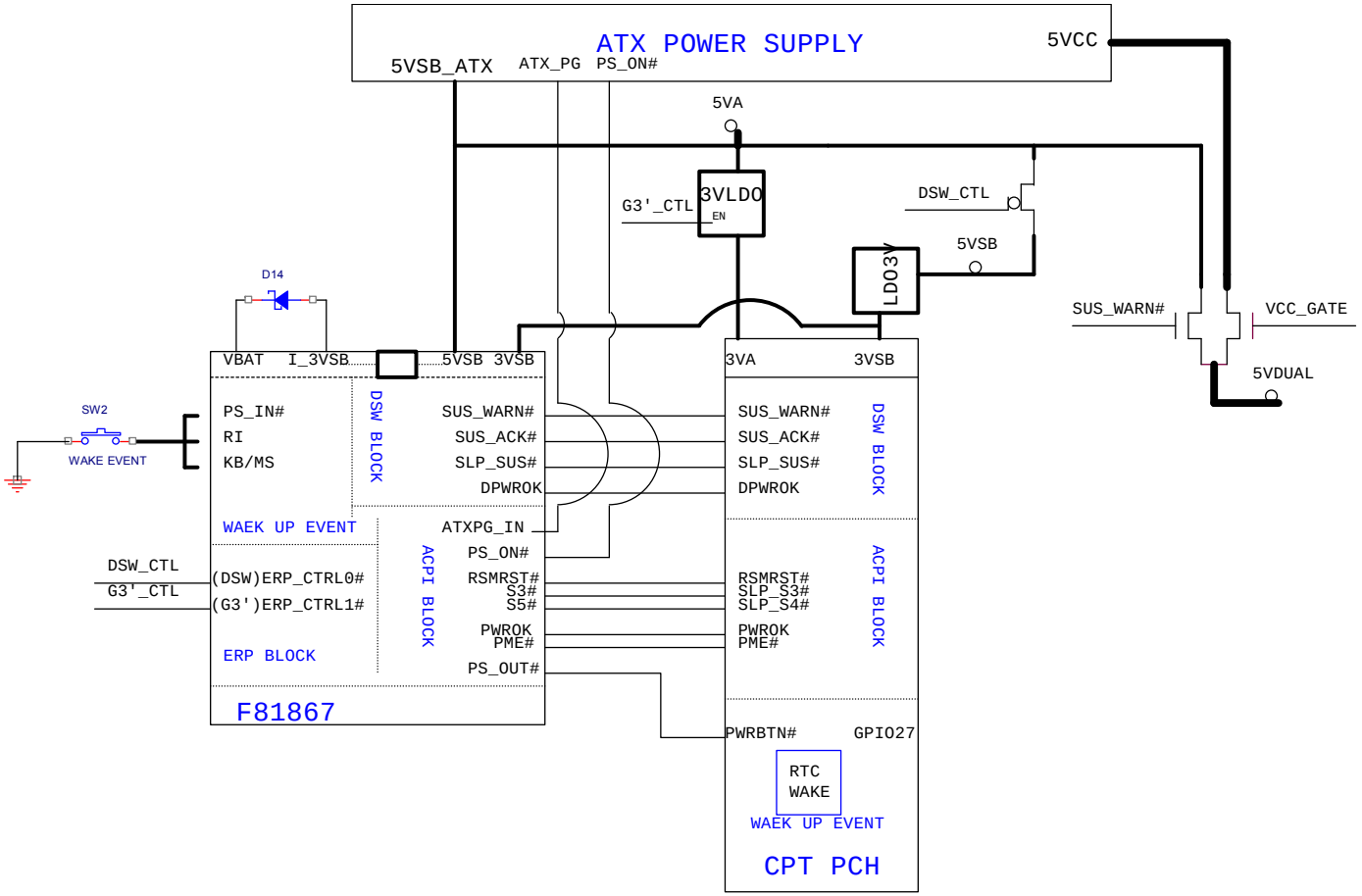
DSW PULL UP



5VDUAL CONTROL

Title	Feature Integration Technology Inc.	
Size B	Document Number F81867	Rev <Rev Code>
Date: Thursday, June 23, 2011	Sheet 7 of 8	

DSW + Fintek G3' Mode



Title	Feature Integration Technology Inc.		
Size B	Document Number F81866		Rev <Rev Code>
Date: Thursday, June 23, 2011	Sheet 8 of 8		

Fintek G3' (ERP) Mode