

CMOS 8–Bit Microcontrollers

TMP90PH44N/TMP90PH44F

1. Outline and Characteristics

The TMP90PH44 is a system evaluation LSI having a built-in One-Time PROM for (16K byte) for TMP90C844.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly the same as the TMP90C844 by programming to the internal PROM.

The different points between TMP90PH44 and TMP90C844 are the memory size (ROM/RAM).

The TMP90PH44N is in a Shrink Dual Inline Package. (SDIP64-P-750)

The TMP90PH44F is in a Quad Flat Package. (QFP64-P-1420A)

The following are the memory map of TMP90PH44 and TMP90C844.

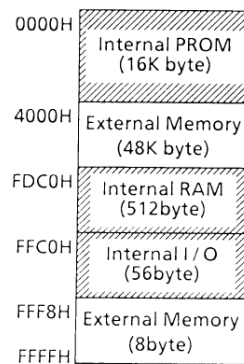


Figure 1.1. TMP90PH44

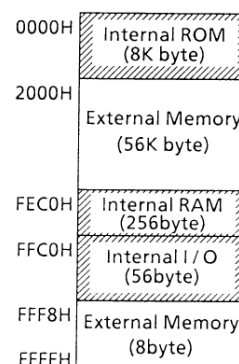


Figure 1.2. TMP90C844

Parts No.	ROM	RAM	Package	Adapter Socket No.
TMP90PH44N	OTP 16384 x 8bit	512 x 8bit	64-SDIP	BM1148 (Under Development)
TMP90PH44F			64-QFP	BM1149 (Under Development)

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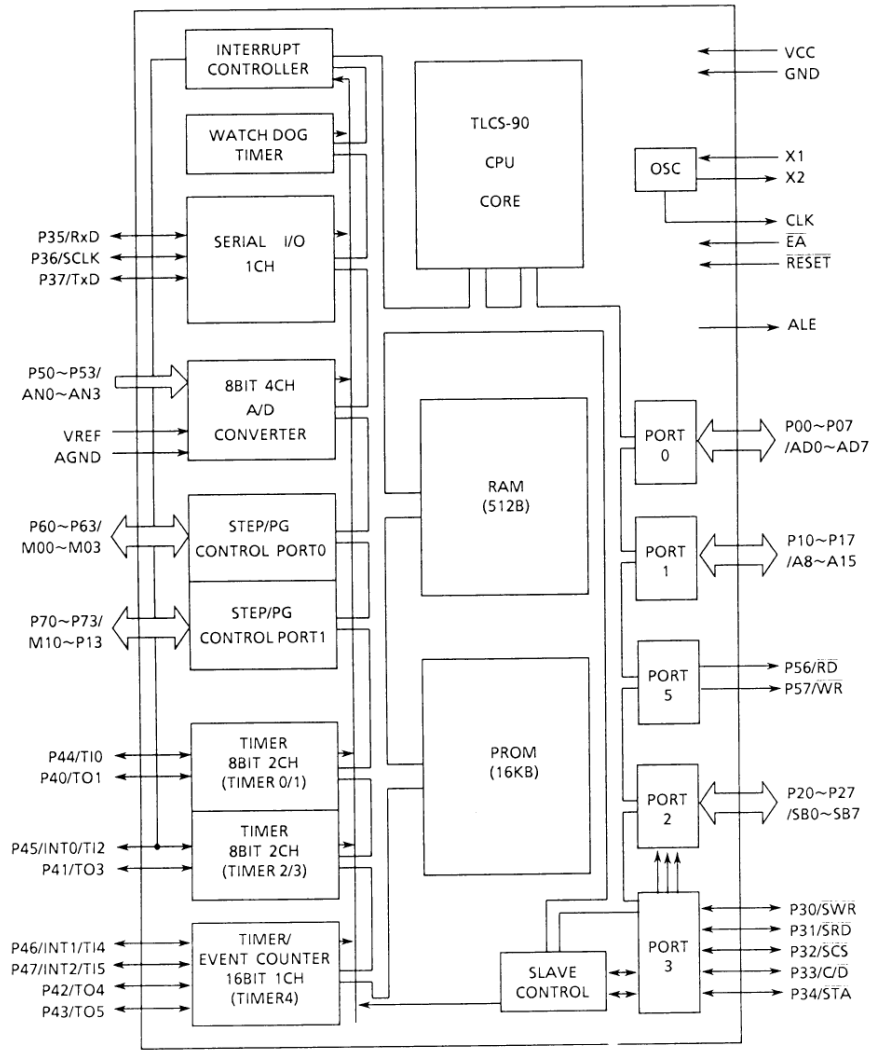


Figure 1. 3. TMP90PH44 Block Diagram

2. Pin Assignment and Functions

The TMP90PH44 pin assignment input/output pins name and functions are shown below.

2.1 Pin Assignment Diagram

The TMP90PH44N pin assignment are shown in Figure 2.1 (1).

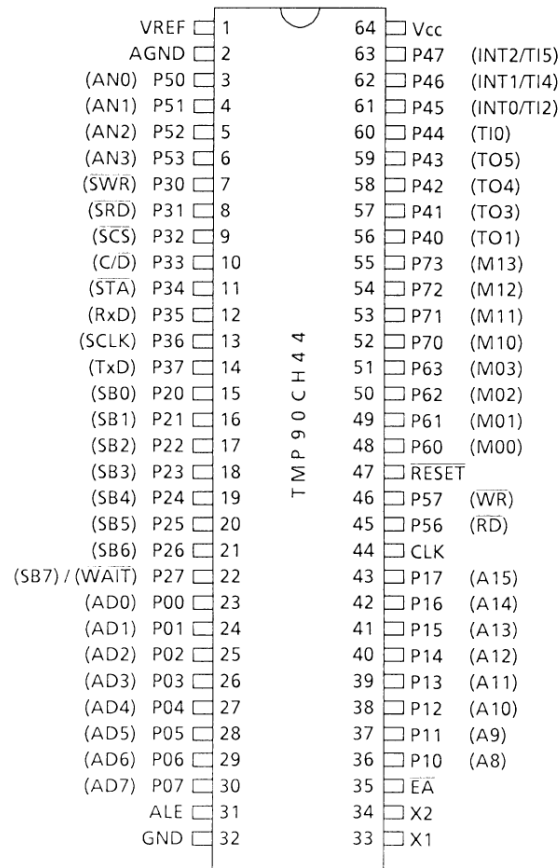


Figure 2.1 (1). Pin Assignment (Shrink DIP)

TMP90PH44

The TMP90PH44F pin assignment are shown in Figure 2.1 (2).

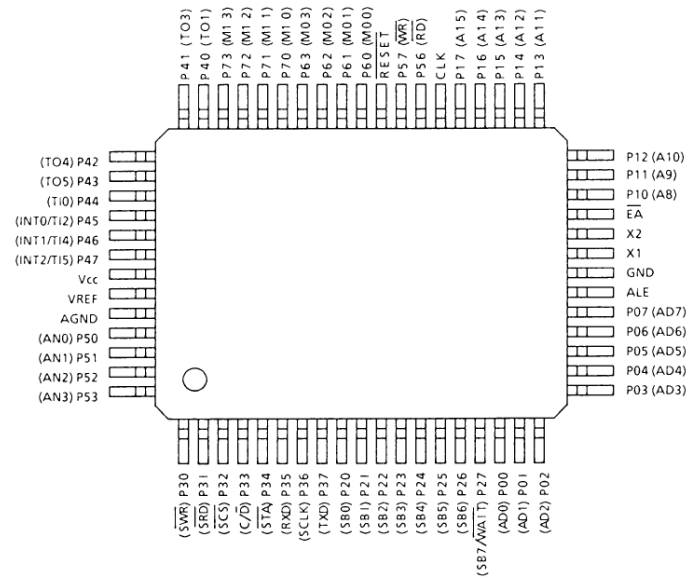


Figure 2.1 (2). Pin Assignment (Flat Package)

2.2 Pin Names and Functions

The TMP90PH44 has MCU mode and PROM mode.

- (1) MCU Mode (The TMP90C844 and the TMP90PH44 are pin compatible).

Table 2.2 Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O or tristate	Function
P00 ~ P07 /AD0 ~ AD7	8	I/O	Port 0: An 8-bit I/O port. Each bit can be set for input or output.
		/Tristate	Address/Data bus: Operates as an 8-bit bidirectional address bus or data bus when using external memory
P10 ~ P17 /A8 ~ A15	8	I/O	Port 1: An 8-bit I/O port. Each bit can be set for input or output.
		Output	Address bus: Operates as an address bus (upper 8 bits) when using external memory.
P20 ~ P27 /SB0 ~ SB7 /WAIT	8	I/O	Port 2: An 8-bit I/O port. Each bit can be set for input or output.
	(8)		Slave bus: When used as a slave processor, operates as the slave bus for the transfer data to and from the master processor.
	(1)		Wait: Used as an input pin when memory or peripheral LSIs with slow access times are controlled.
P30 ~ P37 /SWR /SRD /SCS C/ \bar{D} /STA RxD /SCLK /TxD	8	I/O	Port 3: 8-bit I/O port which allows I/O selection on bit basis (with programmable pull-up resistor).
	(1)	/Input	Slave write: The strobe signal input to write data from the master processor.
	(1)	/Input	Slave read: The strobe signal used by the master processor to read data.
	(1)	/Input	Slave chip select: The chip select signal input from the master processor.
	(1)	Input	Command/data: The command/data select signal input from the master processor.
	(1)	/Output	Status output: Used to report the slave bus status to the master processor.
	(1)	Input	Serial receive data
	(1)	/I/O	Serial clock
	(1)	/Output	Serial transmit data
	P40 ~ P47 /TO1, 3, 4, 5 /TI0, 2, 4, 5 /INT0 /INT1 INT2	8	I/O
(4)		/Output	Timer outputs 1, 3, 4, and 5: Output for timer 0, or timer 1, timer 2, timer 3 and timer 4 (2 lines).
(4)		/Input	Timer inputs 0, 2, 4, and 5: Input for timer 0, or timer 1, timer 2 and timer 4 (2 lines).
(1)		/Input	Interrupt request terminal 0: Interrupt request pin 0: Level/rise edge programmable interrupt request pin
(1)		/Input	Interrupt request terminal 1: Interrupt request pin 1: Rise/fall edge programmable interrupt request pin.
(1)		/Input	Interrupt request terminal 2: Interrupt request pin 2: Rise edge interrupt request pin.
P50 ~ P53 /AN0 ~ AN3		4	Input
	Analog input: 4 analog inputs to A/D converter.		
P56 /RD	1	Output	Port 56: A 1-bit output port.
			Read: Strobe signal output for reading external memory.

Table 2.2 Pin Names and Functions (2/2)

Pin name	No. of pins	I/O or tristate	Function
P57 /WR	1	Output	Port 57: A 1-bit output port. Write: Strobe signal output for writing external memory.
P60 ~ P63 /M00 ~ M03	4	I/O /Output	Port 6: 4-bit I/O port which allows I/O selection on bit basis. Stepping motor control port 0 or pattern generation port 0.
P70 ~ P73 /M10 ~ M13	4	I/O Output	Port 7: 4-bit I/O port which allows I/O selection on bit basis. Stepping motor control port 0 or pattern generation port 1.
ALE	1	Output	Address latch enable
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is pulled up internally during resetting.
\overline{EA}	1	Input	External access: Connects with V _{CC} pin in the TMP90PH44 built ROM is used.
\overline{RESET}	1	Input	Reset: Initializes the TMP90PH44. (pull-up resistance is built-in).
X1, X2	2	I/O	Crystal oscillator connection pin
VREF	1	–	Input of reference voltage to A/D converter
AGND	1	–	GND pin for A/D converter
V _{CC}	1	–	Power supply (+5V +/- 10%)
GND	1	–	GND pin (0V)

(2) PROM Mode

Table 2.3

Pin Function Name	No. of pins	I/O	Function	Pin Name (MCU mode)
A7 ~ A0	8	Input	Program Memory Address Input	P73 ~ P70 P63 ~ P60
A13 ~ A8	6	Input		P15 ~ P10
A14 A15	2	Input		P16 P17
D7 ~ D0	8	I/O	Data Input/Output	P07 ~ P00
\overline{OE}	1	Input	Output Enable Input	P26
\overline{CE}	1	Input	Chip Enable Input	P27
VPP	1	Power Supply	12.5V/5V (Programming Power Supply)	\overline{EA}
VCC	1	Power Supply	5V	VCC
VSS	1	Power Supply	0V	VSS
Pin Name	No. of pins	I/O	Pin Setting	
P20 ~ P27	8	Input	Be fixed to "L" level.	
P40 ~ P44	5	Input	Be fixed to "L or H" level.	
P45, P46	2	Input	Be fixed to "H" level.	
P47	1	Input	Be fixed to "L or H" level.	
P50 ~ P53 P30 ~ P37	4 8	Input	Be fixed to "L or H" level.	
VREF	1	–	Be fixed to "L" level.	
AGND	1	–	Be fixed to "L" level.	
\overline{RESET}	1	Input	Be fixed to "L" level.	
CLK	1	Input	Be fixed to "L" level.	
ALE	1	Output	Open	
X1 X2	1 1	Input Output	Resonator connection pin	

3. Operation

The TMP90PH44 is the OTP version of the TMP90C844 that is replaced an internal ROM from Mask ROM to EPROM.

The function of TMP90PH44 is exactly the same as that of TMP90C844 except the internal ROM/RAM size.

Refer to the TMP90C844 except the functions which are not described this section.

The following is an explanation of the hardware configuration and operation in the relation to the TMP90PH44.

The TMP90PH44 has an MCU mode and a PROM mode.

3.1 MCU Mode

(1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status).

In the MCU mode, the operation is the same as that of TMP90C844.

(2) Memory Map

Figure 1.1 and Figure 1.2 show the memory map of TMP90PH44 and TMP90C844.

Figure 3.1 shows the memory map of TMP90PH44, and the accessing area by the respective addressing mode.

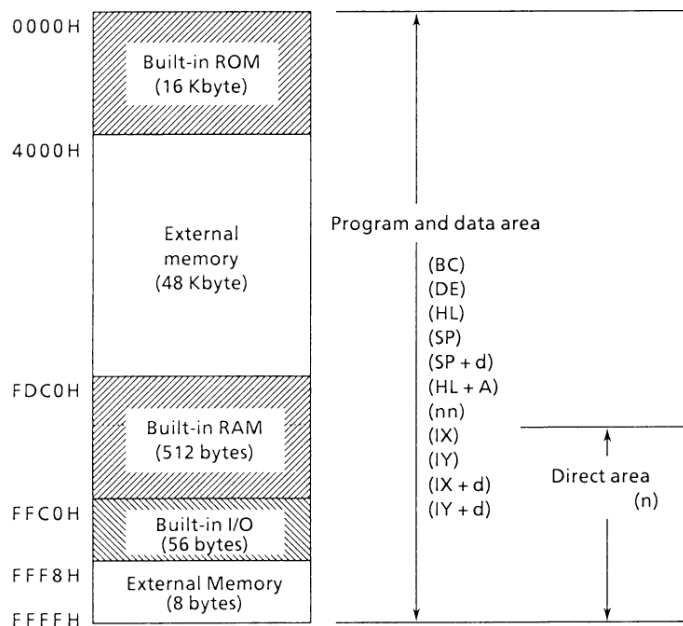


Figure 3.1. TMP90PH44 Memory Map

3.2 PROM Mode

(1) Mode Setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level.

The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket. The device selection (ROM Type) should be "27256" with following conditions.

size: 256K-bit (32K x 8-bit) VPP: 12.5V TPW: 1msec

Figure 3.2 shows the setting of pins in PROM mode.

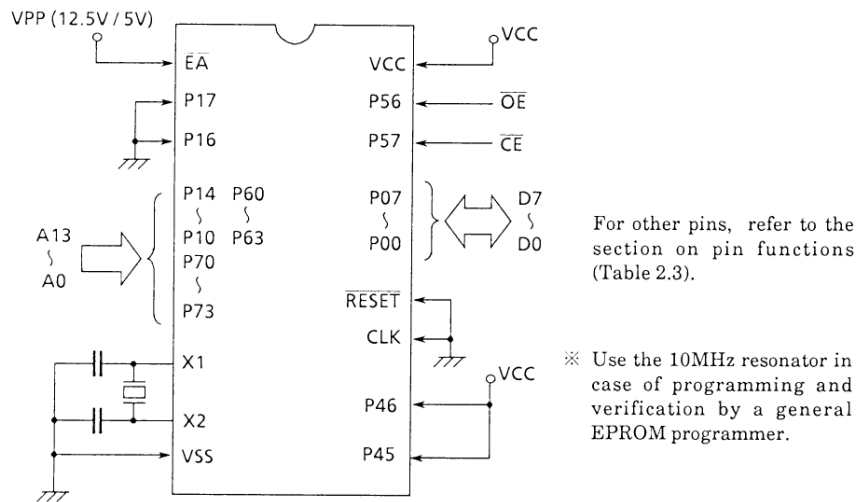


Figure 3.2. PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.5V (programming voltage) to the VPP pin when the following pins are set as follows,

(Vcc : 6.0V) *These conditions can be
 (RESET): "L" level) obtained by using adaptor
 (CLK) : "L" level) socket.

After the address and data have been fixed, a data on the Data Bus is programmed when the CE pin is set to "Low" (1ms plus is required).

General programming procedure of an EPROM programmer is as follows,

- Write a data to a specified address for 1ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writing is performed by using three times longer programming pulse width (1ms x programming times), or using three times more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of Vpp = Vcc = 5V after all data were written.

Figure 3.3 shows the programming flow chart.

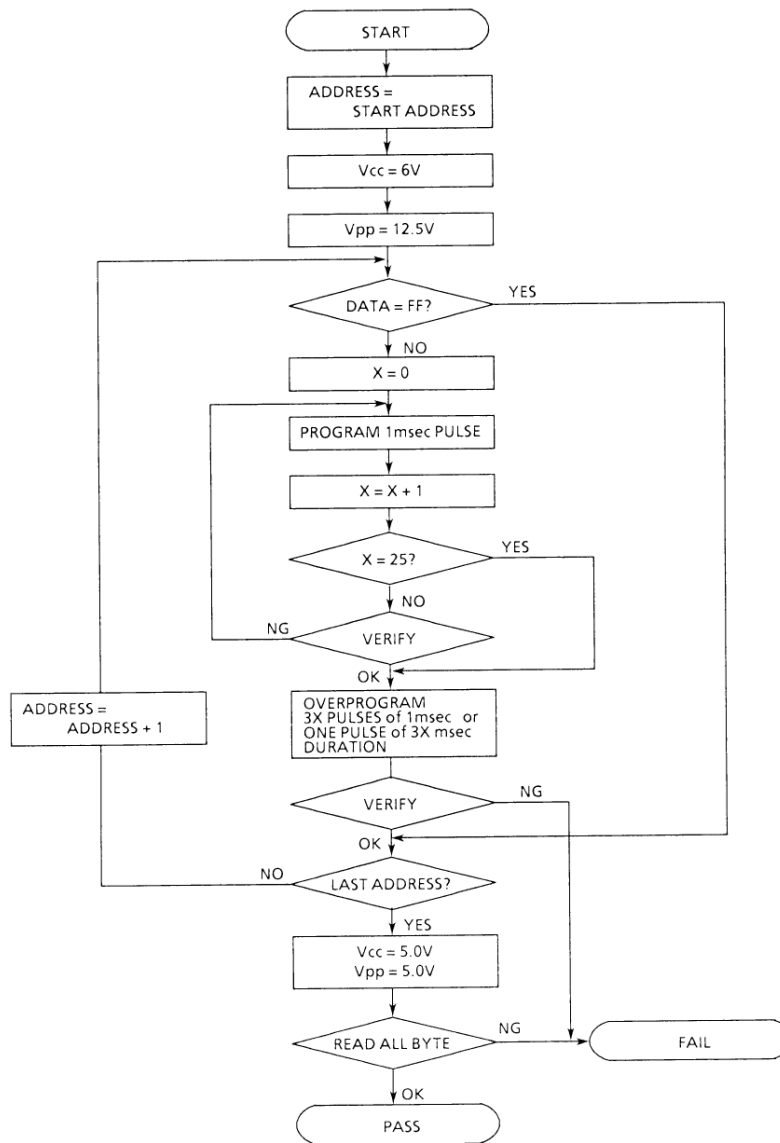


Figure 3.3. Flow Chart

4. Electrical Characteristics (Preliminary)

TMP90PH44N/TMP90PH44F

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Power supply voltage	-0.5 ~ +7	V
V_{IN}	Input voltage	-0.5 ~ $V_{CC} + 0.5$	V
P_D	Power dissipation ($T_a = 85^\circ\text{C}$)	F 500	mW
		N 600	
T_{SOLDER}	Soldering temperature (10s)	260	$^\circ\text{C}$
T_{STG}	Storage temperature	-65 ~ 150	$^\circ\text{C}$
T_{OPR}	Operating temperature	-40 ~ 85	$^\circ\text{C}$

4.2 DC Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = -20 \sim 70^\circ\text{C}$ (1 ~ 16MHz)
 Typical values are for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5V$.

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	-
V_{IL1}	P1, P2, P3, P4, P5, P6, P7	-0.3	$0.3V_{CC}$	V	-
V_{IL2}	$\overline{\text{RESET}}$, P45 (INT0)	-0.3	$0.25V_{CC}$	V	-
V_{IL3}	$\overline{\text{EA}}$	-0.3	0.3	V	-
V_{IL4}	X1	-0.3	$0.2V_{CC}$	V	-
V_{IH}	Input High Voltage (P0)	2.2	$V_{CC} + 0.3$	V	-
V_{IH1}	P1, P2, P3, P4, P5, P6, P7	$0.7V_{CC}$	$V_{CC} + 0.3$	V	-
V_{IH2}	$\overline{\text{RESET}}$, P45 (INT0)	$0.75V_{CC}$	$V_{CC} + 0.3$	V	-
V_{IH3}	$\overline{\text{EA}}$	$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	-
V_{IH4}	X1	$0.8V_{CC}$	$V_{CC} + 0.3$	V	-
V_{OL}	Output Low Voltage	-	0.45	V	$I_{OL} = 1.6\text{mA}$
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 $0.75V_{CC}$ $0.9V_{CC}$	-	V V V	$I_{OH} = -400\mu\text{A}$ $I_{OH} = -100\mu\text{A}$ $I_{OH} = -20\mu\text{A}$
I_{DAR}	Darlington Drive Current (8 I/O pins) (Note)	-1.0	-3.5	mA	$V_{EXT} = 1.5V$ $R_{EXT} = 1.1k\Omega$
I_{LI}	Input Leakage Current	0.02 (Typ)	± 5	μA	$0.0 \leq V_{in} \leq V_{CC}$
I_{LO}	Output Leakage Current	0.05 (Typ)	± 10	μA	$0.2 \leq V_{in} \leq V_{CC} - 0.2$
I_{CC}	Operating Current (RUN)	35 (Typ)	50	mA	$t_{osc} = 16\text{MHz}$
	Idle 1	1.5 (Typ)	5	mA	
	STOP ($T_A = -20 \sim 70^\circ\text{C}$) STOP ($T_A = 0 \sim 50^\circ\text{C}$)	0.2 (Typ)	40 10	μA μA	
V_{STOP}	Power Down Voltage (@STOP)	2.0	6.0	V	$V_{IL2} = 0.2V_{CC}$ $V_{IH2} = 0.8V_{CC}$
R_{RST}	$\overline{\text{RESET}}$ Pull Up Register	50	150	$k\Omega$	-
C_{IO}	Pin Capacitance	-	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{\text{RESET}}$, P45)	0.4	1.0 (Typ)	V	-

4.3 AC Characteristics

 $V_{CC} = 5V \pm 10\%$ TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t _{OSC}	Oscillation cycle (= x)	80	1000	80	–	62.5	–	ns
t _{CYC}	CLK Period	4x	4x	320	–	250	–	ns
t _{WH}	CLK High width	2x - 40	–	120	–	85	–	ns
t _{WL}	CLK Low width	2x - 40	–	120	–	85	–	ns
t _{AL}	A0 ~ 7 effective address → ALE fall	0.5x - 15	–	25	–	16	–	ns
t _{LA}	ALE fall → A0 ~ 7 hold	0.5x - 15	–	25	–	16	–	ns
t _{LL}	ALE Pulse width	x - 40	–	40	–	23	–	ns
t _{LC}	ALE fall RD/WR fall	0.5x - 30	–	10	–	1	–	ns
t _{CL}	RD/WR → ALE rise	0.5x - 20	–	20	–	11	–	ns
t _{ACL}	A0 ~ 7 effective address → RD/WR fall	x - 25	–	55	–	38	–	ns
t _{ACH}	Upper effective address → RD/WR fall	1.5x - 50	–	70	–	44	–	ns
t _{CA}	RD/WR fall → Upper address hold	0.5x - 20	–	20	–	11	–	ns
t _{ADL}	A0 ~ 7 effective address → Effective data input	–	3.0x - 35	–	205	–	153	ns
t _{ADH}	Upper effective address → Effective data input	–	3.5x - 55	–	225	164	164	ns
t _{RD}	RD fall → Effective data input	–	2.0x - 50	–	110	–	75	ns
t _{RR}	RD Pulse width	2.0x - 40	–	120	–	85	–	ns
t _{HR}	RD rise → Data hold	0	–	0	–	0	–	ns
t _{RAE}	RD rise → Address enable	x - 15	–	65	–	48	–	ns
t _{WW}	WR pulse width	2.0x - 40	–	120	–	85	–	ns
t _{DW}	Effective data → WR rise	2.0x - 50	–	110	–	75	–	ns
t _{WD}	WR rise → Effective data hold	0.5x - 10	–	30	–	21	–	ns
t _{ACKH}	Upper address → CLK fall	2.5x - 50	–	150	–	106	–	ns
t _{ACKL}	Lower address → CLK fall	2.0x - 50	–	110	–	75	–	ns
t _{CKHA}	CLK fall → Upper address hold	1.5x - 80	–	40	–	13	–	ns
t _{CKK}	RD/WR → CLK fall	x - 25	–	55	–	37	–	ns
t _{CKHC}	CLK fall → RD/WR rise	x - 60	–	20	–	2	–	ns
t _{DCK}	Valid data CLK fall	x - 50	–	30	–	12	–	ns
t _{CWA}	RD/WR fall → Valid WAIT	–	x - 40	–	40	–	22	ns

4.4 A/D Conversion Characteristics

 $V_{CC} = 5V \pm 10\%$ TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Condition	Min	Max	Unit
V _{REF}	Analog reference voltage	V _{CC} - 1.5	V _{CC}	V _{CC}	V
A _{GND}	Analog reference voltage	V _{SS}	V _{SS}	V _{SS}	
V _{AIN}	Analog input voltage range	V _{SS}	–	V _{CC}	
I _{REF}	Supply current for analog reference voltage	–	0.5	1.0	mA
Error (Quantize error of ±0.5 LSB not included)	Total error (TA = 25°C, V _{CC} = V _{REF} = 5.0V)	–	–	1.0	LSB
	Total error	–	–	2.5	

4.5 Zero-Cross Characteristics

$V_{CC} = 5V \pm 10\%$ $TA = -20 \sim 70^{\circ}C$
 $f = 1 \sim 16MHz$

Symbol	Parameter	Condition	Min	Max	Unit
V_{ZX}	Zero-cross detection input	AC coupling $C = 0.1\mu F$	1	1.8	$V_{AC P-P}$
A_{ZX}	Zero-cross accuracy	50/60Hz sine wave	–	135	mV
F_{ZX}	Zero-cross detection input frequency	–	0.04	1	kHz





4.6 Timer/ Counter Input Clock (TI0, TI2, and TI4)

$V_{CC} = 5V \pm 10\%$ $TA = -20 \sim 70^{\circ}C$
 $f = 1 \sim 16MHz$

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock cycle	$8x + 100$	–	740	–	600	–	ns
t_{VCKL}	Low clock pulse width	$4x + 40$	–	360	–	290	–	ns
t_{VCKH}	High clock pulse width	$4x + 40$	–	360	–	290	–	ns

4.7 Interrupt Operation

$V_{CC} = 5V \pm 10\%$ $TA = -20 \sim 70^{\circ}C$
 $f = 1 \sim 16MHz$

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	INT0 Low level pulse width 	4x	–	320	–	250	–	ns
t_{INTAH}	INT0 High level pulse width 	4x	–	320	–	250	–	ns
t_{INTBL}	INT1, INT2 Low level pulse width 	$8x + 100$	–	740	–	600	–	ns
t_{INTBH}	INT1, INT2 High level pulse width 	$8x + 100$	–	740	–	600	–	ns

4.8 Serial Channel Timing-I/O Interface Mode

(1) SCLK Input Mode

$V_{CC} = 5V \pm 10\%$ $TA = -20 \sim 70^{\circ}C$
 $f = 1 \sim 16MHz$

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16x	–	1.28	–	1	–	μs
t_{OSS}	Output Data \rightarrow rising edge of SCLK	$t_{SCY}/2 - 5x - 50$	–	190	–	137	–	ns
t_{OHS}	SCLK rising edge \rightarrow output data hold	$5x - 100$	–	300	–	212	–	ns
t_{HSR}	SCLK rising edge \rightarrow input data hold	0	–	0	–	0	–	ns
t_{SRD}	SCLK rising edge \rightarrow effective data input	–	$t_{SCY} - 5x - 50$	–	780	–	587	ns

(2) SCLK Output Mode

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t _{SCY}	SCLK cycle (programmable)	16x	8192x	1.28	655.4	1	512	μs
t _{OSS}	Output Data →rising edge of SCLK	t _{SCY} - 2x - 50	–	970	–	725	–	ns
t _{OHS}	SCLK rising edge→output data hold	2x - 80	–	80	–	45	–	ns
t _{HRS}	SCLK rising edge→input data hold	0	–	0	–	0	–	ns
t _{SRD}	SCLK rising edge→ effective data input	–	t _{SCY} - 2x - 150	–	970	–	725	ns

4.9 Slave Bus Interface Timing: \overline{RD} , \overline{WR} Bus Mode

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Min	Max	Unit
T _{SAR}	C/ \overline{D} setup → \overline{SRD} fall	20	–	ns
T _{HRA}	\overline{SRD} rise→ $\overline{C/D}$ hold	5	–	ns
T _{SCR}	\overline{SCS} setup → \overline{SRD} fall	0	–	ns
T _{HRC}	\overline{SRD} rise → \overline{SCS} hold	0	–	ns
T _{WRD}	\overline{SRD} pulse width	120	–	ns
T _{ARD}	\overline{SRD} fall →effective data output	–	80	ns
T _{VRB}	\overline{SRD} rise →effective data hold	10	85	ns
T _{SAW}	C/ \overline{D} setup → \overline{SWR} fall	20	–	ns
T _{HWA}	\overline{SWR} rise → $\overline{C/D}$ hold	5	–	ns
T _{SCW}	\overline{SCR} setup → \overline{SWR} fall	0	–	ns
T _{HWC}	\overline{SWR} rise → \overline{SCS} hold	0	–	ns
T _{WWR}	\overline{SWR} pulse width	120	–	ns
T _{SBW}	effective data input → \overline{SWR} rise	80	–	ns
T _{HWB}	\overline{SWR} rise →effective data hold	10	–	ns

Slave Bus Interface Timing: \overline{DS} , R/ \overline{W} Bus Mode

Symbol	Parameter	Min	Max	Unit
T _{SAD}	C/ \overline{D} setup → \overline{DS} fall	20	–	ns
T _{HDA}	\overline{DS} rise→ C/ \overline{D} hold	5	–	ns
T _{SCD}	\overline{SCS} setup → \overline{DS} fall	0	–	ns
T _{HDC}	\overline{DS} rise → \overline{SCS} hold	0	–	ns
T _{SAD}	\overline{SCS} setup → \overline{DS} fall	20	–	ns
T _{HDA}	\overline{DS} rise →R/ \overline{W} hold	5	–	ns
T _{WDS}	\overline{DS} pulse width	120	–	ns
T _{ADS}	\overline{DS} fall →effective data output	–	80	ns
T _{VDB}	\overline{DS} rise →effective data hold	10	85	ns
T _{SBD}	Effective data input → \overline{DS} rise	80	–	ns
T _{HDB}	\overline{DS} rise →effective data hold	10	–	ns

ST \bar{A} Change Timing

X = 1/fosc

Symbol	Parameter	Variable		16MHz Clock		Unit
		Min	Max	Min	Max	
t _{RPH}	ST \bar{A} fall after Output Buffer is read	–	2x + 50	–	175	ns
t _{WPH}	ST \bar{A} rise after Input Buffer is written	–	2x + 50	–	175	ns

4.10 Read Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = -40 ~ 85°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V _{PP}	V _{PP} Read Voltage	–	4.5	5.5	V
V _{IH1}	Input High Voltage (A0 ~ A15, \overline{CE} , \overline{OE})	–	0.7 x V _{CC}	V _{CC} + 0.3	V
V _{IL1}	Input Low Voltage (A0 ~ A15, \overline{CE} , \overline{OE})	–	-0.3	0.3 x V _{CC}	V
t _{ACC}	Address to Output Delay	C _L = 50pF	–	2.25TCYC + α	ns

TCYC = 400ns (10MHz Clock)
α = 200ns

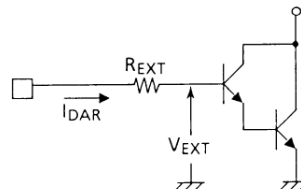
4.11 Programming Operation (PROM Mode)

DC Characteristic, AC Characteristic

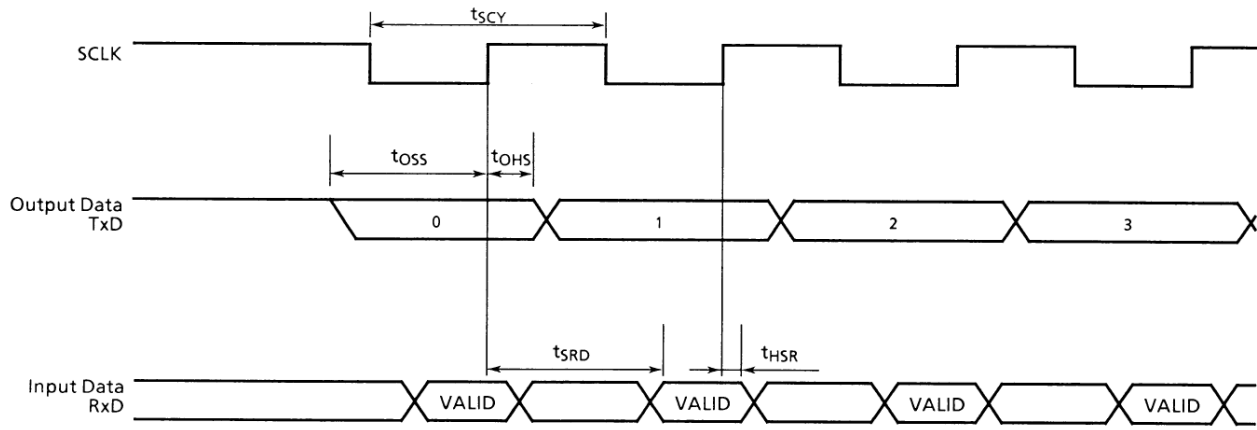
TA = 25 ± 5°C Vcc = 6V ± 0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{PP}	Programming Voltage	–	12.25	12.50	12.75	V
V _{IH}	Input High Voltage (D0 ~ D7)	–	0.2V _{CC} + 1.1		V _{CC} + 0.3	V
V _{IL}	Input Low Voltage (D0 ~ D7)	–	-0.3		0.2V _{CC} - 0.1	V
V _{IH1}	Input High Voltage (A0 ~ A15, \overline{CE} , \overline{OE})	–	0.7V _{CC}		V _{CC} + 0.3	V
V _{IL1}	Input Low Voltage (A0 ~ A15, \overline{CE} , \overline{OE})	–	-0.3		0.3V _{CC}	V
I _{CC}	V _{CC} Supply Current	f _{OSC} = 10MHz	–		50	mA
I _{PP}	V _{PP} Supply Current	V _{PP} = 13.00V	–		50	mA
t _{PW}	\overline{CE} Programming Pulse Width	C _L = 50pF	0.95	1.00	1.05	ms

(Reference) Definition of I_{DAR}

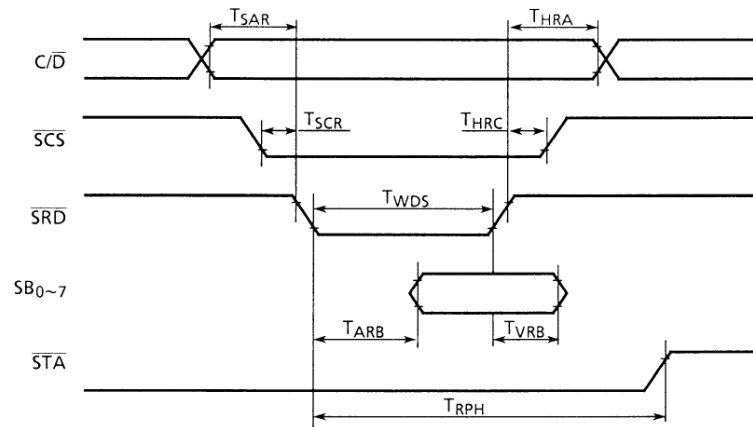


4.13 Timing Chart for I/O Interface Mode

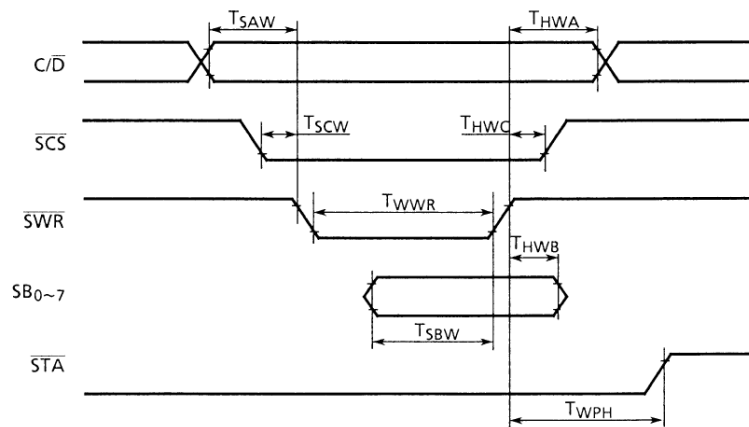


4.14 Timing Chart for Slave Bus Interface: \overline{RD} , \overline{WR} Bus Mode

(1) Read Operation

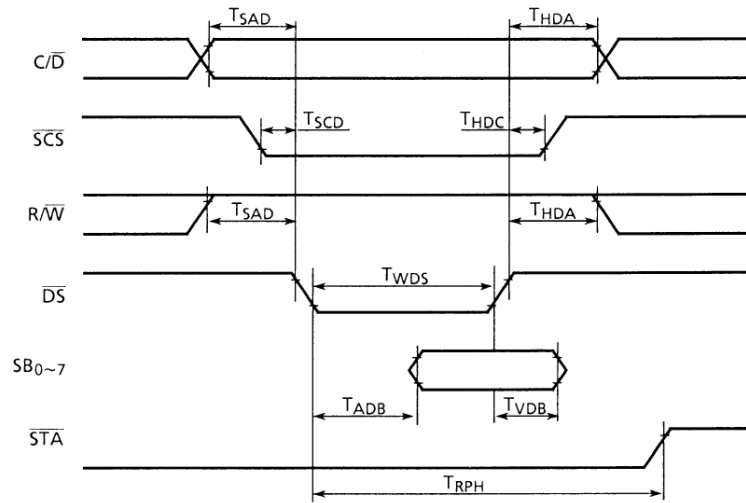


(2) Write Operation

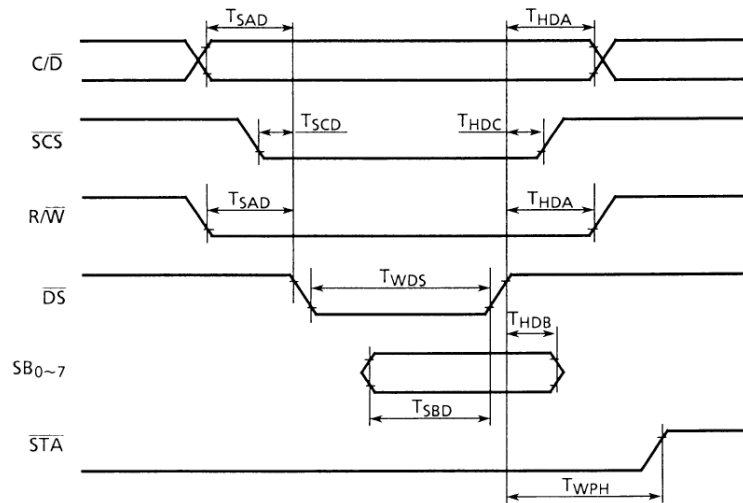


4.15 Timing Chart for Slave Bus Interface: \overline{DS} , R/ \overline{W} Bus Mode

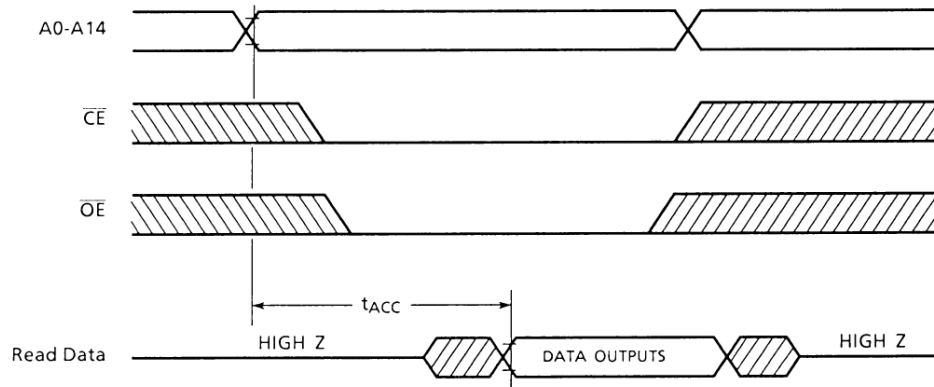
(1) Read Operation



(2) Write Operation



4.16 Read Operation Timing Chart (PROM Mode)



4.17 Programming Operation Timing Chart (PROM Mode)

