SC4910A/B
High Performance Secondary Side Controller with Synchronous Rectifier

POWER MANAGEMENT

Description

The SC4910A/B is an integrated, full featured, secondary side controller designed for use in single ended and isolated switch mode power supplies with synchronous rectification where efficiency and fast transient response are of primary concern. The SC4910A/B has outputs for both primary FET and secondary synchronous rectification. The primary drive output is designed to drive a small and low cost pulse transformer to isolate the primary FET driver. The secondary control makes it much easier to monitor and control the system load with tight control loops and implement load current sharing and synchronous rectification.

The SC4910A/B features synchronous rectification, multiphase link capability, programmable secondary side delay, programmable switching frequency and programmable maximum duty cycle. It is designed for either current mode or voltage mode operation.

The SC4910A has a typical turn-on threshold of 9V and the SC4910B has a threshold of 4.5V.

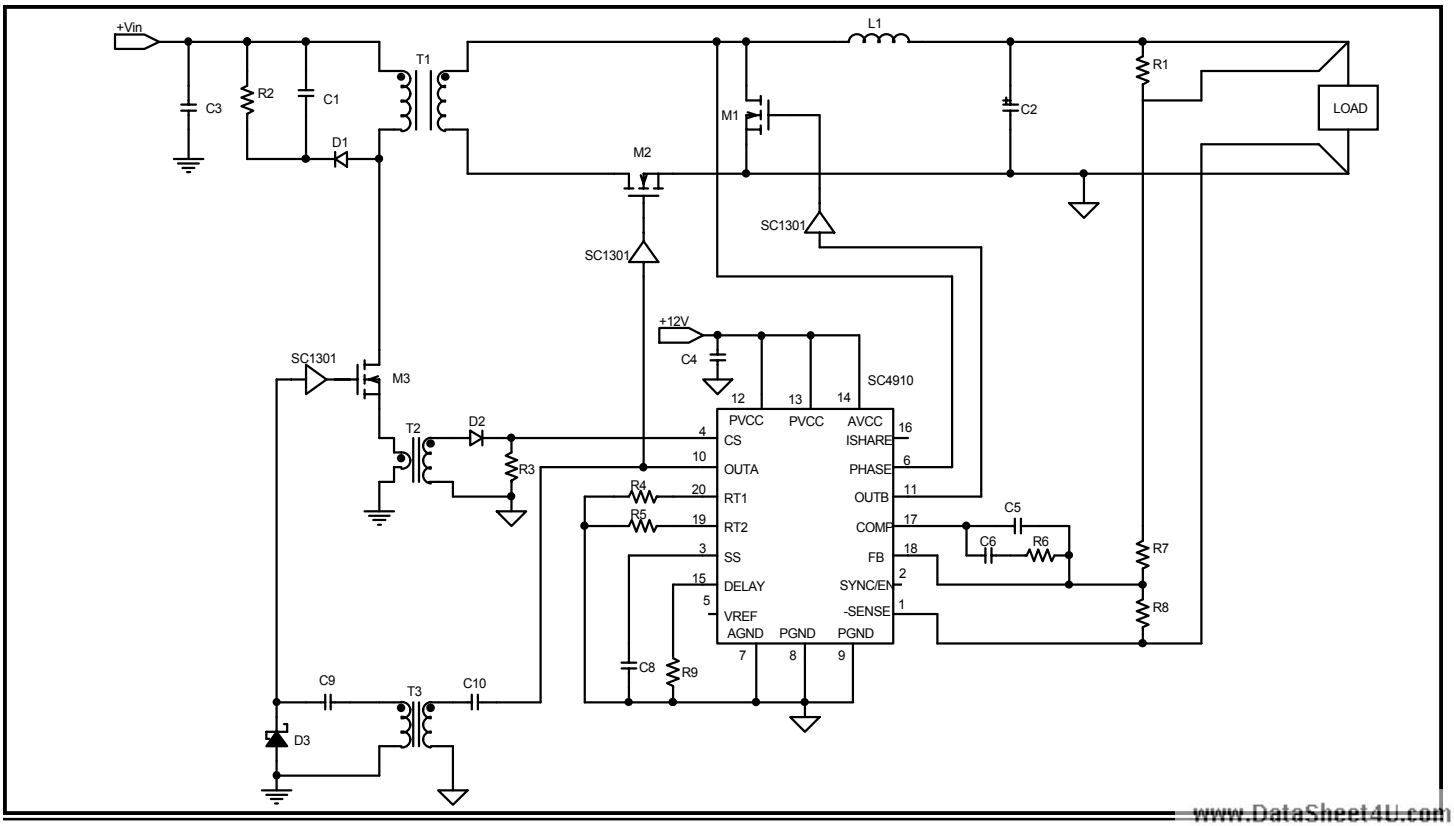
Features

- Synchronous rectification with adaptive control
- Programmable secondary side delay
- Programmable switching frequency
- Programmable max. duty cycle
- Remote voltage sense capability
- Close-loop soft start with active low shutdown
- 0.75V precision reference for low output applications
- Oscillator sychronization
- Undervoltage Lockout
- Operation to 1MHz
- Current-mode or voltage-mode operation
- **Single stage power conversion with multiphase link capability (with SC4201)**
- Monotonic start-up with pre-biased output
- Active current sharing capability
- 20 pin TSSOP package

Applications

- Telecom isolated DC to DC converters
- Isolated VRMS
- Networking power supplies
- Industrial power supplies
- Distributed power architectures
- High density power modules

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Supply Voltage	Vcc	18	V
Output Voltage		Vcc	V
Phase		Vcc	V
FB, COMP, SYNC/EN, ISHARE		-0.3 to 7	V
OUTA & OUTB Current Source or Sink		150	mA
Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-60 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	260	°C

Electrical Characteristics

Unless specified: $T_A = T_J$ = -40°C to 125°C , V_{CC} = 12V, $R_{T1} = R_{T2}$ = 50K, R_{DELAY} = 50K, C_{SS} = 0.1µF.

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
Operating Current	SYNC/EN = Low		10	15	mA
Undervoltage Lockout					
Start Threshold	SC4910A	8.7	9.0	9.3	V
	SC4910B	4.35	4.50	4.75	V
UVLO Hysteresis	SC4910A	400	550	700	mV
	SC4910B	200	300	375	mV
VREF Reference					
Output Voltage	SC4910A	4.75	5.0	5.25	V
	SC4910B	2.97	3.30	3.63	V
Line Regulation	9.3V < Vcc < 15V		15	30	mV
Load Regulation	0mA < I_{REF} < 5mA		2	10	mV
Soft Start					
SS Output			0.75		V
Voltage Accuracy	$T_A = T_J$ = 25°C	-1		+1	%
		-1.5		+1.5	
Line Regulation	9.3V < Vcc < 15V	-5	0	+5	mV
Impedance (2)			7K		Ω

Electrical Characteristics (Cont.)

Unless specified: $T_A = T_J$ = -40°C to 125°C , V_{CC} = 12V, $R_{T1} = R_{T2}$ = 50K, R_{DELAY} = 50K, C_{SS} = 0.1µF.

Parameter	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
Input Bias Current			0.1	5	µA
Offset Voltage			2	7	mV
Open Loop Gain			80		dB
CMRR (1)			70		dB
PSRR (1)			70		dB
Output High Voltage	I_{COMP} = 1.0mA	1.75	1.9		V
Output Low Voltage	I_{COMP} = 1.0mA		0.9	1.0	V
Unity Gain Bandwidth (1)		5.0			MHz
Slew Rate (1)			2.0		V/µS
Oscillator					
Frequency Range	Min. Frequency $R_{T1} = R_{T2}$ = 500K		50		KHz
	Max. Frequency $R_{T1} = R_{T2}$ = 25K		1000		
Frequency		450	500	550	KHz
Peak Voltage (1)			2.5		V
Valley Voltage (1)			1.0		V
Enable Input High		2.0			V
Enable Input Low				0.8	V
Duty Cycle					
Maximum Duty Cycle (2)			90		%
Minimum Duty Cycle			0		%
Duty Cycle Tolerance		-5		+5	%
Current Limit					
Cycle by Cycle Threshold		0.975	1.025	1.075	V
Shutdown Threshold		1.1	1.25	1.4	V
Delay to Output (2)			100		nS
Input Impedance (2)			20		kΩ

Electrical Characteristics (Cont.)

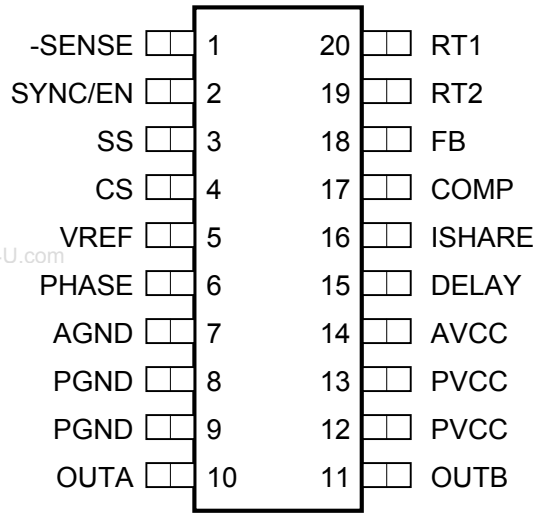
Unless specified: $T_A = T_J$ = -40°C to 125°C , V_{CC} = 12V, $R_{T1} = R_{T2}$ = 50K, R_{DELAY} = 50K, C_{SS} = 0.1µF.

Parameter	Test Conditions	Min	Typ	Max	Unit
OUTA and OUTB					
Output Low	I_{OUTPUT} = 100mA		1	1.3	V
Output High	I_{OUTPUT} = 100mA	9.75	10		V
Rise Time (2)	C_{OUT} = 100pF		20		nS
Fall Time (2)	C_{OUT} = 100pF		20		nS
Delay					
OUTB Falling to OUTA Rising (2)	R_{DELAY} = 50KΩ		70		nS
OUTA Falling to OUTB Rising (2)	PHASE > 1.5V		220		nS
	PHASE < 1.5V		30		
Current Share Error Amplifier					
Transconductance (1)			0.18		mS
Output Source or Sink Current (1)			10		µA

Notes:
(1) Guaranteed by design.
(2) Guaranteed by characterization.
(3) This device is ESD sensitive. Use of standard ESD handling requirements are required.

Pin Configurations

TOP VIEW



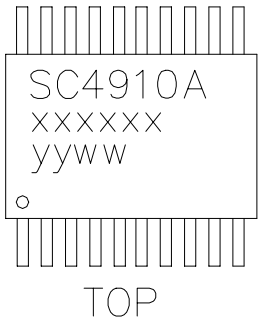
(20 Pin TSSOP)

Ordering Information

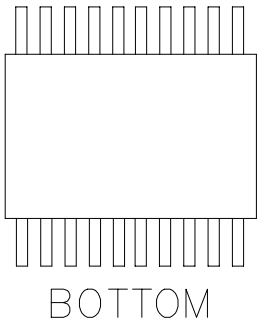
Part Number	Package
SC4910AITSTRT(2)	TSSOP-20(1)
SC4910BITSTRT(2)	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Marking Information

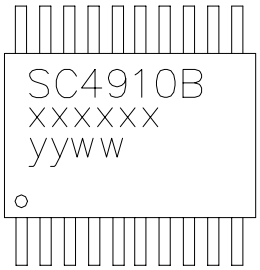


TOP

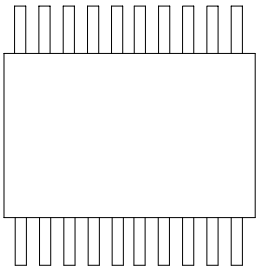


BOTTOM

Part Number (Example: 1471)
yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example: P94A01)



TOP



BOTTOM

Part Number (Example: 1471)
yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example: P94A01)

Pin Descriptions

Pin #	Pin Name	Pin Function
1	-SENSE	Remote voltage sense return.
2	SYNC/EN	Bidirectional synchronization and enable /disable pin. Referenced to -SENSE.
3	SS	Soft start.
4	CS	Current sense input.
5	VREF	5V internal reference output.
6	PHASE	Phase node for synchronous rectification.
7	AGND	Analog ground.
8	PGND	Power ground for OUTA.
9	PGND	Power ground for OUTB.
10	OUTA	Output driver for primary MOSFET and secondary forward MOSFET. Low during UVLO.
11	OUTB	Output the MOSFET driving signal for forward rectifier. Low during UVLO.
12	PVCC	Power supply for OUTB.
13	PVCC	Power supply for OUTA.
14	AVCC	Analog supply voltage.
15	DELAY	Predictive delay between OUTA and OUTB. The delay is from turn-off of the freewheeling MOSFET to turn-on of the forward MOSFET and primary MOSFET. The delay time is 20 to 200nS programmable.
16	ISHARE	Current share bus.
17	COMP	Feedback compensation.
18	FB	Feedback.
19	RT2	Connect to timing resistor RT2 to control the negative ramp of the internal oscillator.
20	RT1	Connect to timing resistor RT1 to control the positive ramp of the internal oscillator.

Block Diagram

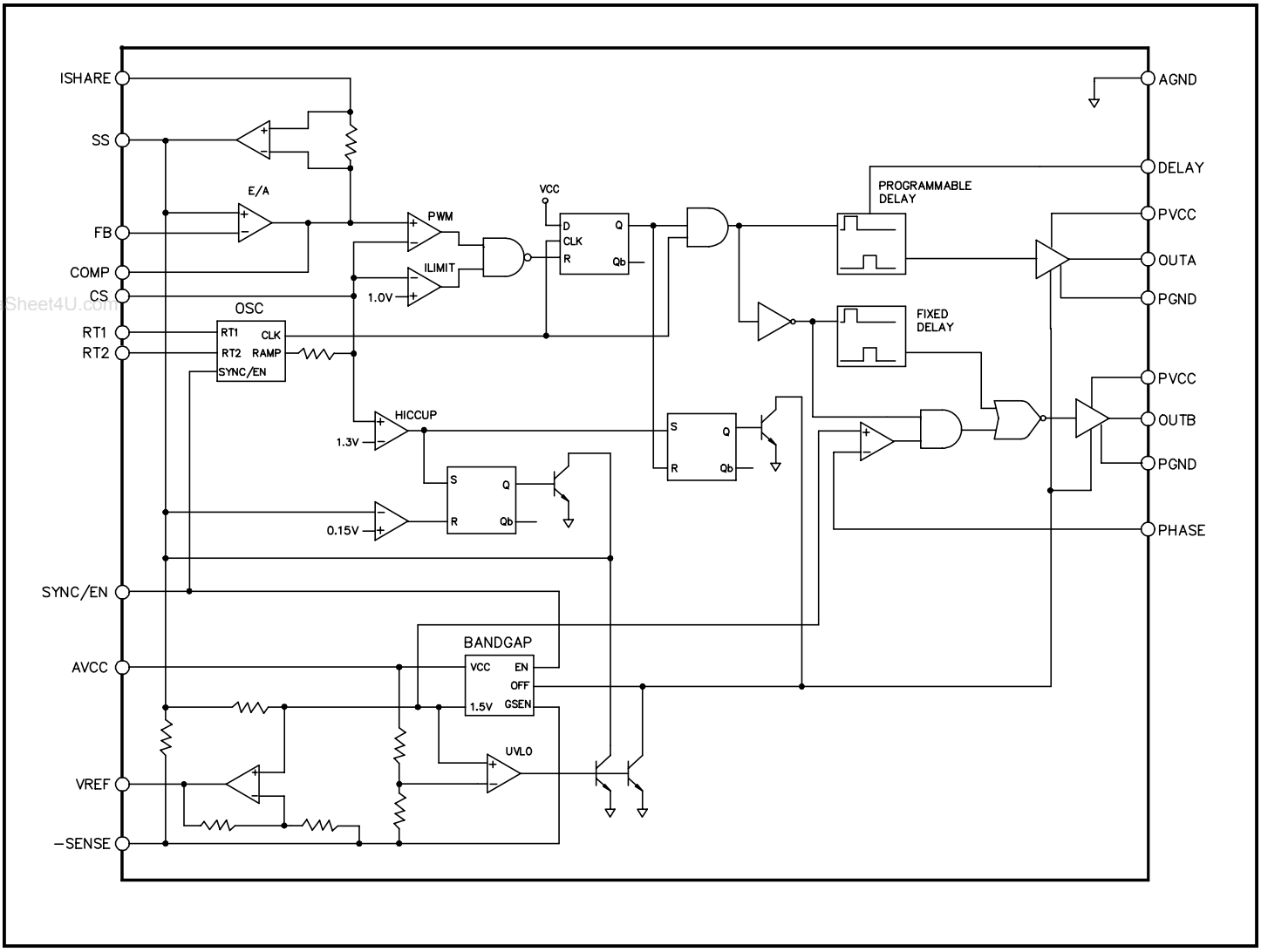


Figure. 1

Applications Information

The SC4910A/B is a secondary side PWM controller working either in current mode or voltage mode mainly for applications of forward converters with synchronous rectification. While the OUTA drives the primary MOSFET through transformer and the secondary forward rectifier, the OUTB drives the secondary freewheeling rectifier. The switching frequency and maximum duty cycle can be programmable with two resistors. The delay time from the falling edge of OUTA to the rising edge of OUTB is adaptive by monitoring the phase node voltage. The delay time from the falling edge of OUTB to the rising edge of OUTA is determined by a programming resistor from the DELAY pin to ground. The ISHARE pin allows for current sharing among the parallel operating units to make current equally distribute load. The -SENSE pin separated from GND pin provides true output voltage remote sense capability. Other features include soft start, sychronization or enable/disable by user, provided 5V reference voltage.

Oscillator

The frequency and duty cycle of the oscillator is controlled by placing two resistors from the RT1 and RT2 pins to ground. The resistor at RT1 controls the maximum “on” duty cycle and the resistor at RT2 controls the “off” portion of a cycle. When the resistor at RT1 is equal to that at RT2, the maximum duty cycle will be approximately 50%. The following formula is used to determine the time duration of the “on” and “off” portions:

$$t = RT \times 20 \times 10^{-12}$$

Current Sense and Current Limit

The CS pin has an input impedance of 20K ohms and swings from 1.0V to 2.5V. With a 5K ohm resistor from CS to ground, the device operates in voltage mode with a ramp that will swing from 0.2V to 0.5V. When the 5K resistor is connect to a voltage that is proportional to the primary side current, the device will operate in current mode. The cycle-by-cycle current limit is triggered when the CS pin voltage rises above 1V. If CS exceeds 1.25V, the faulty latch will be set and the outputs will be driven low. The soft start capacitor is then discharged by the internal current sink. No outputs are allowed until the soft start capacitor is fully discharged to 0.15V. At this point the fault latch will be reset and the SC4910 will begin a soft start process. This results in a hiccup current limit mode for continuous fault conditions.

SYNC/EN

The enable function looks at the SYNC/EN pin and an internal timing capacitor. If the SYNC/EN pin is low and the internal timing capacitor voltage is high, then the SC4910 is disabled with OUTA, OUTB and SS pulled low. When the SYNC/EN pin is held high, the device is enabled and runs off of the internal oscillator. When a rising signal is detected on the SYNC/EN pin a one-shot is triggered and discharges the internal timing capacitor. As long as the internal timing capacitor is below an internal reference level, the device will synchronize with the external pulse. If the internal timing capacitor is allowed to charge up to the internal reference level before another SYNC pulse is detected, the device will switch back to the internal oscillator.

Soft Start

The SS pin is connected to the internal reference, 0.75V, through an internal 6K ohm resistor. The SS pin is also connected to the non-inverting input of the error amplifier. With an external capacitor connected to this pin, the soft start timing will be determined by this RC time constant. During start-up, the SS pin is held low until the undervoltage lockout threshold is reached. Once the UVLO threshold is reach, the SS pin is released and the device will regulate to the voltage on this pin.

Undervoltage Lockout

When the supply voltage V_{CC} is below the undervoltage lockout threshold, both OUTA and OUTB are held low. The SS pin and the COMP pin are also held low. Once the undervoltage lockout threshold has been surpassed, OUTA, OUTB, SS and COMP are released for normal operation.

Applications Information (Cont.)

Programmable Delay

SC4910 is for single ended topologies with secondary side synchronous rectification. It provides outputs to drive the primary MOSFET through a small pulse transformer and the secondary synchronous rectifiers directly. To avoid cross conduction and optimize performance, adjustable delay is necessary between forwarding and freewheeling switches. The delay from falling edge of OUTB to rising edge of OUTA is determined by a resistor from the DELAY pin to ground. The following formula is used to calculate the delay time:

$$t_{DELAY} = R \bullet 1E-12 + 20nS$$

where, R is the delay time setting resistor.
R should be between 20K and 200K.

The delay time from falling edge of OUTA to rising edge of OUTB is adaptive and is triggered when the PHASE node falls below 1.5V. If after 220nS the PHASE node has still not fallen, the device will automatically switch.

Operation Mode

SC4910 could be configured either current mode or voltage mode operation. In current mode, the current sense signal comes to the CS pin while an external resistor could configure slope compensation. In voltage mode, an external resistor forms sawtooth with the internal 20K resistor for voltage mode operation while current limit signal comes to the same pin.
In current mode, which is preferred for application of SC4910, current is sensed by a current transformer for current feedback and over current protection. The current in the primary switch is sensed and controlled by developing a voltage proportional to current across a sense resistor on the secondary. The sensed voltage is then fed into the CS pin of SC4910. The typical current limit threshold in the current sense pin of the SC4910 is 1.0V. The over current limit is assumed typical 120% of full load current. Then the current sense resistor can be calculated by the following equation:

$$Rs = \frac{1.0 \bullet n \bullet N_S}{120\% \bullet I_O(pk)}$$

where
n – Power transformer primary to secondary turns ratio
N_S – Secondary turns of current sense transformer
Io(pk) – Peak inductor current

An example of choosing a current sense resistor is given below. Assume the converter full load current is 20A and peak inductor current is 23A, the power transformer primary to secondary turns ratio is 6:1 and the current sense transformer primary to secondary turns ratio is 1:100, then,

$$Rs = \frac{1.0 \bullet 6 \bullet 100}{120\% \bullet 23} \approx 21\Omega$$

Slope Compensation

Slope compensation is needed to prevent sub-harmonic oscillation at duty cycle higher than 50% and to compensate the peak to average difference in peak current mode control. The following equation can be used to calculate the external slope. If negative Se is obtained by the equation, no slope compensation is needed.

$$Se \geq \frac{2V_O n - V_{IN}}{2(V_{IN} - V_O n)} \bullet \frac{V_{IN} \bullet \Delta I_L}{V_O n} \bullet \frac{R_S}{n \bullet N_S}$$

where
Se – External slope magnitude
Vin – Low input line voltage
Vo – Output voltage
n – Power transformer primary to secondary turns ratio
N_S – Secondary turns of current sense transformer
ΔI_L - Peak-to-peak Inductor current ripple

For example, if the low input line voltage is 36V, output voltage is 3.3V, power transformer primary to secondary turns ratio is 6:1; the peak-to-peak inductor current ripple is 6A, and current sense gain R_S is 21W, then the external slope needed is:

$$Se \geq \frac{2 \bullet 3.3 \bullet 6 - 36}{2(36 - 3.3 \bullet 6)} \bullet \frac{36 \bullet 6}{3.3 \bullet 6} \bullet \frac{21}{6 \bullet 100} \approx 85mV$$

Applications Information (Cont.)

This is the minimum external slope required to avoid sub-harmonic oscillation at low input line.

With SC4910, the external slope is very easy to implement. Referring to Figure 2, R12 is the current sense resistor. R10 and the internal 20KΩ resistor divide the internal slope 1.0V - 2.5V down to the required compensation slope.

$$R10 = \frac{(Se - \frac{V_{IN} \bullet R_S}{L_M \bullet N_S \bullet f_S}) \bullet 20}{(2.5 - 1.0) - (Se - \frac{V_{IN} \bullet R_S}{L_M \bullet N_S \bullet f_S})}$$

where:

LM - Power transformer magnetizing inductance
fS = Switching frequency

In the example,

$$R10 = \frac{(0.085 - \frac{36 \bullet 21}{450E-6 \bullet 100 \bullet 250E3}) \bullet 20}{(2.5 - 1.0) - (0.085 - \frac{36 \bullet 21}{450E-6 \bullet 100 \bullet 250E3})} = 240\Omega$$

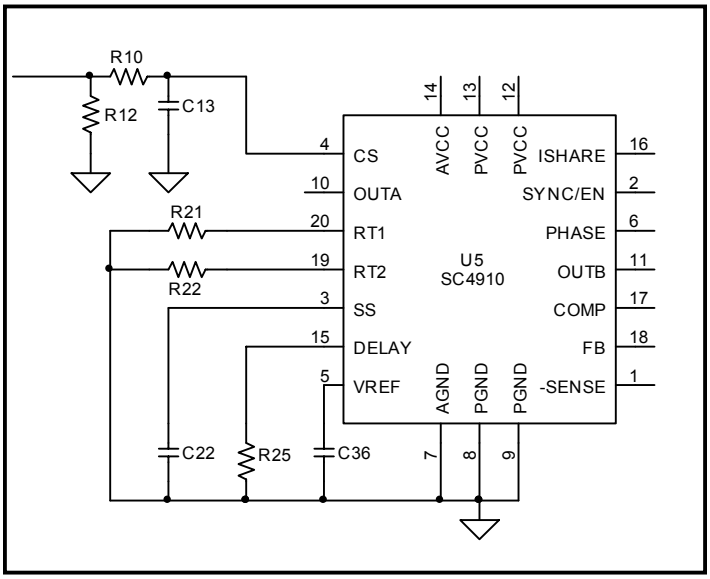


Figure 2

Closed-Loop Compensation

The simplified control-to-output transfer function for the forward converter with current mode control, for small value of external slope (Se ≤ Sn, Sn is on-time slope of sensed current waveform) is given by:

$$G_{vg} = G_{vgo} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

where

$G_{vgo} = \frac{nN_S V_O}{I_O R_S}$ DC gain of power stage with current loop closed

$\omega_P = \frac{1}{RC}$ Dominant pole of power stage with current loop closed

$\omega_Z = \frac{1}{R_{ESR} C}$ ESR zero of power stage

where
R - Load resistance
C - Output capacitance
RESR - Output capacitors ESR

For the given example above, at low line and R = 0.165Ω, C = 2 x 680uF = 1360uF, R_{ESR} = 17mΩ, therefore:

$$G_{vgo} = \frac{6 \bullet 100 \bullet 3.3}{20 \bullet 21} = 4.71 = 13dB$$

$$\omega_P = \frac{1}{0.165 \text{ X } 1360E-6} = 4456 \text{ rad/s} = 710Hz$$

$$\omega_Z = \frac{1}{17E-3 \text{ X } 1360E-6} = 43253 \text{ rad/s} = 6887Hz$$

Applications Information (Cont.)

Type 2 compensator (Figure 3) is needed for the above current mode control. The compensation network gives the following characteristics:

$$G_{COMP} = \frac{\omega_1}{s}\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}$$

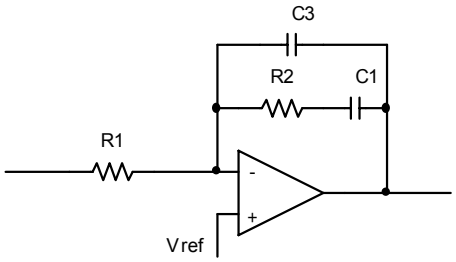


Figure 3

where

$$\omega_1 = \frac{1}{R_1(C_1+C_3)}$$

$$\omega_{ZC} = \frac{1}{R_2 C_1}$$

$$\omega_{PC} = \frac{1}{R_2\frac{C_1C_3}{C_1+C_3}}$$

The loop gain will be given by:

$$T = G_{vg}G_{COMP}K_{FB} = G_{vgo}\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}\bullet\frac{\omega_1}{s}\frac{1+\frac{s}{\omega_{ZC}}}{1+\frac{s}{\omega_{PC}}}\bullet\frac{V_{ref}}{V_O}$$

The goal of the compensation design is to shape the loop with high DC gain, high bandwidth, enough phase margin, and high attenuation for high frequency noises. Figure 4 gives the asymptotic diagrams of the power stage with current loop closed and its loop gain.

One integrator is added to increase the DC gain. W_{zc} is used to cancel the power stage pole w_p so that the loop gain has –20dB rate when it reaches 0 dB line. w_{pc} is placed at output capacitor ESR or half switching frequency, whichever is lower.

Arbitrarily choose R2, then

$$C_1 = \frac{1}{R_2\omega_P}, C_3 = \frac{C_1}{\frac{\omega_{PC}}{\omega_{ZC}}-1}, R_1 = \frac{1}{\omega_l(C_1+C_3)}$$

ω_l is adjusted for satisfactory phase margin and crossover frequency.

Synchronization

Synchronization of oscillators in multiphase operation allows for reduced size of filtering components and improved dynamic response.

SC4910 provides single stage conversion where SC4201 provides the multiphase function. SC4910 and SC4201 are placed on the secondary side, outputs A and C of the SC4201 are fed into the Sync pins of 2 separate SC4910's. Both power supplies operate 180 degrees apart. SC4201 can be configured up to 4 phase operation.

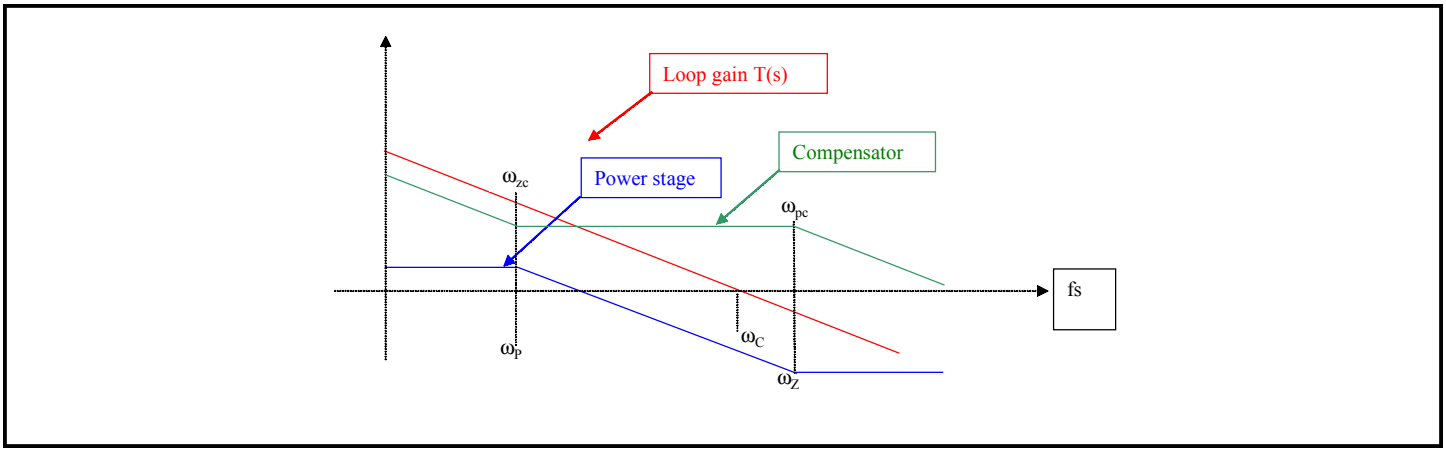


Figure 4

Applications Information (Cont.)

Load Remote Sensing

Dedicated -SENSE pin provides true remote sensing of the regulated supply's output terminal voltage for high current applications. As shown in Figure 5, the bandgap reference "ground " is brought out as –Sense, which is connected to the "load ground" and to the local analog ground by the resistor R10. With this way combined with upper side R1, the voltage drop on power line is offset and the load voltage is truly sensed.

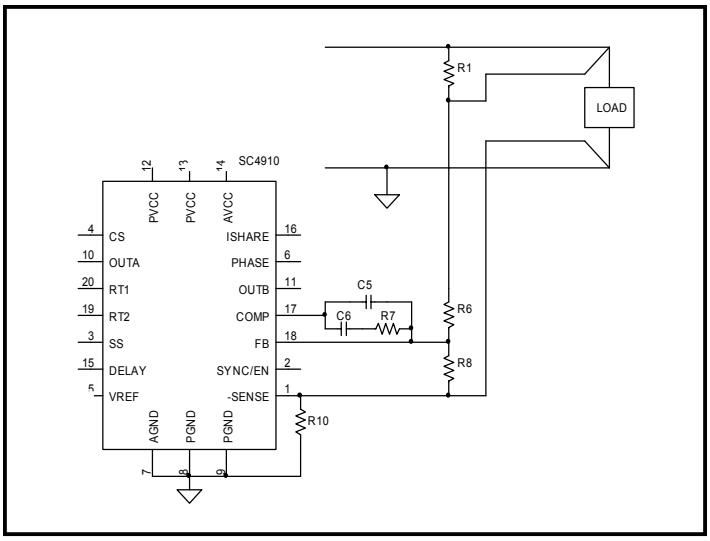


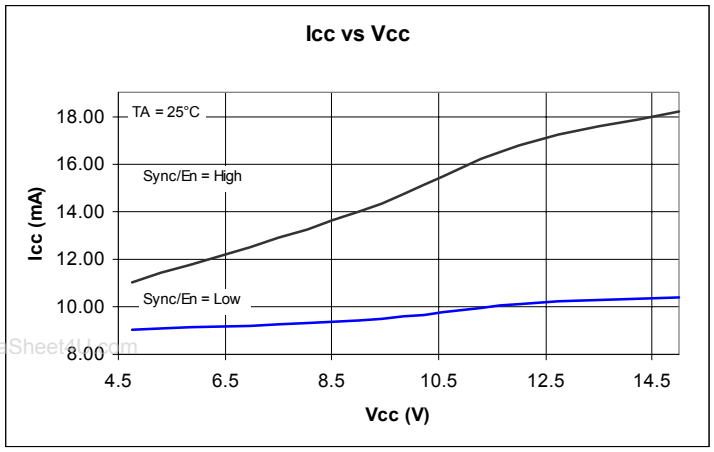
Figure 5

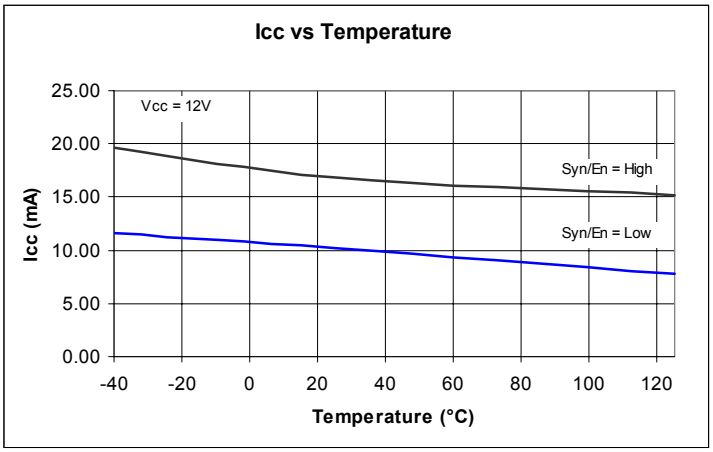
Load Current Sharing

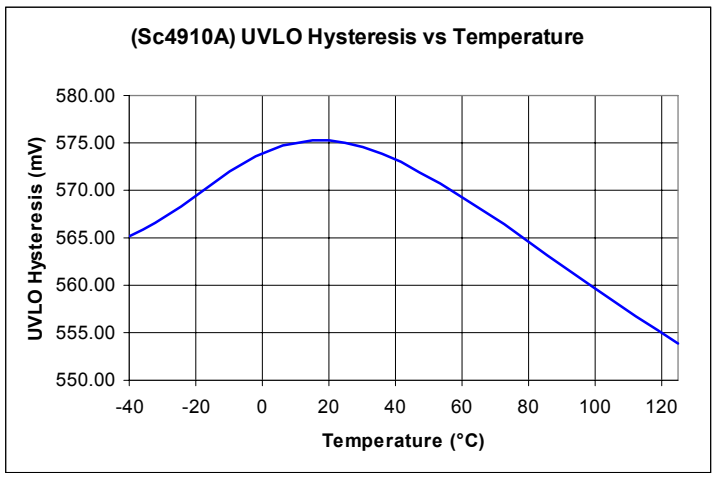
A single wire connected between the ISHARE pins will force current sharing between parallel units for paralleling or n+1 redundant operation.

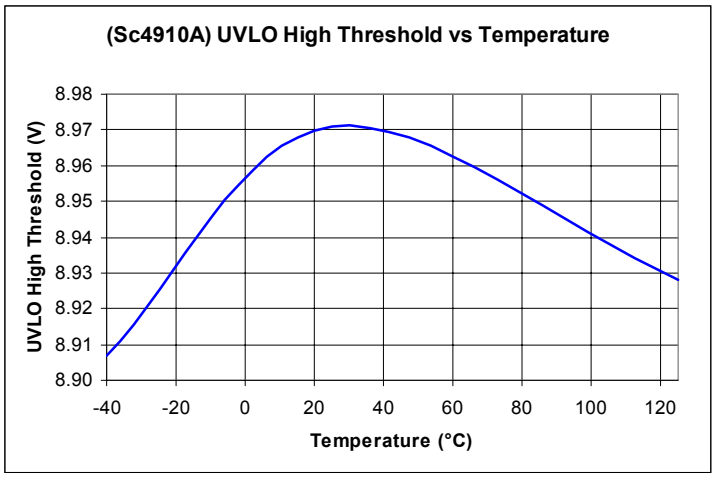
The ISHARE pin allows for current sharing between several parallel units. The ISHARE pin connects internally to the non-inverting input of ISHARE amplifier. An internal 4KΩ resistor is between the inverting and non-inverting inputs of this amplifier, with the inverting input also connected to the COMP pin. The output of the amplifier connects to the SS (0.75V ref) pin. During normal operation, when all devices are sharing the load current equally, the COMP pin voltages on each units should be approximately equal. If one of the devices begins to take on too much or too little of the load, the difference in COMP pin voltage will cause the ISHARE amplifier to adjust the SS (0.75V ref) voltage accordingly. In the event of ISHARE pulled down below 1V, the ISHARE amplifier is disabled to prevent output voltage of the unit lower than specification.

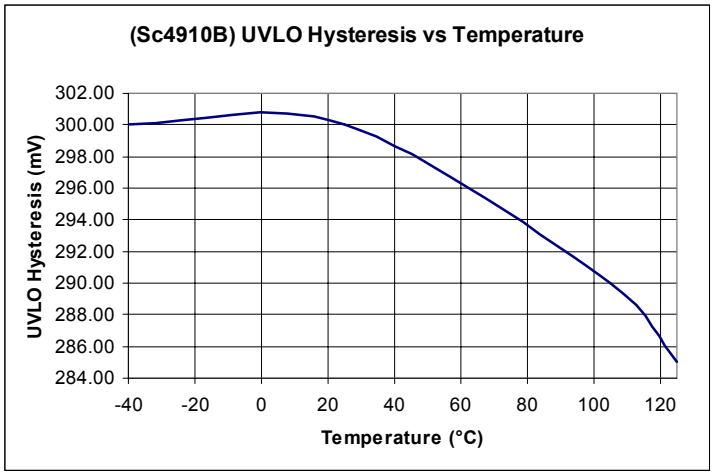
Typical Characteristics

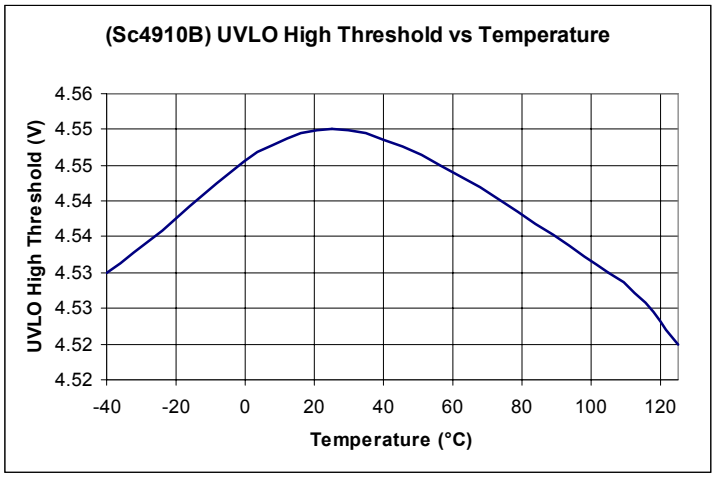




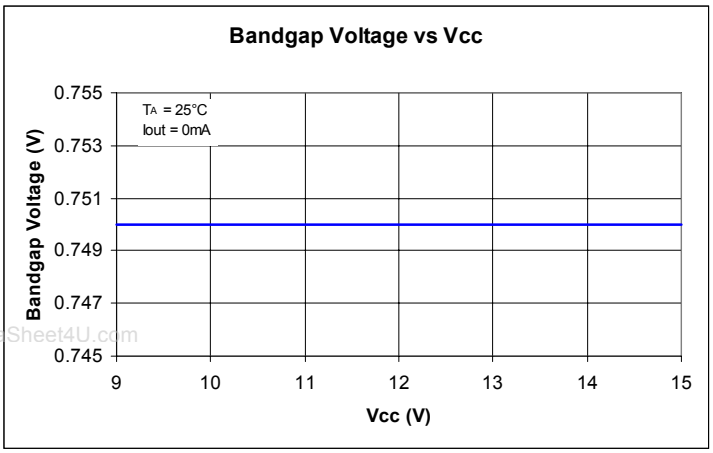


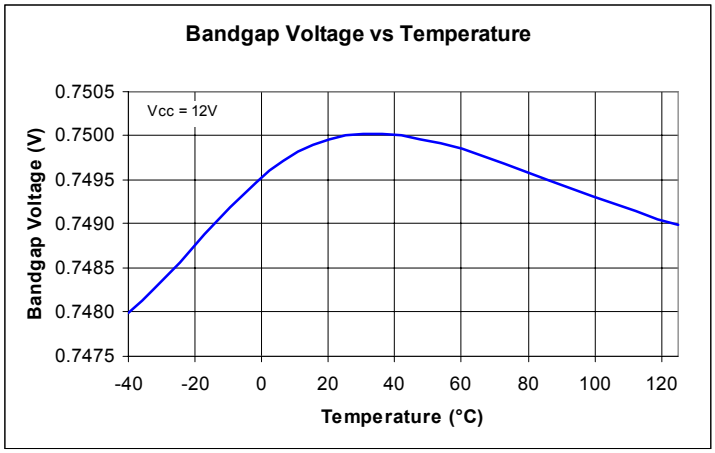


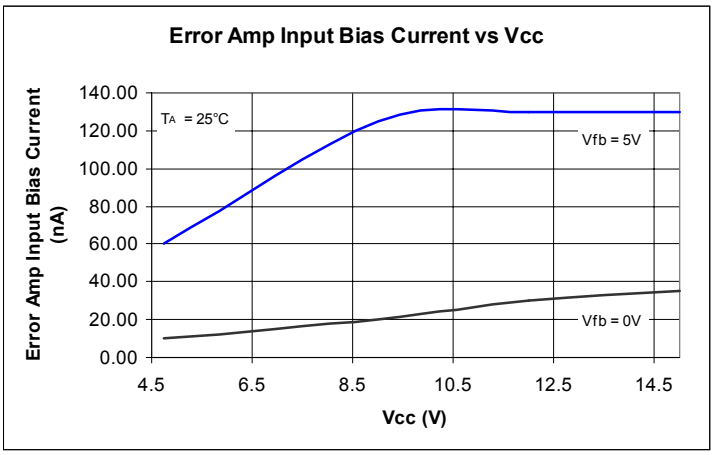


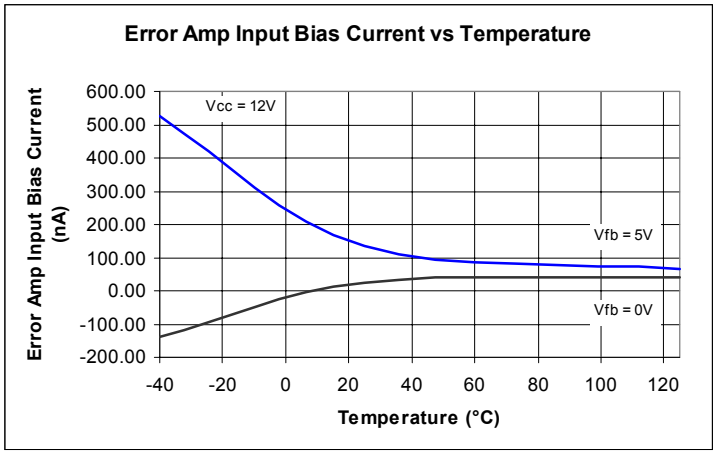


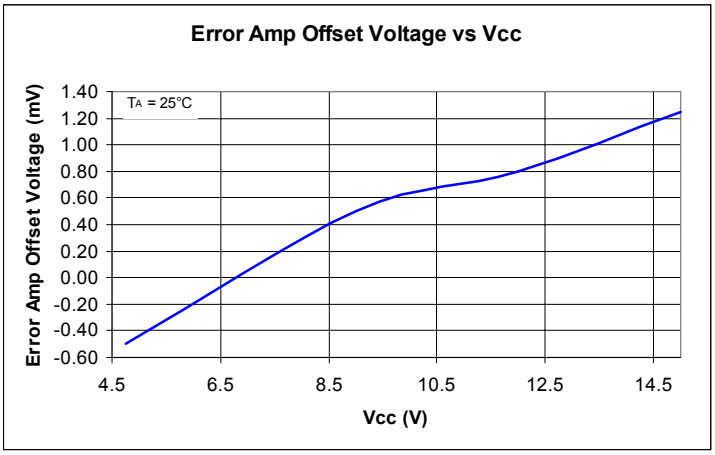
Typical Characteristics (Cont.)

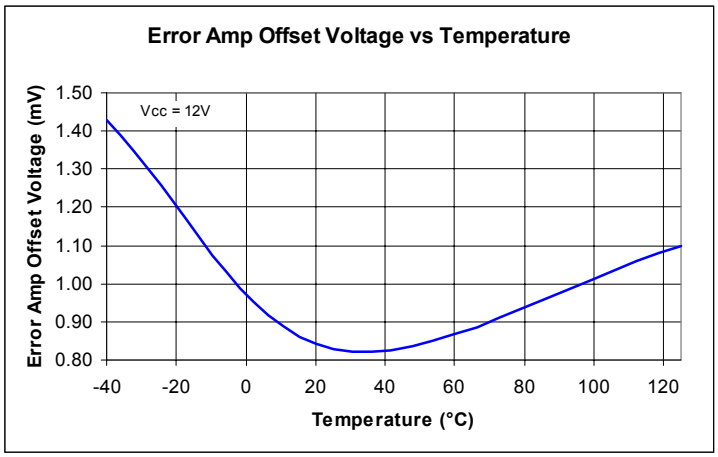






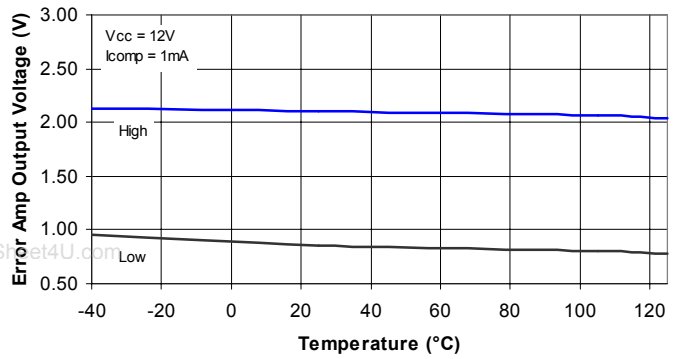




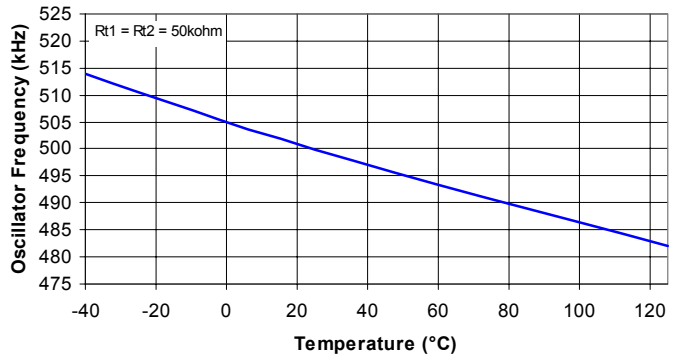


Typical Characteristics (Cont.)

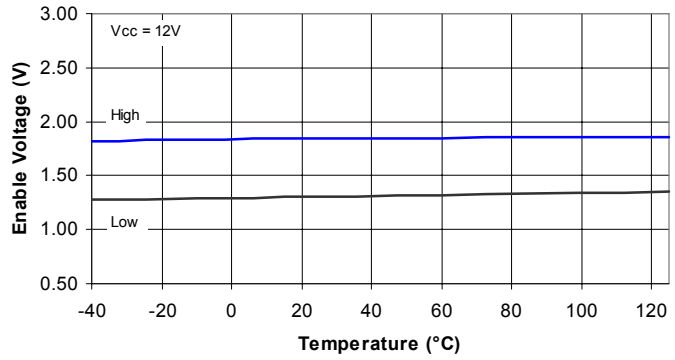
Error Amp Output Voltage vs Temperature



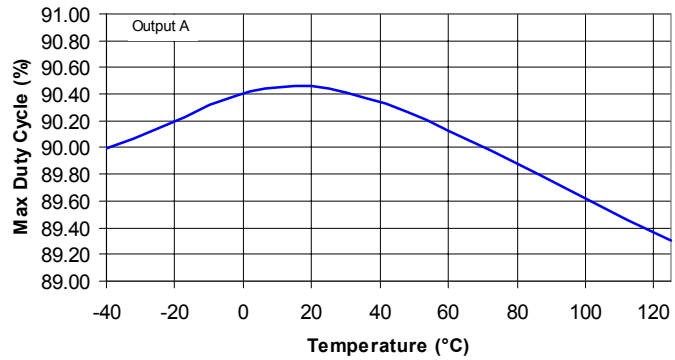
Oscillator Frequency vs Temperature



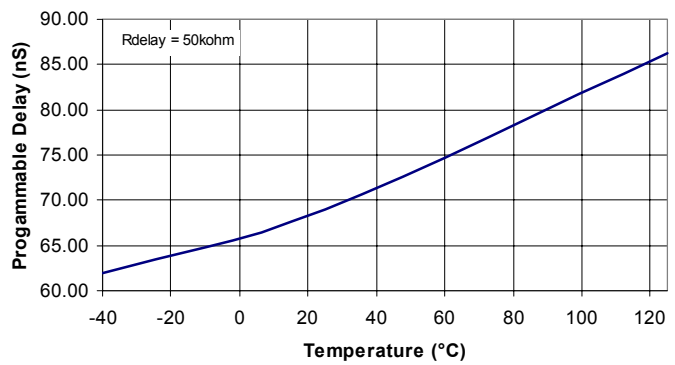
Enable Voltage vs Temperature



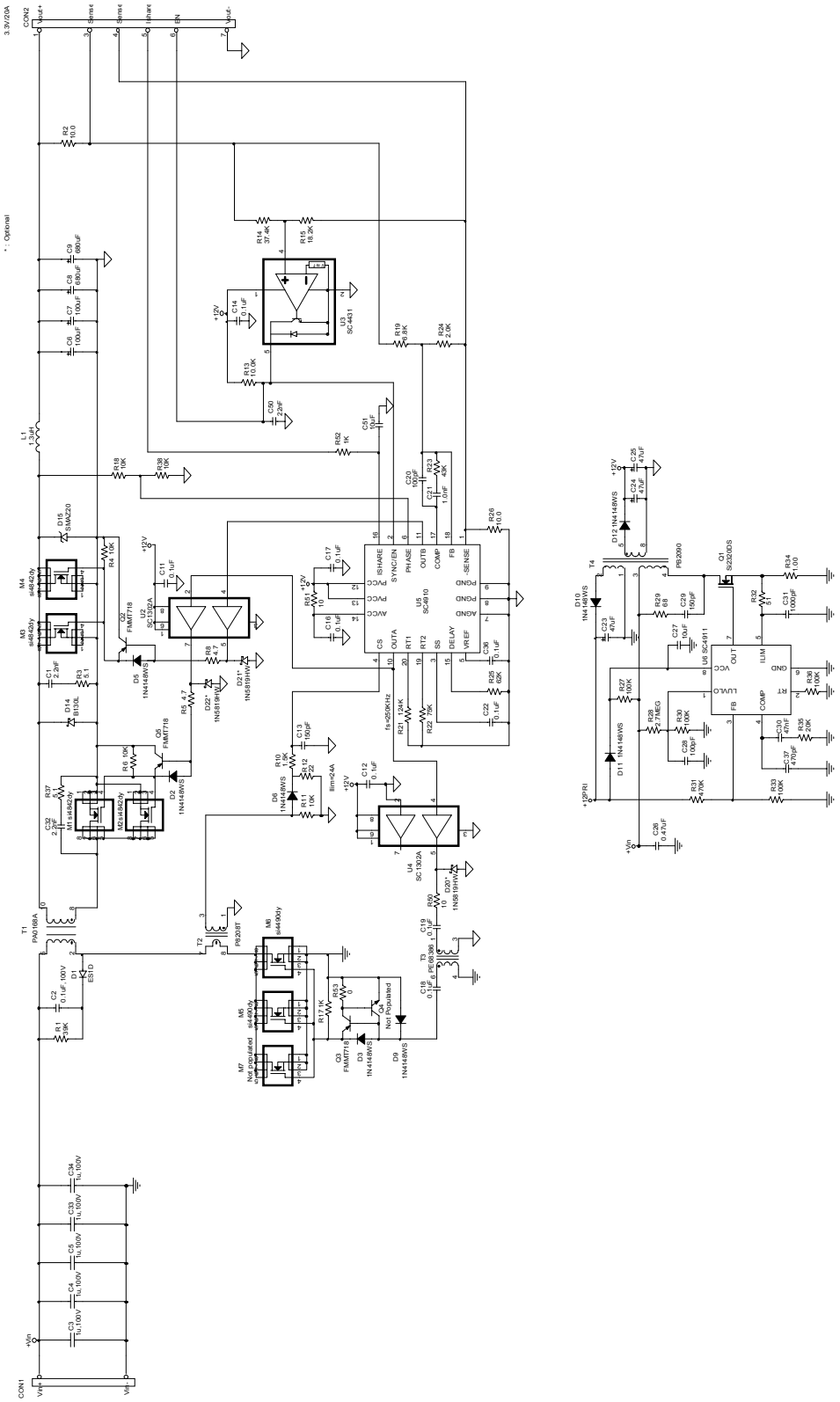
Max Duty Cycle vs Temperature



Progammable Delay vs Temperature



Evaluation Board Schematics



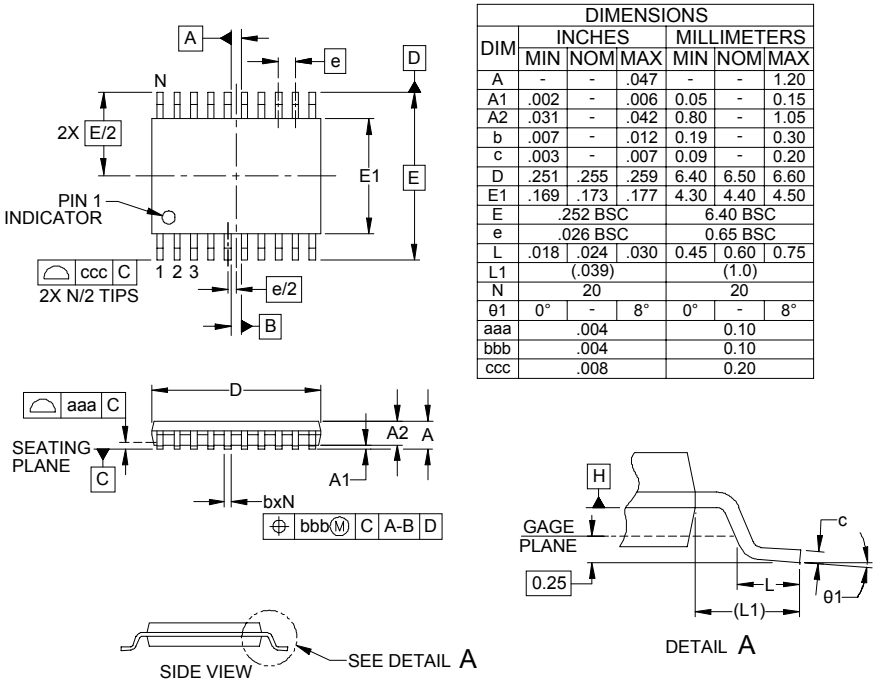
Evaluation Board Bill of Materials

Item	Quantity	Reference	Part	Manufacturer #	Foot Print
3	2	C1,C32	2.2nF		SM/C_0805
4	1	C2	0.1uF,100V	TDK, C3216X7R2A104M	SM/C_1206
5	5	C3,C4,C5,C33,C34	1uF,100V	Murata, GRM55RR72A105KA01B	SM/C_2220
6	4	C6,C7,C8,C9	680uF, 4V	Sanyo, 4TPB680	SM/CT_7343
7	10	C11,C12,C14,C16,C17,C18,C19, C22,C36, C51	0.1uF		SM/C_0805
8	2	C13,C29	150pF		SM/C_0805
9	1	C20	560pF		SM/C_0805
10	1	C21	1.5nF		SM/C_0805
11	3	C23,C24,C25	47uF, 16V	Sanyo, 16TPB47	SM/CT_7343
12	1	C26	0.47uF		SM/C_1206
13	1	C27	10uF, 10V	Murata, GRM32ER61C106KC31L	SM/C_1210
14	1	C28	100pF		SM/C_0805
15	1	C30	47nF		SM/C_0805
16	1	C31	1000pF		SM/C_0805
17	1	C37	470pF		SM/C_0805
18	1	C50	22nF		SM/C_0805
19	1	D1	ES1D	Diodes Inc. ES1D-13	SM/_SMA
20	10	D2,D5,D6,D9, D10,D11,D12,D20,D21,D22	1N5819HW	Diodes Inc. 1N5819HW-7	SOD123
21	1	D14	B130L	Diodes Inc. B130L-13	SMA
22	1	D15	SMAJ20A	Diodes Inc. SMAJ120A-13	SMA
23	1	L1	1.3uH	Panasonic, ETQPAF1R3E	PCC-S1
24	4	M1,M2,M3,M4	si4842dy	Vishay	SO-8
25	2	M5,M6	si4490dy	Vishay	SO-8
26	1	Q1	Si2320DS	Vishay	SM/SOT23_123
27	1	R1	39K		SM/R_0805
28	2	R2,R26	10		SM/R_0805
29	2	R3,R37	5.1		SM/R_0805
30	6	R4,R6,R11,R17,R18,R38	10K		SM/R_0805
31	2	R5, R8	4.7		SM/R_0805

Evaluation Board Bill of Materials

Item	Quantity	Reference	Part	Manufacturer #	Foot Print
32	1	R10	412		SM/R_0805
33	1	R12	22		SM/R_0805
34	1	R13	10.0K		SM/R_0805
35	1	R14	37.4K		SM/R_0805
36	1	R15	18.2K		SM/R_0805
37	1	R19	21.5K		SM/R_0805
38	1	R21	160K		SM/R_0805
39	1	R22	40.2K		SM/R_0805
40	1	R23	43K		SM/R_0805
41	1	R24	6.19K		SM/R_0805
42	1	R25	110K		SM/R_0805
43	3	R27,R30,R33	100K		SM/R_0805
44	1	R28	2.7MEG		SM/R_0805
45	3	R29	68		SM/R_0805
46	1	R31	383K		SM/R_0805
47	1	R32	51		SM/R_0805
48	1	R34	1		SM/R_0805
49	1	R35	4.7K		SM/R_0805
50	1	R36	130K		SM/R_0805
51	2	R50,R51	10		SM/R_0805
52	1	R52	1.0K		SM/R_0805
53	1	T1	PA0168	Pulse	XP4
54	1	T2	P8208T	Pulse	P8208
55	1	T3	PE68386	Pulse	PE68386
56	1	T4	31414R	Midcom	
57	2	U2, U4	SC1302A	Semtech	SOT23_5PIN
58	1	U3	SC4431	Semtech	SOT23_5PIN
59	1	U5	SC4910	Semtech	TSSOP-20
60	1	U6	SC4911	Semtech	MSOP-8

Outline Drawing - TSSOP-20

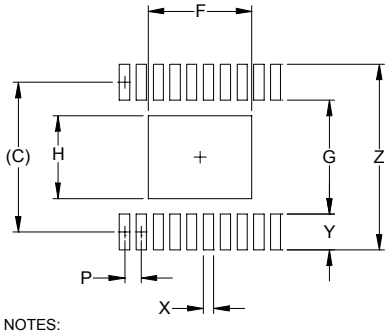


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.251	.255	.259	6.40	6.50	6.60
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	20			20		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20



DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
F	.157	4.00
G	.161	4.10
H	.126	3.20
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804