System Power Supply ICs for CCD Camera of Mobile Phones

Power Supply for CCD Camera Module

BD6029GU

No.10033EAT01

●Description

BD6029GU is system power supply LSI for CCD camera that supplies all voltage sources for CCD camera. This IC has Step up DC/DC converter and LDO for CCD sensor, Inverted DC/DC converter for CCD sensor, Series Regulators for DSP 3ch, CCD I/O 1ch and V-driver 1ch. Each output voltage has an adjustable to the register, and this IC can correspond to various CCD modules. A necessary power supply for CCD camera is integrated into 1chip, and it contributes to space saving. BD6029GU achieves compact size with the chip size package.

●Features

1) The BD6029GU is equipped with all voltage sources for CCD camera.
2) Each output has an adjustable voltage, and hence this IC can correspond to various CCD modules.
3) The BD6029GU has 3ch voltage regulators which have adjustable voltage for DSP, and hence BD6029GU can correspond to various DSP chip sets.
4) The BD6029GU has other 2ch voltage regulators for CCD I/O and V-driver.
5) The BD6029GU is controlled by I^2C BUS format.
6) The BD6029GU employs 4.35mm^2 chip size package, so this IC achieves compact size.

●Functions

1) Step up DC/DC converter and LDO for CCD sensor (+15V/+14.5V/+13V)
2) Inverted DC/DC converter for CCD sensor (-8V/-7.5V/-7V)
3) 5ch Series Regulator
   REG1 : 1.2V/1.8V, Iomax=150mA
   REG2 : 2.7V/3.0V/3.3V, Iomax=150mA
   REG5 : 1.8V/3.0V, Iomax=150mA
   REG6 : 3.0V/3.1V/3.2V/3.3V, Iomax=200mA
   REGA: 1.8V/3.0V/3.3, Iomax=150mA
4) Correspondence to I^2C BUS format
5) Thermal shutdown (Auto-reset type)
6) VCSP85H4 small package (chip size package)

●Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Ratings	Unit
Maximum Applied voltage 1	(Note 1)	VMAX1	20	V
Maximum Applied Voltage 2	(Note 2)	VMAX2	18	V
Maximum Applied Voltage 3	(Note 3)	VMAX3	-13.5	V
Maximum Applied Voltage 4	(Note 4)	VMAX4	6	V
Power Dissipation	(Note 5)	Pd	1925	mW
Operating Temperature Range		Topr	-30 ~ +85	°C
Storage Temperature Range		Tstg	-55 ~ +125	°C

(Note 1) SW, VPLUS1, VPLUS2 pin
(Note 2) VDD3 pin
(Note 3) VDD4 pin
(Note 4) Except Note1~Note3 pin
(Note 5) Power dissipation deleting is 15.4mW/°C, when it's used in over 25°C.
(It's deleting is on the board that is ROHM's standard)

●Recommended Operating Conditions (VBAT≥VIO, Ta=-30~85 °C)

Parameter	Symbol	Limits	Unit
VBAT input voltage	VBAT	2.7 ~ 5.5	V
VIO pin voltage	VIO	1.62 ~ 3.3	V

●**Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V/3.0V)**

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit Current						
VBAT Circuit current 1	IBAT1	-	0.1	3.0	μA	RST=0V, VIO=0V
VBAT Circuit current 2	IBAT2	-	0.5	3.0	μA	RST=0V
VBAT Circuit current 3	IBAT3	-	90	135	μA	REG1:ON, Io=0mA
VBAT Circuit current 4	IBAT4	-	90	135	μA	REG2:ON, Io=0mA
VBAT Circuit current 5	IBAT5	-	90	135	μA	REG5:ON, Io=0mA
VBAT Circuit current 6	IBAT6	-	90	135	μA	REG6:ON, Io=0mA
VBAT Circuit current 7	IBAT7	-	90	135	μA	REGA:ON, Io=0mA
VBAT Circuit current 8	IBAT8	-	9	14	mA	SWREG3:ON,REG3:ON, SWREG4:ON, Io=0mA
SWREG3 (Step up DC/DC)						
Output voltage 1	VoPD1	-	17.0	-	V	Io=60mA
Output voltage 2	VoPD2	-	16.5	-	V	Io=60mA
Output voltage 3	VoPD3	-	14.5	-	V	Io=60mA
Output current	IoPD	-	-	60	mA	(Note 6)
Efficiency	EffPD	-	(80)	-	%	Io=60mA (Note 6)
Oscillator frequency	foscPD	0.8	1.0	1.2	MHz	
SW saturation voltage	VsatPD	-	200	400	mV	Iin=200mA
Over voltage protection	OvPD	18.0	18.5	19.0	V	
Over current protection	OcPD	1.0	1.25	1.5	A	
SWREG4 (Inverted DC/DC)						
Output voltage 1	VoND1	-8.4	-8.0	-7.6	V	Io=100mA
Output voltage 2	VoND2	-7.9	-7.5	-7.1	V	Io=100mA
Output voltage 3	VoND3	-7.4	-7.0	-6.6	V	Io=100mA
Output current	IoND	-	-	100	mA	(Note 6)
Efficiency	EffND	-	(75)	-	%	Io=100mA (Note 6)
Oscillator frequency	foscND	0.8	1.0	1.2	MHz	
Over voltage protection	OvND	-10.5	-10.0	-9.5	V	
Over current protection	OcND	1.0	1.25	1.5	A	
Electric discharge resister at OFF	ROFFN	0.5	1.0	1.5	kΩ	

(Note 6) The power efficiency changes with the fluctuation of external parts and the board mounting condition.

●**Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V/3.0V)**

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
REG1 (1.2V/1.8V LDO)						
Output voltage 1	Vo11	1.140	1.20	1.260	V	Io=150mA
Output voltage 2	Vo12	1.746	1.80	1.854	V	Io=150mA
Output current	Io1	-	-	150	mA	Vo=1.8V
Load stability	ΔVo11	-	10	60	mV	Io=1~150mA, Vo=1.8V
Input stability	ΔVo12	-	10	60	mV	VBAT=3.2~4.5V, Io=100mA, Vo=1.8V
Ripple rejection ratio	RR1	-	65	-	dB	f=100Hz, Vin=200mVp-p, Vo=1.2V Io=50mA, BW=20Hz~20kHz
Current over load limiter	Ilim01	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFF1	-	1.0	1.5	kΩ	
REG2 (2.7V/3.0V/3.3V LDO)						
Output voltage 1	Vo21	2.619	2.70	2.781	V	Io=150mA
Output voltage 2	Vo22	2.910	3.00	3.090	V	Io=150mA
Output voltage 3	Vo23	3.201	3.30	3.399	V	Io=150mA
Output current	Io2	-	-	150	mA	Vo=2.7V
I/O voltage difference	Vsat2	-	0.2	0.3	V	VBAT=2.5V, Io=150mA, Vo=2.7V
Load stability	ΔVo21	-	10	60	mV	Io=1~150mA, Vo=2.7V
Input stability	ΔVo22	-	10	60	mV	VBAT=3.4~4.5V, Io=50mA, Vo=2.7V
Ripple rejection ratio	RR2	-	60	-	dB	f=100Hz, Vin=200mVp-p, Vo=2.7V Io=50mA, BW=20Hz~20kHz
Current over load limiter	Ilim02	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFF2	-	1.0	1.5	kΩ	
REG3 (15V/14.5V/13V LDO)						
Output voltage 1	Vo31	14.05	14.5	14.95	V	Io=60mA
Output voltage 2	Vo32	14.55	15.0	15.45	V	Io=60mA
Output voltage 3	Vo33	12.55	13.0	13.45	V	Io=60mA
I/O voltage difference	Vsat3	-	0.32	0.5	V	VPLUS2=11V, Io=60mA
Load stability	ΔVo31	-	20	80	mV	Io=1～60mA
Input stability	ΔVo32	-	10	60	mV	VPLUS2=16.5～17.5V, Io=60mA
Output voltage temperature fluctuation rate	ΔVo33	-	±100	-	ppm/°C	Ta=-30℃～85℃, Io=60mA
Output ripple voltage	RR3	-	-	3	mVp-p	Io=60mA, BW=20Hz～80kHz(Note 7)
Current over load limiter	Ilim03	-	100	-	mA	Vo=0V
Discharge resister at OFF	ROFF3	0.5	1.0	1.5	kΩ	

(Note 7) BW: Band width

●**Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V/3.0V)**

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
REG5 (1.8V/3.0V LDO)						
Output voltage 1	Vo51	1.746	1.80	1.854	V	Io=150mA
Output voltage 2	Vo52	2.910	3.00	3.090	V	Io=150mA
Output current	Io5	-	-	150	mA	Vo=1.8V
I/O voltage difference	Vsat5	-	0.2	0.3	V	VBAT=2.5V, Io=150mA, Vo=3.0V
Load stability	ΔVo51	-	10	60	mV	Io=1~150mA, Vo=1.8V
Input stability	ΔVo52	-	10	60	mV	VBAT=3.3~4.5V, Io=80mA, Vo=1.8V
Ripple rejection ratio	RR5	-	65	-	dB	f=100Hz, Vin=200mVp-p, Vo=1.8V Io=50mA, BW=20Hz~20kHz
Current over load limiter	Ilim05	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFF5	-	1.0	1.5	kΩ	
REG6 (3.0V/3.1V/3.2V/3.3V LDO)						
Output voltage 1	Vo61	2.910	3.00	3.090	V	Io=200mA
Output voltage 2	Vo62	3.007	3.10	3.193	V	Io=200mA
Output voltage 3	Vo63	3.104	3.20	3.296	V	Io=200mA
Output voltage 4	Vo64	3.201	3.30	3.399	V	Io=200mA
Output current	Io6	-	-	200	mA	Vo=3.0V
I/O voltage difference	Vsat6	-	0.2	0.3	V	VBAT=2.5V, Io=200mA, Vo=3.0V
Load stability	ΔVo61	-	10	60	mV	Io=1~200mA, Vo=3.0V
Input stability	ΔVo62	-	10	60	mV	VBAT=3.4~4.5V, Io=200mA, Vo=3.0V
Ripple rejection ratio	RR6	-	60	-	dB	f=100Hz, Vin=200mVp-p, Vo=3.0V Io=50mA, BW=20Hz~20kHz
Current over load limiter	Ilim06	-	250	500	mA	Vo=0V
Discharge resister at OFF	ROFF6	-	1.0	1.5	kΩ	
REGA (1.8V/3.0V/3.3V LDO)						
Output voltage 1	VoA1	1.746	1.80	1.854	V	Io=150mA
Output voltage 2	VoA2	2.910	3.00	3.090	V	Io=150mA
Output voltage 3	VoA3	3.201	3.30	3.399	V	Io=150mA
Output current	IoA	-	-	150	mA	Vo=1.8V
I/O voltage difference	VsatA	-	0.2	0.3	V	VBAT=2.5V, Io=150mA, Vo=3.0V
Load stability	Δ VoA1	-	10	60	mV	Io=1~150mA, Vo=1.8V
Input stability	Δ VoA2	-	10	60	mV	VBAT=3.4~4.5V, Io=150mA, Vo=1.8V
Ripple rejection ratio	RRA	-	65	-	dB	f=100Hz, Vin=200mVp-p, Vo=1.8V Io=50mA, BW=20Hz~20kHz
Current over load limiter	Ilim0A	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFFA	-	1.0	1.5	kΩ	
I^2C Input (RST, SDA, SCL)						
LOW level input voltage	V_{IL}	-0.3	-	0.25VIO	V	
HIGH level input voltage	V_{IH}	0.75VIO	-	VIO+0.3	V	
Hysteresis of Schmitt trigger input	V_{hys}	0.05VIO	-	-	V	
LOW level output voltage (SDA) at 3mA sink current	V_{OL}	0	-	0.30	V	
Input current each I/O pin	I_i	-10	-	10	μA	input voltage between 0.1 VIO and 0.9 VIO

●Power Dissipation (On the ROHM's standard board)

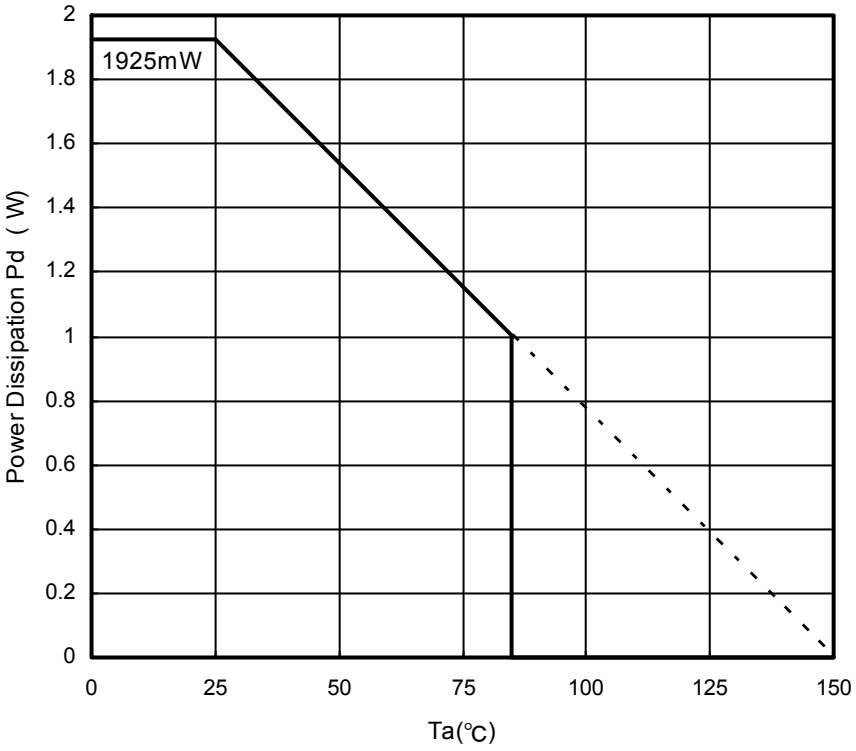
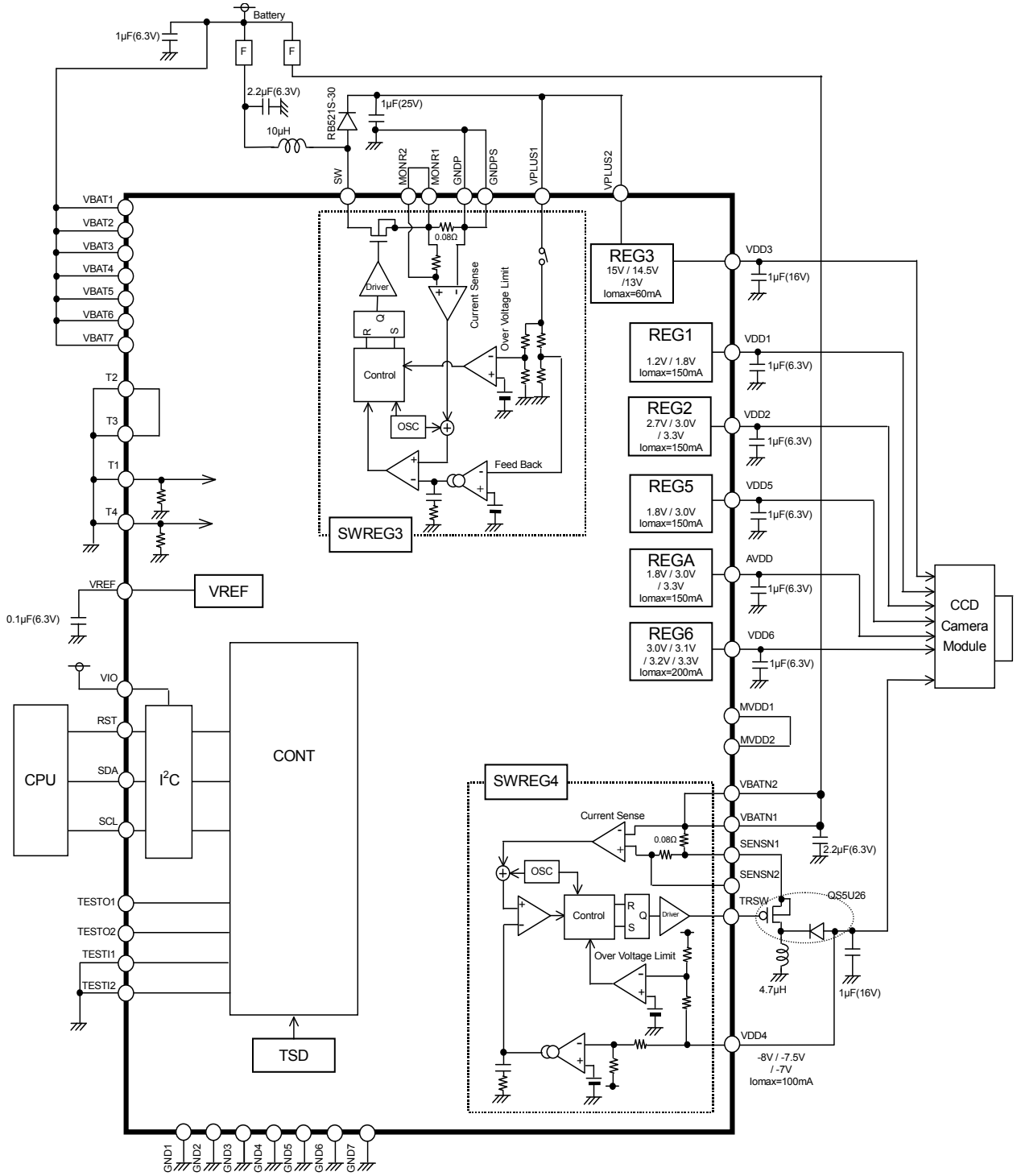


Fig.1 Power Dissipation

Information of the ROHM's standard board
Material : glass-epoxy
Size : 50mm × 58mm × 1.75mm (8 Layer)
Pattern of the board : Refer to P.18

●Block Diagram / Application Circuit example



Pin Connection

T1~T4, TESTI1, TESTI2	: GND short
TEST01, TEST02, MVDD1, MVDD2	: Open
Output of unused LDO	: Open
MONR1-MONR2 short	
MVDD1-MVDD2 short	

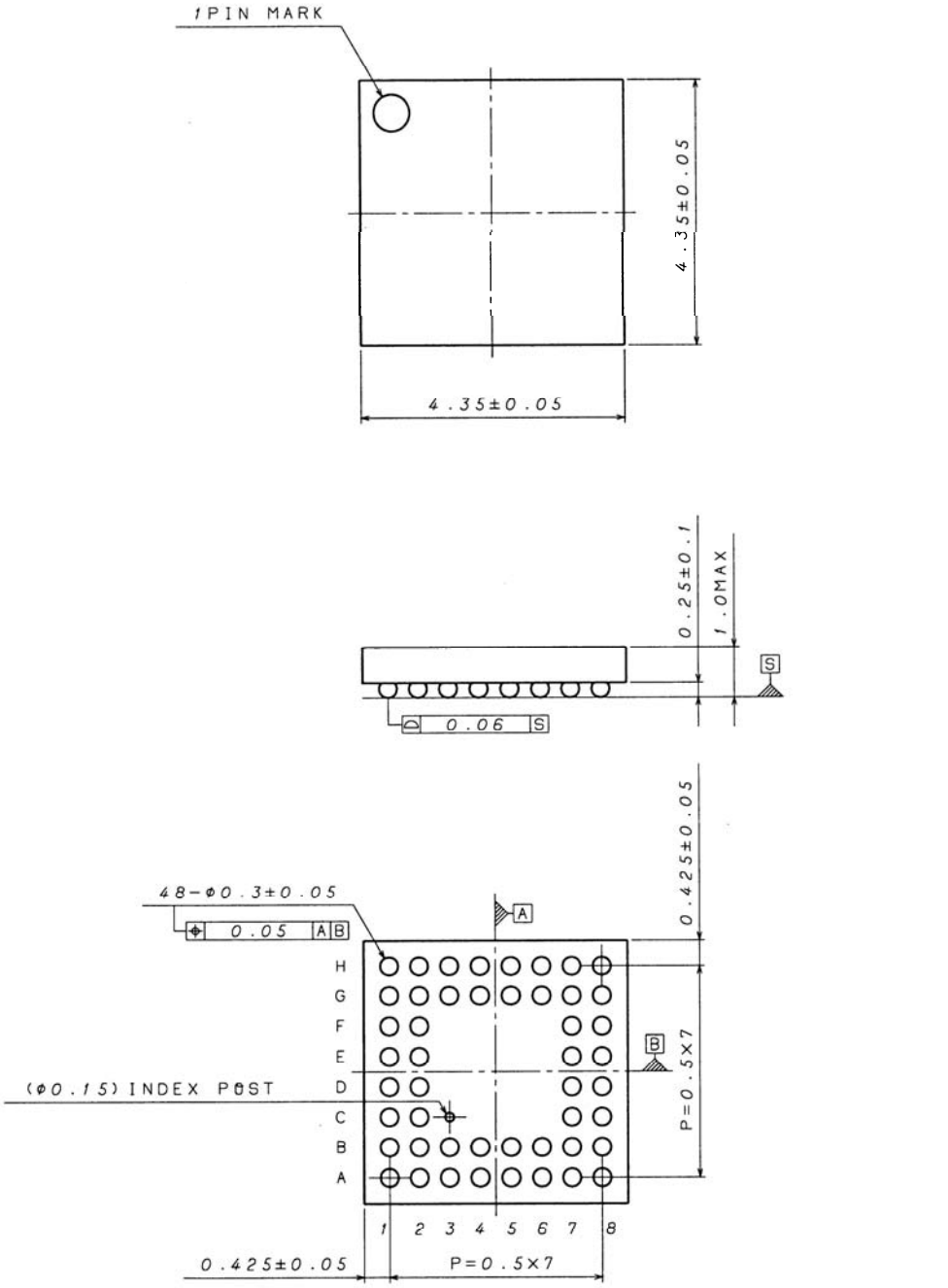
Fig.2 Block Diagram / Application Circuit example

●**Pin Configuration ［Bottom View］**

	1	2	3	4	5	6	7	8
H	T4	VDD3	VPLUS1	GNDP	MONR2	SW	GND6	T3
G	TESTI1	TESTI2	VPLUS2	GNDPS	MONR1	VBAT5	TESTO2	AVDD
F	RST	VIO					VBAT4	VDD5
E	GND7	SDA					VREF	GND5
D	VDD2	SCL					VBAT3	VDD1
C	VBAT6	VBAT7	○				VBAT2	VDD6
B	MVDD2	MVDD1	VBATN1	SENSN2	VBAT1	GND3	TESTO1	GND4
A	T1	GND1	VBATN2	SENSN1	TRSW	GND2	VDD4	T2

●Package Outline

VCSP85H4 (BU6029GU)



(unit:mm)

●**Pin Functions**

No	Pin No	Pin Name	I/O	Input Level	ESD Diode		Functions	Initial Conditions
					For Power	For GND		
1	B5	VBAT1	-	-	-	GND	Battery is connected	-
2	C7	VBAT2	-	-	-	GND	Battery is connected	-
3	D7	VBAT3	-	-	-	GND	Battery is connected	-
4	F7	VBAT4	-	-	-	GND	Battery is connected	-
5	G6	VBAT5	-	-	-	GND	Battery is connected	-
6	C1	VBAT6	-	-	-	GND	Battery is connected	-
7	C2	VBAT7	-	-	-	GND	Battery is connected	-
8	A1	T1	-	-	VBAT	GND	Test pin	-
9	A8	T2	-	-	-	GND	Test pin	-
10	H8	T3	-	-	-	GND	Test pin	-
11	H1	T4	-	-	VBAT	GND	Test pin	-
12	E7	VREF	O	-	VBAT	GND	Reference voltage output	0V output
13	F2	VIO	-	-	VBAT	GND	Power supply for logic	-
14	F1	RST	I	VIO	VIO	GND	Reset input	-
15	E2	SDA	I	VIO	VIO	GND	I^2C data input	-
16	D2	SCL	I	VIO	VIO	GND	I^2C clock input	-
17	A2	GND1	-	-	VBAT	-	Ground	-
18	A6	GND2	-	-	VBAT	-	Ground	-
19	B6	GND3	-	-	VBAT	-	Ground	-
20	B8	GND4	-	-	VBAT	-	Ground	-
21	E8	GND5	-	-	VBAT	-	Ground	-
22	H7	GND6	-	-	VBAT	-	Ground	-
23	E1	GND7	-	-	VBAT	-	Ground	-
24	H6	SW	O	-	-	GND	SWREG3 coil switching pin	Stop operating
25	H5	MONR2	I	-	VBAT	GND	SWREG3 current sense pin	-
26	G5	MONR1	I	-	VBAT	GND	SWREG3 current sense pin	-
27	H4	GNDP	I	-	VBAT	GND	SWREG3 current sense pin	-
28	G4	GNDPS	I	-	VBAT	GND	SWREG3 current sense pin	-
29	H3	VPLUS1	I	-	-	GND	SWREG3 boost voltage feedback pin	-
30	G3	VPLUS2	I	-	-	GND	Power supply input for REG3 (15.5V/14.5V/13V LDO)	-
31	H2	VDD3	O	-	VPLUS2	GND	REG3 (15.5V/14.5V/13V LDO) output pin	0V output
32	D8	VDD1	O	-	VBAT	GND	REG1 (1.2V/1.8V LDO) output pin	0V output
33	D1	VDD2	O	-	VBAT	GND	REG2 (2.7V/3.0V/3.3V LDO) output pin	0V output
34	F8	VDD5	O	-	VBAT	GND	REG5 (1.8V/3.0V LDO) output pin	0V output
35	G8	AVDD	O	-	VBAT	GND	REGA (1.8V/3.0V/3.3V LDO) output pin	0V output
36	C8	VDD6	O	-	VBAT	GND	REG6 (3.0V/3.1V/3.2V/3.3V LDO) output pin	0V output
37	B2	MVDD1	O	-	VBAT	GND	NC	-
38	B1	MVDD2	O	-	VBAT	GND	NC	-
39	B7	TESTO1	O	-	VBAT	GND	Test pin	-
40	G7	TESTO2	O	-	VBAT	GND	Test pin	-
41	G1	TESTI1	I	-	VIO	GND	Test pin	-
42	G2	TESTI2	I	-	VIO	GND	Test pin	-
43	A3	VBATN2	I	-	VBAT	GND	Battery is connected (SWREG4 current sense)	-
44	B3	VBATN1	I	-	VBAT	GND	Battery is connected (SWREG4 current sense)	-
45	A4	SENSN1	I	-	VBAT	GND	SWREG4 current sense pin	-
46	B4	SENSN2	I	-	VBAT	GND	SWREG4 current sense pin	-
47	A5	TRSW	O	-	VBAT	GND	SWREG4 switching Tr. drive pin	Stop operating
48	A7	VDD4	O	-	GND	-	SWREG4 (-8V/-7.5V/-7V) output pin	0V output

Total: 48Pin

●I²C BUS format

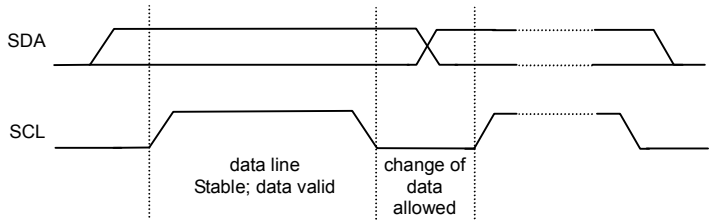
The writing/reading operation is based on the I²C slave standard.

◦ Slave address

A7	A6	A5	A4	A3	A2	A1	R/W
0	0	0	1	0	0	1	1/0

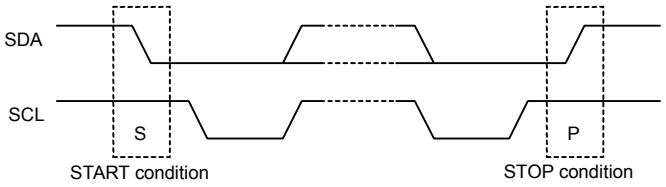
◦ Bit Transfer

SCL transfers 1-bit data during H. SCL cannot change signal of SDA during H at the time of bit transfer. If SDA changes while SCL is H, START conditions or STOP conditions will occur and it will be interpreted as a control signal.



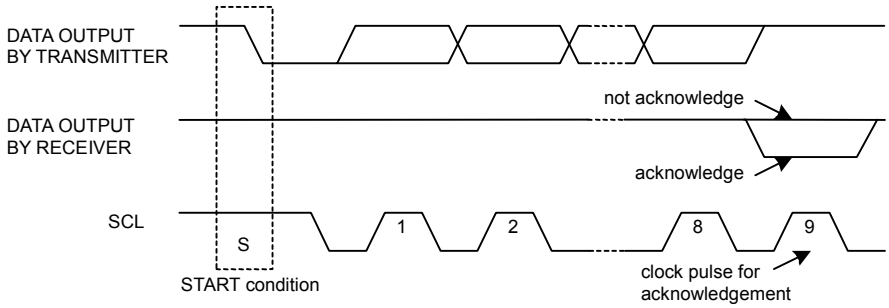
◦ START and STOP condition

When SDA and SCL are H, data is not transferred on the I²C- bus. This condition indicates, if SDA changes from H to L while SCL has been H, it will become START (S) conditions, and an access start, if SDA changes from L to H while SCL has been H, it will become STOP (P) conditions and an access end.



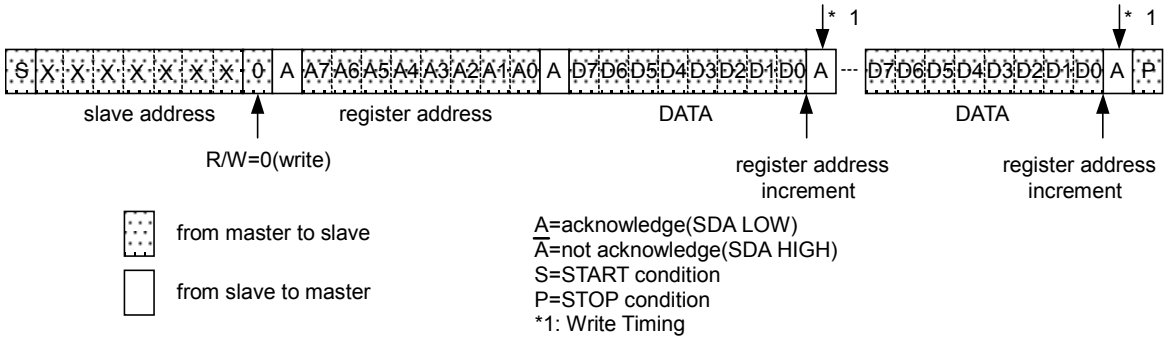
◦ Acknowledge

It transfers data 8 bits each after the occurrence of START condition. A transmitter opens SDA after transfer 8bits data, and a receiver returns the acknowledge signal by setting SDA to L.



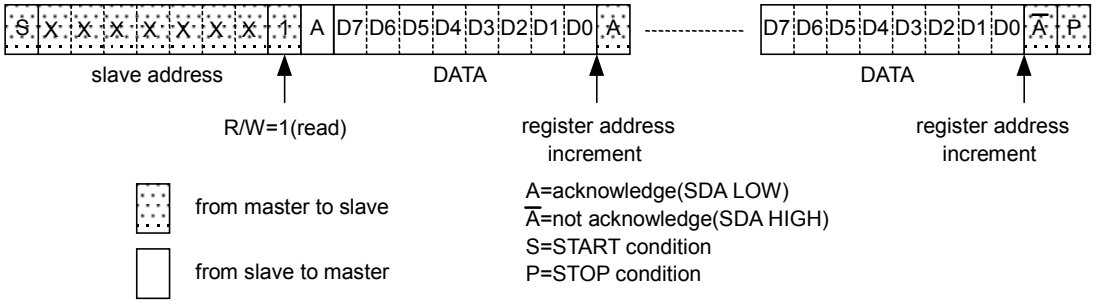
◦ Writing protocol

A register address is transferred by the next 1 byte that transferred the slave address and the write-in command. The 3rd byte writes data in the internal register written in by the 2nd byte, and after 4th byte or, the increment of register address is carried out automatically. However, when a register address turns into the last address(07h), it is set to 00h by the next transmission. After the transmission end, the increment of the address is carried out.



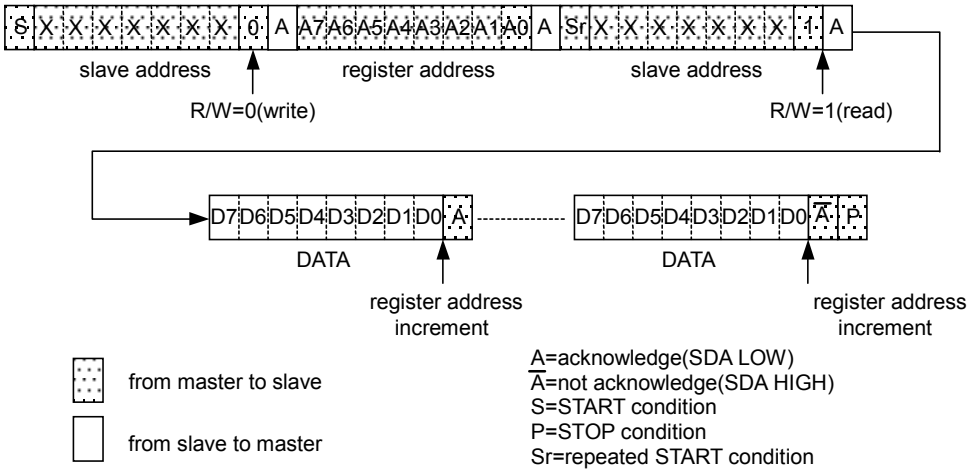
◦ Reading protocol

It reads from the next byte after writing a slave address and R/W bit. The register to read considers as the following address accessed at the end, and the data of the address that carried out the increment is read after it. If an address turns into the last address(07h), the next byte will read out 00h. After the transmission end, the increment of the address is carried out.



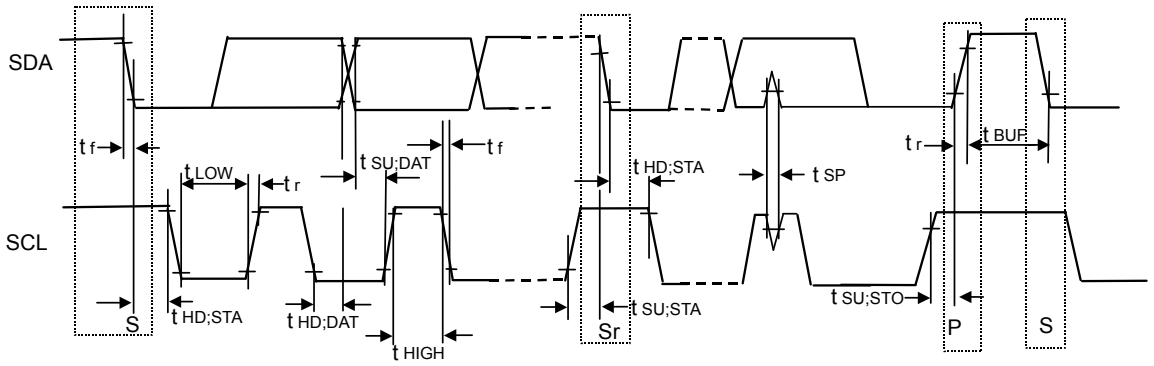
◦ Multiple reading protocols

After specifying an internal address, it reads by repeated START condition and changing the data transfer direction. The data of the address that carried out the increment is read after it. If an address turns into the last address, the next byte will read out 00h. After the transmission end, the increment of the address is carried out.



As for reading protocol and multiple reading protocols, please do A(not acknowledge) after doing the final reading operation. It stops with read when ending by A(acknowledge), and SDA stops in the state of Low when the reading data of that time is 0. However, this state returns usually when SCL is moved, data is read, and A(not acknowledge) is done.

●**Timing Diagram**



●**Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V/3.0V)**

Parameter	Symbol	Standard-mode			Fast-mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I²C BUS format								
SCL clock frequency	f_{SCL}	0	-	100	0	-	400	kHz
LOW period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	µs
Hold time (repeated) START condition After this period, the first clock is generated	$t_{HD;STA}$	4.0	-	-	0.6	-	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	-	0.6	-	-	µs
Data hold time	$t_{HD;DAT}$	0	-	3.45	0	-	0.9	µs
Data set-up time	$t_{SU;DAT}$	250	-	-	100	-	-	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	-	0.6	-	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	µs

●Register List

-	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	Function
Address									Register data								
8bit	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
00h	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	SFTRST	Software reset
01h	0	0	0	0	0	0	0	1	-	REGAPD	REG6PD	REG5PD	SWREG4 PD	REG3PD	REG2PD	REG1PD	Power down
02h	0	0	0	0	0	0	1	0	SWREG4 VSEL1	SWREG4 VSEL0	REG3 VSEL1	REG3 VSEL0	REG2 VSEL1	REG2 VSEL0	REG1 VSEL1	REG1 VSEL0	Output Voltage Setting 1
03h	0	0	0	0	0	0	1	1	-	-	REGA VSEL1	REGA VSEL0	REG6 VSEL1	REG6 VSEL0	REG5 VSEL1	REG5 VSEL0	Output Voltage Setting 2
04h	0	0	0	0	0	1	0	0	-	-	-	-	-	-	-	-	(reserved)
05h	0	0	0	0	0	1	0	1	-	-	-	-	-	-	-	-	(reserved)
06h	0	0	0	0	0	1	1	0	-	-	-	-	-	-	-	-	(reserved)
07h	0	0	0	0	0	1	1	1	reserved								for TEST
08h	0	0	0	0	1	0	0	0	reserved								for TEST

●Register Map

Address 00h <Software reset>

BIT	Name	Initial	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	-	-	-	-
D2	-	-	-	-
D1	-	-	-	-
D0	SFTRST	0	Reset cancel	Reset

Address 01h <Power down>

BIT	Name	Initial	Function	
			0	1
D7	-	-	-	-
D6	REGAPD	0	REGA power OFF	REGA power ON
D5	REG6PD	0	REG6 power OFF	REG6 power ON
D4	REG5PD	0	REG5 power OFF	REG5 power ON
D3	SWREG4PD	0	SWREG4 power OFF	SWREG4 power ON
D2	REG3PD	0	REG3 power OFF	REG3 power ON
D1	REG2PD	0	REG2 power OFF	REG2 power ON
D0	REG1PD	0	REG1 power OFF	REG1 power ON

Address 02h <Output Voltage Setting 1>

BIT	Name	Initial	Function	
			0	1
D7	SWREG4VSEL1	0		
D6	SWREG4VSEL0	0		
D5	REG3VSEL1	0		
D4	REG3VSEL0	0		
D3	REG2VSEL1	0		
D2	REG2VSEL0	0		
D1	REG1VSEL1	0		
D0	REG1VSEL0	0		

SWREG4VSEL1	SWREG4VSEL0	SWREG4 output
0	0	-8V
0	1	-7.5V
1	0	-7V
1	1	-(prohibition of use)

REG3VSEL1	REG3VSEL0	REG3 output
0	0	14.5V
0	1	15V
1	0	13V
1	1	-(prohibition of use)

REG2VSEL1	REG2VSEL0	REG2 output
0	0	3.3V
0	1	-(prohibition of use)
1	0	3.0V
1	1	2.7V

REG1VSEL1	REG1VSEL0	REG1 output
0	0	-
0	1	1.8V
1	0	1.2V
1	1	1.2V

Address 03h <Output Voltage Setting 2>

BIT	Name	Initial	Function	
			0	1
D7	-	-		
D6	-	-		
D5	REGAVSEL1	0		
D4	REGAVSEL0	0		
D3	REG6VSEL1	0		
D2	REG6VSEL0	0		
D1	REG5VSEL1	0		
D0	REG5VSEL0	0		

REGAVSEL1	REGAVSEL0	REGA output
0	0	3.3V
0	1	-(prohibition of use)
1	0	3.0V
1	1	1.8V

REG6VSEL1	REG6VSEL0	REG6 output
0	0	3.3V
0	1	3.1V
1	0	3.0V
1	1	3.2V

REG5VSEL1	REG5VSEL0	REG5 output
0	0	3.0V
0	1	-(prohibition of use)
1	0	1.8V
1	1	1.8V

●Explanation for Operate

1. Reset
   There are two kinds of reset, Software reset and Hardware reset.
   (1) Software reset
   - It shifts to software reset with changing a register (SFTRST) setting “0” → “1”.
   - I The register is returned to the initials value under the state of Soft Reset, and it stops accepting all address except for SFTRST.
   - I It’s possible to release from a state of Soft Reset by setting register “1” → “0”.

   (2) Hardware reset
   - I It shifts to hard reset by changing RST pin “H” → “L”.
   - I The condition of all registers under Hardware Reset pin is returned to the initial value, and it stops accepting all address.
   - I It’s possible to release from a state of hardware reset by setting register “L” → “H”.

   (3) Reset Sequence
   - I When hardware reset was done during software reset, Software reset is canceled when hard reset is canceled. (Because the initial value of Soft Reset is “0”)

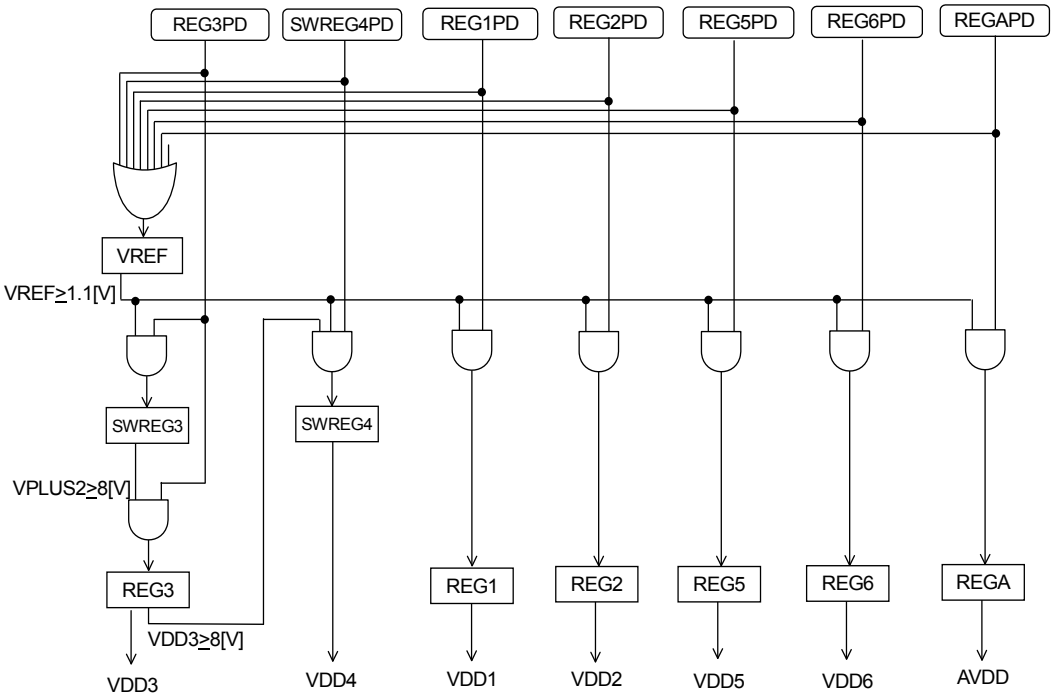
2. Thermal shutdown
   The blocks which thermal shutdown function is effective in
   SWREG3 (Step up DC/DC converter)
   SWREG4 (Inverted DC/DC converter)
   REG1
   REG2
   REG3
   REG5
   REG6
   REGA

   A thermal shutdown function works in about 175 ^{o}C. (Design reference value)

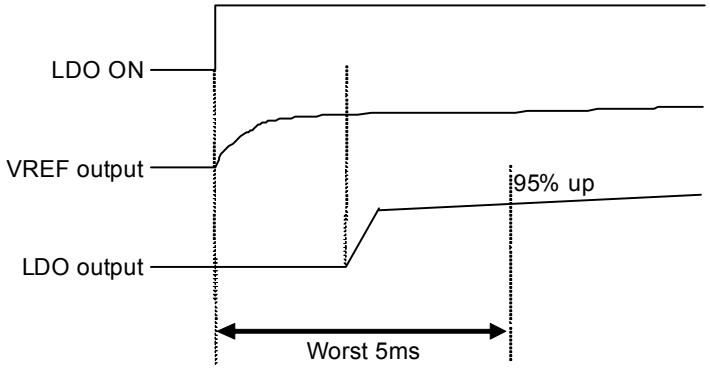
3. Sequencer block

The sequencer block does the power control (like VREF is turned on → SWREG3 is turned on → REG3 is turned on) on the following condition corresponding to resister condition and output voltage of each block.

Block	POWER ON Condition	POWER OFF Condition
VREF	Any one of REG3PD to REGAPD = H	REG3PD to REGAPD = all L
SWREG3	REG3PD = H and VREF ≥ 1.1V	REG3PD=L
REG3	REG3PD = H and VPLUS2 ≥ 8V	REG3PD=L
SWREG4	SWREG4PD = H, VDD3 ≥ 8V and VREF ≥ 1.1V	SWREG4PD=L
REG1	REG1PD = H and VREF ≥ 1.1V	REG1PD=L
REG2	REG2PD = H and VREF ≥ 1.1V	REG2PD=L
REG5	REG5PD = H and VREF ≥ 1.1V	REG5PD=L
REG6	REG6PD = H and VREF ≥ 1.1V	REG6PD=L
REGA	REGAPD = H and VREF ≥ 1.1V	REGAPD=L



When a thermal shutdown hangs, the whole block except for VREF turns off the power.
When it reverts from the thermal shutdown, it starts from the sequence after VREF ON in the above pattern.
The start of SWREG4 (CCD negative power supply) requires the rise-up of REG3 (CCD positive power supply).
This requirement is valid for the reversion from the thermal shutdown and the short circuit.
Detection voltage of VREF's rise-up is 1.1V when static output is 1.2V.
As shown in the former page description, VREF receives a turning on instruction blocked either each and beginsrise up.
Therefore, it is necessary to consider the block started up first at the rise time of VREF.

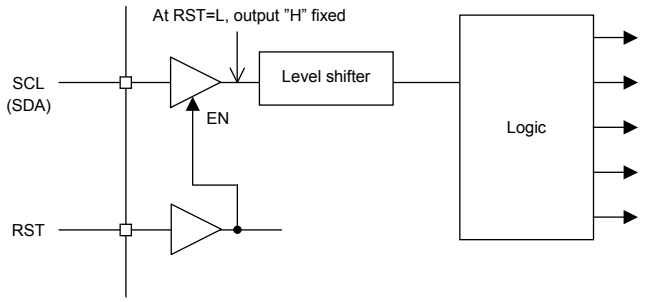


4. I2C BUS

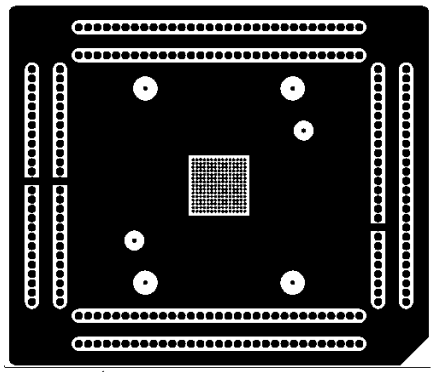
Operation when a signal beyond f_{SCL}=400kHz is input cannot be guaranteed, because this LSI doesn't correspond to the H/S(High Speed) mode of the I^2C BUS format.

When it uses on the serial-bus-system which the F/S(Fast Speed) mode was mixed in with the H/S mode, please connect it and remove a connection by using the mutual connection bridge from the H/S mode section to F/S mode section or in that reverse direction.

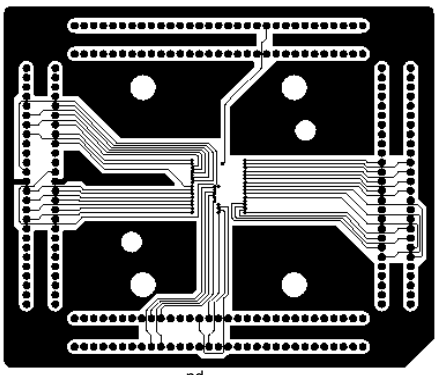
However, an optional input signal never spreads to the logic part of IC, because it stops the operation of the input buffer of SDA and SCL at RST pin=L.



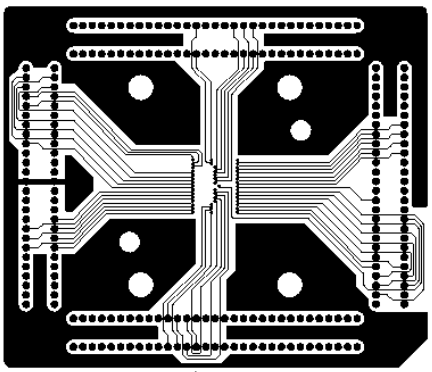
●PCB Pattern of the Power Dissipation Measuring Board



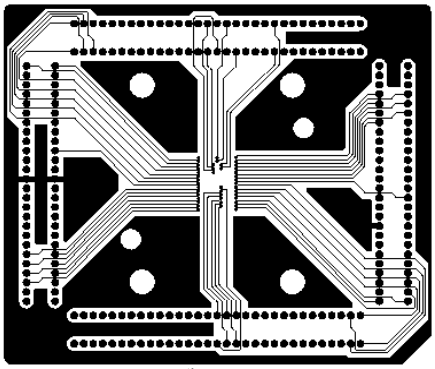
1st layer(component)



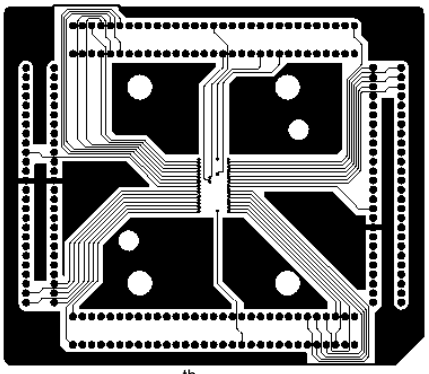
2nd layer



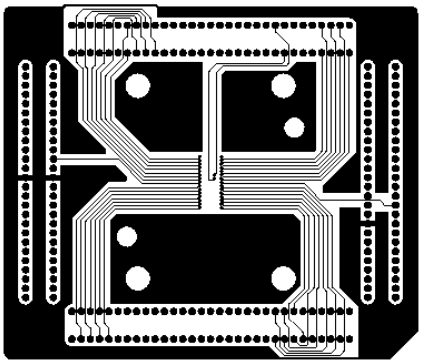
3rd layer



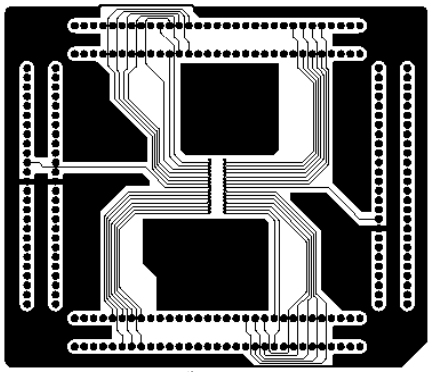
4th layer



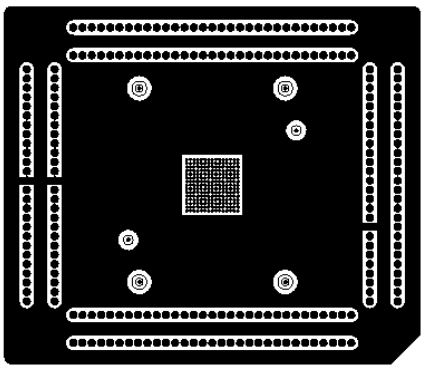
5th layer



6th layer



7th layer



8th layer(solder)

●Ordering part number

B	D	6	0	2	9	G	U	-	E	2

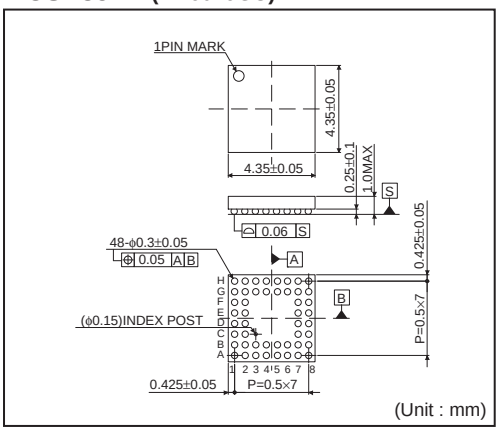
Part No. (BD)

Part No. (6029)

Package
GU: VCSP85H4

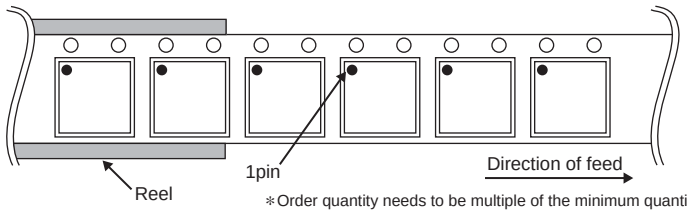
Packaging and forming specification
E2: Embossed tape and reel

VCSP85H4 (BD6029GU)



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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