*New Jersey Semi-Conductor Products, Inc.*

**20 STERN AVE.**
**SPRINGFIELD, NEW JERSEY 07081**
**U.S.A.**

**TELEPHONE: (973) 376-2922**
**(212) 227-6005**
**FAX: (973) 376-8960**

# 2N4203

## Silicon Controlled Rectifier
### Reverse Blocking Triode Thyristor

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Reverse Blocking Voltage (1) ($T_J$ = 105°C) | $V_{RRM}$ | 50 | Volts |
| *Peak Forward Blocking Voltage (1) ($T_C$ = 105°C) | | 700 | |
| Repetitive Peak On-State Current (PW = 3 μs, Duty Cycle = 0.6%, [illegible] 85°C) | $I_{TRM}$ | 100 | Amps |
| Continuous On-State Current ($T_C$ [illegible] 85°C) | $I_T$ | 5 | Amps |
| Current Application Rate (2) | di/dt | 5000 | A/μs |
| Peak Forward Gate Power | $P_{GFM}$ | 20 | Watts |
| Average Forward Gate Power | $P_{GF(AV)}$ | 1 | Watt |
| Peak Forward Gate Current | $I_{GFM}$ | 5 | Amps |
| Peak Gate Voltage — Forward<br>Reverse (3) | $V_{GFM}$<br>$V_{GRM}$ | 10<br>10 | Volts |
| Operating Junction Temperature Range<br>Blocking State<br>Conducting State | $T_J$ | <br>−65 to +105<br>−65 to +200 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +200 | °C |
| Stud Torque | — | 15 | in. lb. |

*JEDEC Registered Data.

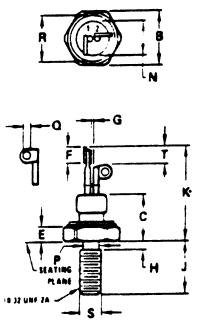
(1) Characterized for unilateral applications where reverse blocking capability is not important. Higher voltage units available upon request. $V_{DRM}$ and $V_{RRM}$ may be applied as a continuous dc voltage for zero or negative gate voltage but positive gate voltage must not be applied concurrently with a negative potential on the anode. When checking blocking capability, do not permit the applied voltage to exceed the rated voltage.

(2) Minimum Gate Trigger Pulse: $i_G$ = 200 mA, PW = 1 μs, $t_r$ = 20 ns.

(3) Do not reverse bias gate during forward conduction if anode current exceeds 10 amperes.

**Designers Data for "Worst Case" Conditions** — The Designers Data Sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

**TO-64**




NOTE:
1. ALL RULES & NOTES ASSOCIATED WITH REFERENCED TO-64 OUTLINE SHALL APPLY.

STYLE 1.
PIN 1 CATHODE
2. GATE
STUD – ANODE

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| B | 10.77 | 11.10 | 0.424 | 0.437 |
| C | 7.62 | 10.16 | 0.300 | 0.400 |
| E | 1.52 | 4.45 | 0.060 | 0.175 |
| F | 2.03 | 3.45 | 0.080 | 0.136 |
| G | 0.33 | – | 0.013 | – |
| H | – | 1.98 | – | 0.078 |
| J | 10.16 | 11.51 | 0.400 | 0.453 |
| K | 17.78 | 21.72 | 0.700 | 0.855 |
| N | – | 10.77 | – | 0.424 |
| P | 4.14 | 4.80 | 0.163 | 0.189 |
| Q | 1.02 | 1.91 | 0.040 | 0.075 |
| R | 10.16 | – | 0.400 | – |
| S | 4.212 | 4.310 | 0.1658 | 0.1697 |
| T | 1.52 | – | 0.060 | – |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted.)

| Characteristic | Fig. No. | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| *Peak Forward or Reverse Blocking Current<br>(Rated $V_{DRM}$ or $V_{RRM}$, gate open) $T_J$ = 25°C<br>$T_J$ = 105°C | 17 | $I_{DRM}$, $I_{RRM}$ | —<br>— | 10<br>2 | μA<br>mA |
| Gate Trigger Current (Continuous dc)<br>(Anode Voltage = 7 Vdc, $R_L$ = 100 ohms, $T_C$ = 25°C)<br>*(Anode Voltage = 7 Vdc, $R_L$ = 100 ohms, $T_C$ = −65°C) | 14 | $I_{GT}$ | —<br>— | 50<br>100 | mA |
| Gate Trigger Voltage (Continuous dc)<br>*(Anode Voltage = rated $V_{DRM}$, $R_L$ = 100 ohms, $T_C$ = 105°C)<br>(Anode Voltage = 7 Vdc, $R_L$ = 100 ohms, $T_C$ = 25°C)<br>*(Anode Voltage = 7 Vdc, $R_L$ = 100 ohms, $T_C$ = −65°C) | 12 | $V_{GT}$ | 0.2<br>—<br>— | —<br>1.5<br>2 | Volts |
| *Holding Current<br>(Anode Voltage = 7 Vdc, gate open, $T_C$ = 105°C) | 18 | $I_H$ | 3 | — | mA |
| *Forward "On" Voltage<br>($I_{TM}$ = 5 Adc, PW = 1 ms max, Duty cycle ≤ 1%) | 8 | $V_{TM}$ | 2.6 | — | Volts |
| *Dynamic Forward "On" Voltage<br>(0.5 μs after 50% decay point on dynamic forward voltage waveform)<br>Forward Current: 30 A pulse<br>Gate Pulse: at 200 mA, PW = 1 μs, $t_r$ = 20 ns | 7 | $V_{TM}$ | — | 25 | Volts |
| *Turn-On Time (2) $I_{TM}$ = 30 A<br>Delay Time — All types<br>Rise Time — 2N4203 and 2N4204 | <br>1, 9<br>1, 11 | <br>$t_d$<br>$t_r$ | <br>—<br>— | <br>200<br>100 | ns |
| *Pulse Turn-Off Time<br>Test Conditions: PFN discharge; Forward Current = 30 A pulse; Reverse Current = 5 A, $T_C$ = 85°C, dv/dt = 250 V/μs to Rated $V_{DRM}$; Reverse anode voltage during turn-off interval = 0 V; Reverse gate bias during turn-off interval = 5 V | 2, 13 | $t_q$ | — | 20 | μs |
| *Forward Voltage Application Rate (Linear Rise Voltage)<br>($T_C$ = 105°C, gate open, $V_D$ = Rated $V_{DRM}$) | 16 | dv/dt | 250 | — | V/μs |

*$V_{DRM}$ for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. When checking forward or reverse blocking capability, these devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage. Other voltage units available upon request.