Empowered by Innovation NEC

Analog/Digital Mixed ASIC

MIXED SIGNAL ASIC

MA-8A, MA-9 Family

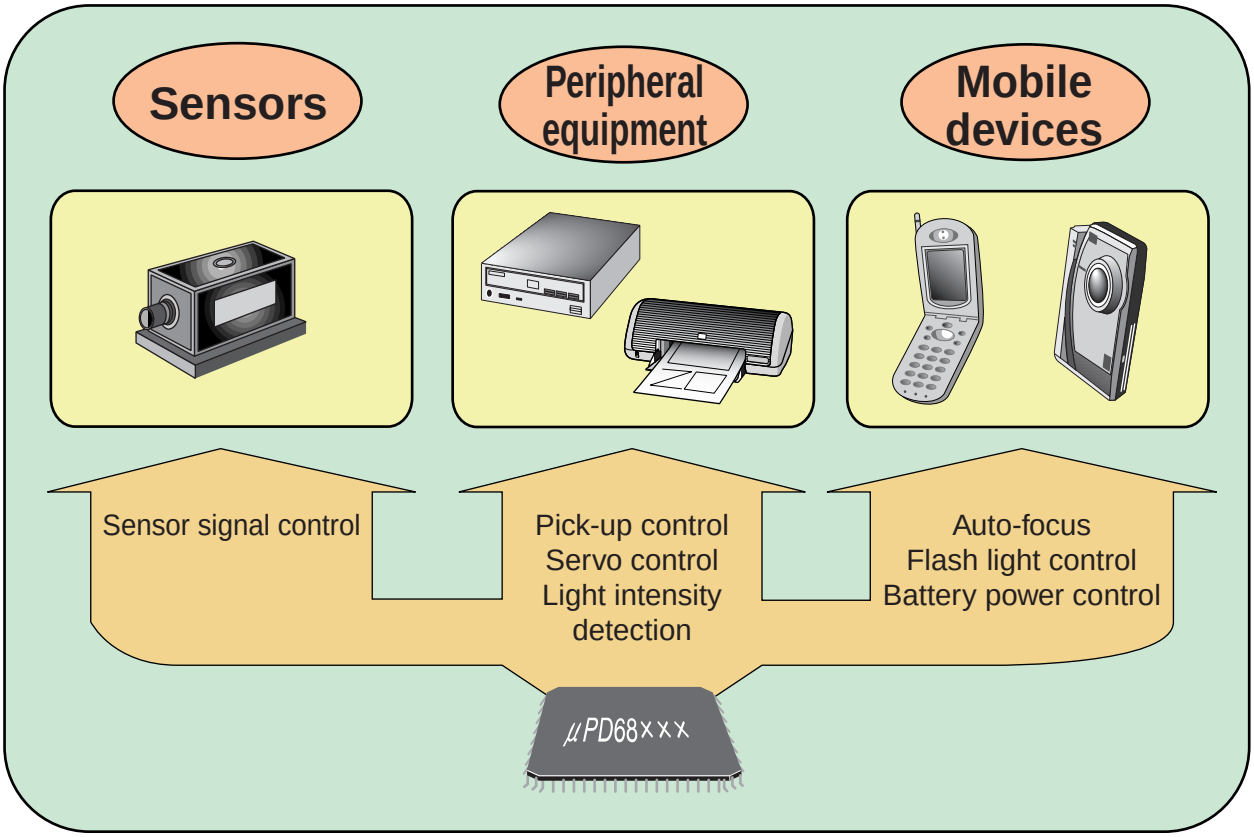
June 2003

CONTENTS

NEC Electronics' mixed signal solutions
Taking on New Challenges Toward the Next Generation

Mixed Signal Applications

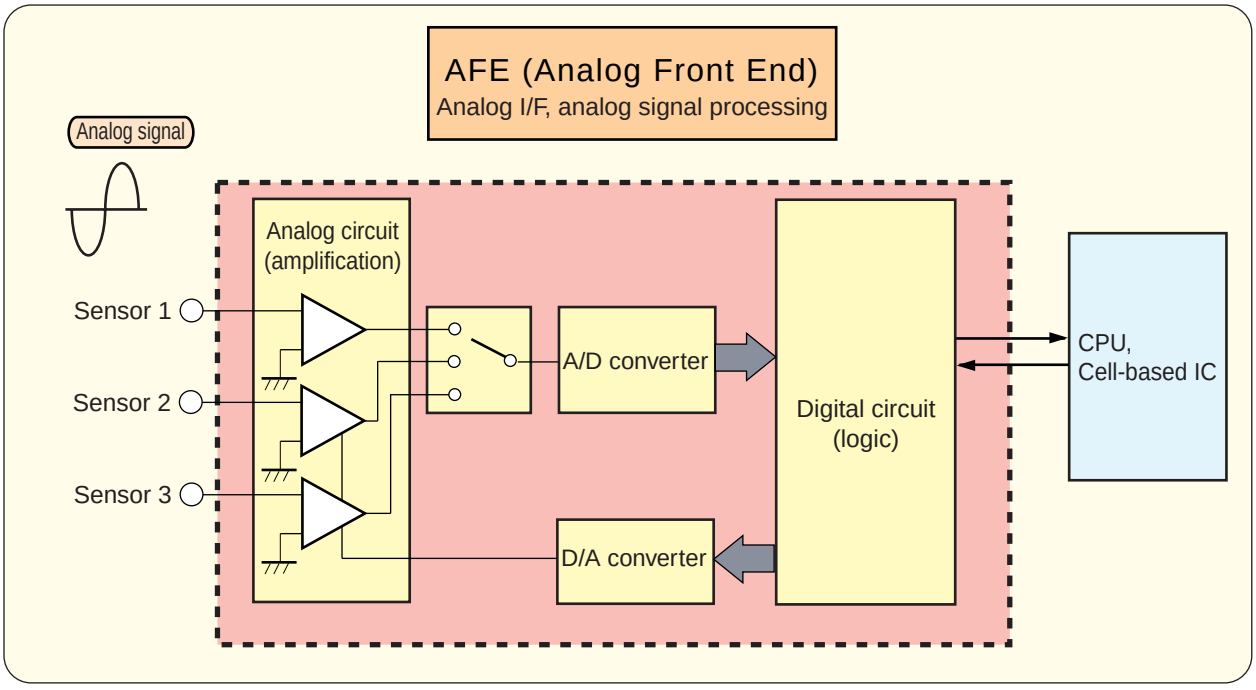
Mixed signal ASICs enable higher quality and a better cost performance in AFE (analog front end) circuits and battery management circuits for applications such as sensors, PC peripheral equipment, and mobile devices.

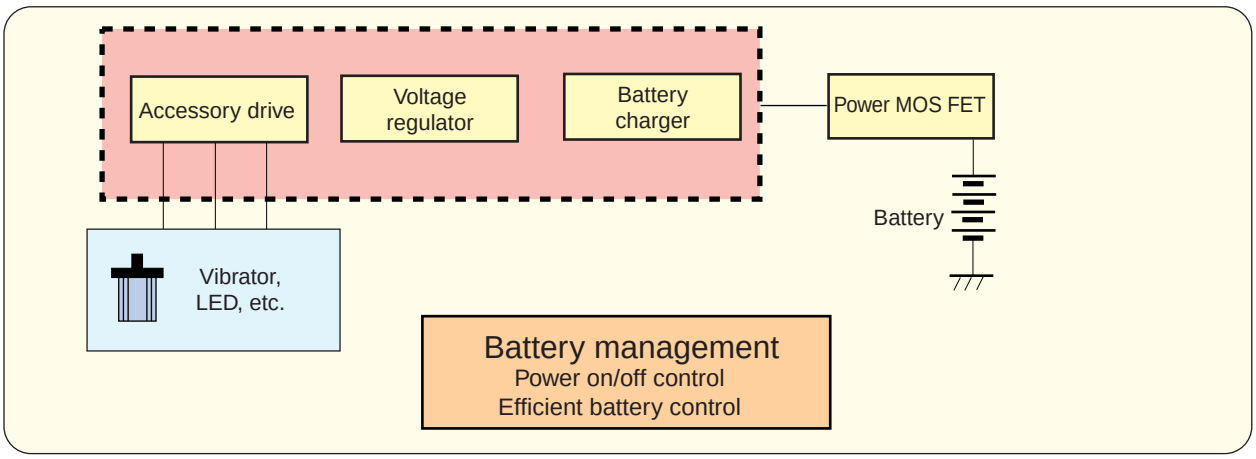


Application Concept

Applications dealing with "minute analog signal input in a wide band" require signal amplifiers or analog-digital arithmetic circuits (analog front end: AFE) for the analog interface. Also, for mobile equipment, the need to extend the battery life means an improved power efficiency is essential.

NEC Electronics provides a custom-built battery management IC for cellular phones and other mobile applications.





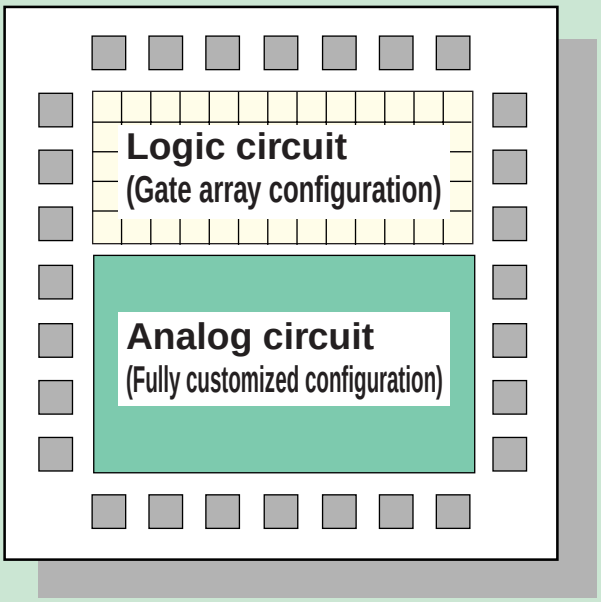
Mixed Signal ASIC Product Lines

NEC Electronics offers mixed signal ASICs that employ a BiCMOS process with a process rule of 0.65 μm to 0.35 μm. Furthermore, the 0.35 μm BiCMOS can incorporate our 0.35 μm cell-based IC CB-9 Family VX Type analog core.

MA-8A (μPD688××)

0.65 μm BiCMOS process

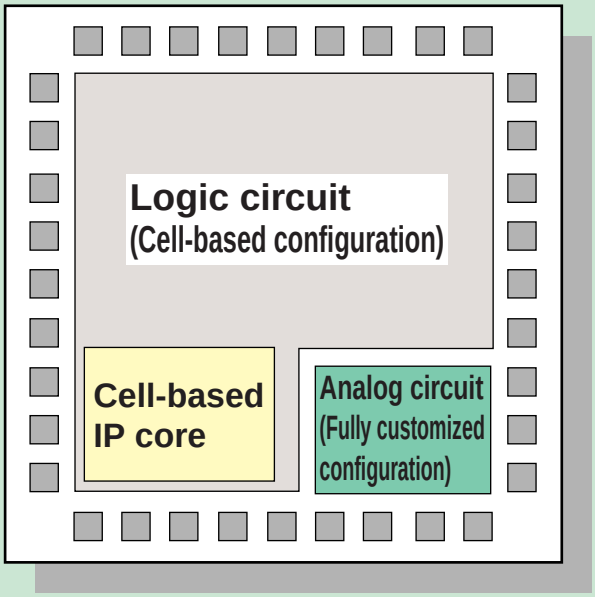
5 V power supply
(supports 3.3 V library)



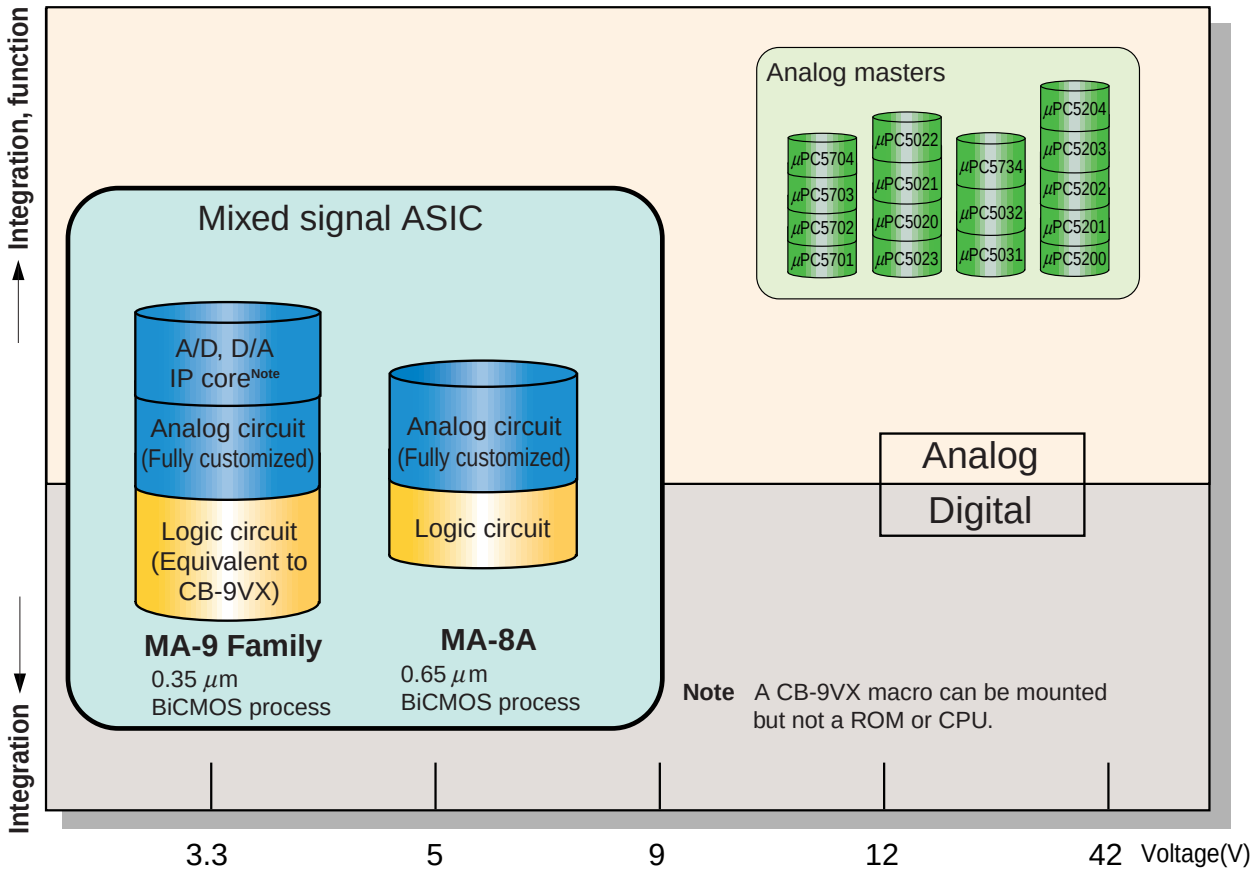
MA-9 Family (μPD681××)

0.35 μm BiCMOS process
(Equivalent to CB-9VX)

3.3 V power supply
For large-scale systems

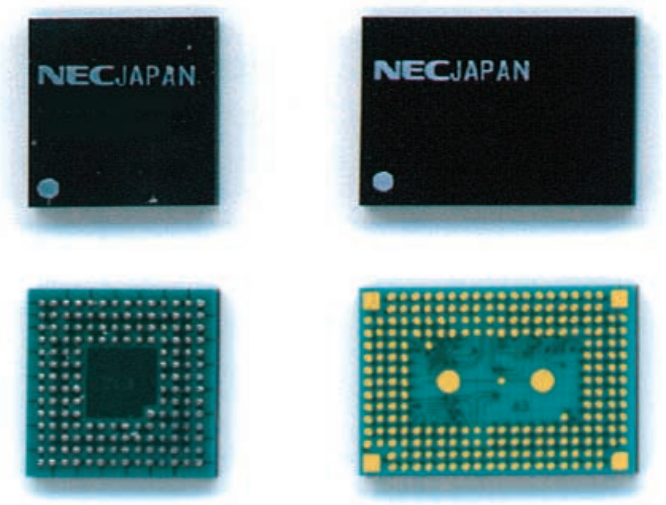


Mixed Signal ASIC Product Lines



Support of Small-Scale Packages

In addition to conventional mold packages, various CSPs (chip size packages) are available to support set downsizing.



FPBGA™ (Fine-pitch BGA)

FPLGA (Fine-pitch LGA)

Features

Support of digital/analog mixed circuits

By employing the latest BiCMOS process, the MA-8A realizes the integration of a 0.65 μm CMOS gate array and analog ASIC (analog master) on a single chip.

Analog block element configuration prioritizing circuit functions

Analog circuits that mix bipolar transistors and CMOS transistors can be created through the use of the BiCMOS process:

High input impedance operational amplifiers
Sample and hold circuits
Analog switches, etc.

Simple design and short development time

The logic block can be easily developed with OPENCAD™ (NEC Electronics' original CAE tool).
Furthermore, a short development time can be achieved, which is another advantage of ASICs.

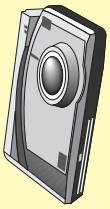
Application Fields

The MA-8A can be used to integrate analog/digital mixed circuits applied to multimedia and various other fields on one chip.

Mobile devices (battery management/speaker drive)

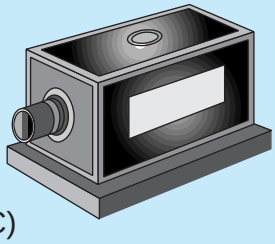
- ○Cellular phones (PDC, PHS, CDMA, GSM, GPRS)
- ○PDAs
- ○Portable game equipment

PC peripheral equipment



- ○DSCs, single-lens reflex cameras
  Flash light control, zoom lens control
- ○Storage equipment
  Servo controller
- ○LCD panels (active matrix)
  Grayscale power supply controller

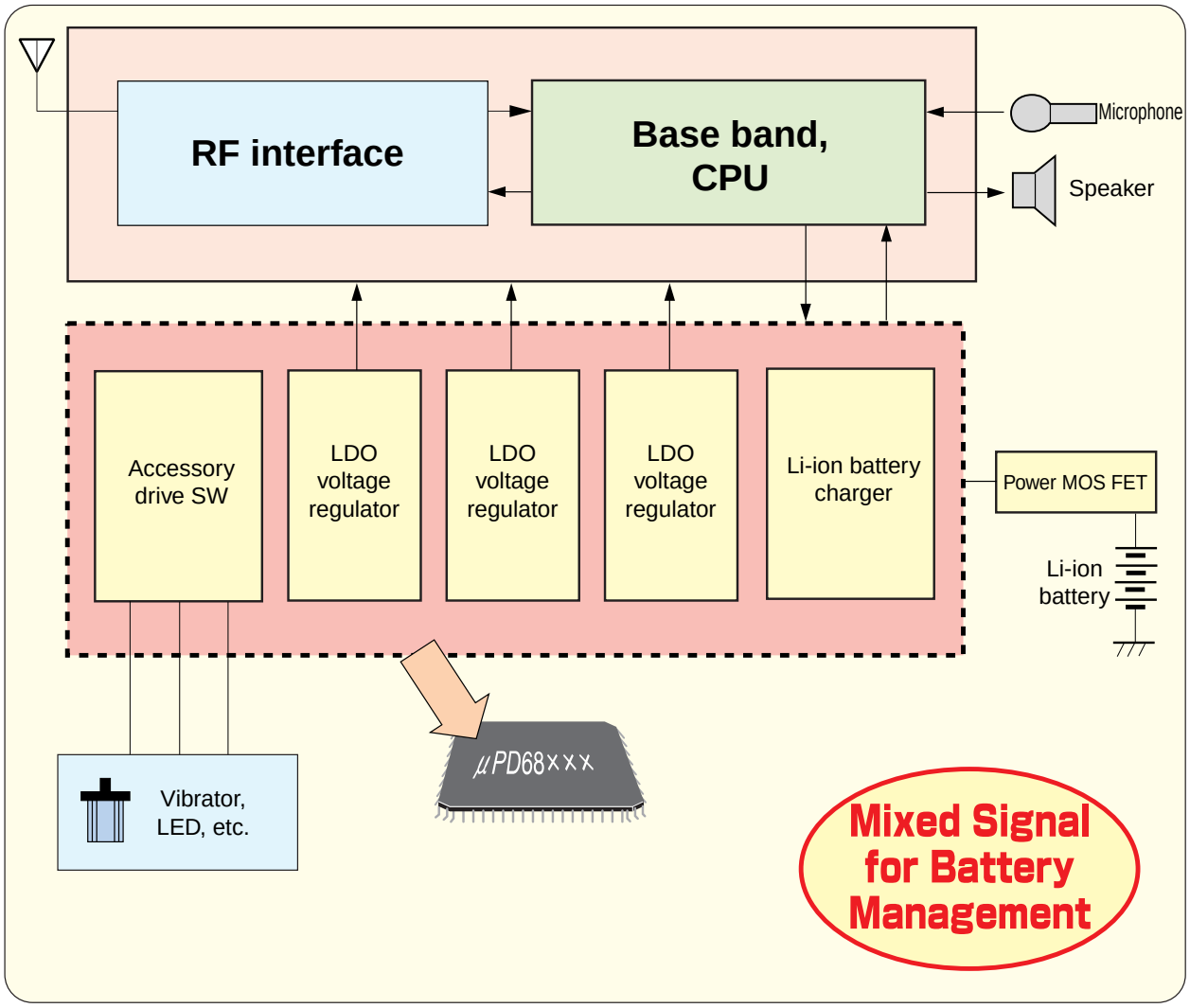
Sensor modules



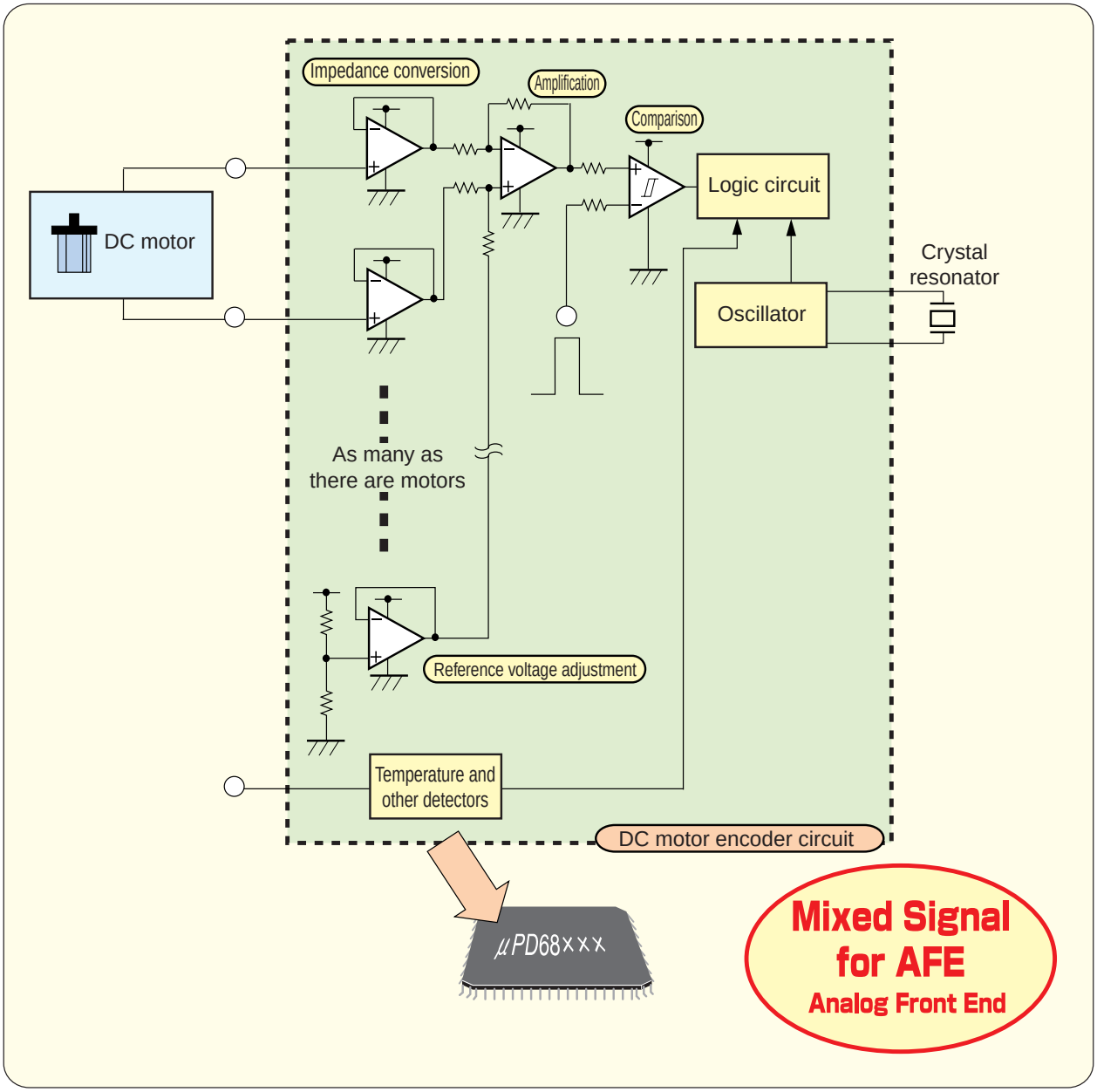
- ○Geomagnetic sensors
  (cellular phone GPS, etc.)
- ○Gyro sensors
  (compensating for hand-shake in DSC, DVC)
- ○Magnetic sensors (DC motor control, etc.)

MA-8A Application Examples

Cellular Phones (Battery Management)

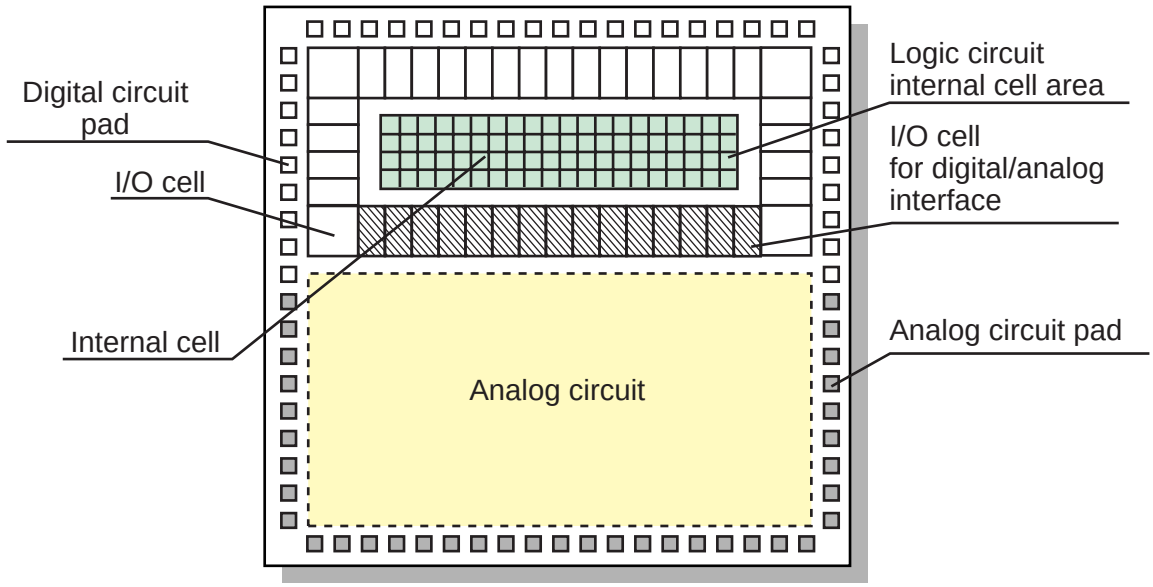


Digital Still Cameras, Single Lens Reflex Cameras (Zoom Lens Control)

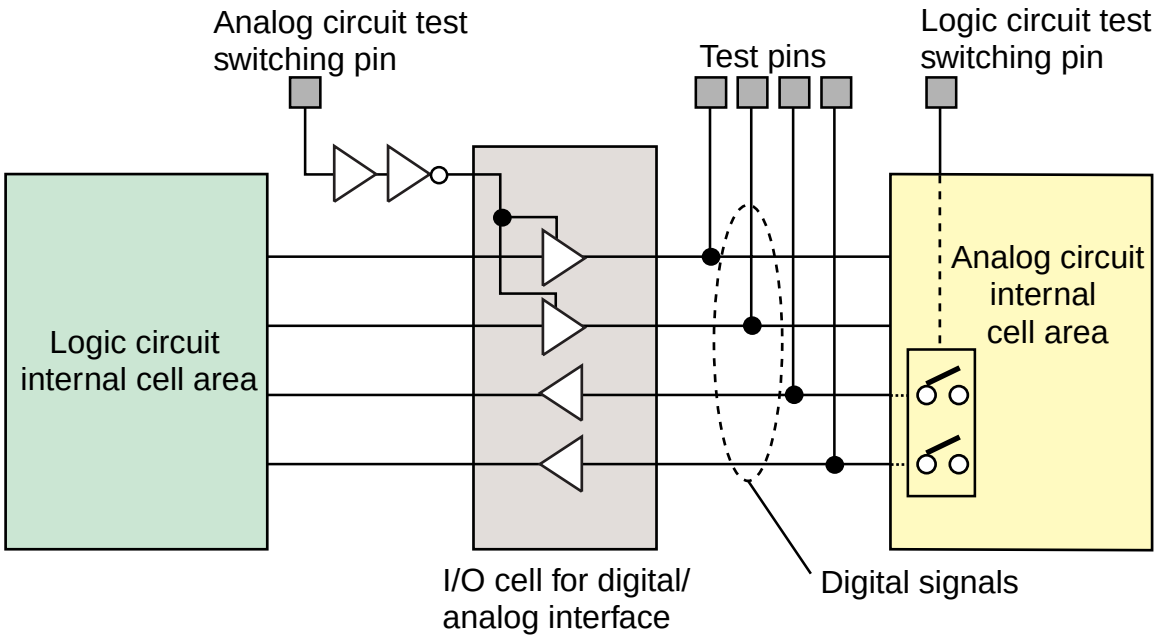


Chip Configuration

The MA-8A is mainly composed of a logic circuit (gate array block) and an analog circuit. The I/O cells for the digital/analog interface perform input/output of digital signals between the logic circuit and the analog circuit.



I/O Cells for Digital/Analog Interface



Basic Specifications

Logic Circuit

Part number		μPD688XX
Process		0.65 μm BiCMOS process
Supply voltage		5.0 V ±0.5 V (I/O block, internal gates)
Interface level		CMOS, TTL
Delay time	Internal gates[Note 1]	190 ps (TYP.)
	Input buffer[Note 2]	340 ps (TYP.)
	Output buffer[Note 3]	2.13 ns (TYP.)

Notes 1. Value assuming 2-input NAND power gate, fan-out 1, and wiring length 0.6 mm/1 pin pair.
2. Value assuming fan-out 2, wiring length 0.6 mm/1 pin pair.
3. Value assuming load capacitance 15 pF, block name FO01.

Remark The logic circuit characteristics are the same as those of NEC Electronics' CMOS-8 Family.

Analog Circuit

Part number		μPD688XX
Process		0.65 μm BiCMOS process
Supply voltage		5.0 V ±0.5 V
Transistors	NPN type	f_T = 10 GHz, h_{FE} = 80 (all TYP.)
	PNP type (lateral)	f_T = 10 MHz, h_{FE} = 70 (all TYP.)
	MOS	N-ch type, P-ch type for analog circuit
Polysilicon resistor[Note]		Absolute precision: ±20%, relative precision: ±2% (all MAX.)
Capacitor (MOS type)[Note]		Absolute precision: ±15%, relative precision: ±2% (all MAX.)

Note Values indicated are for reference only. The relative precision applies only to when the element is positioned in an adjacent location.

Electrical Specifications

Absolute Maximum Ratings

Item	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD},V_{CC}		–0.5 to +6.0	V
Input/output voltage (logic circuit)	V_I / V_O		–0.5 to V_{DD} + 0.5	V
Input current (logic circuit)	I_I		20	mA
Output current (logic circuit)	I_O	I_{OL} = 3 mA	10	mA
		I_{OL} = 6 mA	15	mA
		I_{OL} = 9 mA	20	mA
		I_{OL} = 12 mA	30	mA
		I_{OL} = 18 mA	40	mA
		I_{OL} = 24 mA	60	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Definition of absolute maximum rating terms

Item	Symbol	Meaning
Supply voltage	V_{DD}	The range of voltage that, if applied to the V_{DD} pin, will not cause destruction or lower reliability.
Input voltage	V_I	The range of voltage that, if applied to the input pin, will not cause destruction or lower reliability.
Output voltage	V_O	The range of voltage that, if applied to the output pin, will not cause destruction or lower reliability.
Input current	I_I	The absolute value of current capacity that, if applied to the input pin, will not cause latchup to occur.
Output current	I_O	The absolute value of DC current capacity that, if output from or input to the output pin, will not cause destruction or lower reliability.
Operating ambient temperature	T_A	Range of ambient temperature in which normal logical operation will occur.
Storage temperature	T_{stg}	Range of pin temperature that will not cause destruction or lower reliability when voltage and current are not applied.

Recommended Operating Range (Logic Circuit)

Standard specification CMOS interface conditions

V_{DD} = 5 V ±10%, T_A = –40 to +85°C (T_J = –40 to +125°C)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
High-level input voltage	V_{IH}	CMOS interface	0.7V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}		0		0.3V_{DD}	V
Positive trigger voltage	V_P		1.80		4.00	V
Negative trigger voltage	V_N		0.60		3.10	V
Hysteresis voltage	V_H		0.30		1.50	V
High-level input voltage	V_{IH}	TTL interface	2.29		V_{DD}	V
Low-level input voltage	V_{IL}		0		0.77	V
Positive trigger voltage	V_P		1.15		2.54	V
Negative trigger voltage	V_N		0.59		1.85	V
Hysteresis voltage	V_H		0.27		1.50	V
Input rise time	t_{ri}	Normal input	0		200	ns
Input fall time	t_{fi}		0		200	ns
Input rise time	t_{ri}	Schmitt input[Note]	0		10	ms
Input fall time	t_{fi}		0		10	ms

Note Do not use this for the clock signal.

Remark If a signal with a long rise/fall time is input, use a Schmitt trigger input buffer to prevent malfunction due to noise superimposed on the signal line.
Fluctuation of power caused by simultaneous operation of output buffers lowers the capability of the Schmitt trigger input buffer, and therefore, care must be exercised in laying out the pins.

Standard specification TTL interface conditions

V_{DD} = 5 V ±10%, T_A = 0 to +70°C (T_J = 0 to +100°C)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
High-level input voltage	V_{IH}	CMOS interface	0.7V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}		0.0		0.3V_{DD}	V
Positive trigger voltage	V_P		1.90		4.00	V
Negative trigger voltage	V_N		0.63		3.10	V
Hysteresis voltage	V_H		0.31		1.50	V
High-level input voltage	V_{IH}	TTL interface	2.20		V_{DD}	V
Low-level input voltage	V_{IL}		0.0		0.8	V
Positive trigger voltage	V_P		1.20		2.40	V
Negative trigger voltage	V_N		0.60		1.80	V
Hysteresis voltage	V_H		0.30		1.50	V
Input rise time	t_{ri}	Normal input	0		200	ns
Input fall time	t_{fi}		0		200	ns
Input rise time	t_{ri}	Schmitt input[Note]	0		10	ms
Input fall time	t_{fi}		0		10	ms

Note Do not use this for the clock signal.

Remark If a signal with a long rise/fall time is input, use a Schmitt trigger input buffer to prevent malfunction due to noise superimposed on the signal line.
Fluctuation of power caused by simultaneous operation of output buffers lowers the capability of the Schmitt trigger input buffer, and therefore, care must be exercised in laying out the pins.

MA-8A Development Procedure

Development of the MA-8A is carried out by both the user and NEC Electronics by dividing the work between gate array design using the design resources of the user and circuit design applying NEC Electronics' analog ASIC technology, which results in a shorter development time.

The transition of development work between the user and NEC Electronics is called "interfacing." The interface level depends on how far the user carries out development work and what data the user provides to NEC Electronics.

- Circuit diagram level interface

  In this development method, the user takes care of system circuit design, and the subsequent LSI circuit design and simulation are performed by NEC Electronics.

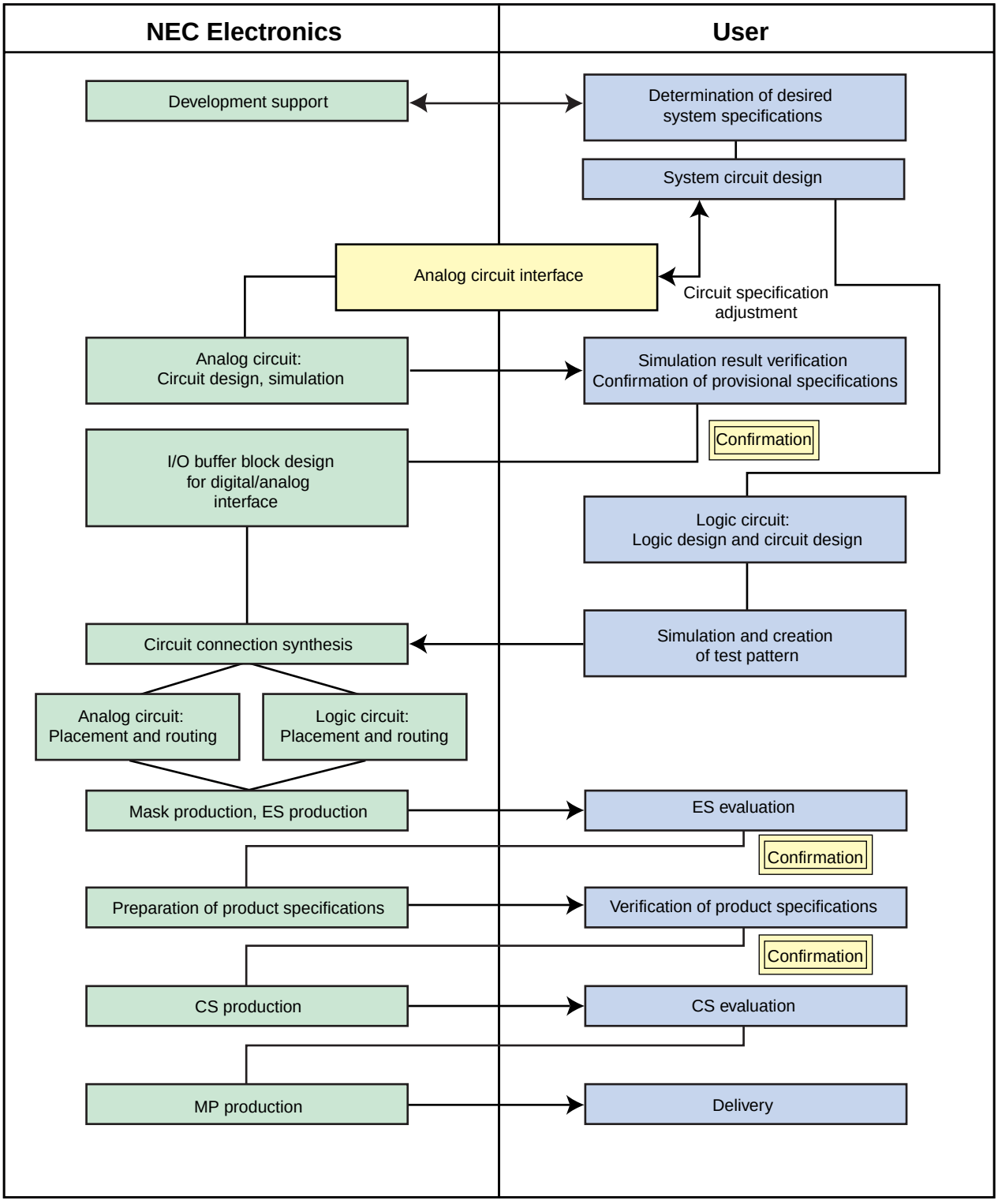
- Simulation level interface

  In this development method, the user is in charge of development from circuit design to simulation using engineering workstations (EWS) and CAD system simulation tools, and NEC Electronics is responsible for the rest of the development work.

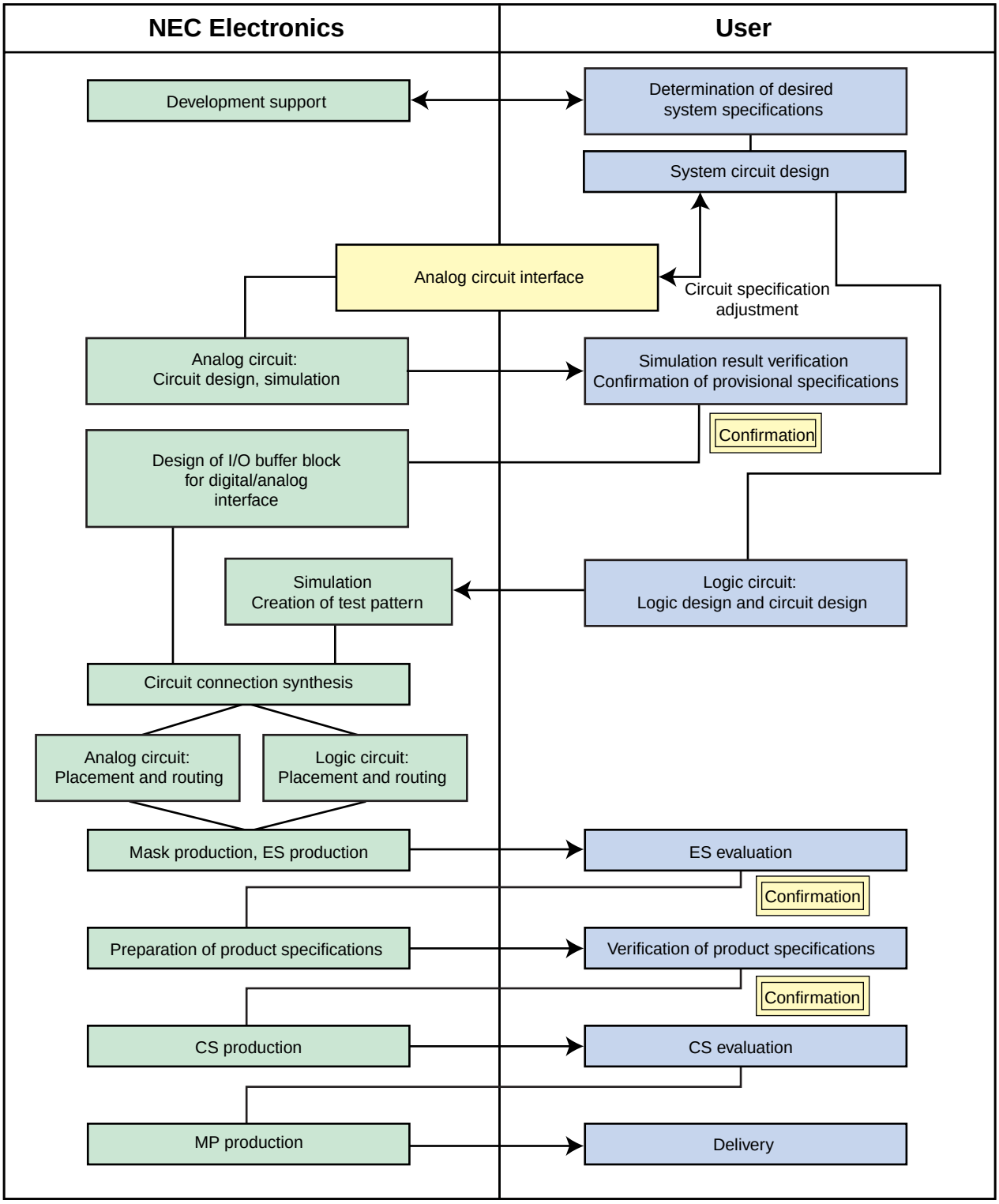
The MA-8A is divided into a logic circuit and an analog circuit, and two kinds of development methods combining the above-described interface levels are available.

Development Method		System Circuit Design	LSI Circuit Design	Circuit Synthesis	Layout Design	ES Production
①	[Logic circuit] Simulation level interface		(User side)		(NEC Electronics side)	
	[Analog circuit] Circuit diagram level interface					
②	[Logic circuit] Circuit diagram level interface					
	[Analog circuit] Circuit diagram level interface					

① Logic circuit: Simulation level interface
Analog circuit: Circuit diagram level interface



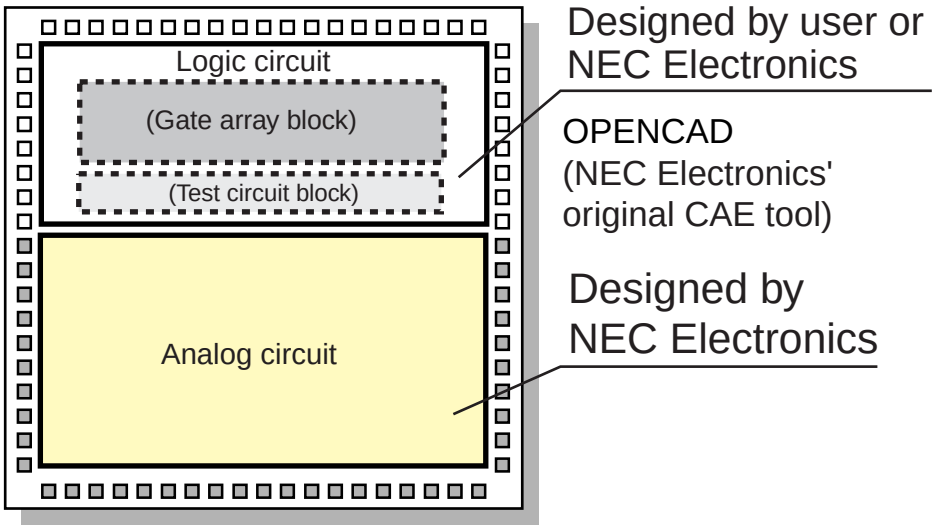
② Logic circuit: Circuit diagram level interface
Analog circuit: Circuit diagram level interface



MA-8A Development Tools

The MA-8A provides development tools that support ASIC development by the user for the logic circuits. NEC Electronics will take charge of circuit design for the analog circuits according to the user's specifications.

Caution **A pin should be drawn out as a test pin where the analog circuit is connected to the logic circuit. Configure the area where the analog circuit is connected to the logic circuit, as well as the test circuit of the logic circuit in the test circuit block.**



Features

The MA-9 Family (μPD681XX) consists of mixed signal ASICs that aim for system-on-a-chip through the use of a leading-edge 0.35 μm BiCMOS process pioneered by NEC Electronics.

Support of analog IP core

The MA-9 Family can utilize analog circuit design resources such as the A/D converter and D/A converter of NEC Electronics' 0.35 μm cell-based IC.

Leading-edge BiCMOS process

High-speed digital circuits and high-accuracy, sophisticated analog circuits can now be realized on a single chip by employing NEC Electronics' leading-edge 0.35 μm BiCMOS process.

Low power consumption

A low power consumption is achieved for LSIs by employing a low-voltage operation process (3.3 V).

Flexible mixed signal development environment

NEC Electronics' development environment for the CB-9 Family VX Type cell-based IC can be used for the internal logic.

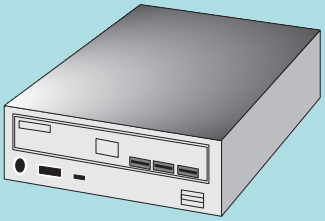
Application Fields

Since CB-9 and later submicron cell-based ICs cannot configure an analog circuit, they may not support CB solutions. Furthermore, if they incorporate an A/D converter and D/A converter, a good cost performance is not possible due to the restrictions on cell-based IC allocation.

In these cases, by integrating the entire cell-based IC, or the A/D converter, D/A converter, and analog circuit blocks on a single chip, the MA-9 Family provides the user with the best solution.

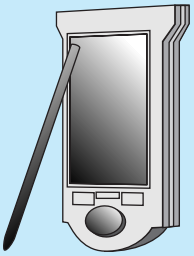
Storage equipment

- ○ Servo/write control
  DVD-ROM/RAM drives
  CD-R/W drives



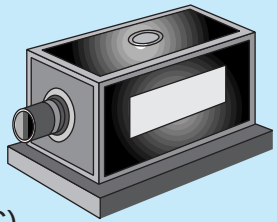
PC peripheral terminals

- ○ Analog front end (A/D converter, D/A converter, analog circuit)
- ○ Sensor signal amplification
  Color LCD panels
  Printers
  PDAs



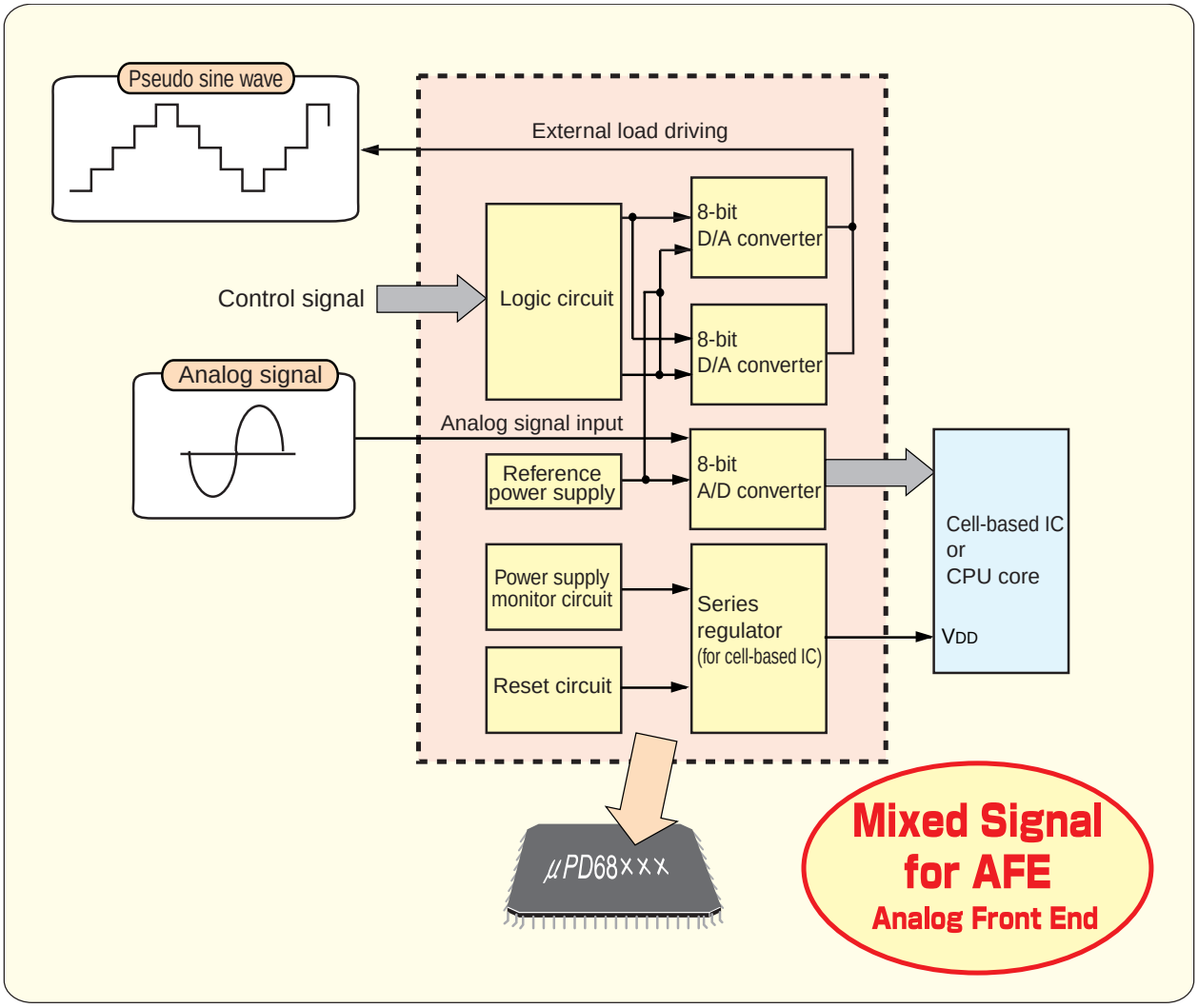
Sensor modules

- ○ Geomagnetic sensors
  (cellular phone GPS, etc.)
- ○ Gyro sensors
  (compensating for hand-shake in DSC, DVC)
- ○ Magnetic sensors (DC motor control, etc.)

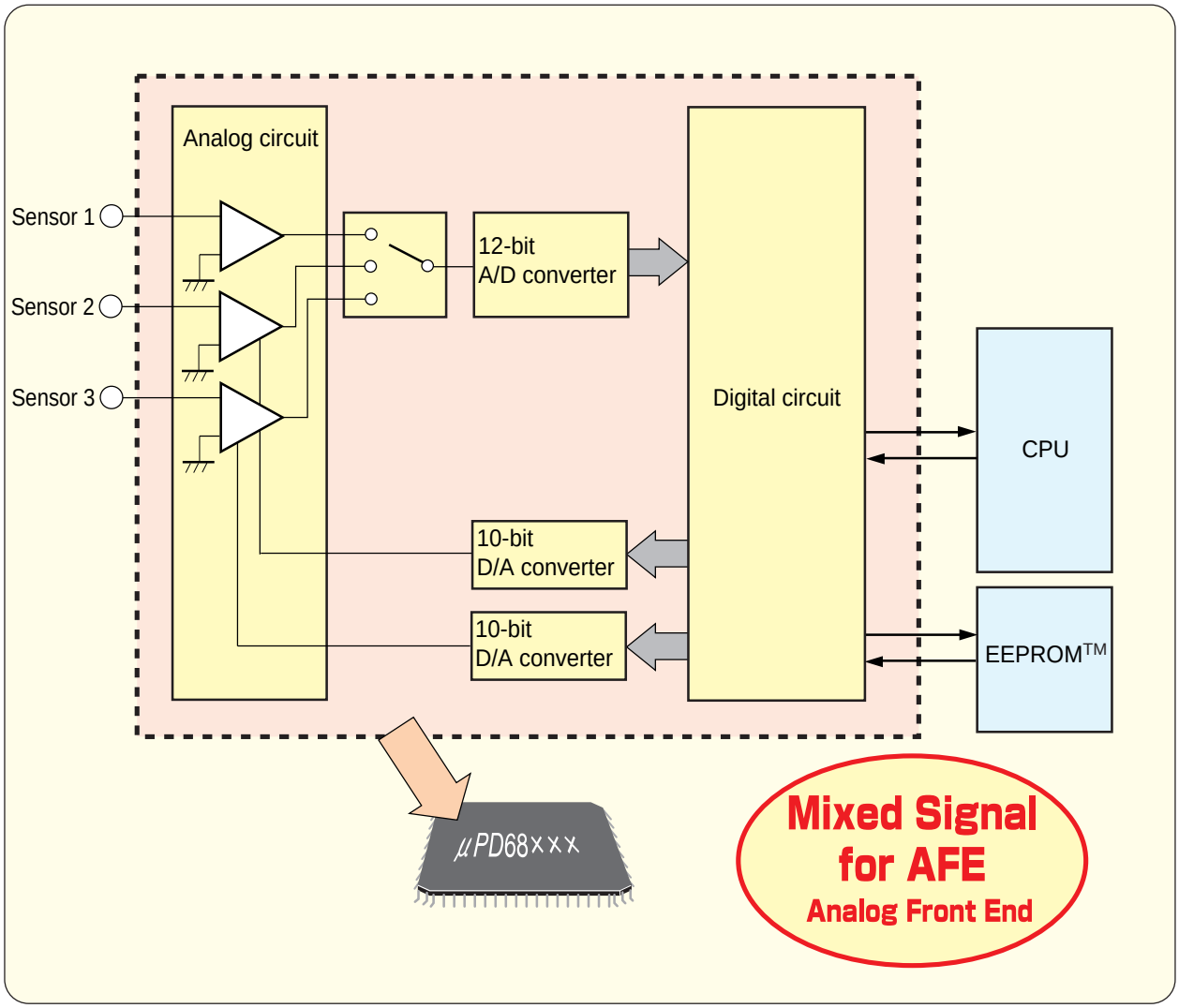


MA-9 Family Application Examples

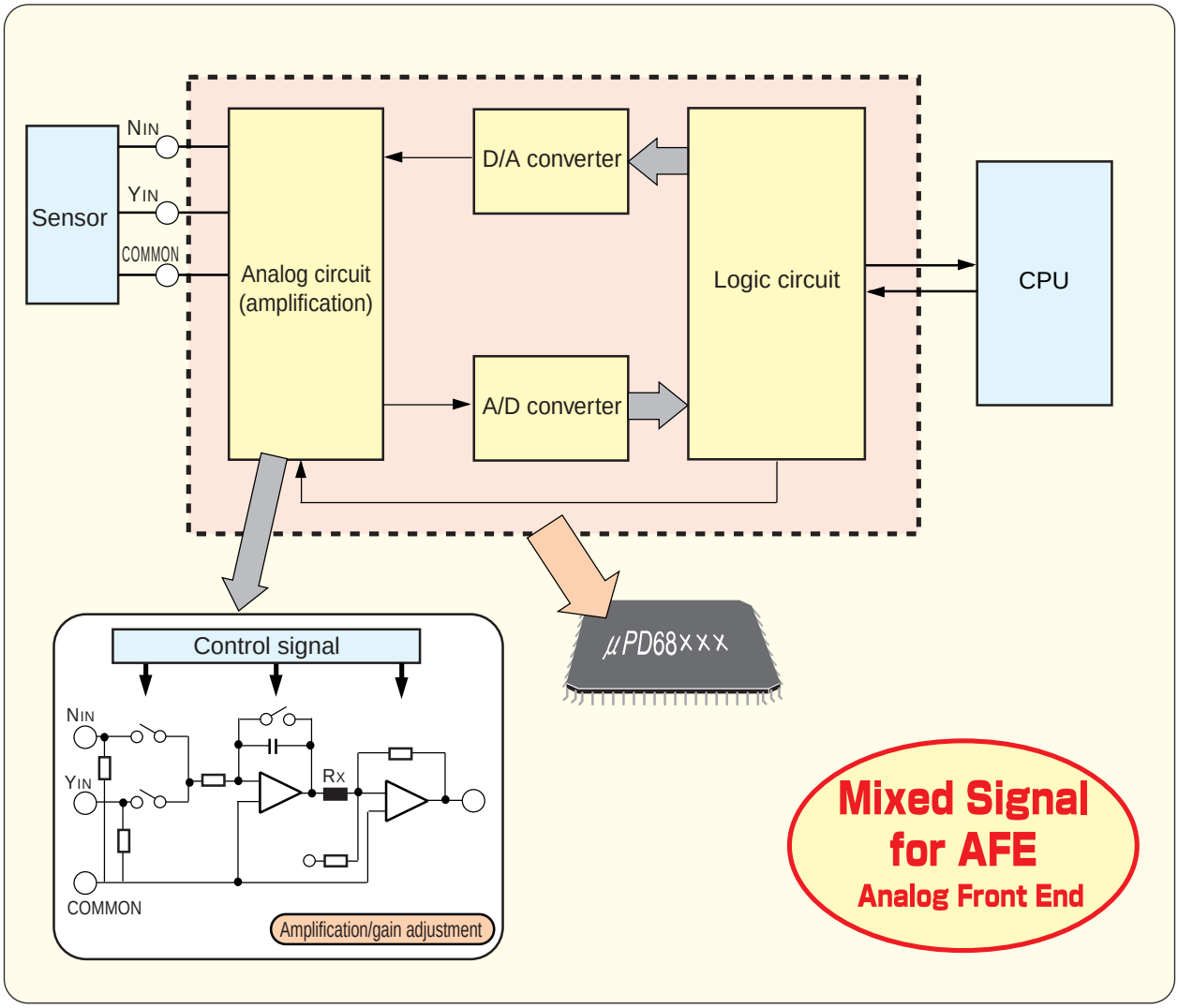
Analog Front End for PC Peripherals (Printer, Tablet)



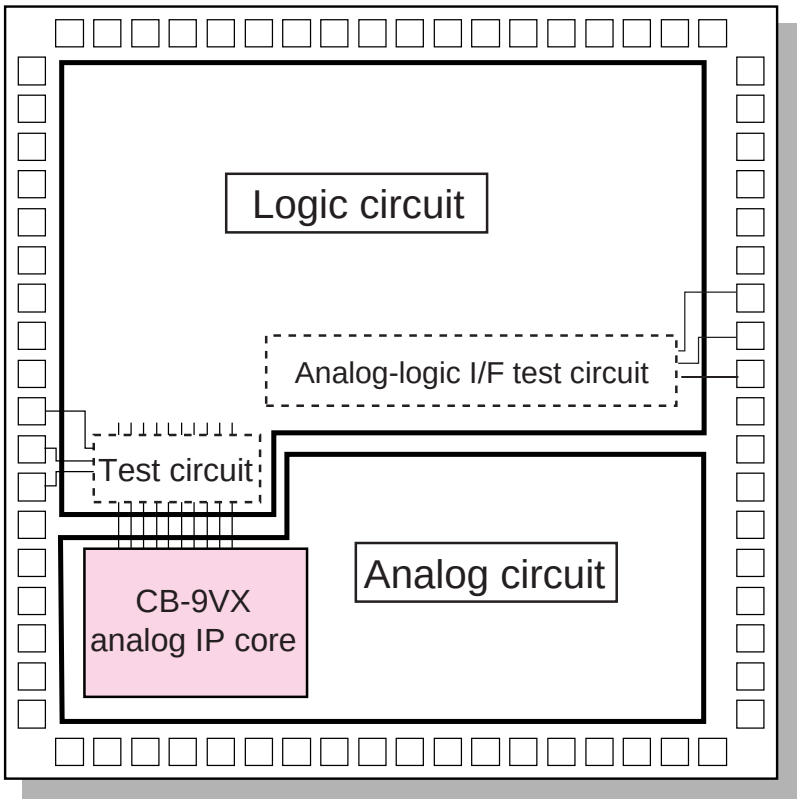
Gyro Sensor/Magnetic Sensor (1/2) (Sensor Signal Amplification + A/D Conversion)



Gyro Sensor/Magnetic Sensor (2/2) (Sensor Signal Amplification + A/D Conversion)



Chip Configuration



Logic circuit

- ○User logic (logic gates)
- ○A/D or D/A converter macro (CB-9 Family VX Type)[Note]
- ○Test circuit
  Test circuit including analog-logic I/F block

Note Neither a CPU nor ROM can be mounted.

Analog circuit

- ○Configured by operational amplifier, comparator, reference power supply, analog switch, etc.

  NEC Electronics designs the circuit according to the user's circuit specifications.

Basic Specifications

Logic Circuit

Part number		μPD681XX
Process		0.35 μm BiCMOS process
Supply voltage		3.3 V ±0.3 V (I/O block, internal gates)
Maximum integration (logic only)		1.7 million gates (usable)
Interface level		LVTTL
Delay time	Internal gates[Note 1]	114 ps (TYP.)
	Input buffer[Note 2]	169 ps (TYP.)
	Output buffer[Note 3]	864 ps (TYP.)

Notes 1. Value assuming 2-input NAND power gate, fan-out 2, and standard wiring length.
2. Value assuming fan-out 2 and standard wiring length.
3. Value assuming load capacitance 15 pF, I_{OL} = 18 mA.

Remark The logic circuit characteristics are the same as those of NEC Electronics' CB-9 Family.

Analog Circuit

Part number		μPD681XX
Process		0.35 μm BiCMOS process
Supply voltage		3.3 V ±0.3 V
Transistors	NPN type	f_T = 10 GHz, h_{FE} = 70 (all TYP.)
	PNP type (vertical type)	f_T = 2 GHz, h_{FE} = 30 (all TYP.)
	MOS	N-ch type, P-ch type for analog circuit
Polysilicon resistor[Note]		Absolute precision: ±20%, relative precision: ±2%
Capacitor (MIM type)[Note]		Absolute precision: ±20%, relative precision: ±2%

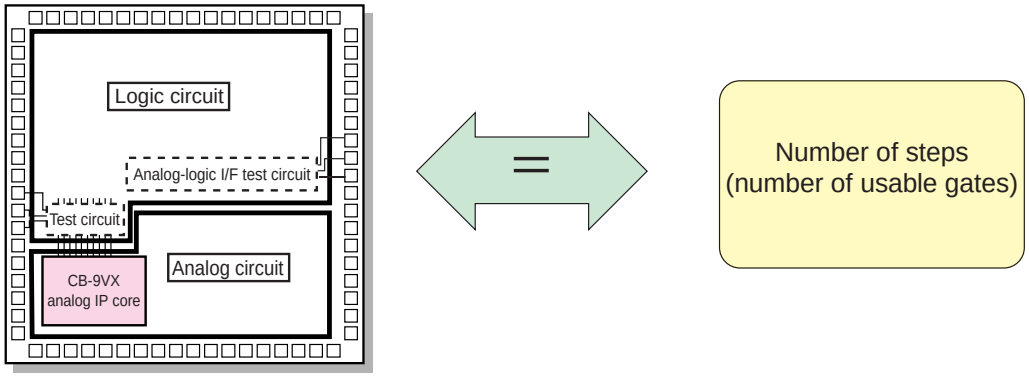
Note Values indicated are for reference only. The relative precision applies only to when the element is positioned in an adjacent location.

Number of Steps and Usable Gates

Step Number	Number of Usable Gates	
	VX Type	
	2-Layer Wiring	3-Layer Wiring
B60	89,600	131,800
C02	117,700	174,200
C40	142,000	211,500
C78	176,100	264,200
D01	195,700	293,600
D26	215,900	326,200
D52	242,200	365,900
D90	277,900	422,900
E16	308,300	469,200
E54	344,200	535,400
E80	373,300	572,400
F18	412,800	647,300
F44	448,300	703,000
F70	479,800	741,500
G08	521,600	824,900
G34	554,300	876,600
G72	612,600	954,500
H10	655,600	1,045,900
H49	714,700	1,140,200
H87	775,400	1,218,600
J26	813,300	1,309,300
J51	855,900	1,377,800
K15	968,800	1,536,000
K92	1,071,600	1,741,400

Remark The number of usable gates is calculated using 2-input NAND gate conversion.
Moreover, the above-indicated number of usable gates depends on the megafunctions that are provided and the logic use efficiency, and should therefore be treated as a reference value.

Remark The number of steps and number of usable gates given for the MA-9 Family indicate the size of the entire internal logic including the mixed signal core.



Electrical Specifications

Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}			
3.3 V			–0.5 to +4.6	V
I/O voltage	V_I/V_O			
LVTTL buffer		$V_I/V_O < V_{DD} + 0.5$ V	–0.5 to +4.6	V
Output current	I_O	I_{OL} = 1 mA	3	mA
		I_{OL} = 2 mA	7	mA
		I_{OL} = 3 mA	10	mA
		I_{OL} = 6 mA	20	mA
		I_{OL} = 9 mA	30	mA
		I_{OL} = 12 mA	40	mA
		I_{OL} = 18 mA	60	mA
		I_{OL} = 24 mA	75	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Definition of absolute maximum rating terms

Item	Symbol	Meaning
Supply voltage	V_{DD}	The range of voltage that, if applied to the V_{DD} pin, will not cause destruction or lower reliability.
Input voltage	V_I	The range of voltage that, if applied to the input pin, will not cause destruction or lower reliability.
Output voltage	V_O	The range of voltage that, if applied to the output pin, will not cause destruction or lower reliability.
Input current	I_I	The absolute value of current capacity that, if applied to the input pin, will not cause latchup to occur.
Output current	I_O	The absolute value of DC current capacity that, if output from or input to the output pin, will not cause destruction or lower reliability.
Operating ambient temperature	T_A	Range of ambient temperature in which normal logical operation will occur.
Storage temperature	T_{stg}	Range of pin temperature that will not cause destruction or lower reliability when voltage and current are not applied.

Recommended Operating Range

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}	3.3 V power supply	3.0	3.3	3.6	V
Negative trigger voltage	V_N	LVTTL buffer	0.6		1.8	V
Positive trigger voltage	V_P	LVTTL buffer	1.2		2.4	V
Hysteresis voltage	V_H	LVTTL buffer	0.3		1.5	V
Low-level input voltage	V_{IL}	LVTTL buffer	0		0.8	V
High-level input voltage	V_{IH}	LVTTL buffer	2.0		V_{DD}	V
Input rise time	t_{ri}	Normal input	0		200	ns
Input fall time	t_{fi}		0		200	ns
Input rise time	t_{ri}	Schmitt input	0		10	ms
Input fall time	t_{fi}		0		10	ms

Remark The logic circuit characteristics are the same as those of NEC Electronics' CB-9 Family.

Analog IP Core

A/D Converter

Core Name	Power Consumption (MAX.)	Differential Linearity Error (MAX.)	Integral Linearity Error (MAX.)	Circuit Type	Operating Power Supply Voltage
10 bit-100 kHz-1ch	18.0 mW	±1.0LSB	±1.5LSB	Successive approximation	2.7 to 3.6 V
10 bit-100 kHz-8ch_Mpx	18.0 mW	±1.0LSB	±1.5LSB	Successive approximation	3.0 to 3.6 V
12 bit-300 kHz-4ch_Mpx	20.2 mW	±1.0LSB	±4.0LSB	Successive approximation	2.7 to 3.6 V
6 bit-70 MHz	504 mW	±1.0LSB	±2.0LSB	Flash	3.0 to 3.6 V
8 bit-200 kHz-1ch	28.8 mW	±1.0LSB	±2.0LSB	Successive approximation	3.3 V (TYP.)
8 bit-200 kHz-8ch					
8 bit-50 MHz	108 mW	±1.0LSB (TYP.)	±1.0LSB (TYP.)	Sub-ranging	3.0 to 3.6 V
8 bit-8 MHz					

Remark T_A = –40 to +85°C

D/A Converter

Core Name	Power Consumption (MAX.)	Differential Linearity Error (MAX.)	Integral Linearity Error (MAX.)	Circuit Type	Operating Power Supply Voltage
10 bit-100 kHz-1ch	3.6 mW	±1.0LSB	±1.0LSB	Resistor string	3.3 V (TYP.)
10 bit-135 kHz-1ch	374 mW	±1.0LSB	±1.5LSB	Resistor string	3.0 to 3.6 V
10 bit-30 MHz-1ch	90 mW	±0.5LSB	±2.25LSB	Resistor string	3.0 to 3.6 V
10 bit-30 MHz-2ch	180 mW	±0.5LSB	±2.25LSB	Resistor string	3.0 to 3.6 V
10 bit-30 MHz-3ch	266.4 mW	±0.5LSB	±2.25LSB	Resistor string	3.0 to 3.6 V
8 bit-200 kHz-1ch	7.2 mW	±1.0LSB	±1.0LSB	Resistor string	3.3 V (TYP.)
8 bit-30 MHz-1ch	90 mW	±0.5LSB	±1.0LSB	Resistor string	3.0 to 3.6 V
8 bit-30 MHz-2ch	180 mW	±0.5LSB	±1.0LSB	Resistor string	3.0 to 3.6 V
8 bit-30 MHz-3ch	T.B.D.	±1.0LSB	±3.0LSB	Resistor string	Under development (V_O = 0.75 V)

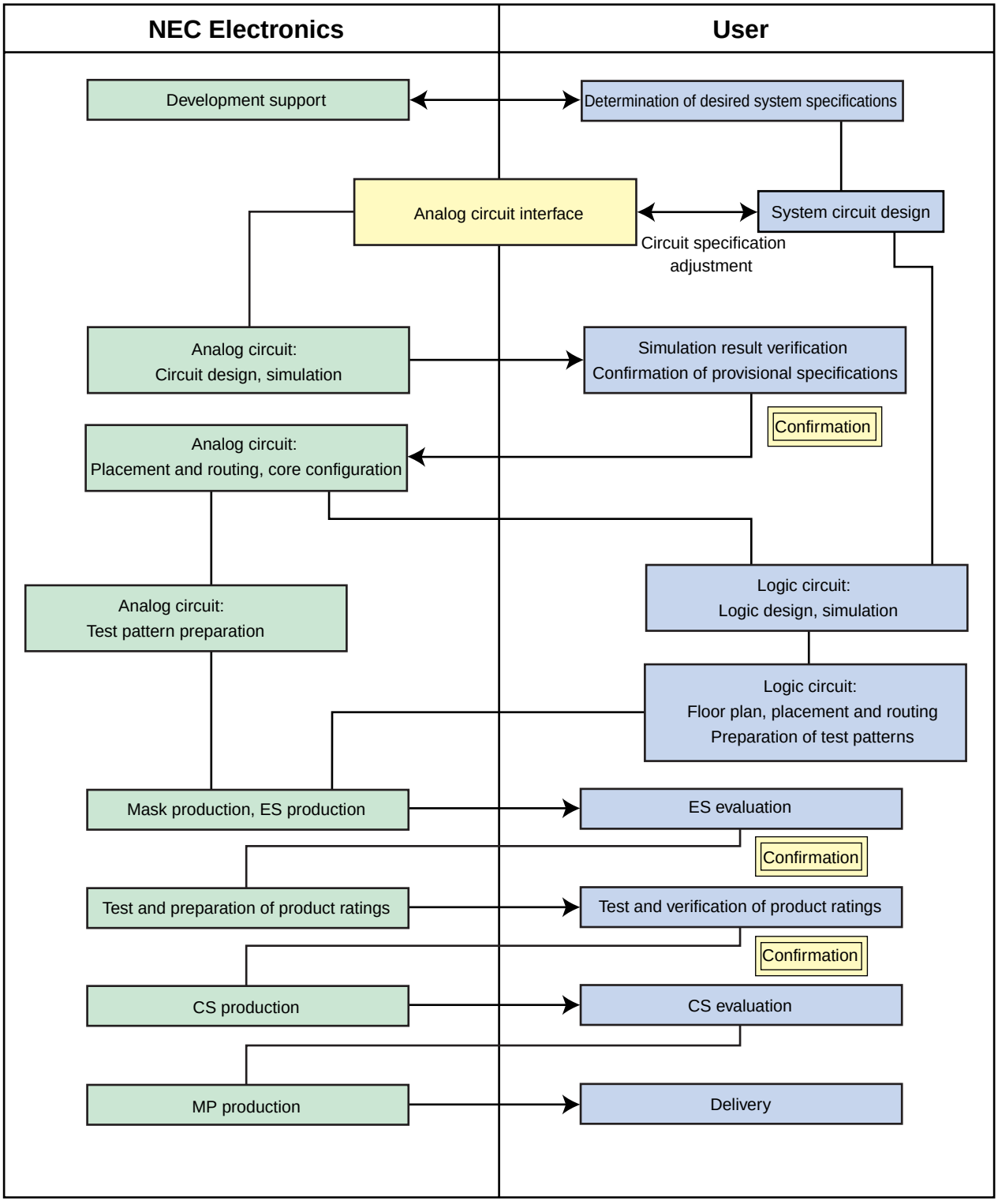
Remark T_A = –40 to +85°C

MA-9 Family Development Procedure

The MA-9 Family is developed by separating the logic circuit and analog circuit and combining the circuit diagram level interface and simulation level interface.

Development Method	System Circuit Design	LSI Circuit Design	Circuit Synthesis	Layout Design	ES Production
[logic circuit] Simulation level interface		(User side)		(NEC Electronics side)	
[Analog circuit] Circuit diagram level interface					

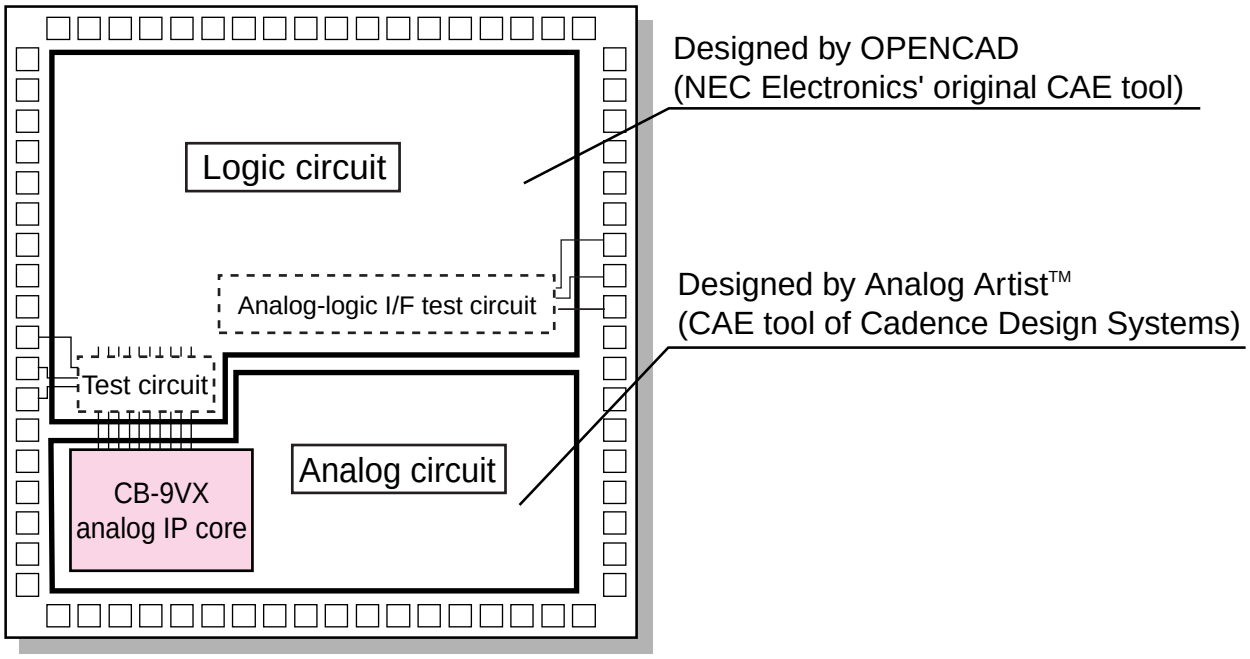
Logic circuit: Simulation level interface
Analog circuit: Circuit diagram level interface



MA-9 Family Development Tools

The MA-9 Family provides development tools that support ASIC development by the user for each logic circuit and analog circuit separately.

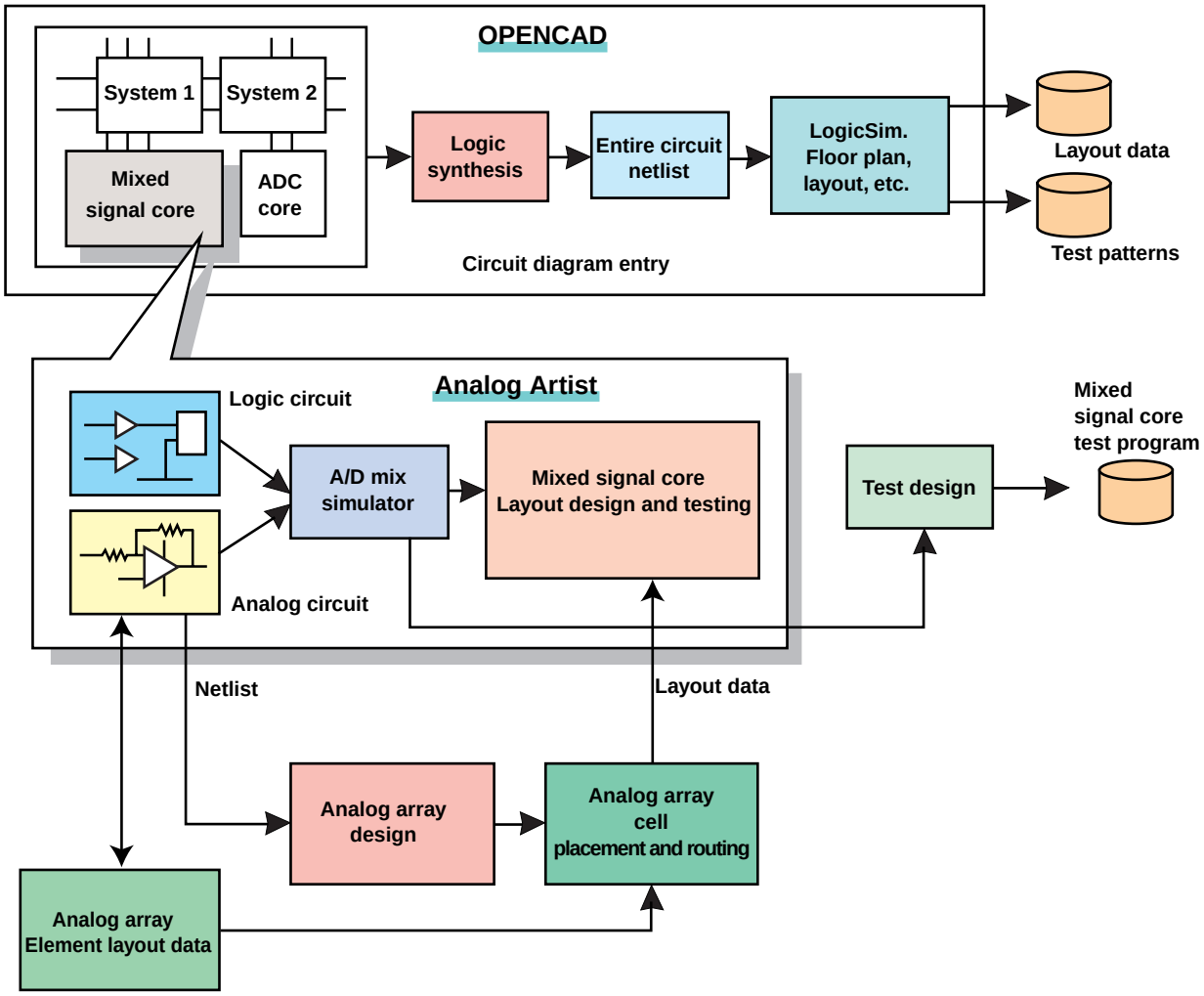
For the logic circuits, a simple design environment is enabled by using OPENCAD, NEC Electronics' original CAE tool, and for the analog circuits, the design environment is enabled by using a CAE tool ideal for digital-analog integrated circuits.



Analog Artist

Circuit diagram entry: Composer™
Simulator: Spectre/Verilog™HDL
Layout editor: DLE,Virtuoso
Layout tester: Diva

Design Flowchart



Packages

MA-8A

The MA-8A supports various packages, enabling users to select the package type and optimum number of pins for their system and circuit scale (chip size).

Mold Packages

Package	No. of Pins	Lead Pitch (mm)	Nominal Size	Body Size (mm)	Main Unit Thickness (mm)
SOP	20	1.27	7.62 mm (300)	–	–
SSOP	16	0.65	5.72 mm (225)	–	–
	20	0.65	5.72 mm (225)	–	–
	20	0.65	7.62 mm (300)	–	–
	24	0.65	7.62 mm (300)	–	–
	30	0.65	7.62 mm (300)	–	–
	36	0.65	7.62 mm (300)	–	–
	38	0.65	7.62 mm (300)	–	–
	42	0.65	9.53 mm (375)	–	–
	48	0.65	9.53 mm (375)	–	–
QFP	44	0.8	–	10 × 10	2.70
	44	0.8	–	10 × 10	1.40
	48	0.5	–	7 × 7	1.00
	48	0.65	–	10 × 10	2.20
	52	0.65	–	10 × 10	1.40
	52	1.00	–	14 × 14	2.55
	64	0.5	–	10 × 10	1.00
	64	0.8	–	14 × 14	1.40
	64	1.0	–	14 × 20	2.00
	68	0.65	–	10 × 14	2.20
	72	0.5	–	10 × 10	2.20
	74	1.0	–	20 × 20	3.70
	80	0.5	–	12 × 12	1.00
	80	0.65	–	14 × 14	2.00
	80	0.8	–	14 × 20	2.70
	100	0.4	–	12 × 12	1.00
	100	0.5	–	14 × 14	1.40
	100	0.5	–	14 × 14	1.00
	100	0.65	–	14 × 20	2.20
	120	0.4	–	14 × 14	1.00
	120	0.5	–	20 × 20	2.70
	144	0.5	–	20 × 20	1.40
	160	0.5	–	24 × 24	1.40
	176	0.4	–	20 × 20	1.40
	208	0.5	–	28 × 28	1.40
	240	0.5	–	32 × 32	1.40

CSP (Chip Size Package)

Package	No. of Pins	Ball Array	Body Size (mm)	Production Status	Package	No. of Pins	Ball Array	Body Size (mm)	Production Status
FPBGA	61	3	6 × 6	○	FPLGA	64	3	6 × 6	○
	80	4	7 × 7			84	4	7.5 × 7.5	○
	161	4	10 × 10	○		100	Full	8 × 7	○
	209	4	12 × 12	○ Note		108	Full	7.5 × 7.5	○
	225	4	13 × 13	○		112	4	8 × 8	○
	249	4	13 × 13	○		168	4	11 × 11	○
	257	4	14 × 14	○		192	4	11 × 11	○ Note
	273	4	15 × 15	○ Note		224	4	13 × 13	○
	303	4	16 × 16	○		304	4	16 × 16	○
	393	4-0-2	16 × 16	○ Note		405	4-0-2	16 × 16	○ Note

Note Under development

Remarks 1. FPBGA: Fine Pitch Ball Grid Array, FPLGA: Fine Pitch Land Grid Array

2. ○: Can be produced Blank: In planning

3 Development costs, including the board and sorting jig, will be charged for a CSP.

MA-9 Family

The MA-9 Family supports various packages, enabling users to select the package type and optimum number of pins for their system and circuit scale (chip size).

For packages other than QFP, contact NEC Electronics.

Package					Step Size								
Type	No. of Pins	External Dimensions (mm)	Lead Pitch (mm)	Resin Thickness (mm)	B60	C02	C40	C78	D01	D26	D52	D90	E16
QFP (FP)	100	14 × 14	0.50	1.45	○	○	○				○	○	
	120	20 × 20	0.50	2.70	–								
	144	20 × 20	0.50	2.70	–	–	–						
	160Note	20 × 20	0.50	2.70	–	–	–	–	○	○	○	○	○
	176Note	24 × 24	0.50	2.70	–	–	–	–		△	△	○	○
	208Note	28 × 28	0.50	3.20	–	–	–	–		○	○	○	○
	240Note	32 × 32	0.50	3.20	–	–	–	–		○	○	○	○
	304Note	40 × 40	0.50	3.20	–	–	–	–	–	–	–	–	–
TQFP	100	14 × 14	0.50	1.00	○						○		○

Note Low-thermal-resistance type

Remark ○: Can be used, △: Under development, –: Cannot be used, Blank: Under study

Package					Step Size							
Type	No. of Pins	External Dimensions (mm)	Lead Pitch (mm)	Resin Thickness (mm)	E54	E80	F18	F44	F70	G08	G34	G72
QFP (FP)	100	14 × 14	0.50	1.45						–	–	–
	120	20 × 20	0.50	2.70								
	144	20 × 20	0.50	2.70				○				
	160Note	20 × 20	0.50	2.70	○	○	○	○	○	○		
	176Note	24 × 24	0.50	2.70	○	○	○	○	○	○	○	
	208Note	28 × 28	0.50	3.20	○	○	○	○	○	○	○	○
	240Note	32 × 32	0.50	3.20	○	○	○	○	○	○	○	○
	304Note	40 × 40	0.50	3.20	–	○	○	○	○	○	○	○
TQFP	100	14 × 14	0.50	1.00						–	–	–

Note Low-thermal-resistance type

Remark ○: Can be used, △: Under development, –: Cannot be used, Blank: Under study

Package					Step Size						
Type	No. of Pins	External Dimensions (mm)	Lead Pitch (mm)	Resin Thickness (mm)	H10	H49	H87	J26	J51	K15	K92
QFP (FP)	100	14 × 14	0.50	1.45	–	–	–	–	–	–	–
	120	20 × 20	0.50	2.70				–	–	–	–
	144	20 × 20	0.50	2.70				–	–	–	–
	160[Note]	20 × 20	0.50	2.70							
	176[Note]	24 × 24	0.50	2.70							
	208[Note]	28 × 28	0.50	3.20	○	○			○		○
	240[Note]	32 × 32	0.50	3.20	○	○			○		○
	304[Note]	40 × 40	0.50	3.20	○	○					○
TQFP	100	14 × 14	0.50	1.00	–	–	–	–	–	–	–

Note Low-thermal-resistance type

Remark ○: Can be used, △: Under development, –: Cannot be used, Blank: Under study

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