THOMSON COMPONENTS MOSTEK

MK4532A • MK4542A(N,K)-30/35/45

HIGH-SPEED 2K x 8 CMOS DUAL-PORT RAM

ADVANCE INFORMATION

MEMORY COMPONENTS

FEATURES

- High speed:
  — 30, 35, and 45 ns access
- Fully static operation
- Full contention arbitration
- MK4542A slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Low power:
  — 150 mA (max) operating
- 48-pin DIP or 52-pin PLCC
- $\overline{\text{BUSY}}$ output status flag for MK4532A (master), $\overline{\text{BUSY}}$ input for MK4542A (slave)
- Dual interrupt flags in PLCC

DESCRIPTION

The MK4532A and MK4542A are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The MK4532 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "master" dual-port RAM with the MK4542A "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

The MK4532A/MK4542A feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The BiPort™ memory cell is designed to enable simultaneous read and/or write operations from either port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the port delayed. This flag stays set until the first port's operation is complete.

MK4532A • MK4542A

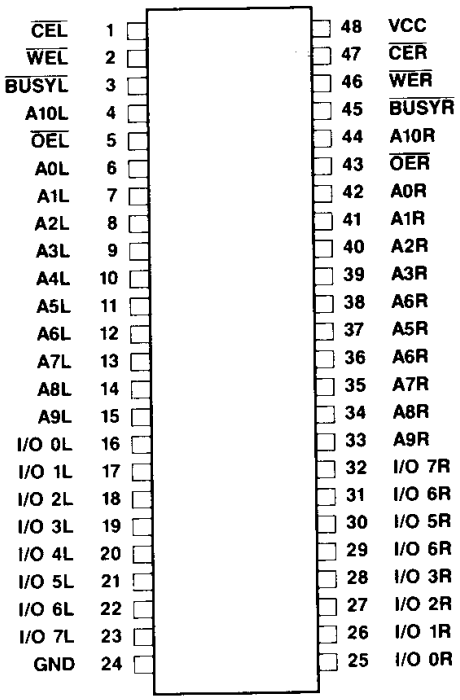


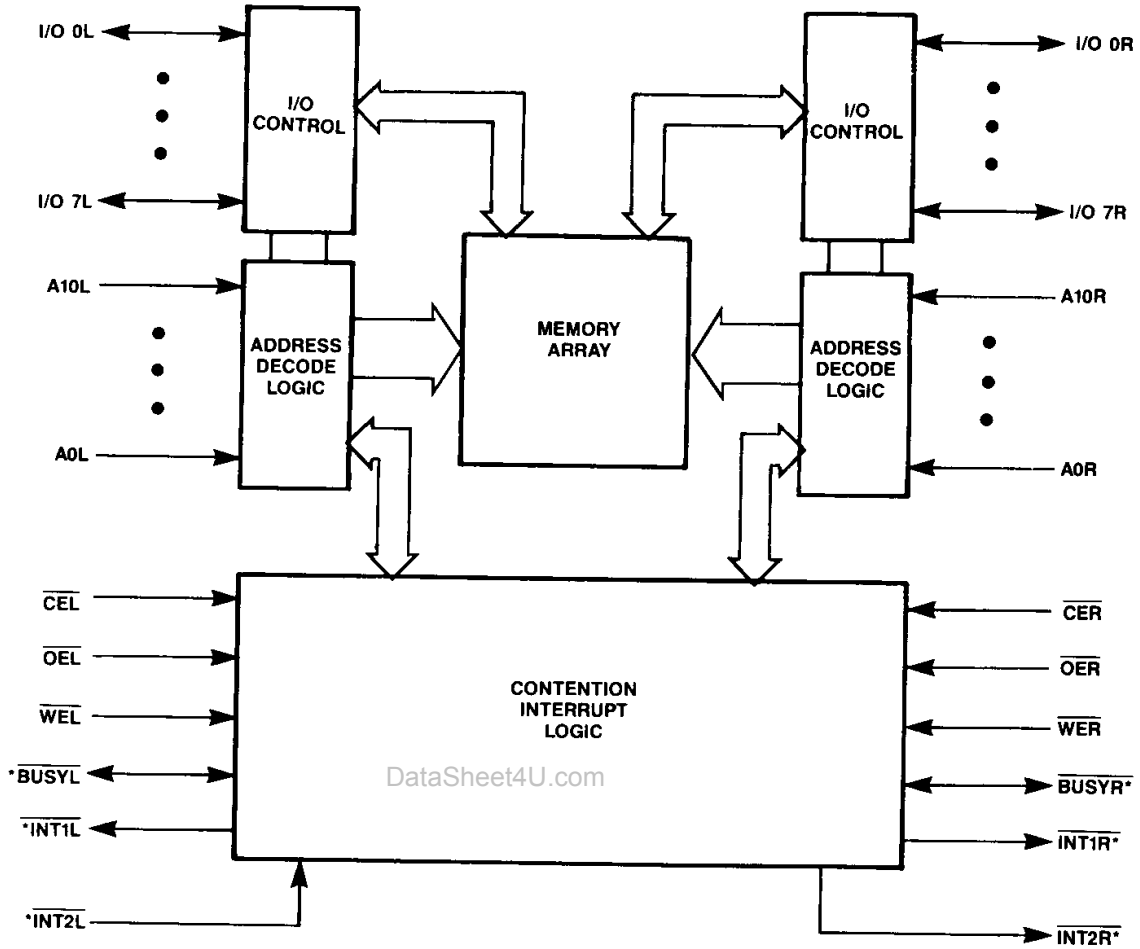
Figure 1. Pin Connections

When used in the 52-pin PLCC package, a dual-level interrupt function is available. The interrupt function acts like writable flags and is provided to allow communication between systems. When the flag's location (7FF/7FE) is written from one port, the other port's $\overline{\text{INT1}}$ pin goes low until the flag location is read by that same port. One flag is set during a write operation to any location ($\overline{\text{INT2}}$) and the other flag is set during a write to location 7FF/7FE ($\overline{\text{INT1}}$).

Both Interrupt and Busy flags are open drain for simple wired OR operation.

Automatic power down for each port is controlled independently by its Chip Enable input.

Interfacing to the MK4532A/MK4542A is further simplified by the incorporation of an Output Enable control for each port.



*INTERRUPT ARE AVAILABLE ONLY ON THE 52 PIN PLCC PACKAGE
*BUSY OUTPUT ON MASTER (4532A); BUSY INPUT ON SLAVE (4542A)

Figure 2. Block Diagram

ABSOLUTE MAJXIMUM RATINGS

Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65 to +150°C
Supply Voltage to Ground Potential . . . . . −0.5 to +7.0 V
Applied Output Voltage . . . . . −0.5 to +7.0 V
Applied Input Voltage . . . . . −0.5 to +7.0 V
Power Dissipation . . . . . 1.0 W
DC Output Current . . . . . 50 mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

TA = 0°C to +70°C, VCC = 5 V ±10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage			5	μA	V_{CC} = 5.5 V
I_{OL}	Output Leakage			5	μA	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}
I_{CC1}	Active Current			150	mA	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IL}
I_{CC2}	Standby Current			10	mA	$\overline{CEL}$ = $\overline{CER}$ = V_{IH}
I_{CC3}	Standby Current			70	mA	$\overline{CEL}$ or $\overline{CER}$ = V_{IH}
I_{CC4}	CMOS Standby			100	μA	$\overline{CEL}$ = $\overline{CER}$ = $\overline{OER}$ = $\overline{OEL}$ ≥ V_{CC} −0.2 V
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1V	V	
V_{OL1}	Output Low Voltage			0.4	V	I_{OL} = 6 mA
V_{OL2}	Output Low Voltage			0.5	V	I_{OL} = 16 mA Open Drain Outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −4.0 mA

DATA RETENTION CHARACTERISTICS

T_A = 25°C, V_{CC} = 2 V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DR}	V_{CC} for Retention Data	2.0		—	V	V_{CC} = 2.0 V, $\overline{CE}$ ≥ V_{CC} −0.2 V
I_{CCDR}	Data Retention Current	—		50	μA	V_{IN} ≥ V_{CC} −2.0 V or V_{IN} ≤ 0.2 V
t_{CDR}	Chip Deselect to Data Retention Time	0		—	ns	Note 2
t_R	Operation Recovery Time	t_{RC}		—	ns	Note 1, 2

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	TYP	MAX	UNIT	CONDITIONS
C_{OUT}	Output Capacitance		10	pF	Note 2
C_{IN}	Input Capacitance		10	pF	Note 2

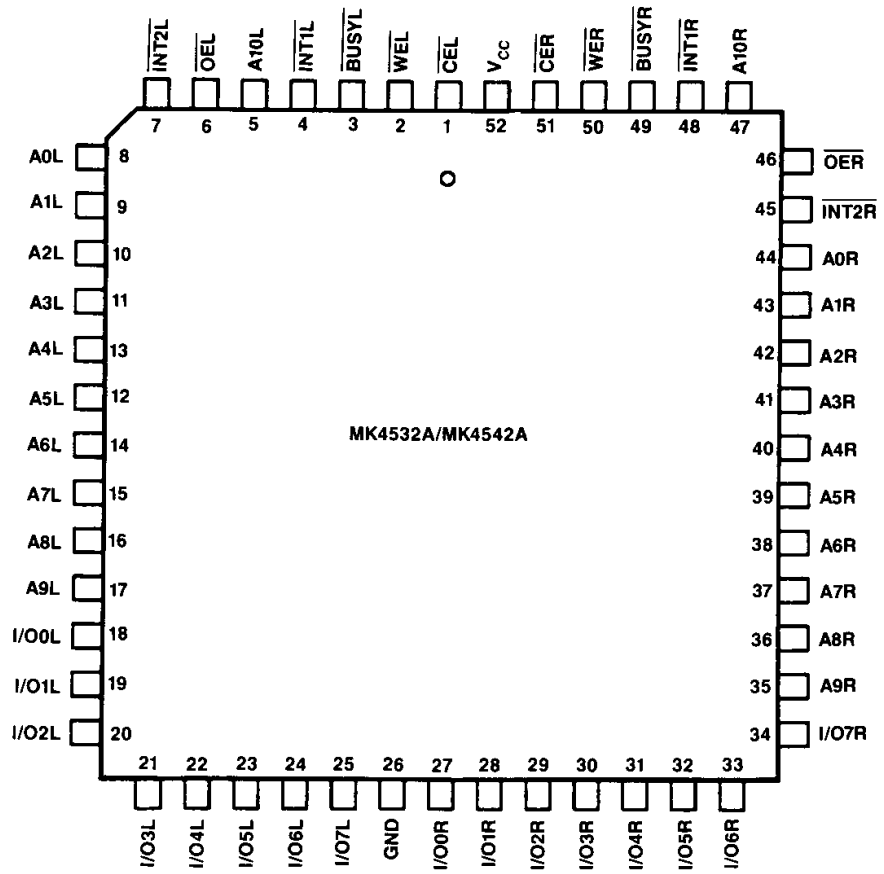


Figure 3. Leadless Chip Carrier Pinout

AC CHARACTERISTICS
READ CYCLE

T_A = 0°C to +70°C, V_{CC} = 5 V ±10%

SYMBOL		PARAMETER	MK4532A/42A-30		MK4532A/42A-35		MK4532A/42A-45		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}		Read Cycle Time	30		35		45		ns
t_{AA}		Address Access Time		30		35		45	ns
t_{ACE}		Chip Enable Access Time		30		35		45	ns
t_{AOE}		Output Enable Access Time		15		15		20	ns
t_{OH}		Output Hold from Address Change	0		0		0		ns
t_{LZ}	Note 2, 3	Output Low Z Time	0		0		0		ns
t_{HZ}	Note 2, 3	Output High Z Time		15		15		20	ns
t_{PU}	Note 2	Chip Enable to Power Up Time	0		0		0		ns
t_{PD}	Note 2	Chip Disable to Power Down Time		15		15		15	ns

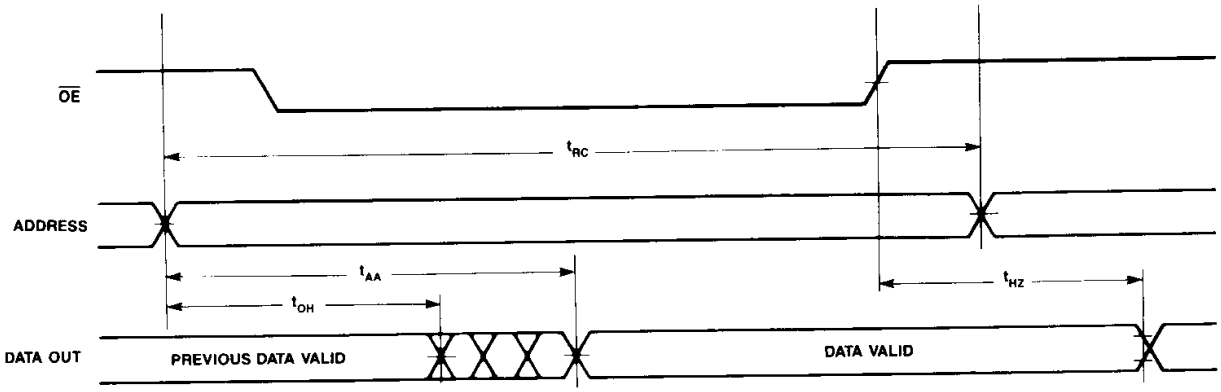


Figure 4. Read Cycle No. 1 [4, 5] - Either Port

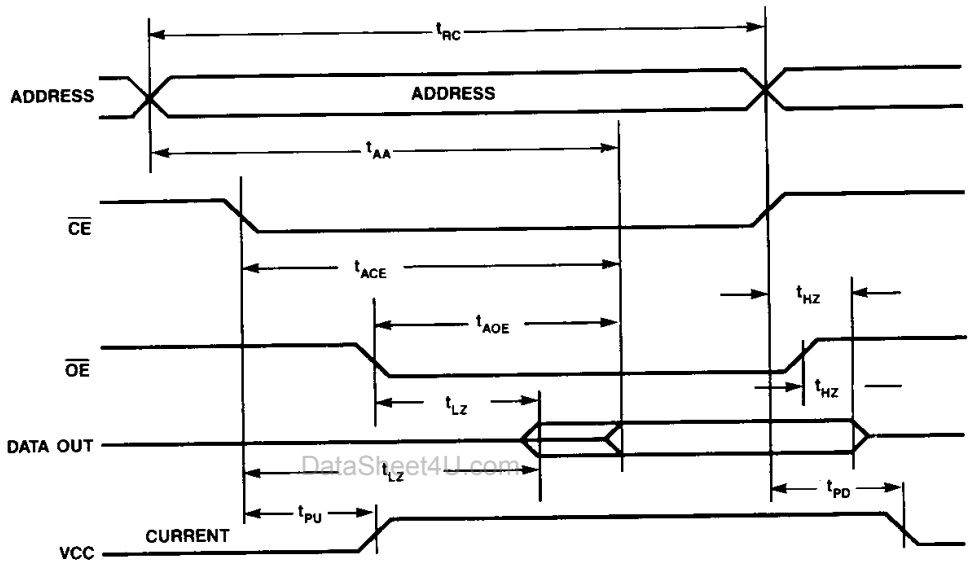


Figure 5. Read Cycle No. 2 [4, 6] - Either Port

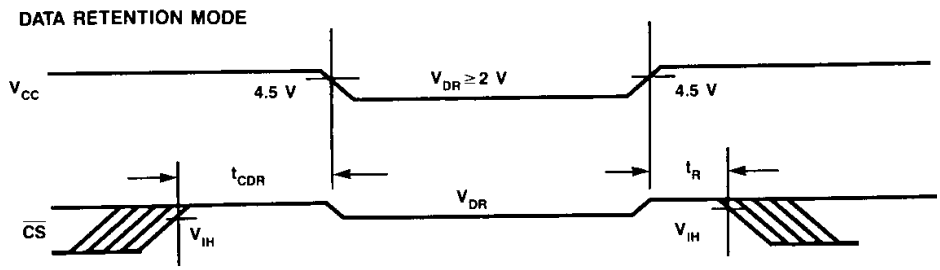


Figure 6. Data Retention Mode Timing

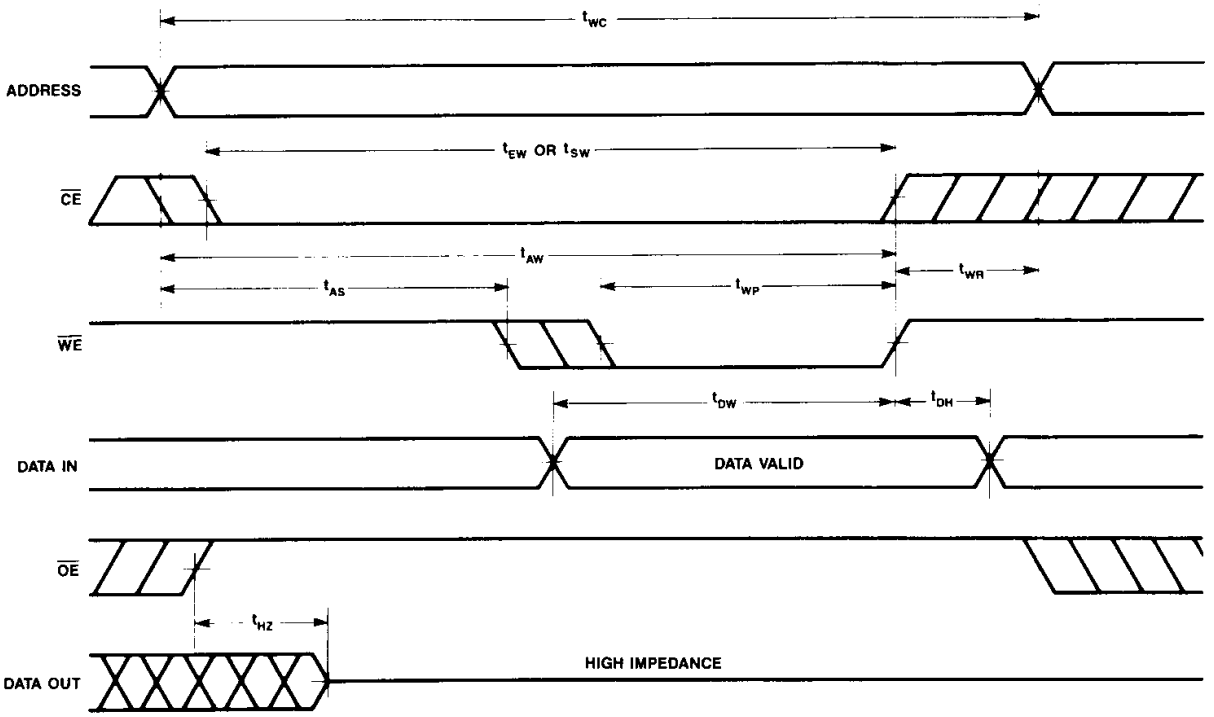


Figure 7. Write Cycle No. 1 [7] - Either Port

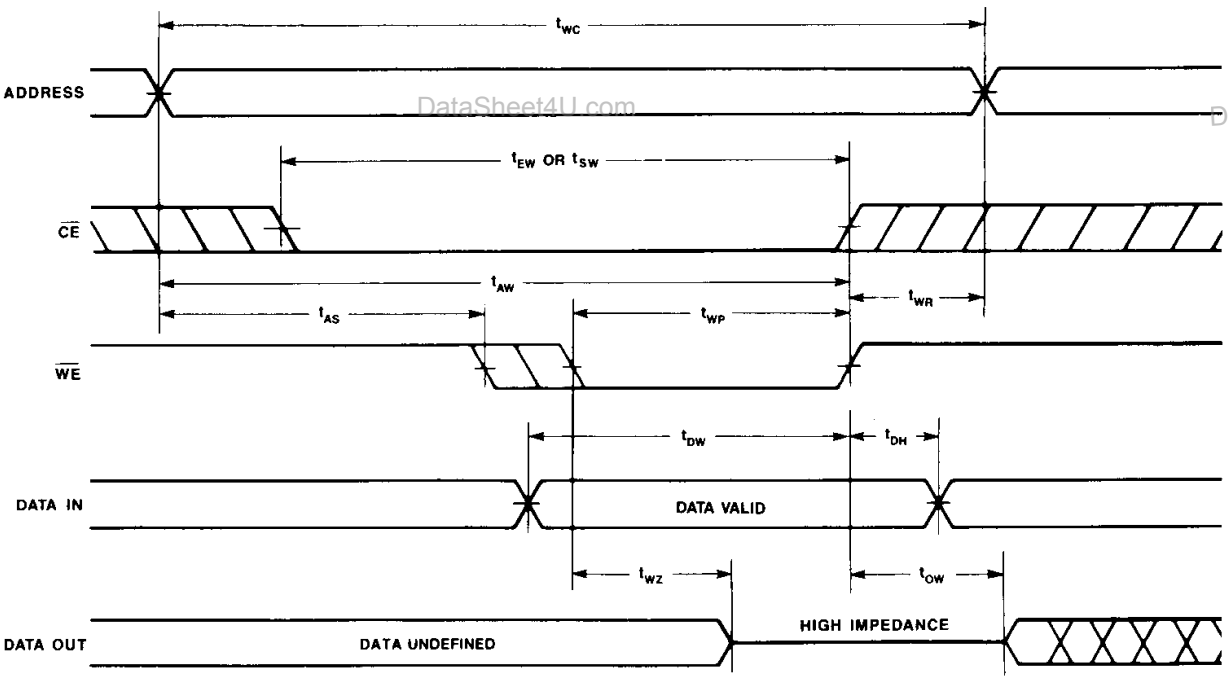


Figure 8. Write Cycle No. 2, Either Port (OE = VIL)[7]

AC CHARACTERISTICS
WRITE CYCLE

T_A = 0°C to +70°C, V_{CC} = 5 V ±10%

SYMBOL	PARAMETER	MK4532A/42A-30		MK4532A/42A-35		MK4532A/42A-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC} Note 13	Write Cycle Time	30		35		45	—	ns
t_{EW}	Chip Enable to End of Write	30		30		35	—	ns
t_{AW}	Address Valid to End of Write	25		30		35	—	ns
t_{AS}	Address Setup Time	0		0		0	—	ns
t_{WP}	Write Pulse Width	20		20		30	—	ns
t_{WR}	Write Recovery Time	0		0		0	—	ns
t_{DW}	Data Valid to End of Write	15		15		20	—	ns
t_{DH}	Data Hold Time	0		0		0	—	ns
t_{WZ} Note 2, 3	Write Enable to Output in High Z	—	15	—	15	—	20	ns
t_{OW} Note 2, 3	Output Active from End of Write	0		0		0	—	ns

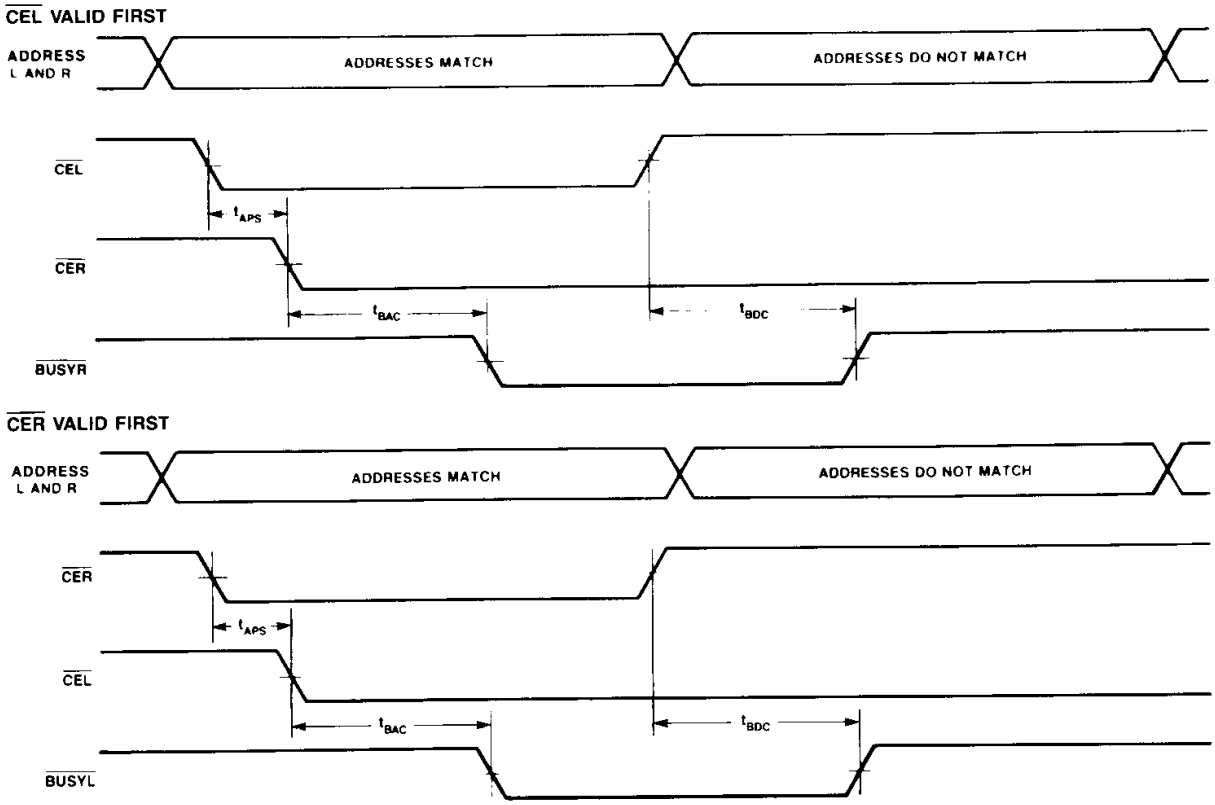


Figure 9. Contention Cycle No. 1, $\overline{CE}$ Contention Arbitration Mode[14]

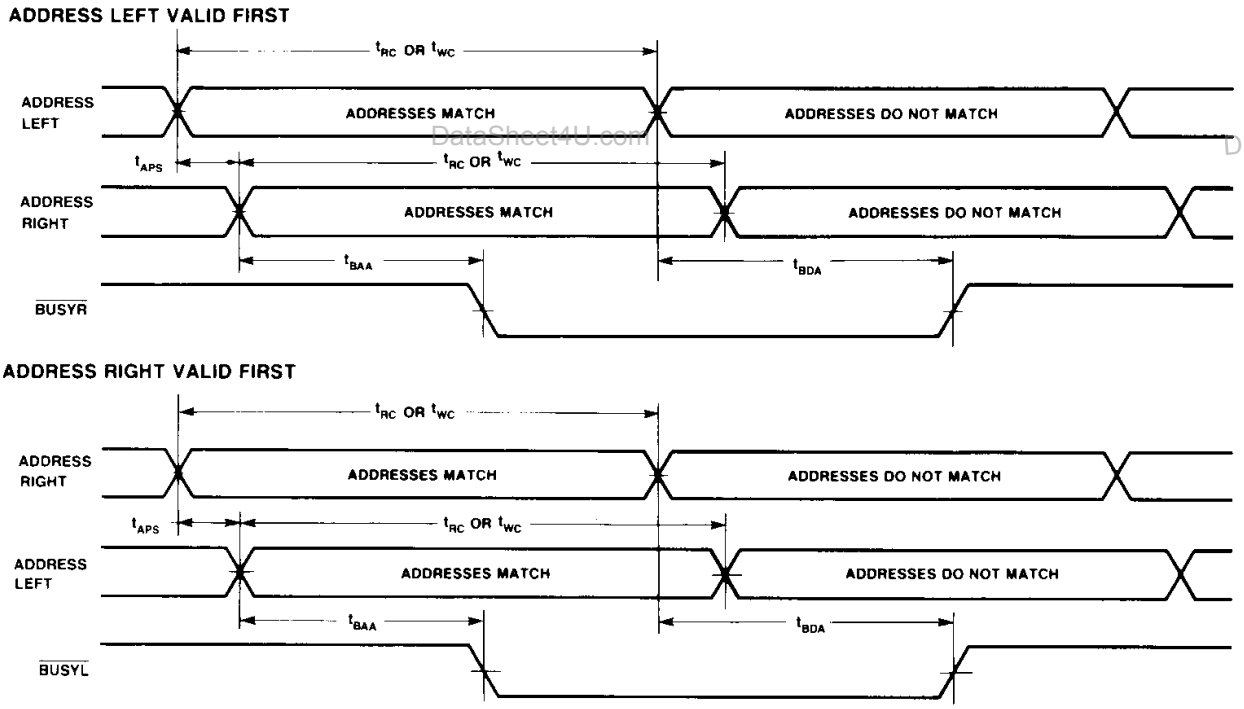


Figure 10. Contention Cycle No. 2, Address Contention Arbitration Mode[14, 15]

AC CHARACTERISTICS
BUSY CYCLE

T_A = 0°C to +70°C, V_{CC} = 5 V ±10%

SYMBOL	PARAMETER	MK4532A/42A-30		MK4532A/42A-35		MK4532A/42A-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WB} Note 8, 9	Write to BUSY	−5		−10		−10		ns
t_{WH}	Write Hold After BUSY	20		20		30		ns
t_{BAA}	BUSY Access Time to Address		20		25		30	ns
t_{BDA}	BUSY Disable Time to Address		20		25		30	ns
t_{BAC}	BUSY Access Time to Chip Enable		20		25		30	ns
t_{BDC}	BUSY Disable Time to Chip Enable		20		25		30	ns
t_{WDD} Note 10	Write Pulse to Data Delay		35		40		50	ns
t_{DDD} Note 10	Write Data Valid to Read Data Delay		35		40		50	ns
t_{BDD} Note 11	BUSY Disable to Valid Data		note 11		note 11		note 11	ns
t_{APS}	Arbitration Priority Set Up Time	2		5		5		ns
t_{AOS}	Arbitration Override Set Up Time	5		5		5		ns

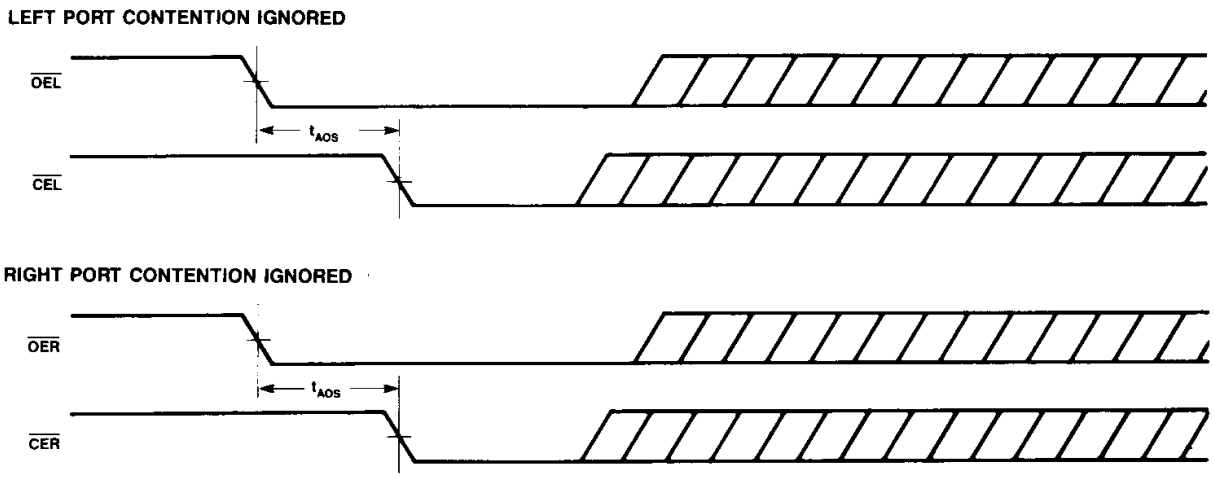


Figure 11. Contention Cycle No. 3, Contention Override Mode[16]

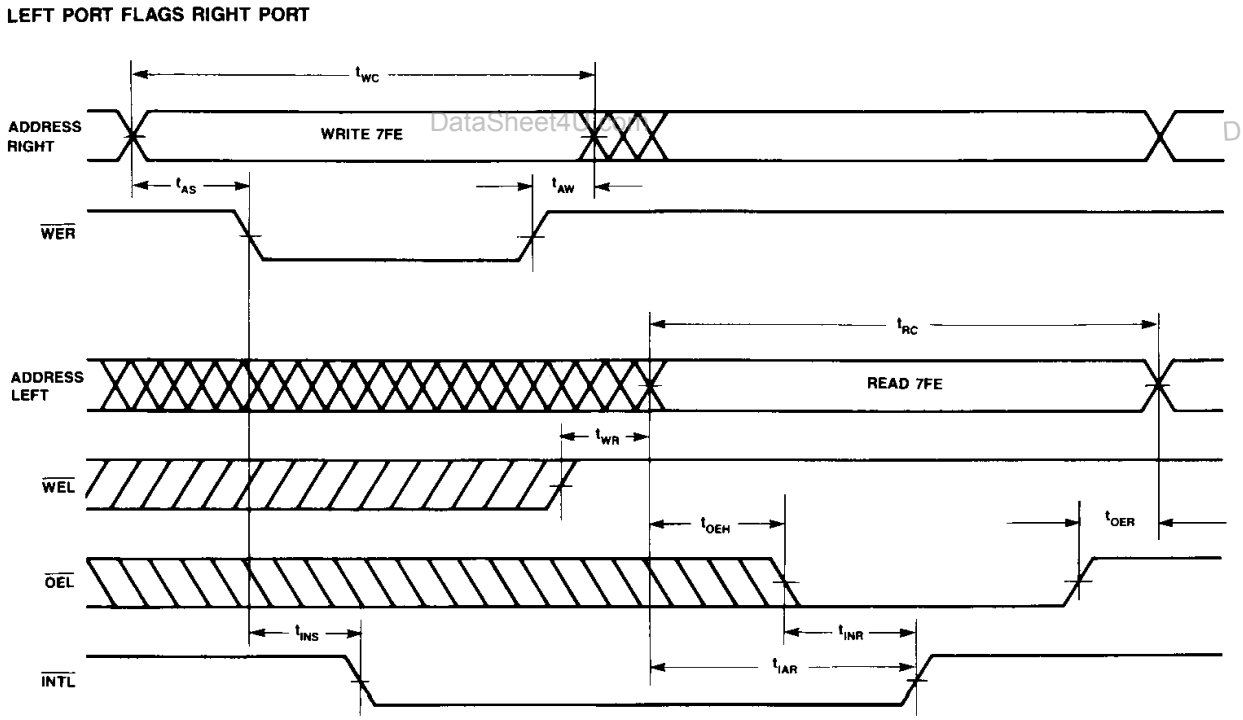


Figure 12. Interrupt Mode[15]

RIGHT PORT FLAGS LEFT PORT

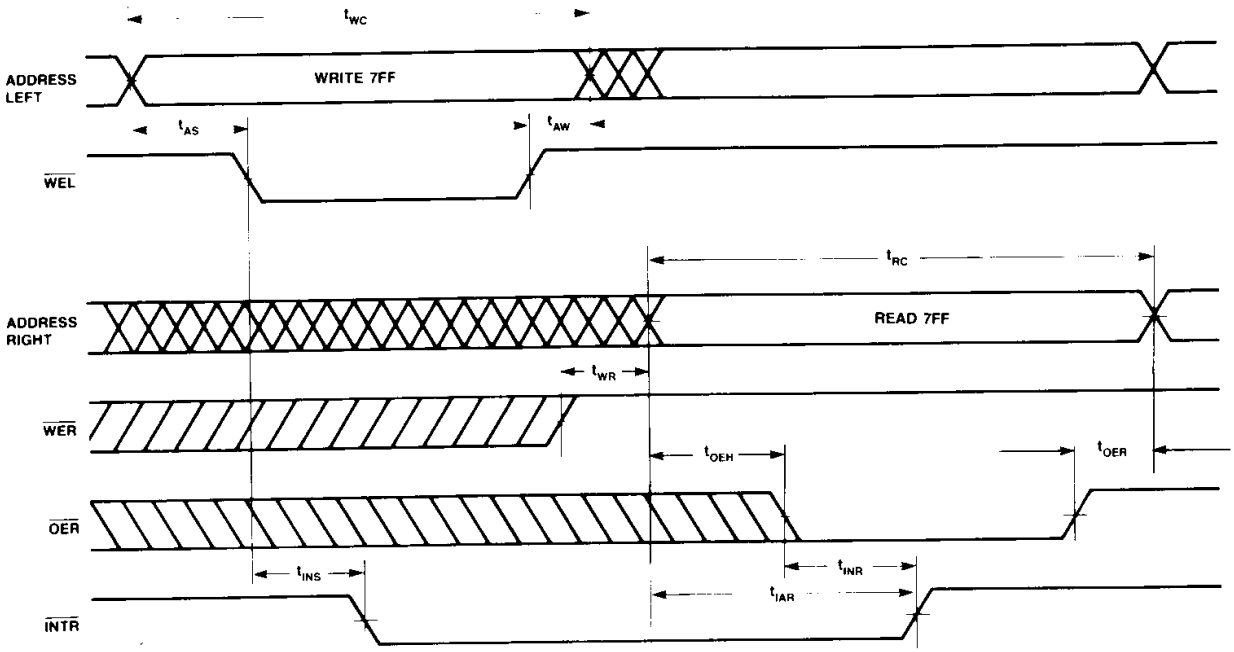


Figure 12. Interrupt Mode (Continued)

INTERRUPT TIMING

SYMBOL	PARAMETER	MK4532A/42A-30		MK4532A/42A-35		MK4532A/42A-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AS}	Address Set Up Time	0		0		0		ns
t_{AW}	Write Recovery Time	0		0		0		ns
t_{INS}	Interrupt Set Time		20		25		30	ns
t_{INR}	Interrupt Reset Time		20		25		30	ns
t_{IAR}	Interrupt Address Recovery Time		20		25		30	ns
t_{OER}	Output Enable Recovery Time		20		25		30	ns

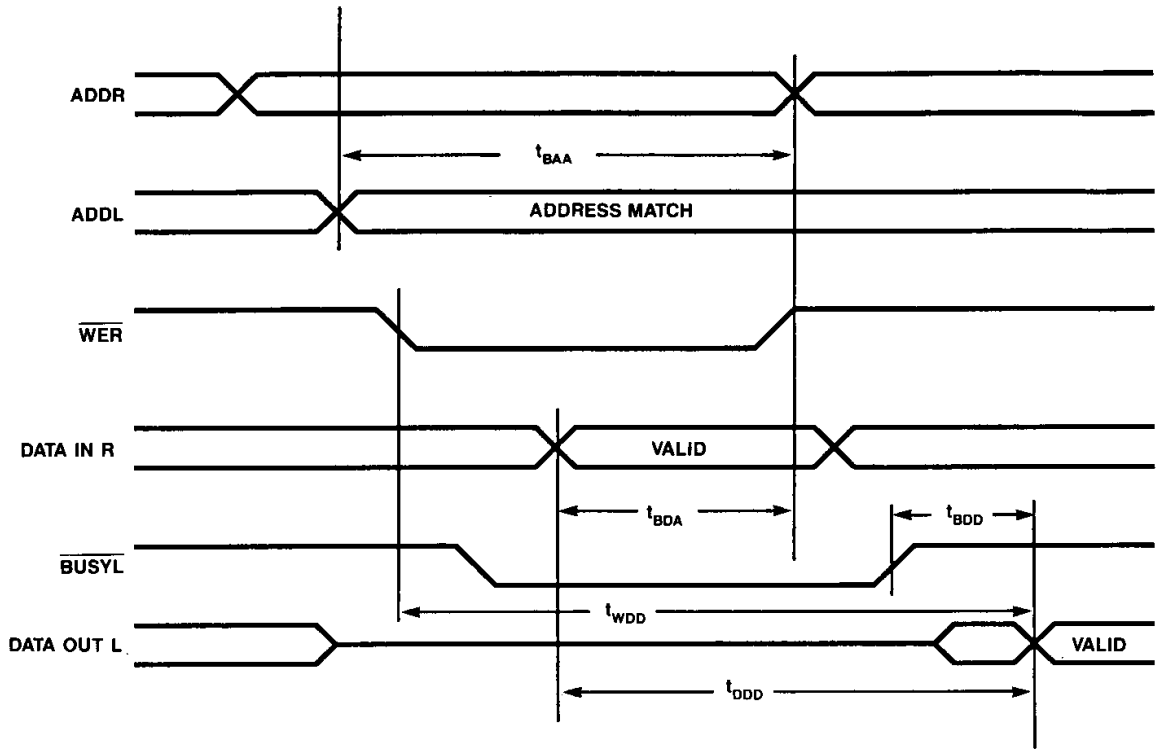


Figure 13. Read With $\overline{BUSY}$ Flag

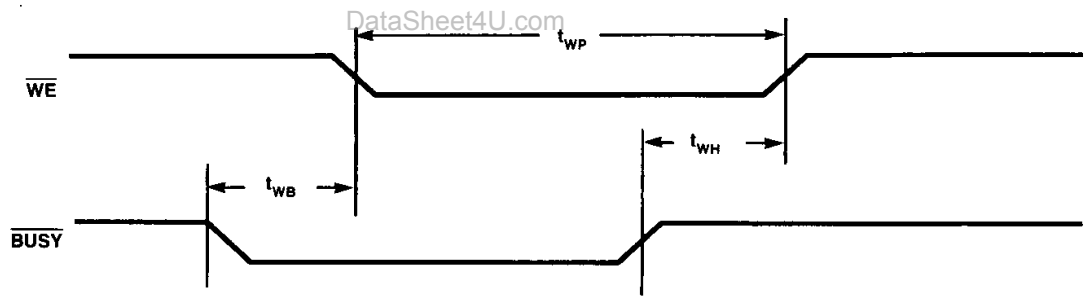


Figure 14. Write With $\overline{BUSY}$-Slave Only (MK4542A)

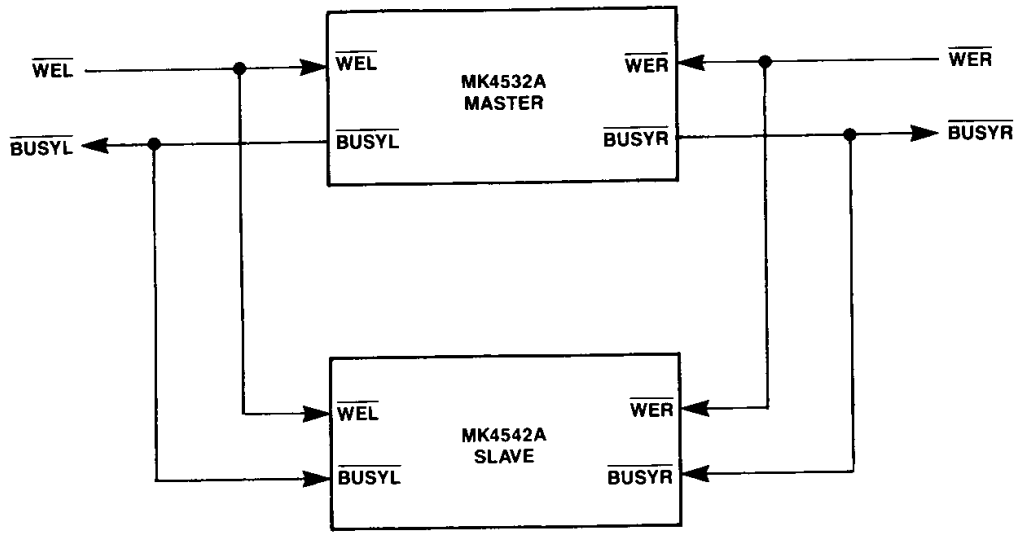
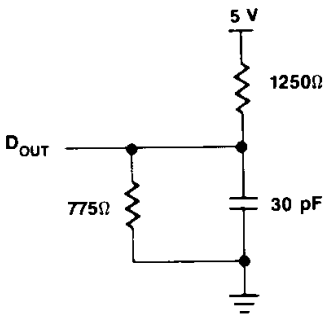


Figure 15. Master Slave Expansion to 16-Bit Memory System

AC TEST CONDITIONS

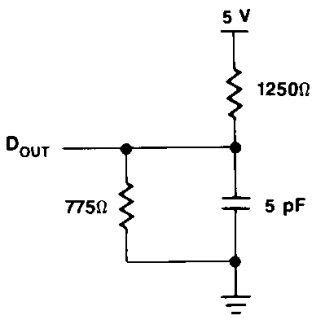
Input Voltage Levels	0 V to +3 V
Input Rise and Fall Times	5 ns
Input Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	Load A, B, C

OUTPUT LOAD CIRCUIT (3A)



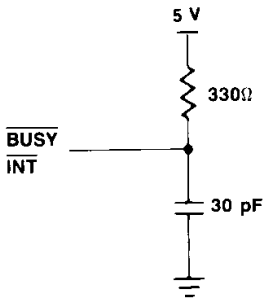
LOAD A

OUTPUT LOAD CIRCUIT (3B)



LOAD B

OUTPUT LOAD CIRCUIT (3C)



LOAD C

Figure 16. AC Testing Load Circuits

FUNCTIONAL DESCRIPTION

The MK4532A/MK4542A is a 16,384 bit dual port RAM that features two separate I/O ports. Each port allows independent access for read or write to any location in the memory.

The MK4532A/MK4542A features separate left and right port Chip Enable controls ($\overline{CEL}$ and $\overline{CER}$). Each Chip Enable activiates its respective port when it goes LOW and controls automatic power-down circuitry that allows its respective side to remain in a standby power mode as long as it remains HIGH. When a port is active, it is allowed access to the entire memory array.

Each port has an Output Enable control ($\overline{OEL}$ and $\overline{OER}$) that keeps its respective output in a high impedance mode when HIGH. When a port's $\overline{OE}$ is LOW, that port's output drivers are turned on, providing its $\overline{WE}$ is HIGH.

Separate Write Enable inputs ($\overline{WEL}$ and $\overline{WER}$) control writing of new data into any location in the RAM from either port. When $\overline{WEL}$ is LOW, new data is written into the location selected by the left address field. When a port's Write Enable is HIGH, data can be read from that port if its respective $\overline{OE}$ is LOW. When $\overline{WEL}$ is HIGH and $\overline{OEL}$ is LOW, data is read from the location selected by the left address field. When $\overline{WER}$ is HIGH and $\overline{OER}$ is LOW, data is read from the location selected by the right address field.

There is one situation where contention can occur. When both left and right ports are active, both addresses match and $\overline{WEL}$, $\overline{WER}$ are both LOW. Two modes of operation are provided for this situation: (a) on-chip control logic arbitrates the situation; or (b) contention is ignored and both ports are given access to that memory location. $\overline{OE}$ controls the latter mode of operation. IF $\overline{CE}$ is LOW before $\overline{OE}$ goes LOW when both addresses match, then on-chip control logic arbitrates the situation. Priority is given to the port whose $\overline{CE}$ became valid first; the other port will not be allowed access to the memory core until that port's operation is completed.

If both port's $\overline{CE}$ controls become valid at the same time when their $\overline{OE}$s are HIGH, the port meeting t_{APS} is given priority. If both $\overline{CE}$ pins are valid before their respective $\overline{OE}$ controls go LOW and an address change causes an address match while $\overline{OE}$ is HIGH, then priority is given to the port whose address became valid first; the other port is not allowed access to the memory until that port's operation is completed. If both addresses became valid at the same time and match, and $\overline{OE}$ is HIGH, then the port meeting t_{APS} is given priority.

In the other mode, contention is ignored and one or both ports have access to the memory core at all times. This is accomplished by having $\overline{OE}$ LOW when the contention occurs. That is, the RAM core is accessible from a port even if the on-chip control logic would have delayed its access provided: (a) the port's $\overline{OE}$ is LOW when its $\overline{CE}$ goes low during an address match;l or (b) both ports are active and their $\overline{OE}$s are LOW when an address change causes an address match. Therefore, it is possible for both ports to have access to the same memory location at the same time, even in a WRITEL-WRITER situation.

Separate Busy Flags ($\overline{BUSYL}$ and $\overline{BUSYR}$) are provided to signal when a port's access to the memory core has been delayed. When both ports try to access the same memory location, the on-chip arbitration logic causes the $\overline{BUSY}$ Flag to go LOW on the side that is delayed. These flags are provided to allow the user to stop the processor if desired. $\overline{BUSY}$ is driven out fast enough for the processor's address and data to be preserved if desired. The $\overline{BUSY}$ Flags are operational even when the device is operating in the mode where contention is ignored, and function the same as described for contention mode operation. This permits their use to signal the processor that an address match has occurred and data may have been changed.

Interrupt logic is included on-chip to provide a means for two processors to communicate with one another. If the left port writes to memory location 7FF, then the right port Interrupt Flag ($\overline{INT1R}$) is latched LOW until the right port reads data from that same location. If the right port writes to memory location 7FE, then the left port Interrupt Flag ($\overline{INT1L}$) is latched LOW until the left port reads data from that same location. If both ports are enabled and contention occurs, the Busy circuitry will disable the address decoder from setting or resetting the Interrupt Flags. In addition each side has a more general interrupt flag. If the left port writes to any location the right port Interrupt Flag ($\overline{INT2R}$) is latched low until the right port reads any location. The feature has an identical function on the other port. By using this feature the total memory can serve as a system mail box.

Expanding the data bus width beyond 8-bits in a dual port RAM system implies that more than one memory chip will be active at the same time. Due to system timing and skews the result could be the $\overline{BUSYL}$ being active on one device while the $\overline{BUSYR}$ being active on another. To avoid this lock-out problem the MASTER/SLAVE approach allows only one of the memory chips to perform the arbitration. The system would use only one MK4532A MASTER unit with additional MK4542A SLAVE units to fill the additional bus width. The MK4542A SLAVE has $\overline{BUSY}$ inputs which interface with the $\overline{BUSY}$ outputs of the MK4532A without the need for external components and maintains the system performance.

When expanding dual port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip

may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. The same pulse to the SLAVE should be delayed by the maximum arbitration time, t_{BAA} or t_{BAC}, of the MASTER. If a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

READ/WRITE CONTROL FUNCTIONS

LEFT PORT				RIGHT PORT				LEFT PORT			RIGHT PORT			
WEL	CEL	OEL	AOL-A9L	WER	CER	OER	AOR-A9R	BUSYL	INT1L	INT2L	BUSYR	INT1R	INT2R	FUNCTION
X	H	X	X	X	X	X	X	H	X	X	H	X	X	LEFT POWER DOWN
X	X	X	X	X	H	X	X	H	X	X	H	X	X	RIGHT POWER DOWN
H	L	L	X	X	X	X	X	H	X	X	X	X	X	READ LEFT PORT
H	L	H	X	X	H	X	X							LEFT NO-OP, ICC ACTIVE, HI-Z
X	X	X	X	H	L	L	X	X	X	X	H	X	X	READ RIGHT PORT
X	H	X	X	H	L	H	X							RIGHT NO-OP, ICC ACTIVE, HI-Z
L	L	L	≠	X	X	X	≠	H	X	L	X	X	X	WRITE LEFT PORT
X	X	X	≠	L	L	L	≠	X	X	X	H	X	L	WRITE RIGHT PORT
L	L	L	=	L	L	L	=	H	X	X	L	X	X	RIGHT PORT BUSY
L	L	L	=	L	L	L	=	L	X	X	H	X	X	LEFT PORT BUSY
L	L	X	7FF	X	X	X	X	H	X	L	H	L	X	LEFT FLAG RIGHT
X	X	X	X	L	L	X	7FE	H	L	X	H	X	X	RIGHT FLAG LEFT

APPLICATION
TTL AND CMOS LEVELS

To achieve full compatibility with TTL-based devices, CMOS memories are typically designed to convert TTL input levels to the CMOS levels required for internal operation. Greater power efficiency is achieved, however, when an entire design takes advantage of the lower consumption capabilities of CMOS technology. When CMOS levels are used throughout a design and not only in the memory, lower current specifications can be achieved, resulting in a lower over-all power requirement.

POWER DISTRIBUTION AND LINE TERMINATION CONSIDERATIONS

The operating margins of all devices on a board using very-high-speed memory can best be maintained by providing a quiet environment that is free of noise spikes, undershoot, and excessive ringing. Key elements in creating such an atmosphere are observing proper power distribution techniques and proper termination of TTL drive lines.

POWER DISTRIBUTION

A power distribution scheme that effectively maintains wide operating margins combines power trace layout with decoupling capacitor placement to minimize the series impedance in the decoupling path, which runs from the power pin of a memory device through its decoupling capacitor to the ground pin.

The total impedance of this path is established by the power line impedance and the impedance of the capacitor itself. In practice, the capacitive effects of the decoupling path are minimal because of the very-high-frequency components of the current transients associated with memory operation. This makes the line inductance the dominant impedance factor.

To reduce the line inductance, the power and ground traces should either be gridded or be provided by separate power planes. The ground grid should extend to the TTL driver peripheral circuitry, providing a solid ground reference for the TTL drivers. This arrangement also prevents the loss of driver operating margin that can be caused by differential ground noise.

The decoupling capacitor, which provides energy for the high-frequency transients, should be placed as near the memory device as possible in order to have the shortest practical lead lengths. The capacitor should be of a low-inductance type and, at a minimum, be 0.1 μF. For the greatest efficiency, it should be placed between the power supply and ground pins of each device, but it may be sufficient to place it between the rows of memory devices (see figure 17).

Low-frequency current transients can be handled by a larger tantalum capacitor placed near the memory board edge connector, where the power traces meet the backplane power distribution system. Such large capacitors provide bulk energy storage that prevents voltage drops caused by the long inductive path between the memory board and the power supply.

TRACE TERMINATION

On a memory board, trace lines have the appearance of shorted transmission lines to TTL-level driver signals. This can cause reflections of TTL signals propagating down the lines, particularly low-going signals. These reflections can be reduced or eliminated by proper line termination.

Trace line termination can be either series or parallel, although series termination is recommended. This type of termination has the advantage of drawing no dc current, and also requires the smallest number of components to implement. It simply calls for placing a series resistor in the signal line to dampen reflections. The resistor is placed at the output of the TTL driver, as close as possible to the driver package. The driver/termination combination is placed close to the memory array to minimize lead length.

In most applications, a series resistor of from 10 ohms to 33 ohms is sufficient to dampen reflections. However, because the characteristic impedance of each layout is different, some experimentation may be necessary to determine the optimum value for a specific configuration.

SIGNAL FIDELITY

When the layout is complete and the power distribution and line termination requirements have been met, it is good procedure to verify signal fidelity by observation with a wideband oscilloscope and probe. When doing so, however, care should be taken to avoid bus contention situations, particularly in write cycle 1. In this mode, $\overline{WE}$ going high with $\overline{CE}$ low causes the output buffers to be active t_{OW} after the rising edge of $\overline{WE}$. If the address does not change, the data output is the same as the data written in. If the data input during the previous cycle is still valid after the address changes, bus contention may be the result. Contention may also occur if $\overline{CE}$ goes low before $\overline{WE}$ when input data is valid early in the cycle.

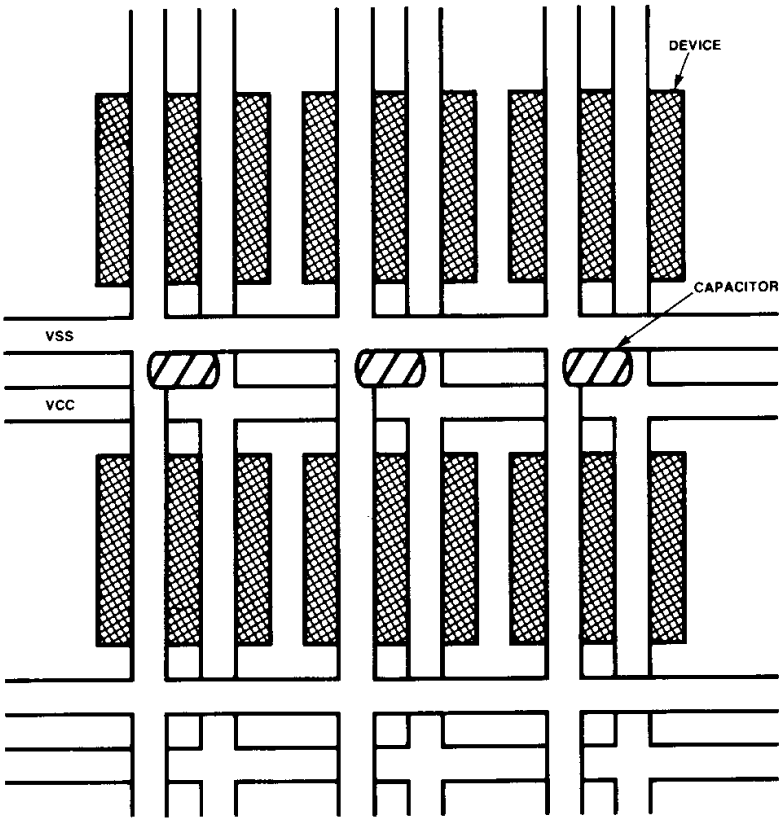
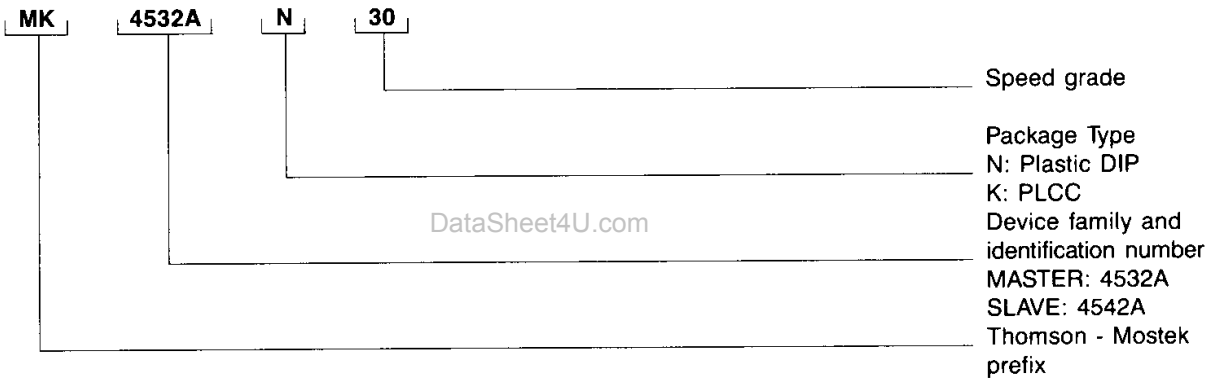


Figure 17. Power Trace Grid With Decoupling Capacitors

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
MK4532AN-30	30 ns	Plastic DIP
MK4532AK-30	30 ns	Plastic Leaded Chip Carrier (PLCC)
MK4542AN-30	30 ns	Plastic DIP
MK4542AK-30	30 ns	Plastic Leaded Chip Carrier (PLCC)
MK4532AN-35	35 ns	Plastic DIP
MK4532AK-35	35 ns	Plastic Leaded Chip Carrier (PLCC)
MK4542AN-35	35 ns	Plastic DIP
MK4542AK-35	35 ns	Plastic Leaded Chip Carrier (PLCC)
MK4532AN-45	45 ns	Plastic DIP
MK4532AK-45	45 ns	Plastic Leaded Chip Carrier (PLCC)
MK4542AN-45	45 ns	Plastic DIP
MK4542AK-45	45 ns	Plastic Leaded Chip Carrier (PLCC)

Operating Temperature Range: 0°C to +70°C



NOTES

1. t_{RC} = Read Cycle Time
2. This parameter is guaranteed but not tested.
3. Transition is measured ±500 mV from LOW or HIGH impedance voltage with load (Figures A, B, C)
4. $\overline{WE}$ is HIGH for read cycles.
5. Device is continuously enabled ($\overline{CE}$ = V_{IL}).
6. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
7. If $\overline{CE}$ goes high at the same time $\overline{WE}$ goes high, the outputs remain in a high-impedance state.
8. For Slave (MK4542A) only.
9. To ensure that the write cycle is inhibited during contention.
10. Port to port delay through RAM cells from writing port to reading port.
11. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{DW} (actual).
12. To ensure that a write cycle is completed after a contention.
13. For MASTER/SLAVE combination, t_{WC} = t_{BAA} + t_{WR} + t_{WP}.
14. $\overline{OE}$ = V_{IH} when contention occurs.
15. $\overline{CEL}$ = $\overline{CER}$ = V_{IL}.
16. Busy timing is identical to contention cycle 1 and 2 timing.

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