# HYS64D64020HBDL–5–C
# HYS64D64020GBDL–5–C
# HYS64D64020HBDL–6–C
# HYS64D64020GBDL–6–C

## 200-Pin Small Outline Dual-In-Line Memory Modules
## SO-DIMM
## DDR SDRAM

Memory Products

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| **Revision History: Rev. 1.1** | **2004-05** |
|---|---|
| Previous Version: Rev. 1.0 | 2004-05 |

| Page | Subjects (major changes since last revision) |
|---|---|
| all | |
| **6**,**7** | Updated Performance table, Order information |
| **13** | Updated Block diagram |
| **19** | Update AC Timing table |
| **17**,**18** | Updated Idd currents to final for DDR333 and DDR400 |
| **21** | Added SPD Codes for DDR400 |
| | |
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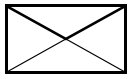

**Table of Contents**

# 1 Overview

## 1.1 Features

- Non-parity 200-Pin Small Outline Dual-In-Line Memory Modules
- Two ranks 64M ×64 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM)
- Single +2.5 V (± 0.2 V) power supply and Single +2.6V (± 0.1 V) power supply for DDR400
- Built with 256 Mbit DDR SDRAMs organised as ×8 in P–TFBGA–60 packages
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with $E^2$PROM
- Jedec standard form factor: 67.60 mm × 31.75 mm × 3.80 mm
- Gold plated contacts

**Table 1 Performance**

| Part Number Speed Code | | | –5 | –6 | Unit |
|---|---|---|---|---|---|
| Speed Grade | Component | | DDR400B | DDR333B | — |
| | Module | | PC3200–3033 | PC2700–2533 | — |
| max. Clock Frequency | @CL3 | $f_{CK3}$ | 200 | 166 | MHz |
| | @CL2.5 | $f_{CK2.5}$ | 166 | 166 | MHz |
| | @CL2 | $f_{CK2}$ | 133 | 133 | MHz |

## 1.2 Description

The HYS64D64020HBDL–5–C and HYS64D64020GBDL–5–C are industry standard 200-Pin Small Outline Dual-In-Line Memory Modules (SO-DIMMs) organized as 64M ×64. The memory array is designed with Double Data Rate Synchronous DRAMs (DDR SDRAM). A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial $E^2$PROM device using the 2-pin $I^2C$ protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

**Notes**

1. *All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS64D32020GDL-6-B, indicating rev. B dies are used for SDRAM components.*
2. *The Compliance Code is printed on the module labels describing the speed sort (for example “PC2700”), the latencies and SPD code definition (for example “2033–0” means CAS latency of 2.0 clocks, RCD[1)] latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definiton version 0), and the Raw Card used for this module.*

1) RCD: Row-Column-Delay

**Table 2 Ordering Information**

| Type | Compliance Code | Description | SDRAM Technology |
|---|---|---|---|
| **PC3200 (CL=3.0)** | | | |
| HYS64D64020GBDL–5–C | PC3200S–3033–1–Z | two ranks 512 MB SO-DIMM | 32 MBit (×8) |
| **PC2700 (CL=2.5)** | | | |
| HYS64D64020GBDL–6–C | PC2700S–2533–0–Z | two ranks 512 MB SO-DIMM | 32 MBit (×8) |
| **PC3200 (CL=3.0)** | | | green Product |
| HYS64D64020HBDL–5–C | PC3200S–3033–1–Z | two ranks 512 MB SO-DIMM | 32 MBit (×8) |
| **PC2700 (CL=2.5)** | | | |
| HYS64D64020HBDL–6–C | PC2700S–2533–0–Z | two ranks 512 MB SO-DIMM | 32 MBit (×8) |

# 2 Pin Configuration

The pin configuration of the Unbuffered Small Outline DDR SDRAM DIMM is listed by function in **Table 3** (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 4** and **Table 5** respectively. The pin numbering is depicted in **Figure 1**.

**Table 3 Pin Configuration of SO-DIMM**

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Clock Signals** | | | | |
| 35 | CK0 | I | SSTL | **Clock Signal** |
| 160 | CK1 | I | SSTL | **Clock Signal** |
| 89 | CK2 | I | SSTL | **Clock Signal**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: non-ECC type module* |
| 37 | $\overline{CK0}$ | I | SSTL | **Complement Clock** |
| 158 | $\overline{CK1}$ | I | SSTL | **Complement Clock** |
| 91 | $\overline{CK2}$ | I | SSTL | **Complement Clock**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: non-ECC type module* |
| 96 | CKE0 | I | SSTL | **Clock Enable Rank 0** |
| 95 | CKE1 | I | SSTL | **Clock Enable Rank 1**<br>*Note: 2-rank module* |
| | NC | NC | – | *Note: 1-rank module* |
| **Control Signals** | | | | |
| 121 | $\overline{S0}$ | I | SSTL | **Chip Select Rank 0** |
| 122 | $\overline{S1}$ | I | SSTL | **Chip Select Rank 1**<br>*Note: 2-ranks module* |
| | NC | NC | – | *Note: 1-rank module* |
| 118 | $\overline{RAS}$ | I | SSTL | **Row Address Strobe** |
| 120 | $\overline{CAS}$ | I | SSTL | **Column Address Strobe** |
| 119 | $\overline{WE}$ | I | SSTL | **Write Enable** |
| **Address Signals** | | | | |
| 117 | BA0 | I | SSTL | **Bank Address Bus 1:0** |
| 116 | BA1 | I | SSTL | |

**Table 3 Pin Configuration of SO-DIMM** (cont'd)

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 112 | A0 | I | SSTL | **Address Bus 11:0** |
| 111 | A1 | I | SSTL | |
| 110 | A2 | I | SSTL | |
| 109 | A3 | I | SSTL | |
| 108 | A4 | I | SSTL | |
| 107 | A5 | I | SSTL | |
| 106 | A6 | I | SSTL | |
| 105 | A7 | I | SSTL | |
| 102 | A8 | I | SSTL | |
| 101 | A9 | I | SSTL | |
| 115 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| 100 | A11 | I | SSTL | |
| 99 | A12 | I | SSTL | **Address Signal 12**<br>*Note: Module based on 256 Mbit or larger dies* |
| | NC | NC | – | *Note: 128 Mbit based module* |
| 123 | A13 | I | SSTL | **Address Signal 13**<br>*Note: 1 Gbit based module* |
| | NC | NC | – | *Note: Module based on 512 Mbit or smaller dies* |
| **Data Signals** | | | | |
| 5 | DQ0 | I/O | SSTL | **Data Bus 63:0** |
| 7 | DQ1 | I/O | SSTL | |
| 13 | DQ2 | I/O | SSTL | |
| 17 | DQ3 | I/O | SSTL | |
| 6 | DQ4 | I/O | SSTL | |
| 8 | DQ5 | I/O | SSTL | |
| 14 | DQ6 | I/O | SSTL | |
| 18 | DQ7 | I/O | SSTL | |
| 19 | DQ8 | I/O | SSTL | |
| 23 | DQ9 | I/O | SSTL | |
| 29 | DQ10 | I/O | SSTL | |
| 31 | DQ11 | I/O | SSTL | |
| 20 | DQ12 | I/O | SSTL | |
| 24 | DQ13 | I/O | SSTL | |

**Table 3 Pin Configuration of SO-DIMM** (cont'd)

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 30 | DQ14 | I/O | SSTL | **Data Bus 63:0** |
| 32 | DQ15 | I/O | SSTL | |
| 41 | DQ16 | I/O | SSTL | |
| 43 | DQ17 | I/O | SSTL | |
| 49 | DQ18 | I/O | SSTL | |
| 53 | DQ19 | I/O | SSTL | |
| 42 | DQ20 | I/O | SSTL | |
| 44 | DQ21 | I/O | SSTL | |
| 50 | DQ22 | I/O | SSTL | |
| 54 | DQ23 | I/O | SSTL | |
| 55 | DQ24 | I/O | SSTL | |
| 59 | DQ25 | I/O | SSTL | |
| 65 | DQ26 | I/O | SSTL | |
| 67 | DQ27 | I/O | SSTL | |
| 56 | DQ28 | I/O | SSTL | |
| 60 | DQ29 | I/O | SSTL | |
| 66 | DQ30 | I/O | SSTL | |
| 68 | DQ31 | I/O | SSTL | |
| 127 | DQ32 | I/O | SSTL | |
| 129 | DQ33 | I/O | SSTL | |
| 135 | DQ34 | I/O | SSTL | |
| 139 | DQ35 | I/O | SSTL | |
| 128 | DQ36 | I/O | SSTL | |
| 130 | DQ37 | I/O | SSTL | |
| 136 | DQ38 | I/O | SSTL | |
| 140 | DQ39 | I/O | SSTL | |
| 141 | DQ40 | I/O | SSTL | |
| 145 | DQ41 | I/O | SSTL | |
| 151 | DQ42 | I/O | SSTL | |
| 153 | DQ43 | I/O | SSTL | |
| 142 | DQ44 | I/O | SSTL | |
| 146 | DQ45 | I/O | SSTL | |
| 152 | DQ46 | I/O | SSTL | |
| 154 | DQ47 | I/O | SSTL | |
| 163 | DQ48 | I/O | SSTL | |
| 165 | DQ49 | I/O | SSTL | |
| 171 | DQ50 | I/O | SSTL | |
| 175 | DQ51 | I/O | SSTL | |
| 164 | DQ52 | I/O | SSTL | |
| 166 | DQ53 | I/O | SSTL | |

**Table 3 Pin Configuration of SO-DIMM** (cont'd)

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 172 | DQ54 | I/O | SSTL | **Data Bus 63:0** |
| 176 | DQ55 | I/O | SSTL | |
| 177 | DQ56 | I/O | SSTL | |
| 181 | DQ57 | I/O | SSTL | |
| 187 | DQ58 | I/O | SSTL | |
| 189 | DQ59 | I/O | SSTL | |
| 178 | DQ60 | I/O | SSTL | |
| 182 | DQ61 | I/O | SSTL | |
| 188 | DQ62 | I/O | SSTL | |
| 190 | DQ63 | I/O | SSTL | |
| 71 | CB0 | I/O | SSTL | **Check Bit 0**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 73 | CB1 | I/O | SSTL | **Check Bit 1**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 79 | CB2 | I/O | SSTL | **Check Bit 2**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 83 | CB3 | I/O | SSTL | **Check Bit 3**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 72 | CB4 | I/O | SSTL | **Check Bit 4**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 74 | CB5 | I/O | SSTL | **Check Bit 5**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |

**Table 3 Pin Configuration of SO-DIMM** (cont'd)

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 80 | CB6 | I/O | SSTL | **Check Bit 6**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 84 | CB7 | I/O | SSTL | **Check Bit 7**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 11 | DQS0 | I/O | SSTL | **Data Strobes 7:0**<br>*Note: See block diagram for corresponding DQ signals* |
| 25 | DQS1 | I/O | SSTL | |
| 47 | DQS2 | I/O | SSTL | |
| 61 | DQS3 | I/O | SSTL | |
| 133 | DQS4 | I/O | SSTL | |
| 147 | DQS5 | I/O | SSTL | |
| 169 | DQS6 | I/O | SSTL | |
| 183 | DQS7 | I/O | SSTL | |
| 77 | DQS8 | I/O | SSTL | **Data Strobe 8**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| 12 | DM0 | I | SSTL | **Data Mask 7:0** |
| 26 | DM1 | I | SSTL | |
| 48 | DM2 | I | SSTL | |
| 62 | DM3 | I | SSTL | |
| 134 | DM4 | I | SSTL | |
| 148 | DM5 | I | SSTL | |
| 170 | DM6 | I | SSTL | |
| 184 | DM7 | I | SSTL | |
| 78 | DM8 | I | SSTL | **Data Mask 8**<br>*Note: ECC type module* |
| | NC | NC | – | *Note: Non-ECC module* |
| **EEPROM** | | | | |
| 195 | SCL | I | CMOS | **Serial Bus Clock** |
| 193 | SDA | I/O | OD | **Serial Bus Data** |
| 194 | SA0 | I | CMOS | **Slave Address Select Bus 2:0** |
| 196 | SA1 | I | CMOS | |
| 198 | SA2 | I | CMOS | |

**Table 3 Pin Configuration of SO-DIMM** (cont'd)

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Power Supplies** | | | | |
| 1,2 | $V_{REF}$ | AI | – | **I/O Reference Voltage** |
| 197 | $V_{DDSPD}$ | PWR | – | **EEPROM Power Supply** |
| 9,10, 21, 22, 33, 34, 36, 45, 46, 57, 58, 69, 70, 81, 82, 92, 93, 94, 113, 114, 131, 132, 143, 144, 155, 156, 157, 167, 168, 179, 180, 191, 192 | $V_{DD}$ | PWR | – | **Power Supply** |

**Table 3 Pin Configuration of SO-DIMM** (cont'd)

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 3,4, 15, 16, 27, 28, 38, 39, 40, 51, 52, 63, 64, 75, 76, 87, 88, 90, 103, 104, 125, 126, 137, 138, 149, 150, 159, 161, 162, 173, 174, 185, 186 | $V_{SS}$ | GND | – | **Ground Plane** |
| **Other Pins** | | | | |
| 199 | $V_{DDID}$ | O | OD | **$V_{DD}$ Identification**<br>*Note: Pin in tristate, indicating $V_{DD}$ and $V_{DDQ}$ nets connected on PCB* |

**Table 3 Pin Configuration of SO-DIMM** (cont'd)

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 85, 86, 97, 98, 124, 200 | NC | NC | – | **Not connected**<br>*Note: Pins not connected on Infineon SO DIMMs* |

**Table 4 Abbreviations for Pin Type**

| Abbreviation | Description |
|---|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NC | Not Connected |

**Table 5 Abbreviations for Buffer Type**

| Abbreviation | Description |
|---|---|
| SSTL | Serial Stub Terminalted Logic (SSTL2) |
| LV-CMOS | Low Voltage CMOS |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. |

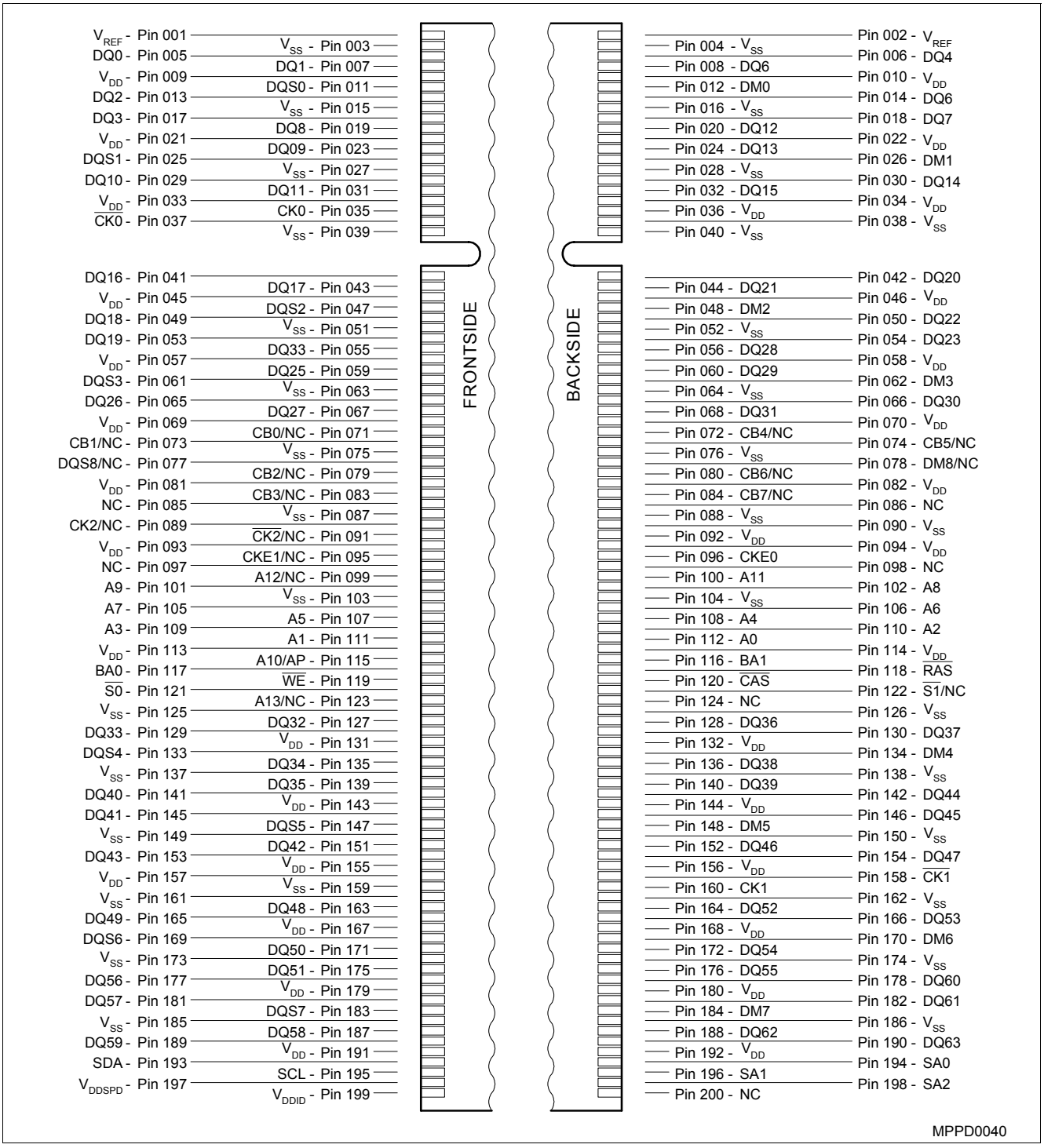


**Figure 1 Pin Configuration Diagram 200-Pin SO-DIMM**

**Table 6 Address Format**

| Density | Organization | Memory Ranks | SDRAMs | # of SDRAMs | # of row/bank/ columns bits | Refresh | Period | Interval |
|---|---|---|---|---|---|---|---|---|
| 512MB | 64M ×64 | 2 | 32M ×8 | 16 | 13/2/10 | 8K | 64 ms | 7.8 µs |

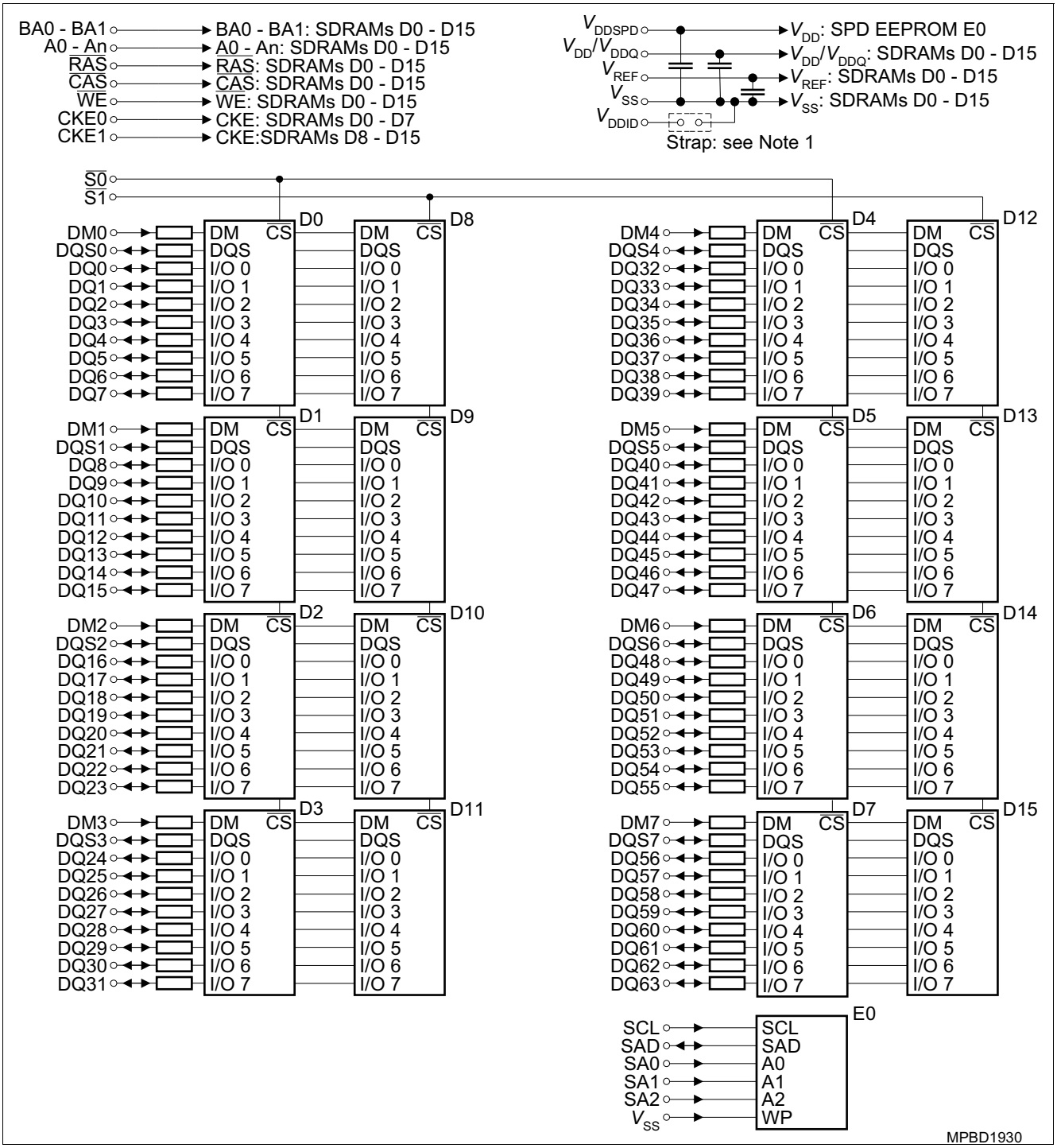


**Figure 2 Block Diagram SO-DIMM Raw Card A (×64, 2 Ranks, ×8)**

*Note:*

1. *$V_{DD}$ = $V_{DDQ}$, therefore $V_{DDID}$ strap open*
2. *DQ, DQS, DM resistors are 22 Ω ±5 %*

**Table 7 Clock Signal Loads**

| Clock Input | Number of SDRAMs | Note |
|---|---|---|
| CK0, $\overline{CK0}$ | 8 SDRAMs | — |
| CK1, $\overline{CK1}$ | 8 SDRAMs | — |
| CK2, $\overline{CK2}$ | 0 SDRAMs | — |

# 3 Electrical Characteristics

## 3.1 Operating Conditions

**Table 8 Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Voltage on I/O pins relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | –0.5 | – | $V_{DDQ}$ + 0.5 | V | – |
| Voltage on inputs relative to $V_{SS}$ | $V_{IN}$ | –1 | – | +3.6 | V | – |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | –1 | – | +3.6 | V | – |
| Voltage on $V_{DDQ}$ supply relative to $V_{SS}$ | $V_{DDQ}$ | –1 | – | +3.6 | V | – |
| Operating temperature (ambient) | $T_A$ | 0 | – | +70 | °C | – |
| Storage temperature (plastic) | $T_{STG}$ | -55 | – | +150 | °C | – |
| Power dissipation (per SDRAM component) | $P_D$ | – | 1 | – | W | – |
| Short circuit output current | $I_{OUT}$ | – | 50 | – | mA | – |

***Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.***

**Table 9 Electrical Characteristics and DC Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note/Test Condition [1] |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | $V_{DD}$ | 2.3 | 2.5 | 2.7 | V | $f_{CK} \leq 166$ MHz |
| Device Supply Voltage | $V_{DD}$ | 2.5 | 2.6 | 2.7 | V | $f_{CK} > 166$ MHz [2] |
| Output Supply Voltage | $V_{DDQ}$ | 2.3 | 2.5 | 2.7 | V | $f_{CK} \leq 166$ MHz |
| Output Supply Voltage | $V_{DDQ}$ | 2.5 | 2.6 | 2.7 | V | $f_{CK} > 166$ MHz [2] |
| EEPROM supply voltage | $V_{DDSPD}$ | 2.3 | 2.5 | 3.6 | V | — |
| Supply Voltage, I/O Supply Voltage | $V_{SS}$, $V_{SSQ}$ | 0 | | 0 | V | — |
| Input Reference Voltage | $V_{REF}$ | 0.49 × $V_{DDQ}$ | 0.5 × $V_{DDQ}$ | 0.51 × $V_{DDQ}$ | V | [3] |
| I/O Termination Voltage (System) | $V_{TT}$ | $V_{REF}$ – 0.04 | | $V_{REF}$ + 0.04 | V | [4] |
| Input High (Logic1) Voltage | $V_{IH(DC)}$ | $V_{REF}$ + 0.15 | | $V_{DDQ}$ + 0.3 | V | [7] |
| Input Low (Logic0) Voltage | $V_{IL(DC)}$ | –0.3 | | $V_{REF}$ – 0.15 | V | [7] |
| Input Voltage Level, CK and $\overline{CK}$ Inputs | $V_{IN(DC)}$ | –0.3 | | $V_{DDQ}$ + 0.3 | V | [7] |
| Input Differential Voltage, CK and $\overline{CK}$ Inputs | $V_{ID(DC)}$ | 0.36 | | $V_{DDQ}$ + 0.6 | V | [7][5] |
| VI-Matching Pull-up Current to Pull-down Current | $VI_{Ratio}$ | 0.71 | | 1.4 | — | [6] |

**Table 9 Electrical Characteristics and DC Operating Conditions** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note/Test Condition [1] |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Leakage Current | $I_I$ | –2 | | 2 | µA | Any input 0 V ≤ $V_{IN}$ ≤ $V_{DD}$; All other pins not under test = 0 V [7)8)] |
| Output Leakage Current | $I_{OZ}$ | –5 | | 5 | µA | DQs are disabled; 0 V ≤ $V_{OUT}$ ≤ $V_{DDQ}$ [7)] |
| Output High Current, Normal Strength Driver | $I_{OH}$ | — | | –16.2 | mA | $V_{OUT}$ = 1.95 V [7)] |
| Output Low Current, Normal Strength Driver | $I_{OL}$ | 16.2 | | — | mA | $V_{OUT}$ = 0.35 V [7)] |

1) 0 °C ≤ $T_A$ ≤ 70 °C

2) DDR400 conditions apply for all clock frequencies above 166 MHz

3) Peak to peak AC noise on $V_{REF}$ may not exceed ± 2% $V_{REF\ (DC)}$. $V_{REF}$ is also expected to track noise variations in $V_{DDQ}$.

4) $V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors, is expected to be set equal to $V_{REF}$, and must track variations in the DC level of $V_{REF}$.

5) $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

6) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

7) Inputs are not recognized as valid until $V_{REF}$ stabilizes.

8) Values are shown per DDR SDRAM component

## 3.2 Current Specification and Conditions

**Table 10 $I_{DD}$ Conditions**

| Parameter | Symbol |
|---|---|
| **Operating Current 0**<br>one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle;<br>address and control inputs changing once every two clock cycles. | $I_{DD0}$ |
| **Operating Current 1**<br>one bank; active/read/precharge; Burst Length = 4; see component data sheet. | $I_{DD1}$ |
| **Precharge Power-Down Standby Current**<br>all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$ | $I_{DD2P}$ |
| **Precharge Floating Standby Current**<br>$\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$;<br>address and other control inputs changing once per clock cycle; $V_{IN}$ = $V_{REF}$ for DQ, DQS and DM. | $I_{DD2F}$ |
| **Precharge Quiet Standby Current**<br>$\overline{CS}$ ≥ $V_{IHMIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; $V_{IN}$ = $V_{REF}$ for DQ, DQS and DM;<br>address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$. | $I_{DD2Q}$ |
| **Active Power-Down Standby Current**<br>one bank active; power-down mode; CKE ≤ $V_{ILMAX}$; $V_{IN}$ = $V_{REF}$ for DQ, DQS and DM. | $I_{DD3P}$ |
| **Active Standby Current**<br>one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; $t_{RC}$ = $t_{RAS,MAX}$;<br>DQ, DM and DQS inputs changing twice per clock cycle;<br>address and control inputs changing once per clock cycle. | $I_{DD3N}$ |
| **Operating Current Read**<br>one bank active; Burst Length = 2; reads; continuous burst;<br>address and control inputs changing once per clock cycle;<br>50% of data outputs changing on every clock edge;<br>CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; $I_{OUT}$ = 0 mA | $I_{DD4R}$ |
| **Operating Current Write**<br>one bank active; Burst Length = 2; writes; continuous burst;<br>address and control inputs changing once per clock cycle;<br>50% of data outputs changing on every clock edge;<br>CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B | $I_{DD4W}$ |
| **Auto-Refresh Current**<br>$t_{RC}$ = $t_{RFCMIN}$, burst refresh | $I_{DD5}$ |
| **Self-Refresh Current**<br>CKE ≤ 0.2 V; external clock on | $I_{DD6}$ |
| **Operating Current 7**<br>four bank interleaving with Burst Length = 4; see component data sheet. | $I_{DD7}$ |

**Table 11 $I_{DD}$ Specification for HYS64D64020[G/H]BDL–5–C**

| **Product Type** | **HYS64D64020GBDL–5–C HYS64D64020HBDL–5–C** | | **Unit** | **Note 1)2)** |
|---|---|---|---|---|
| **Organization** | **512MB** | | | |
| | **×64** | | | |
| | **2 Ranks** | | | |
| | **–5** | | | |
| **Symbol** | **Typ.** | **Max.** | | |
| $I_{DD0}$ | 940 | 1150 | mA | 3) |
| $I_{DD1}$ | 1100 | 1310 | mA | 3)4) |
| $I_{DD2P}$ | 480 | 580 | mA | 5) |
| $I_{DD2F}$ | 320 | 450 | mA | 5) |
| $I_{DD2Q}$ | 210 | 290 | mA | 5) |
| $I_{DD3P}$ | 610 | 720 | mA | 5) |
| $I_{DD3N}$ | 690 | 860 | mA | 5) |
| $I_{DD4R}$ | 1140 | 1390 | mA | 3)4) |
| $I_{DD4W}$ | 1140 | 1470 | mA | 3) |
| $I_{DD5}$ | 360 | 450 | mA | 3) |
| $I_{DD6}$ | 16 | 17.6 | mA | 5) |
| $I_{DD7}$ | 2020 | 2430 | mA | 3)4) |

1) Module $I_{DD}$ values are calculated on the basis of component $I_{DD}$ and can be measured differently according to DQ loading capacity.

2) Test condition for maximum values: $V_{DD}$ = 2.7 V, $T_A$ = 10 °C

3) The module $I_{DDx}$ values are calculated from the $I_{DDx}$ values of the component data sheet as follows: **m** × $I_{DDx}$[component] + **n** × $I_{DD3N}$[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O ($I_{DDQ}$) currents are not included in the calculations (see note 1)

5) The module $I_{DDx}$ values are calculated from the corrponent $I_{DDx}$ data sheet values as: (**m** + **n**) × $I_{DDx}$[component]

**Table 12 $I_{DD}$ Specification for HYS64D64020[G/H]BDL–6–C**

| **Product Type** | **HYS64D64020GBDL–6–-C<br>HYS64D64020HBDL–6–C** | | **Unit** | **Note 1)2)** |
|---|---|---|---|---|
| **Organization** | **512MB** | | | |
| | **×64** | | | |
| | **2 Ranks** | | | |
| | **–6** | | | |
| **Symbol** | **Typ.** | **Max.** | | |
| $I_{DD0}$ | 810 | 960 | mA | 3) |
| $I_{DD1}$ | 930 | 1120 | mA | 3)4) |
| $I_{DD2P}$ | 400 | 480 | mA | 5) |
| $I_{DD2F}$ | 270 | 380 | mA | 5) |
| $I_{DD2Q}$ | 180 | 240 | mA | 5) |
| $I_{DD3P}$ | 510 | 610 | mA | 5) |
| $I_{DD3N}$ | 580 | 720 | mA | 5) |
| $I_{DD4R}$ | 970 | 1160 | mA | 3)4) |
| $I_{DD4W}$ | 1010 | 1240 | mA | 3) |
| $I_{DD5}$ | 300 | 380 | mA | 3) |
| $I_{DD6}$ | 16 | 17.6 | mA | 5) |
| $I_{DD7}$ | 1730 | 2080 | mA | 3)4) |

1) Module $I_{DD}$ values are calculated on the basis of component $I_{DD}$ and can be measured differently according to DQ loading capacity.

2) Test condition for maximum values: $V_{DD}$ = 2.7 V, $T_A$ = 10 °C

3) The module $I_{DDx}$ values are calculated from the $I_{DDx}$ values of the component data sheet as follows: **m** × $I_{DDx}$[component] + **n** × $I_{DD3N}$[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O ($I_{DDQ}$) currents are not included in the calculations (see note 1)

5) The module $I_{DDx}$ values are calculated from the corrponent $I_{DDx}$ data sheet values as: (**m** + **n**) × $I_{DDx}$[component]

## 3.3 AC Characteristics

**Table 13 AC Timing - Absolute Specifications for PC3200 and PC2700**

| Parameter | Symbol | –5 | | –6 | | Unit | Note/ Test Condition [1] |
|---|---|---|---|---|---|---|---|
| | | DDR400B | | DDR333 | | | |
| | | Min. | Max. | Min. | Max. | | |
| DQ output access time from CK/$\overline{CK}$ | $t_{AC}$ | –0.5 | +0.5 | –0.7 | +0.7 | ns | 2)3)4)5) |
| DQS output access time from CK/$\overline{CK}$ | $t_{DQSCK}$ | –0.6 | +0.6 | –0.6 | +0.6 | ns | 2)3)4)5) |
| CK high-level width | $t_{CH}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | 2)3)4)5) |
| CK low-level width | $t_{CL}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | 2)3)4)5) |
| Clock Half Period | $t_{HP}$ | min. ($t_{CL}$, $t_{CH}$) | | min. ($t_{CL}$, $t_{CH}$) | | ns | 2)3)4)5) |
| Clock cycle time | $t_{CK}$ | 5 | 8 | 6 | 12 | ns | CL = 3.0 2)3)4)5) |
| | | 6 | 12 | 6 | 12 | ns | CL = 2.5 2)3)4)5) |
| | | 7.5 | 12 | 7.5 | 12 | ns | CL = 2.0 2)3)4)5) |
| DQ and DM input hold time | $t_{DH}$ | 0.4 | — | 0.45 | — | ns | 2)3)4)5) |
| DQ and DM input setup time | $t_{DS}$ | 0.4 | — | 0.45 | — | ns | 2)3)4)5) |
| Control and Addr. input pulse width (each input) | $t_{IPW}$ | 2.2 | — | 2.2 | — | ns | 2)3)4)5)6) |
| DQ and DM input pulse width (each input) | $t_{DIPW}$ | 1.75 | — | 1.75 | — | ns | 2)3)4)5)6) |
| Data-out high-impedance time from CK/$\overline{CK}$ | $t_{HZ}$ | — | +0.7 | –0.7 | +0.7 | ns | 2)3)4)5)7) |
| Data-out low-impedance time from CK/$\overline{CK}$ | $t_{LZ}$ | –0.7 | +0.7 | –0.7 | +0.7 | ns | 2)3)4)5)7) |
| Write command to 1st DQS latching transition | $t_{DQSS}$ | 0.72 | 1.25 | 0.75 | 1.25 | $t_{CK}$ | 2)3)4)5) |
| DQS-DQ skew (DQS and associated DQ signals) | $t_{DQSQ}$ | — | +0.40 | — | +0.40 | ns | TFBGA 2)3)4)5) |
| Data hold skew factor | $t_{QHS}$ | — | +0.50 | — | +0.50 | ns | TFBGA 2)3)4)5) |
| DQ/DQS output hold time | $t_{QH}$ | $t_{HP}$ –$t_{QHS}$ | | | | ns | 2)3)4)5) |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | 0.35 | — | $t_{CK}$ | 2)3)4)5) |
| DQS falling edge to CK setup time (write cycle) | $t_{DSS}$ | 0.2 | — | 0.2 | — | $t_{CK}$ | 2)3)4)5) |
| DQS falling edge hold time from CK (write cycle) | $t_{DSH}$ | 0.2 | — | 0.2 | — | $t_{CK}$ | 2)3)4)5) |
| Mode register set command cycle time | $t_{MRD}$ | 2 | — | 2 | — | $t_{CK}$ | 2)3)4)5) |
| Write preamble setup time | $t_{WPRES}$ | 0 | — | 0 | — | ns | 2)3)4)5)8) |
| Write postamble | $t_{WPST}$ | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 2)3)4)5)9) |
| Write preamble | $t_{WPRE}$ | 0.25 | — | 0.25 | — | $t_{CK}$ | 2)3)4)5) |
| Address and control input setup time | $t_{IS}$ | 0.6 | — | 0.75 | — | ns | fast slew rate 3)4)5)6)10) |
| | | 0.7 | — | 0.8 | — | ns | slow slew rate 3)4)5)6)10) |
| Address and control input hold time | $t_{IH}$ | 0.6 | — | 0.75 | — | ns | fast slew rate 3)4)5)6)10) |
| | | 0.7 | — | 0.8 | — | ns | slow slew rate 3)4)5)6)10) |

**Table 13 AC Timing - Absolute Specifications for PC3200 and PC2700**

| Parameter | Symbol | –5 | | –6 | | Unit | Note/ Test Condition [1] |
|---|---|---|---|---|---|---|---|
| | | DDR400B | | DDR333 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Read preamble | $t_{RPRE}$ | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | 2)3)4)5) |
| Read postamble | $t_{RPST}$ | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 2)3)4)5) |
| Active to Precharge command | $t_{RAS}$ | 40 | 70E+3 | 42 | 70E+3 | ns | 2)3)4)5) |
| Active to Active/Auto-refresh command period | $t_{RC}$ | 55 | — | 60 | — | ns | 2)3)4)5) |
| Auto-refresh to Active/Auto-refresh command period | $t_{RFC}$ | 70 | — | 72 | — | ns | 2)3)4)5) |
| Active to Read or Write delay | $t_{RCD}$ | 15 | — | 18 | — | ns | 2)3)4)5) |
| Precharge command period | $t_{RP}$ | 15 | — | 18 | — | ns | 2)3)4)5) |
| Active to Autoprecharge delay | $t_{RAP}$ | $t_{RCD}$ or $t_{RASmin}$ | | | | ns | 2)3)4)5) |
| Active bank A to Active bank B command | $t_{RRD}$ | 10 | — | 12 | — | ns | 2)3)4)5) |
| Write recovery time | $t_{WR}$ | 15 | — | 15 | — | ns | 2)3)4)5) |
| Auto precharge write recovery + precharge time | $t_{DAL}$ | $(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$ | | | | $t_{CK}$ | 2)3)4)5)11) |
| Internal write to read command delay | $t_{WTR}$ | 2 | — | 1 | — | $t_{CK}$ | 2)3)4)5) |
| Exit self-refresh to non-read command | $t_{XSNR}$ | 75 | — | 75 | — | ns | 2)3)4)5) |
| Exit self-refresh to read command | $t_{XSRD}$ | 200 | — | 200 | — | $t_{CK}$ | 2)3)4)5) |
| Average Periodic Refresh Interval | $t_{REFI}$ | — | 7.8 | — | 7.8 | µs | 2)3)4)5)12) |

1) 0 °C ≤ $T_A$ ≤ 70 °C; $V_{DDQ}$ = 2.5 V ± 0.2 V, $V_{DD}$ = +2.5 V ± 0.2 V (DDR333); $V_{DDQ}$ = 2.6 V ± 0.1 V, $V_{DD}$ = +2.6 V ± 0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is $V_{REF}$. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until $V_{REF}$ stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is $V_{TT}$.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) $t_{HZ}$ and $t_{LZ}$ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on $t_{DQSS}$.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. $t_{CK}$ is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

# 4 SPD Contents

**Table 14 SPD Codes for HYS64D64020HBDL–5–C and HYS64D64020GBDL–5–C**

| **Product Type** | | **HYS64D64020GBDL–5–C** | **HYS64D64020HBDL–5–C** |
|---|---|---|---|
| **Organization** | | **512 MB** | **512 MB** |
| | | **×64** | **×64** |
| | | **2 Ranks (×8)** | **2 Ranks (×8)** |
| **Label Code** | | **PC3200S–3033–1** | |
| **JEDEC SPD Revision** | | **Rev 1.0** | **Rev 1.0** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 0 | Programmed SPD Bytes in E2PROM | 80 | 80 |
| 1 | Total number of Bytes in E2PROM | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D |
| 4 | Number of Column Addresses | 0A | 0A |
| 5 | Number of DIMM Ranks | 02 | 02 |
| 6 | Data Width (LSB) | 40 | 40 |
| 7 | Data Width (MSB) | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 |
| 9 | $t_{CK}$ @ $CL_{max}$ (Byte 18) [ns] | 50 | 50 |
| 10 | $t_{AC}$ SDRAM @ $CL_{max}$ (Byte 18) [ns] | 50 | 50 |
| 11 | Error Correction Support | 00 | 00 |
| 12 | Refresh Rate | 82 | 82 |
| 13 | Primary SDRAM Width | 08 | 08 |
| 14 | Error Checking SDRAM Width | 00 | 00 |
| 15 | $t_{CCD}$ [cycles] | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 |
| 18 | CAS Latency | 1C | 1C |
| 19 | CS Latency | 01 | 01 |
| 20 | Write Latency | 02 | 02 |
| 21 | DIMM Attributes | 20 | 20 |
| 22 | Component Attributes | C1 | C1 |
| 23 | $t_{CK}$ @ $CL_{max}$ -0.5 (Byte 18) [ns] | 60 | 60 |
| 24 | $t_{AC}$ SDRAM @ $CL_{max}$ -0.5 [ns] | 50 | 50 |
| 25 | $t_{CK}$ @ $CL_{max}$ -1 (Byte 18) [ns] | 75 | 75 |
| 26 | $t_{AC}$ SDRAM @ $CL_{max}$ -1 [ns] | 50 | 50 |
| 27 | $t_{RPmin}$ [ns] | 3C | 3C |
| 28 | $t_{RRDmin}$ [ns] | 28 | 28 |
| 29 | $t_{RCDmin}$ [ns] | 3C | 3C |
| 30 | $t_{RASmin}$ [ns] | 28 | 28 |
| 31 | Module Density per Rank | 40 | 40 |
| 32 | $t_{AS}$, $t_{CS}$ [ns] | 60 | 60 |

**Table 14 SPD Codes for HYS64D64020HBDL–5–C and HYS64D64020GBDL–5–C** (cont'd)

| **Product Type** | | **HYS64D64020GBDL–5–C** | **HYS64D64020HBDL–5–C** |
|---|---|---|---|
| **Organization** | | **512 MB** | **512 MB** |
| | | **×64** | **×64** |
| | | **2 Ranks (×8)** | **2 Ranks (×8)** |
| **Label Code** | | **PC3200S–3033–1** | |
| **JEDEC SPD Revision** | | **Rev 1.0** | **Rev 1.0** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 33 | $t_{AH}$, $t_{CH}$ [ns] | 60 | 60 |
| 34 | $t_{DS}$ [ns] | 40 | 40 |
| 35 | $t_{DH}$ [ns] | 40 | 40 |
| 36 - 40 | not used | 00 | 00 |
| 41 | $t_{RCmin}$ [ns] | 37 | 37 |
| 42 | $t_{RFCmin}$ [ns] | 41 | 41 |
| 43 | $t_{CKmax}$ [ns] | 28 | 28 |
| 44 | $t_{DQSQmax}$ [ns] | 28 | 28 |
| 45 | $t_{QHSmax}$ [ns] | 50 | 50 |
| 46 | not used | 00 | 00 |
| 47 | DIMM PCB Height | 01 | 01 |
| 48 - 61 | not used | 00 | 00 |
| 62 | SPD Revision | 10 | 10 |
| 63 | Checksum of Byte 0-62 | 0F | 0F |
| 64 | JEDEC ID Code of Infineon (1) | C1 | C1 |
| 65 - 71 | JEDEC ID Code of Infineon (2 - 8) | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx |
| 73 | Part Number, Char 1 | 36 | 36 |
| 74 | Part Number, Char 2 | 34 | 34 |
| 75 | Part Number, Char 3 | 44 | 44 |
| 76 | Part Number, Char 4 | 36 | 36 |
| 77 | Part Number, Char 5 | 34 | 34 |
| 78 | Part Number, Char 6 | 30 | 30 |
| 79 | Part Number, Char 7 | 32 | 32 |
| 80 | Part Number, Char 8 | 30 | 30 |
| 81 | Part Number, Char 9 | 47 | 48 |
| 82 | Part Number, Char 10 | 42 | 42 |
| 83 | Part Number, Char 11 | 44 | 44 |
| 84 | Part Number, Char 12 | 4C | 4C |
| 85 | Part Number, Char 13 | 35 | 35 |
| 86 | Part Number, Char 14 | 43 | 43 |
| 87 | Part Number, Char 15 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 |
| 89 | Part Number, Char 17 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 |

**Table 14 SPD Codes for HYS64D64020HBDL–5–C and HYS64D64020GBDL–5–C** (cont'd)

| **Product Type** | | **HYS64D64020GBDL–5–C** | **HYS64D64020HBDL–5–C** |
|---|---|---|---|
| **Organization** | | **512 MB** | **512 MB** |
| | | **×64** | **×64** |
| | | **2 Ranks (×8)** | **2 Ranks (×8)** |
| **Label Code** | | **PC3200S–3033–1** | |
| **JEDEC SPD Revision** | | **Rev 1.0** | **Rev 1.0** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 91 | Module Revision Code | 0x | 0x |
| 92 | Test Program Revision Code | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx |
| 95 - 98 | Module Serial Number (1 - 4) | xx | xx |
| 99 - 127 | not used | 00 | 00 |

**Table 15 SPD Codes for HYS64D64020HBDL–6–C and HYS64D64020GBDL–6–C**

| **Product Type** | | **HYS64D64020GBDL–6–C** | **HYS64D64020HBDL–6–C** |
|---|---|---|---|
| **Organization** | | **512MB** | **512MB** |
| | | **×64** | **×64** |
| | | **2 Ranks (×8)** | **2 Ranks (×8)** |
| **Label Code** | | **PC2700S–2533–0** | |
| **JEDEC SPD Revision** | | **Rev. 0.0** | **Rev. 0.0** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 0 | Programmed SPD Bytes in E2PROM | 80 | 80 |
| 1 | Total number of Bytes in E2PROM | 08 | 08 |
| 2 | Memory Type DDR = 07h | 07 | 07 |
| 3 | # of Row Addresses | 0D | 0D |
| 4 | # Number of Column Addresses | 0A | 0A |
| 5 | # of DIMM Ranks | 02 | 02 |
| 6 | Data Width (LSB) | 40 | 40 |
| 7 | Data Width (MSB) | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 |
| 9 | tCK @ CLmax (Byte 18) [ns] | 60 | 60 |
| 10 | tAC SDRAM @ CLmax (Byte 18) [ns] | 70 | 70 |
| 11 | DIMM Configuration Type (non- / ECC) | 00 | 00 |
| 12 | Refresh Rate | 82 | 82 |
| 13 | Primary SDRAM width | 08 | 08 |
| 14 | Error Checking SDRAM width | 00 | 00 |
| 15 | tCCD [cycles] | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E |
| 17 | Number of Banks on SDRAM | 04 | 04 |
| 18 | CAS Latency | 0C | 0C |
| 19 | CS Latency | 01 | 01 |

**Table 15 SPD Codes for HYS64D64020HBDL–6–C and HYS64D64020GBDL–6–C** (cont'd)

| **Product Type** | | **HYS64D64020GBDL–6–C** | **HYS64D64020HBDL–6–C** |
|---|---|---|---|
| **Organization** | | **512MB** | **512MB** |
| | | **×64** | **×64** |
| | | **2 Ranks (×8)** | **2 Ranks (×8)** |
| **Label Code** | | **PC2700S–2533–0** | |
| **JEDEC SPD Revision** | | **Rev. 0.0** | **Rev. 0.0** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 20 | WE (Write) Latency | 02 | 02 |
| 21 | DIMM Attributes | 20 | 20 |
| 22 | Component Attributes | C1 | C1 |
| 23 | $t_{CK}$ @ CLmax -0.5 (Byte 18) [ns] | 75 | 75 |
| 24 | $t_{AC}$ SDRAM @ CLmax -0.5 [ns] | 70 | 70 |
| 25 | $t_{CK}$ @ CLmax -1 (Byte 18) [ns] | 00 | 00 |
| 26 | $t_{AC}$ SDRAM @ CLmax -1 [ns] | 00 | 00 |
| 27 | $t_{RPmin}$ (ns) | 48 | 48 |
| 28 | $t_{RRDmin}$ [ns] | 30 | 30 |
| 29 | $t_{RCDmin}$ [ns] | 48 | 48 |
| 30 | $t_{RASmin}$ [ns] | 2A | 2A |
| 31 | Module Density per Rank | 40 | 40 |
| 32 | $t_{AS}$, $t_{CS}$ [ns] | 75 | 75 |
| 33 | $t_{AH}$, $t_{CH}$ [ns] | 75 | 75 |
| 34 | $t_{DS}$ [ns] | 45 | 45 |
| 35 | $t_{DH}$ [ns] | 45 | 45 |
| 36 - 40 | not used | 00 | 00 |
| 41 | $t_{RCmin}$ [ns] | 3C | 3C |
| 42 | $t_{RFCmin}$ [ns] | 48 | 48 |
| 43 | $t_{CKmax}$ [ns] | 30 | 30 |
| 44 | $t_{DQSQmax}$ [ns] | 28 | 28 |
| 45 | $t_{QHSmax}$ [ns] | 50 | 50 |
| 46 - 61 | not used | 00 | 00 |
| 62 | SPD Revision | 00 | 00 |
| 63 | Checksum of Byte 0-62 (LSB only) | F8 | F8 |
| 64 | JEDEC ID Code for Infineon | C1 | C1 |
| 65 | JEDEC ID Code for Infineon | 00 | 00 |
| 66 | JEDEC ID Code for Infineon | 00 | 00 |
| 67 | JEDEC ID Code for Infineon | 00 | 00 |
| 68 | JEDEC ID Code for Infineon | 00 | 00 |
| 69 | JEDEC ID Code for Infineon | 00 | 00 |
| 70 | JEDEC ID Code for Infineon | 00 | 00 |
| 71 | JEDEC ID Code for Infineon | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx |
| 73 | Part Number, Char 1 | 36 | 36 |

**Table 15 SPD Codes for HYS64D64020HBDL–6–C and HYS64D64020GBDL–6–C** (cont'd)

| **Product Type** | | **HYS64D64020GBDL–6–C** | **HYS64D64020HBDL–6–C** |
|---|---|---|---|
| **Organization** | | **512MB** | **512MB** |
| | | **×64** | **×64** |
| | | **2 Ranks (×8)** | **2 Ranks (×8)** |
| **Label Code** | | **PC2700S–2533–0** | |
| **JEDEC SPD Revision** | | **Rev. 0.0** | **Rev. 0.0** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 74 | Part Number, Char 2 | 34 | 34 |
| 75 | Part Number, Char 3 | 44 | 44 |
| 76 | Part Number, Char 4 | 36 | 36 |
| 77 | Part Number, Char 5 | 34 | 34 |
| 78 | Part Number, Char 6 | 30 | 30 |
| 79 | Part Number, Char 7 | 32 | 32 |
| 80 | Part Number, Char 8 | 30 | 30 |
| 81 | Part Number, Char 9 | 47 | 48 |
| 82 | Part Number, Char 10 | 42 | 42 |
| 83 | Part Number, Char 11 | 44 | 44 |
| 84 | Part Number, Char 12 | 4C | 4C |
| 85 | Part Number, Char 13 | 36 | 36 |
| 86 | Part Number, Char 14 | 43 | 43 |
| 87 | Part Number, Char 15 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 |
| 89 | Part Number, Char 17 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 |
| 91 | Module Revision Code | xx | xx |
| 92 | Test Program Revision Code | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx |
| 99 - 127 | not used | 00 | 00 |

# 5 Package Outlines

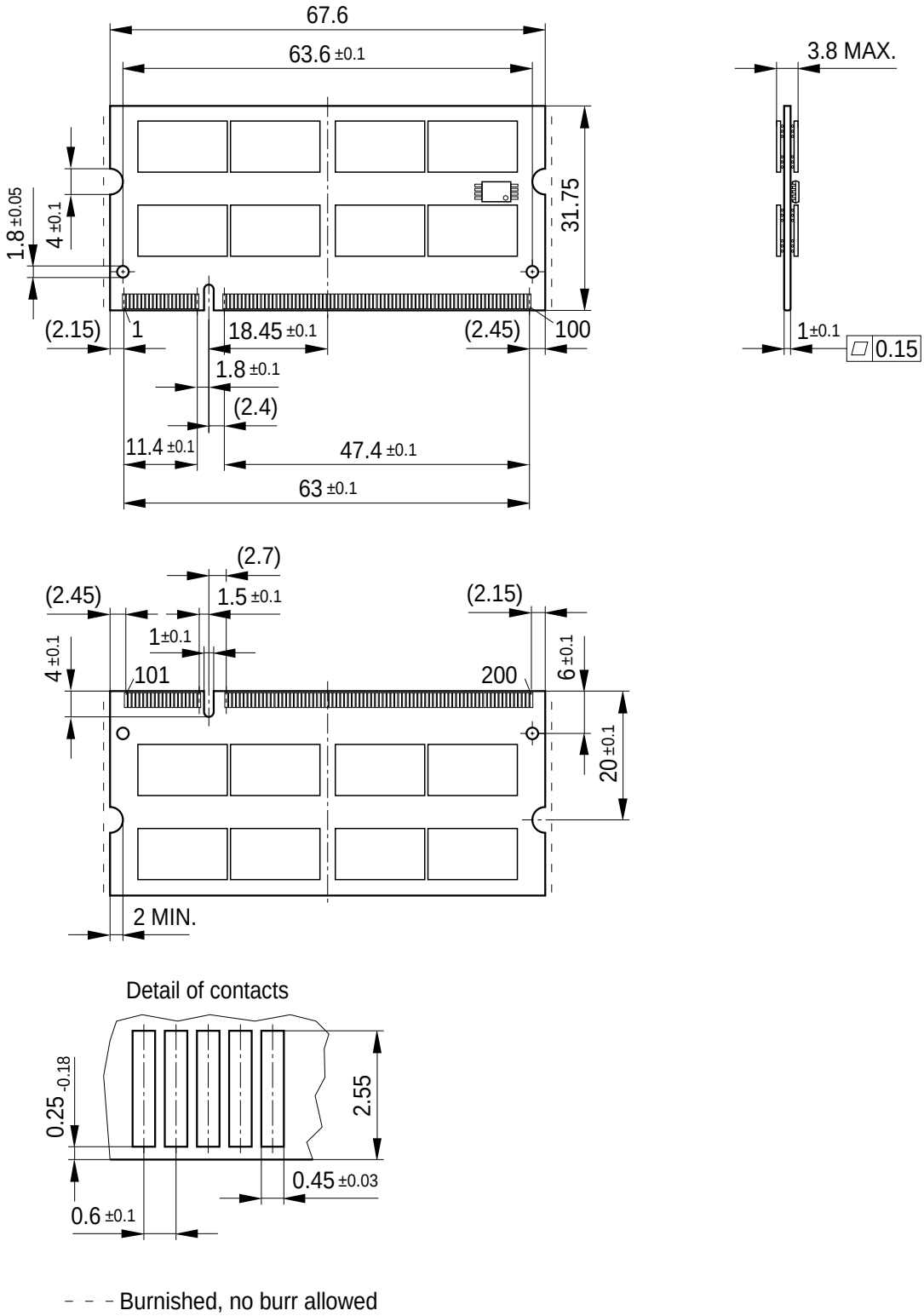


**Figure 3 Package Outline SO-DIMM Raw Card Z (L-DIM-200-9)**

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