HARRIS

HD-15530

CMOS Manchester Encoder-Decoder

Features

- Support of MIL-STD-1553
- 1.25 Megabit/Sec Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Low Operating Power..........................50mW @ 5 Volts
- Full -55°C to +125°C Temperature Range Operation

Description

The Harris HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits.
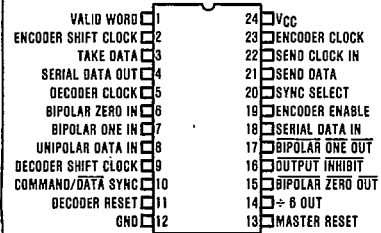
The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

The HD-15530 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable of fiber optic cable throughout the building.
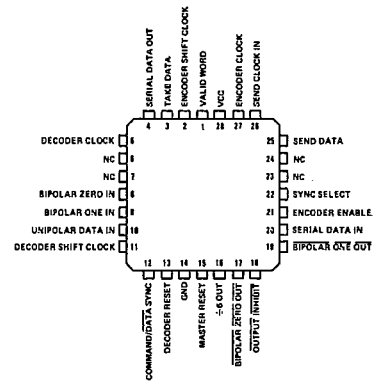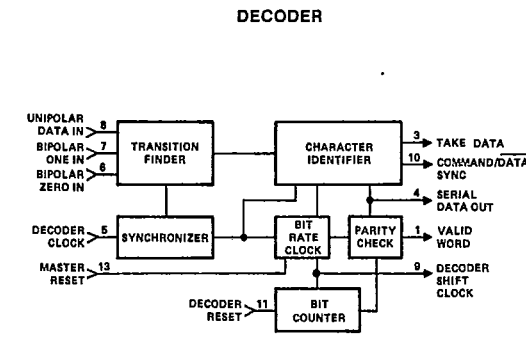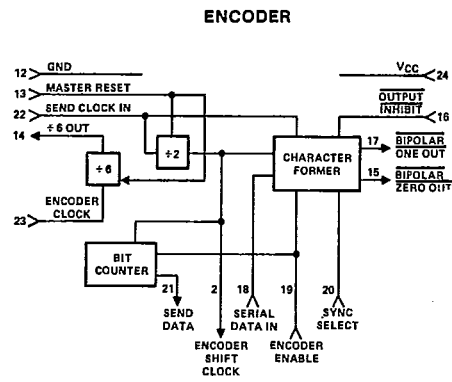
Pinouts

TOP VIEW

Pin	Signal		Pin	Signal
1	VALID WORD		24	Vcc
2	ENCODER SHIFT CLOCK		23	ENCODER CLOCK
3	TAKE DATA		22	SEND CLOCK IN
4	SERIAL DATA OUT		21	SEND DATA
5	DECODER CLOCK		20	SYNC SELECT
6	BIPOLAR ZERO IN		19	ENCODER ENABLE
7	BIPOLAR ONE IN		18	SERIAL DATA IN
8	UNIPOLAR DATA IN		17	BIPOLAR ONE OUT
9	DECODER SHIFT CLOCK		16	OUTPUT INHIBIT
10	COMMAND/DATA SYNC		15	BIPOLAR ZERO OUT
11	DECODER RESET		14	÷ 6 OUT
12	GND		13	MASTER RESET

LCC
BOTTOM VIEW

Block Diagrams

ENCODER

DECODER

Caution: These devices are sensitive to electronic discharge. Proger I.C. handling procedures should be followed.

Specifications HD-15530   T-75-57

HD-15530

Absolute Maximum Ratings

Supply Voltage...+7.0 Volts
Input, Output or I/O Voltage Applied ....GND -0.3V to VCC +0.3V
Storage Temperature Range ....-65°C to +150°C
Maximum Package Power Dissipation..1 Watt
θ_{jc}.....................18°C/W (CERDIP package), 22°C/W (LCC package)

θ_{ja}.........................55°C/W (CERDIP package), 60°C/W (LCC package)
Gate Count.. 456 Gates
Junction Temperature..+150°C
Lead Temperature (Soldering, Ten Seconds)...................................+275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ....+4.5V to +5.5V
Operating Temperature Range
  HD-15530-9 ....-40°C to +85°C
  HD-15530-2/-8 ....-55°C to +125°C

Electrical Specifications

T_A = -40°C to +85°C (HD-15530-9), T_A = 55°C to +125°C (HD-15530-2/-8)

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	V_{IN} = V_{CC} or GND, DIP Pins 5-8, 11, 13, 16, 18, 19, 20, 22, 23
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	II	Input Leakage	-1.0		+1.0	μA	
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2.0	mA	V_{IN} = V_{CC} = 5.5V Outputs Open
	I_{CCOP}	Supply Current Operating *		8.0	10.0	mA	V_{CC} = 5.5V f = 15MHz

(*Guaranteed but not 100% tested)

ENCODER TIMING V_{CC} = 5.0V ± 10%

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
A.C.	(1) F_{EC}	Encoder Clock Frequency	0		15	MHz	C_L = 50pF
	(2) F_{ESC}	Send Clock Frequency	0		2.5	MHz	
	(3) T_{ECR}	Encoder Clock Rise Time			8	ns	
	(4) T_{ECF}	Encoder Clock Fall Time			8	ns	
	(5) F_{ED}	Data Rate	0		1.25	MHz	
	(6) T_{MR}	Master Reset Pulse Width	150			ns	
	(7) T_{E1}	Shift Clock Delay			125	ns	
	(8) T_{E2}	Serial Data Setup	75			ns	
	(9) T_{E3}	Serial Data Hold	75			ns	
	(10) T_{E4}	Enable Setup	90			ns	
	(11) T_{E5}	Enable Pulse Width	100			ns	
	(12) T_{E6}	Sync Setup	55			ns	
	(13) T_{E7}	Sync Pulse Width	150			ns	
	(14) T_{E8}	Send Data Delay	0		50	ns	
	(15) T_{E9}	Bipolar Ouput Delay			130	ns	
	(16) T_{E10}	Enable Hold	10			ns	
	(17) T_{E11}	Sync Hold	95			ns	

DECODER TIMING V_{CC} = 5.0V ± 10%

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
A.C.	(18) F_{DC}	Decoder Clock Frequency	0		15	MHz	C_L = 50pF
	(19) T_{DCR}	Decoder Clock Rise Time			8	ns	
	(20) T_{DCF}	Decoder Clock Fall Time			8	ns	
	(21) F_{DD}	Data Rate	0		1.25	MHz	
	(22) T_{DR}	Decoder Reset Pulse Width	150			ns	
	(23) T_{DRS}	Decoder Reset Setup Time	75			ns	
	(24) T_{DRH}	Decoder Reset Hold Time	10			ns	
	(25) T_{MR}	Master Reset Pulse	150			ns	
	(26) T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	(Note 1)
	(27) T_{D2}	Sync Transition Span		18T_{DC}		ns	(Note 1)
	(28) T_{D3}	One Zero Overlap			T_{DC} -10	ns	(Note 1)
	(29) T_{D4}	Short Data Transition Span		6T_{DC}		ns	(Note 1)
	(30) T_{D5}	Long Data Transition Span		12T_{DC}		ns	(Note 1)
	(31) T_{D6}	Sync Delay (ON)	-20		110	ns	
	(32) T_{D7}	Take Data Delay (ON)	0		110	ns	
	(33) T_{D8}	Serial Data Out Delay			80	ns	
	(34) T_{D9}	Sync Delay (OFF)	0		110	ns	
	(35) T_{D10}	Take Data Delay (OFF)	0		110	ns	
	(36) T_{D11}	Valid Word Delay	0		110	ns	

NOTE 1. TDC = Decoder Clock Period = $\dfrac{1}{FDC}$ (These parameters are guaranteed but not 100% tested)

Capacitance T_A = 25°C; Frequency = 1MHz

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5.0	pF	Al measurements are referenced to device GND
C_O	Output Capacitance	8.0	pF	

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CMOS DATA COMMUNICATIONS

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Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNIPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12		GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	BIPOLAR ZERO OUT	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	OUTPUT INHIBIT	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	BIPOLAR ONE OUT	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24		V_{CC}	Both	VCC is the +5V power supply pin. A 0.1μF decoupling capacitor from V_{CC} (pin 24) to GROUND (pin 12) is recommended.

I = Input   O = Output

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Encoder Timing

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixteen periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK

so it can be sampled on the low-to-high transition ③ - ④. After the sync and Manchester II coded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.
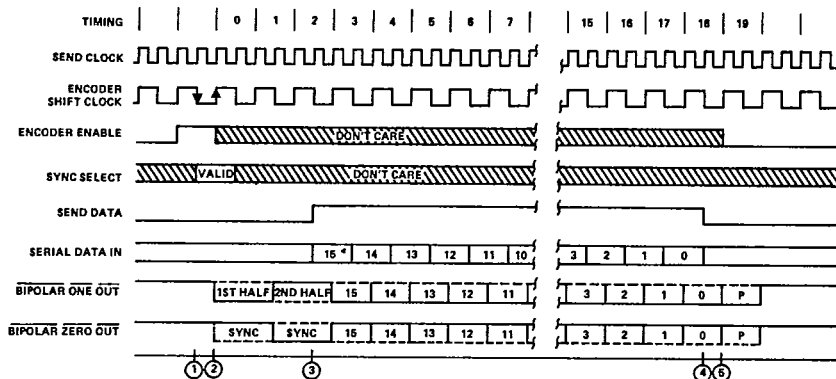
Decoder Timing

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT of an Encoder through an inverter to Unipolar Data Input).
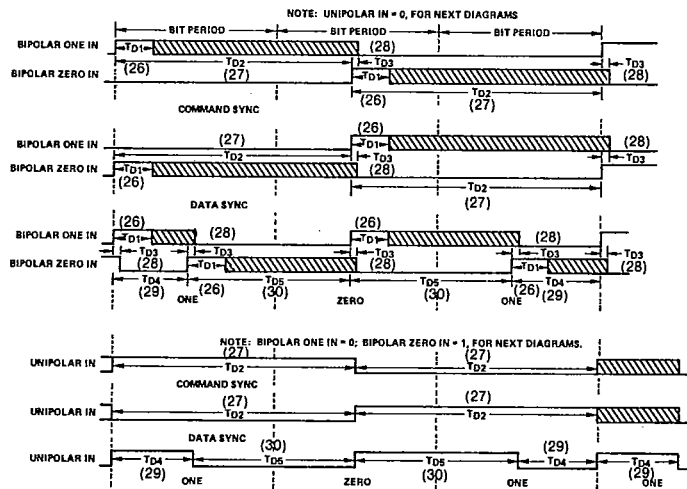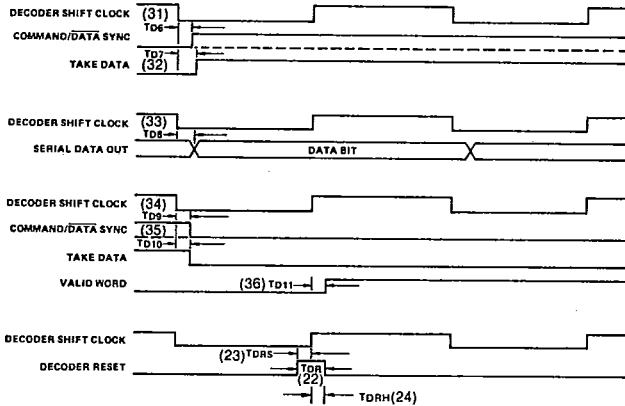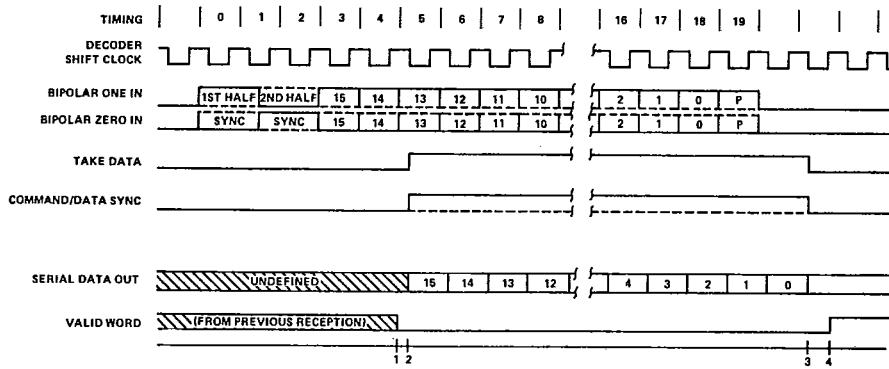
The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/DATA SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixten DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT

is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.
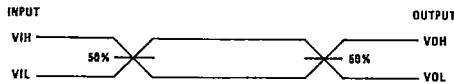
After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.
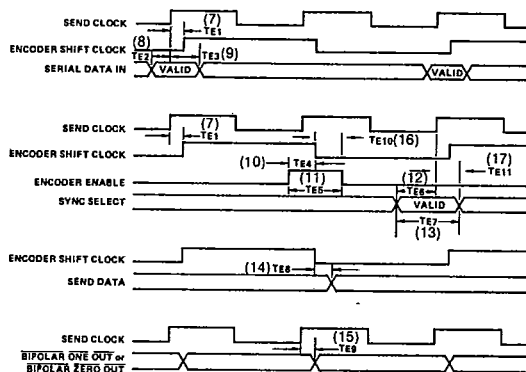
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Decoder Timing

TIMING | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | | 16 | 17 | 18 | 19 | | | |

DECODER SHIFT CLOCK

BIPOLAR ONE IN — 1ST HALF | 2ND HALF | 15 | 14 | 13 | 12 | 11 | 10 | 2 | 1 | 0 | P

BIPOLAR ZERO IN — SYNC | SYNC | 15 | 14 | 13 | 12 | 11 | 10 | 2 | 1 | 0 | P

TAKE DATA

COMMAND/DATA SYNC

SERIAL DATA OUT — UNDEFINED | 15 | 14 | 13 | 12 | 4 | 3 | 2 | 1 | 0

VALID WORD — (FROM PREVIOUS RECEPTION)

1 2   3 4

DECODER SHIFT CLOCK (31)
T_{D6}
COMMAND/DATA SYNC
T_{D7}
TAKE DATA (32)

DECODER SHIFT CLOCK (33)
T_{D8}
SERIAL DATA OUT — DATA BIT

DECODER SHIFT CLOCK (34)
T_{D9}
COMMAND/DATA SYNC (35)
T_{D10}
TAKE DATA
VALID WORD (36) T_{D11}

DECODER SHIFT CLOCK
(23) T_{DRS}
DECODER RESET
T_{DR} (22)
T_{DRH} (24)

NOTE: UNIPOLAR IN = 0, FOR NEXT DIAGRAMS

BIT PERIOD — BIT PERIOD — BIT PERIOD

BIPOLAR ONE IN — T_{D1} (28) T_{D3}
BIPOLAR ZERO IN — (26) T_{D2} (27) T_{D1} (28) T_{D3}
(26) (27)
COMMAND SYNC

BIPOLAR ONE IN — (27) (26) T_{D1} (28) T_{D3}
T_{D2}
BIPOLAR ZERO IN — T_{D1} (28) T_{D3}
(26) T_{D2}
(27)
DATA SYNC

BIPOLAR ONE IN — (26) T_{D1} (28) (26) T_{D1} (28)
BIPOLAR ZERO IN — T_{D3} (28) T_{D3} T_{D1} (28) T_{D3} (26) T_{D3} (28)
T_{D4} (29) ONE (26) T_{D5} (30) ZERO T_{D5} (30) ONE (26) T_{D4} (29)

NOTE: BIPOLAR ONE IN = 0; BIPOLAR ZERO IN = 1, FOR NEXT DIAGRAMS.
UNIPOLAR IN — (27) T_{D2} (27) T_{D2}
COMMAND SYNC
UNIPOLAR IN — (27) T_{D2} (27) T_{D2}
DATA SYNC (30)
UNIPOLAR IN — T_{D4} (29) ONE T_{D5} ZERO T_{D5} (30) ONE T_{D4} (29) ONE

A. C. Testing Input, Output Waveform

INPUT
VIH
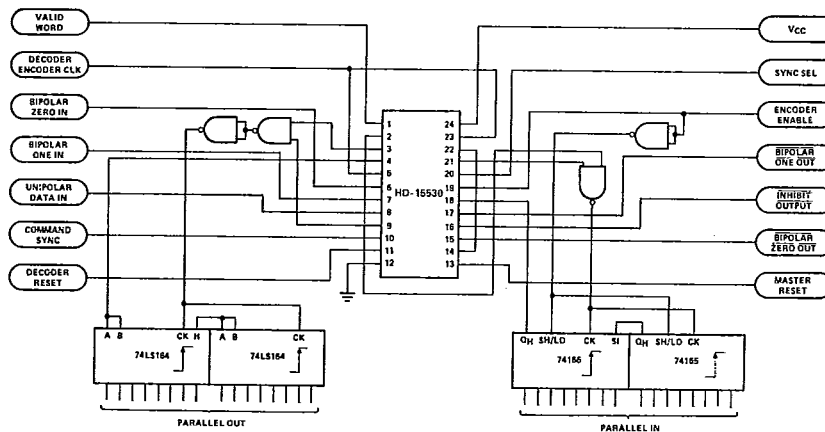VIL
50%

OUTPUT
VOH
VOL
50%

A.C. Testing: All input signals must switch between VIL and VIH. Input rise and fall times are driven at 1 nsec per volt.
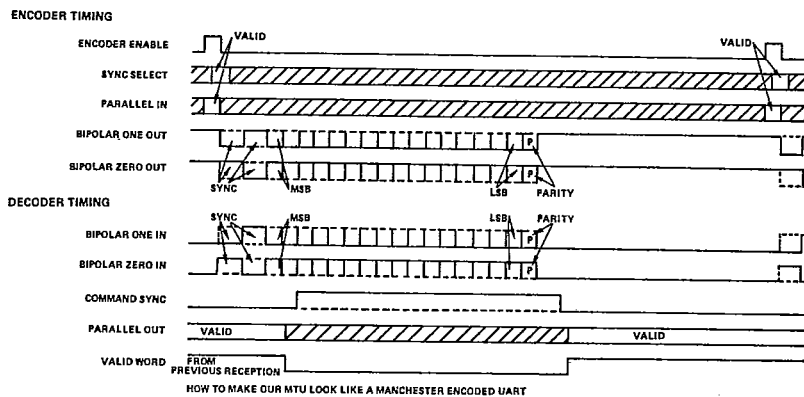
Encoder Timing

Applications

How to Make Our MTU Look Like a Manchester Encoded UART

Typical Timing Diagram for a Manchester Encoded UART

HOW TO MAKE OUR MTU LOOK LIKE A MANCHESTER ENCODED UART

MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15530 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. Each word is preceded by a synchronizing pulse, and fol-

lowed by parity bit, occupying a total of 20μ sec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P   Parity, which is defined to be odd, taken across all 17 bits.

R/T Receive on logical zero, transmit on ONE.

ME   Message Error if logical 1.

TF   Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.
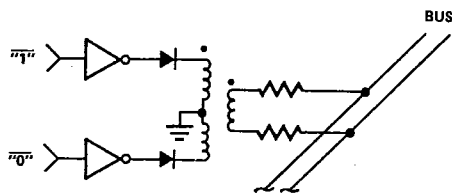

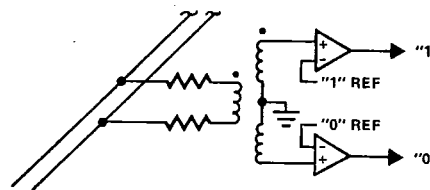FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER
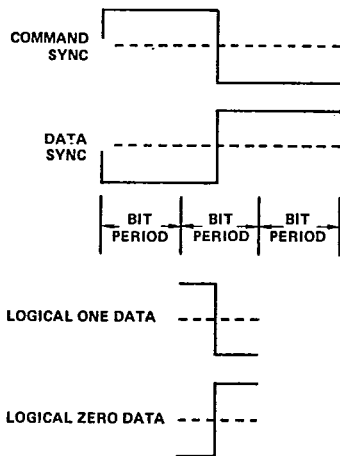

FIGURE 2. SIMPLIFIED MIL-STD-1553 RECEIVER

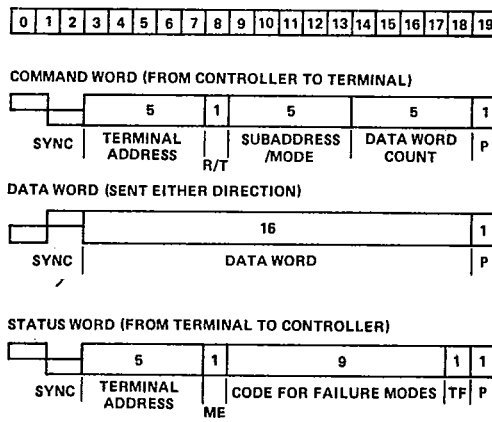FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15530.