Features

- Fast Access Time - 35 ns
- Low Power Dissipation
  - 100 µA Standby Current (AT28HC191L)
  - 80 mA Active Current
- E^2PROM Technology - 100% Reprogrammable
- Direct Replacement for Bipolar PROMs
- Reprogrammable 1000 times
- Chip Clear
- JEDEC Approved Byte-Wide Pinout
  - Industry Standard 600-mil Wide Package
- CMOS and TTL Compatible Inputs and Outputs
- High Reliability High Speed CMOS Technology
- Full Military, Commercial, and Industrial Temperature Ranges

16K (2K x 8) High Speed Electrically Erasable CMOS PROM

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Description

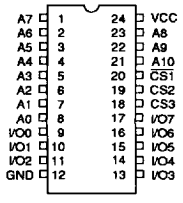
The AT28HC191/191L are a pair of high-speed, low-power 2,048 words by 8 bit CMOS PROMs. The high speed AT28HC191 offers access times to 35 ns while the AT28HC191L provides low standby current consumption of just 100 µA. Both devices are packaged in 24 pin dual inline packages using the JEDEC approved pinout for byte-wide PROMs. The AT28HC191 and AT28HC191L are packaged in the industry standard 600-mil wide package.

These devices are plug-in replacements for 16k bipolar PROMs, while offering distinct advantages in power consumption, performance and programming. Atmel's low power CMOS devices provide a direct power saving upgrade to systems originally using bipolar PROMs. The ultra-low standby power of the 28HC191L brings bipolar speeds to battery powered systems.

The electrically erasable and programmable memory cell allows for 100% testing of each memory location. The E^2PROM cell's low programming current permits devices to be programmed one byte at a time. On chip circuitry automatically erases each byte and rewrites it with the new data, permitting in socket reprogramming. The entire memory array can also be erased simultaneously, if desired, by using the device's "chip- clear" mode.

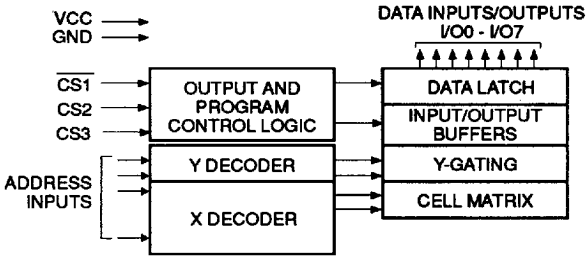
The fast access time of the devices makes them suitable for high-performance applications such as micro-control storage. In such an application the device allows for fast execution speeds, without penalizing storage density or power consumption. With a memory capacity of 2K bytes, these devices provide economical, reliable and high-performance means of storing program instructions. System reliability is enhanced by the low power and inherent reliability of Atmel's 1.5 micron floating poly technology.

Pin Configurations



Pin Name	Function
A0-A10	Addresses
$\overline{CS1}$	Chip Select (Power Down Option)
CS2	Chip Select
CS3	Chip Select
I/O0-I/O7	Data

Block Diagram



Operating Modes

Mode	CS3	CS2	$\overline{CS1}$	I/O
Read	V_{IH}	V_{IH}	V_{IL}	D_{OUT}
Standby	X(1)	X	V_{IH}	High Z
Output Disable	V_{IL}	X	X	High Z
Output Disable	X	V_{IL}	X	High Z
Write(2)	V_{IL}	V_{IL}	V_H (3)	D_{IN}
Verify	V_{IH}	V_{IH}	V_H	D_{OUT}
Chip Clear	V_{IL}	V_H	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0 \pm 0.5$ V.

Device Operation

READ: When $\overline{CS1}$ is low and CS2 and CS3 are high, the data stored at the memory location determined by the address inputs is asserted on the outputs of the device. The outputs are put in a high impedance state whenever CS2 or CS3 is low or whenever $\overline{CS1}$ is high. The availability of three control lines gives the designer flexibility in preventing bus contention.

STANDBY: The AT28HC191L consumes less than 550 µW when deselected by raising $\overline{CS1}$ to V_{CC}-0.3 V. This part retains the fast chip select times from CS2 and CS3 that are common to the AT28HC191.

PROGRAMMING: A 12 volt input is required on the $\overline{CS1}$ pin in order to program the devices. This input voltage is not needed to supply the programming current required by the memory cells as all high voltages used inside the chip are self-generated. After $\overline{CS1}$ is raised to 12 volts with CS2 low and CS3 high, CS3 is pulsed low to begin the internally timed write cycle. The address location presented to the device on the falling edge of the CS3 signal is written with the data that is presented to the device on the rising edge of CS3. An entire eight bit byte is programmed during each programming cycle. Any byte can be programmed to any data pattern regardless of the current data in that byte. An internal timer uses 1 ms to program a byte. No additional time is required nor are any additional programming pulses.

VERIFY: A verify of programmed data may be performed with $\overline{CS1}$ at 12 volts by taking CS2 and CS3 to V_{IH}. The verify works exactly as a device read except that $\overline{CS1}$ is at 12 volts rather than V_{IL}.

MEMORY CELL: The AT28HC191 family of parts uses fully reprogrammable E^2PROM cells to store data. Unlike the one time programmable fuse link cells commonly found in bipolar PROMs, E^2PROM cells allow each bit to be fully tested before shipment by Atmel. The electrical reprogrammability of E^2PROM cells allows for multiple patterns to be written into each device during testing to ensure proper programming, functioning, and timing. All cells may be reprogrammed up to 1000 times by the user.

CHIP CLEAR: The entire contents of these memory devices may be set to the high state by the chip clear function. By setting $\overline{CS1}$ low and CS2 to 12 volts, the chip is cleared when a 10 msec low pulse is applied to CS3.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{CS1}$, CS2 and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28HC191-35	AT28HC191-45 AT28HC191L-45	AT28HC191-55 AT28HC191L-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	—	-40°C - 85°C	-40°C - 85°C
	Mil.	—	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{CC1}	V_{CC} Standby Current	$\overline{CS1}$ = V_{IH} ADDR = 0/V_{CC}	AT28HC191L		3	mA
			AT28HC191		60	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

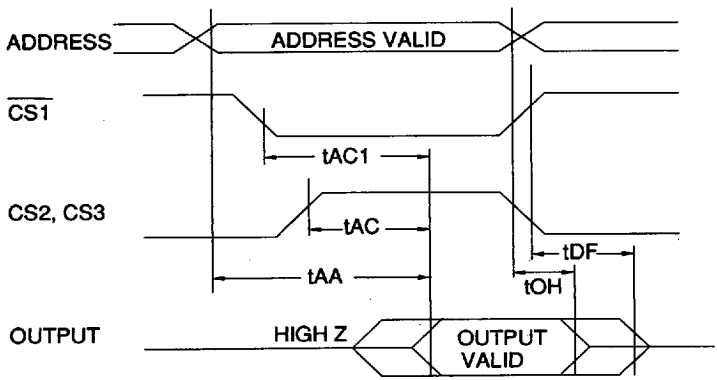
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is only characterized and is not 100% tested.

A.C. Characteristics for Read Operation [1]

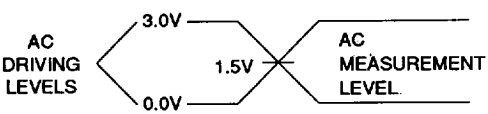
Symbol	Parameter	AT28HC191 -35 Min	AT28HC191 -35 Max	AT28HC191 -45 Min	AT28HC191 -45 Max	AT28HC191 -55 Min	AT28HC191 -55 Max	AT28HC191L -45 Min	AT28HC191L -45 Max	AT28HC191L -55 Min	AT28HC191L -55 Max	Units
t_{AA} [2]	Address to Output Delay		35		45		55		45		55	ns
t_{AC} [2]	CS2, CS3 to Output Delay		25		30		40		30		40	ns
t_{AC1} [2]	$\overline{CS1}$ to Output Delay		30		35		40		45		55	ns
t_{DF} [3,4]	$\overline{CS1}$, CS2, CS3 to Output Float	0	25	0	30	0	40	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{CS1}$,CS2, CS3, or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms



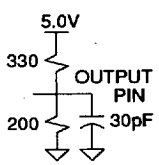
Notes:
1. CL = 30 pF
2. $\overline{CS}$, CS2 or CS3 may be delayed up to t_{AA}-t_{AC} after the address transition without impact on t_{AA}.
3. t_{DF} is specified from $\overline{CS1}$, CS2, or CS3, whichever occurs first.
4. This parameter is only characterized and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns

Output Test Load



A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	50		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WC}	Write Cycle Time	1			ms
t_{VPS}	Programming Set-up Time	2			µs
t_{AA}	Address to Output Delay			100	ns
t_{AC}	CSn to Output Delay			100	ns
t_{DF}	CSn to Output Float			60	ns

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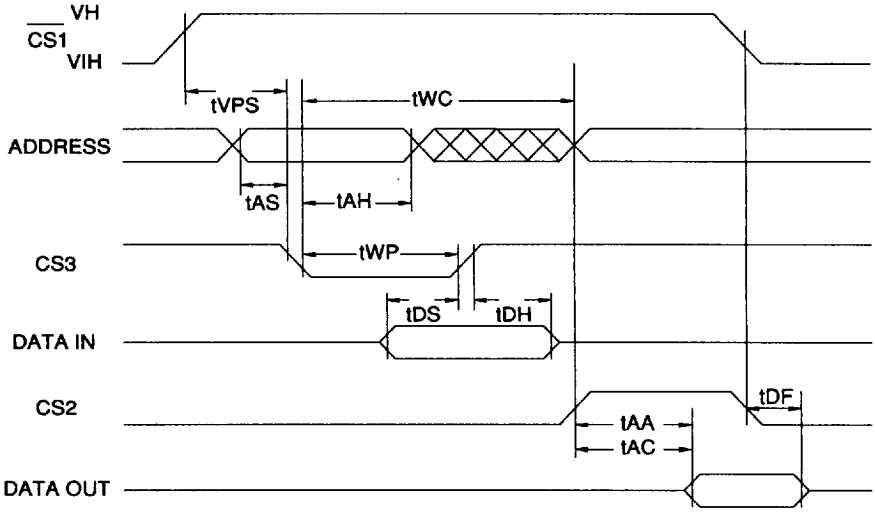
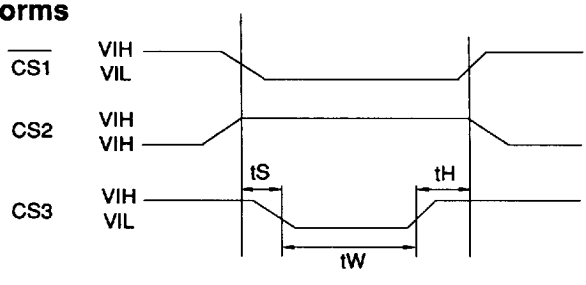
A.C. Write Waveforms



Chip Erase Waveforms



$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12 \pm 0.5$ V

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	80	60	AT28HC191-35DC AT28HC191-35PC	24D6 24P6	Commercial (0° to 70°C)
45	80	60	AT28HC191-45DC AT28HC191-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-45DI AT28HC191-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-45DM	24D6	Military (-55° to 125°C)
			AT28HC191-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	60	AT28HC191-55DC AT28HC191-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-55DI AT28HC191-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-55DM	24D6	Military (-55° to 125°C)
			AT28HC191-55DM/883	24D6	Military Class B, Fully Compliant (-55° to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC191L-45DC AT28HC191L-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-45DI AT28HC191L-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-45DM	24D6	Military (-55° to 125°C)
			AT28HC191L-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC191L-55DC AT28HC191L-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-55DI AT28HC191L-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-55DM	24D6	Military (-55° to 125°C)
			AT28HC191L-55DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)

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Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)