T-46-19-09

EPM7032 EPLD

High-Performance 32-Macrocell Device

May 1992, ver. 1

Data Sheet Supplement

Preliminary Information

This data sheet supplement should be used together with the *EPM7032 EPLD High-Performance, 32-Macrocell Device Data Sheet*. This supplement updates information on the AC operating conditions for the 10-ns EPM7032-1 EPLD. Updated values are provided both for internal and external timing parameters. All DC parameters listed in the *EPM7032 EPLD High-Performance, 32-Macrocell Device Data Sheet* also apply to the EPM7032-1.

AC Operating Conditions *See Note (3)*

External Timing Parameters			EPM7032-1		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10	ns
t_{PD2}	I/O input to non-registered output			10	ns
t_{SU}	Global clock setup time		8		ns
t_{H}	Global clock hold time		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5	ns
t_{CH}	Global clock high time		4		ns
t_{CL}	Global clock low time		4		ns
t_{ASU}	Array clock setup time		3		ns
t_{AH}	Array clock hold time		3		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10	ns
t_{ACH}	Array clock high time		4		ns
t_{ACL}	Array clock low time		4		ns
t_{CNT}	Minimum global clock period			10	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	100		MHz
t_{ACNT}	Minimum array clock period			10	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	100		MHz
f_{MAX}	Maximum clock frequency	*See Note (6)*	125		MHz

Notes to tables:

(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.

(5) Measured with a device programmed as a 16-bit counter in each LAB.

(6) The f_{MAX} values represent the highest frequency for pipelined data.

(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

AC Operating Conditions (continued) *See Note (3)*

Internal Timing Parameters			EPM7032-1		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			1	ns
t_{IO}	I/O input pad and buffer delay			1	ns
t_{SEXP}	Shared expander delay			5	ns
t_{PEXP}	Parallel expander delay			2	ns
t_{LAD}	Logic array delay			5	ns
t_{LAC}	Logic control array delay			5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2	ns
t_{ZX}	Output buffer enable delay			5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5	ns
t_{SU}	Register setup time		3		ns
t_{H}	Register hold time		3		ns
t_{RD}	Register delay			1	ns
t_{COMB}	Combinatorial delay			1	ns
t_{IC}	Array clock delay			5	ns
t_{EN}	Register enable time			5	ns
t_{GLOB}	Global control delay			1	ns
t_{PRE}	Register preset time			3	ns
t_{CLR}	Register clear time			3	ns
t_{PIA}	Prog. Interconnect Array delay			1	ns
t_{LPA}	Low power adder	*See Note (7)*		5	ns

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7032JC44-1, EPM7032LC44-1
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

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EPM7032 EPLD

High-Performance 32-Macrocell Device

December 1991, ver. 1

T-90-01

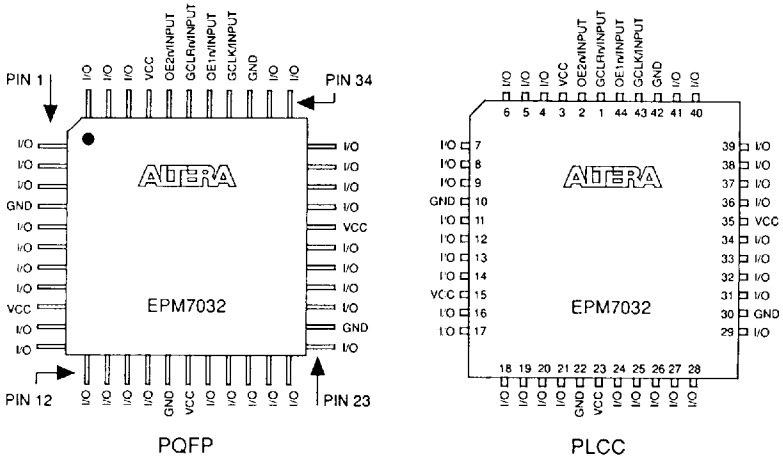
Data Sheet

Features...

- High-performance erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - Combinatorial speeds with t_{PD} = 12 ns
  - Clock frequencies up to 125 MHz
- Advanced 0.8-micron CMOS electrically erasable (EEPROM) technology
- Programmable I/O architecture allowing up to 36 inputs and 32 outputs
- 32 advanced macrocells to efficiently implement registered or complex combinatorial logic
- Configurable expander product-term distribution allowing 32 product terms in a single macrocell
- Programmable registers providing D, T, JK, or SR flipflops with individual asynchronous Clear, Preset, and Clock Enable controls
- Independent clocking of all registers from array or global (fast) Clock signals
- Programmable power-saver mode for 50% or more power reduction in each macrocell
- Programmable Security Bit for total protection of proprietary designs
- Available in 44-pin reprogrammable plastic J-lead (PLCC) and plastic EIAJ-standard quad flat pack (PQFP) packages (see Figure 1)

Preliminary Information

Figure 1. EPM7032 Package Pin-Out Diagrams *Package outlines not drawn to scale.*



...and More Features

- ❑ 100% generically testable to provide 100% programming yield
- ❑ Software design support featuring Altera's MAX+PLUS II development system available for PC and HP/Apollo and Sun workstation platforms
- ❑ Programming support from Altera's Master Programming Unit (MPU) and third-party programmers

General Description

The Altera EPM7032 EPLD is a high-performance, high-density CMOS Erasable Programmable Logic Device (EPLD) based on Altera's second-generation MAX 7000 architecture. Fabricated on a 0.8-micron Electrically Erasable (EEPROM) technology, the EPM7032 EPLD provides in-system speeds of 83.3 MHz and propagation delays of 12 ns. The EPM7032 architecture supports 100% TTL emulation and allows the integration of SSI, MSI, and custom logic functions. It can replace multiple 20- and 24-pin PLDs. The EPM7032 EPLD is available in 44-pin reprogrammable plastic J-lead chip carrier (PLCC) or EIAJ-standard quad flat pack (QFP) packages and can accommodate designs with up to 36 inputs and 32 outputs.

The EPM7032 EPLD uses CMOS EEPROM cells to configure logic functions within the device. EPM7032 architecture is user-configurable to accommodate a variety of independent logic functions, and the device can be reprogrammed for quick and efficient iterations during design development and debug cycles. Each device is guaranteed for 100 erase/rewrite cycles.

The EPM7032 EPLD consists of 32 macrocells organized into two Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable Clock, Clock Enable, Clear, and Preset functions. For building complex logic functions, each macrocell can be supplemented with shared and high-speed parallel logic expanders to allow up to 32 product terms per macrocell.

The EPM7032 EPLD provides programmable speed/power optimization. Speed-critical portions of the design can run at high speed/full power while the remainder runs at reduced speed/low power. This feature enables the user to configure individual macrocells to operate at 50% or less power while adding only a nominal timing delay.

Altera's MAX+PLUS II development system provides a completely integrated design entry, compilation, verification, and programming environment. MAX+PLUS II is available on 386- or 486-based IBM PC and compatible computers; it will be available on Sun and HP/Apollo workstations in early 1992. The Windows-based graphical interface supports hierarchical graphic, text, and waveform design entry with over 300 TTL macrofunctions that are optimized for the EPM7032 architecture. MAX+PLUS II includes the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, and truth table

entry methods. In addition, MAX+PLUS II provides highly automated compilation, automatic multi-EPLD partitioning, timing simulation and analysis, automatic error location, device programming and verification, and a comprehensive on-line help system. MAX+PLUS II also imports and exports industry-standard EDIF 2 0 0 netlist files, providing a convenient interface to popular third-party CAE tools.

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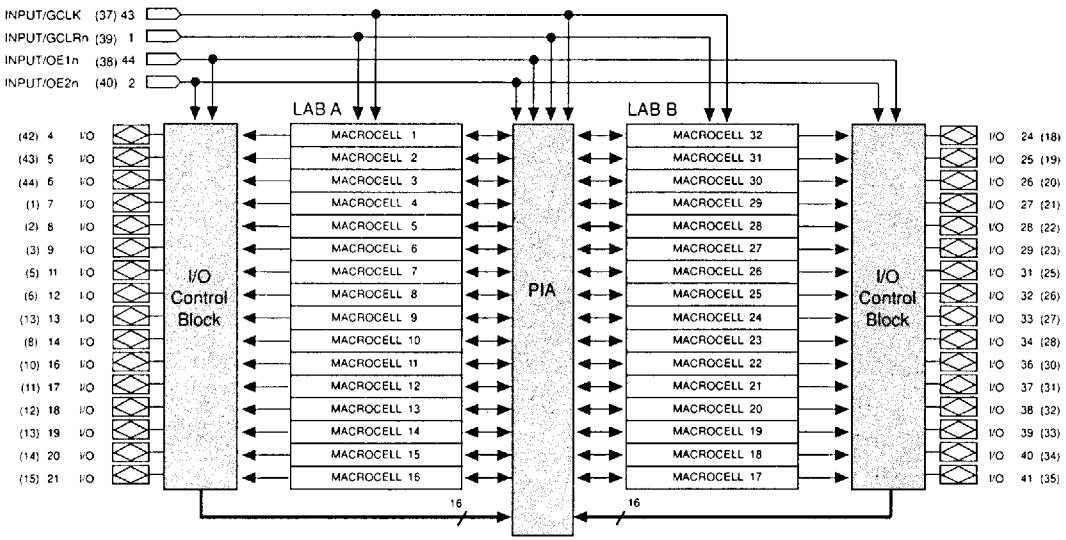
Functional Description

The EPM7032, shown in Figure 2, is a 32-macrocell EPLD that has been optimized for integrating multiple TTL, PAL, and GAL devices. The EPM7032 EPLD has 32 I/O pins that can be individually configured for input, output, or bidirectional operation. It also has 4 dedicated input pins that can be programmed as general-purpose inputs or high-speed global control signals (Clock, Clear, and 2 Output Enables) for each macrocell and I/O pin.

Figure 2. EPM7032 Block Diagram

Pin numbers in parentheses are for the PQFP package.



The EPM7032 EPLD contains the following architectural building blocks:

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- Logic Array Blocks
- Macrocells
- Logic expanders (shared and parallel)
- Programmable Interconnect Array
- I/O control blocks

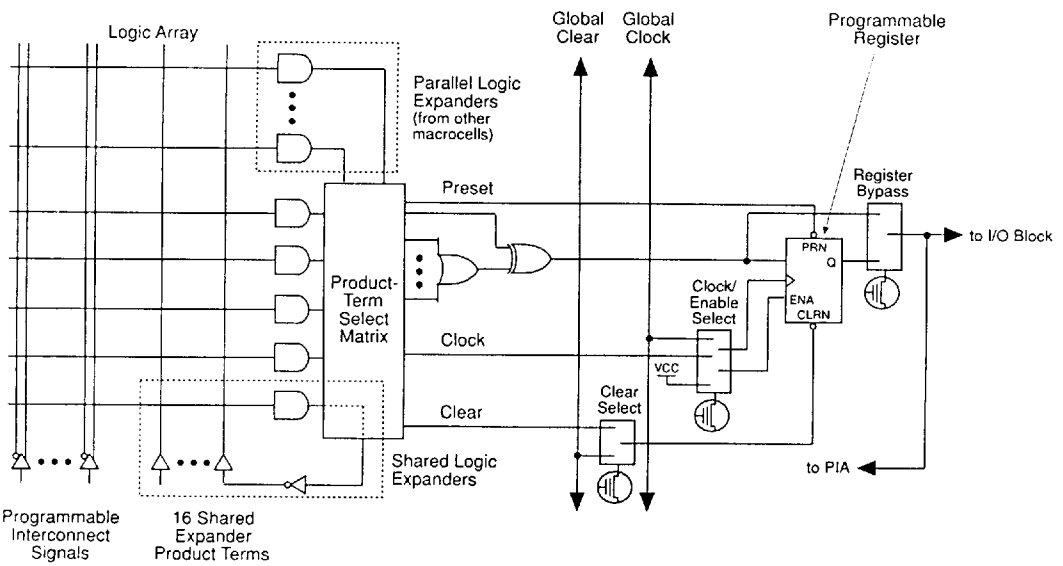
Logic Array Blocks

MAX 7000 architecture is based on the concept of linking small, high-performance, flexible logic array modules called Logic Array Blocks (LABs). Multiple LABs are linked together via a global bus called the Programmable Interconnect Array (PIA), which is fed by all EPM7032 dedicated inputs, I/O pins, and macrocells. The PIA routes only the signals required to implement logic in each LAB. The EPM7032 EPLD has 2 LABs, each of which contains 16 macrocells.

Macrocells

The EPM7032 macrocell, shown in Figure 3, provides both sequential and combinatorial logic capabilities. It can be individually configured for registered or combinatorial operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Figure 3. EPM7032 Macrocell



Combinatorial logic is implemented in the logic array, which contains five product terms. These are allocated by the product-term select matrix for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs for the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. One product term per macrocell can be used as a shared logic expander if it is fed back into the logic array. Based on the logic requirements of the design, the product-term select matrix automatically optimizes product-term allocation.

In registered functions, each macrocell flipflop can be individually programmed for D, T, JK, or SR operation with programmable Clock control. If necessary, the flipflop can be bypassed for combinatorial operation. During design entry, the user can specify the desired flipflop type or allow MAX+PLUS II to select the most efficient flipflop operation for each registered logic function to minimize the resources needed by the design.

The programmable register can be configured in three clocking modes:

- It can be clocked from the dedicated global Clock pin (GCLK). In this mode, the flipflop is positive-edge-triggered, and the fastest Clock-to-output performance is achieved.
- It can be clocked with the array Clock using a product term. In this mode, the flipflop can be configured for positive- or negative-edge-triggered operation. Array Clocks allow any signal source or gated logic function to clock the flipflop.
- It can be clocked from the global Clock pin and enabled by a product term. The register is enabled when the flipflop ENA input is high. Each flipflop can be activated individually while taking advantage of the fast Clock-to-output delay of the global Clock pin.

Each register also supports the asynchronous Preset and Clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the register is designed for active-low Preset and Clear, active-high control is also provided when the signal is inverted within the logic array. In addition, each register Clear function can be individually connected to the EPM7032 dedicated global Clear pin (GCLRn). In this mode, the Clear function is active low.

Logic Expanders

Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Instead of using another macrocell to supply the needed logic resources, the MAX 7000 architecture has both

shared and parallel logic expanders that provide additional product terms directly to any macrocell.

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Shared Logic Expanders

Each LAB has up to 16 shared expanders, which can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverting outputs that feed back into the logic array. Each shared logic expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shared logic expanders can also be cross-coupled to build additional buried flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shared logic expanders are used.

Parallel Logic Expanders

Parallel logic expanders are unused product terms from macrocells in the LAB that can be allocated to any macrocell by the product-term select matrix to implement fast, complex logic functions. With parallel logic expanders, up to 20 product terms can directly feed the macrocell OR logic (5 product terms from the macrocell and 15 parallel logic expanders provided by other macrocells in the LAB).

The MAX+PLUS II Compiler can automatically route parallel logic expanders to the necessary macrocells in sets of 1 to 5. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler will allocate 2 sets of parallel logic expanders (the first set equals 5 product terms, the second set equals 4 product terms, increasing the total delay by $2 \times t_{PEXP}$), in addition to the 5 product terms already in the macrocell.

The EPM7032 EPLD can use shared and parallel logic expanders to allocate additional product terms to any macrocell, ensuring that logic is synthesized with the fewest logic resources to obtain the fastest possible speed.

Programmable Interconnect Array

Logic is routed between the EPM7032 LABs on the Programmable Interconnect Array (PIA). This global bus is a programmable path that allows any signal source to reach any destination on the device. Although EPM7032 dedicated inputs, I/O pin feedbacks, and macrocell feedbacks all feed the PIA, the PIA routes only the required signals needed by each macrocell back into each LAB.

While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA eliminates skew between signals, making timing performance easy to predict.

I/O Control Blocks

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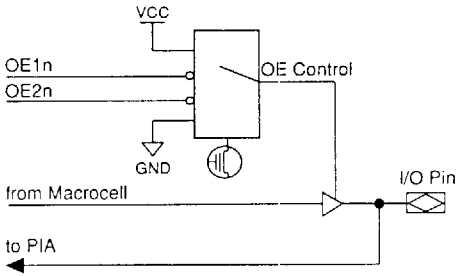
The I/O control block, shown in Figure 4, allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is connected to one of two global active-low Output Enable pins (OE1n and OE2n) or directly to GND or VCC. When the I/O tri-state buffer is connected to GND, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the I/O tri-state buffer is connected to VCC, the output is enabled.

Figure 4. I/O Control Block



The EPM7032 EPLD provides dual feedback. The macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Programmable Speed/Power Control

The EPM7032 EPLD offers a power-saver mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since only a small fraction of all gates operate at maximum frequency in most logic applications.

Each macrocell in the EPM7032 EPLD can be individually programmed by the designer for either high-speed (Turbo) or low-power operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, and t_{SEXP} parameters.

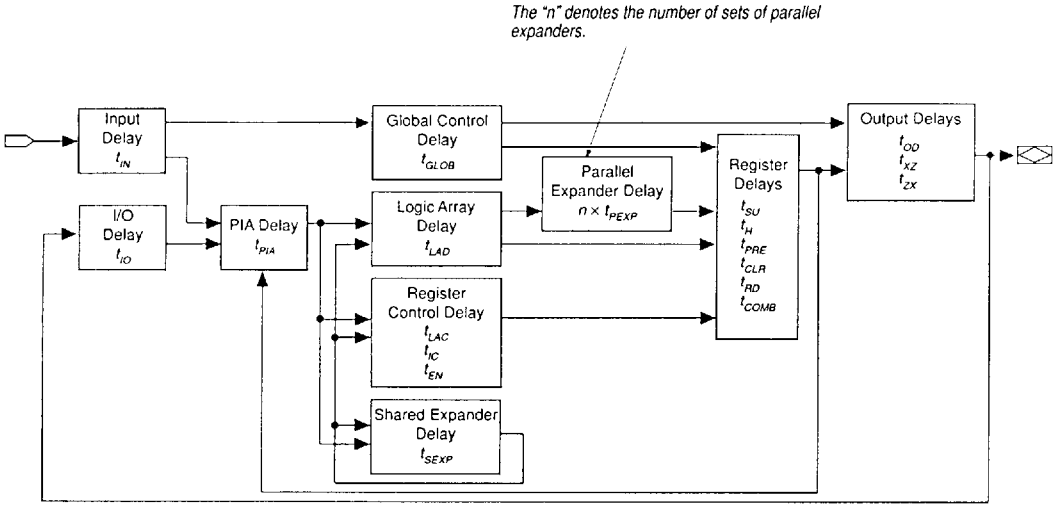
Design Security

The EPM7032 EPLD contains a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EEPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when the EPLD is erased.

Timing Model

Timing within the EPM7032 EPLD can be analyzed either with the MAX+PLUS II software or with the timing model shown in Figure 5. The EPM7032 EPLD has fixed internal delays that allow the user to determine the worst-case timing for any design. For complete timing information, MAX+PLUS II software provides complete timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 5. Timing Model



Timing information can be calculated with the timing model and the timing parameters for a particular EPLD. External timing parameters are derived from the sum of internal parameters and represent pin-to-pin timing delays. Figure 6 shows the internal timing relationship for internal and external delay parameters.

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Figure 6. Switching Waveforms (Part 1 of 2)

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

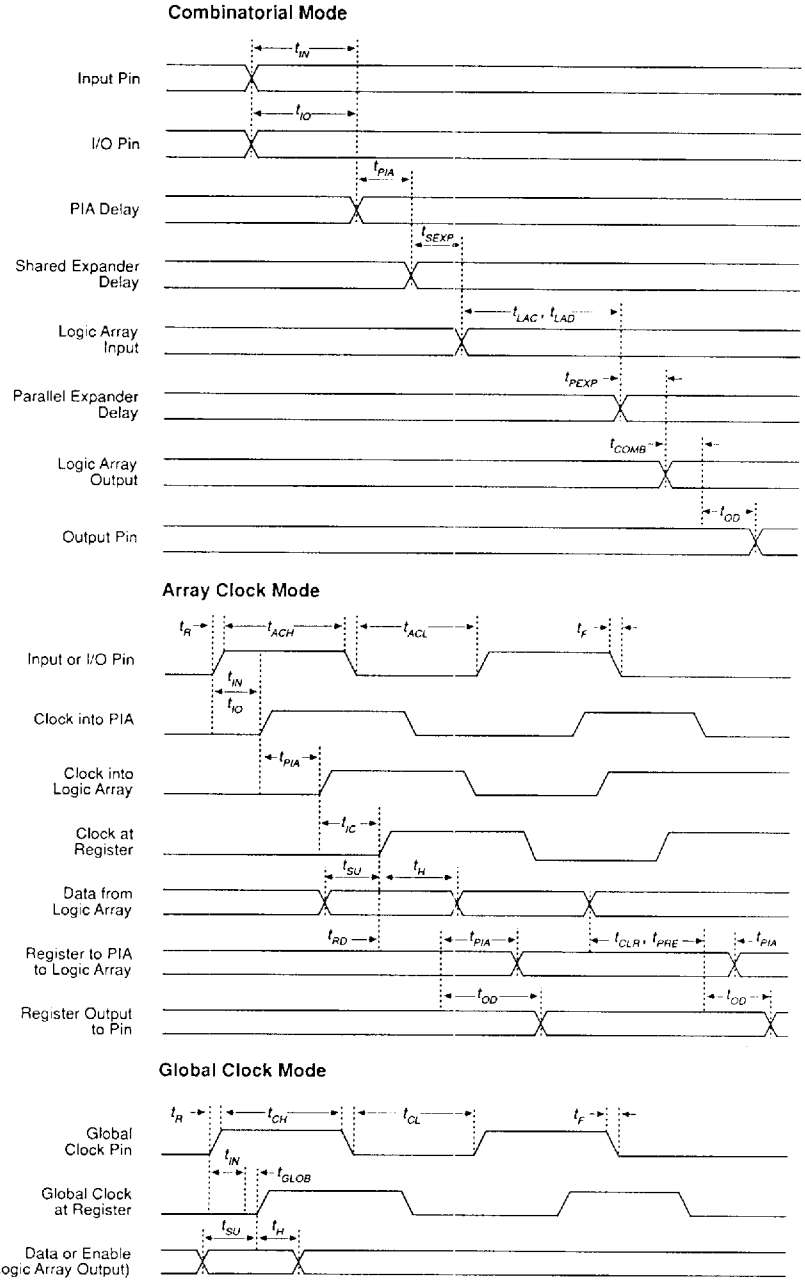

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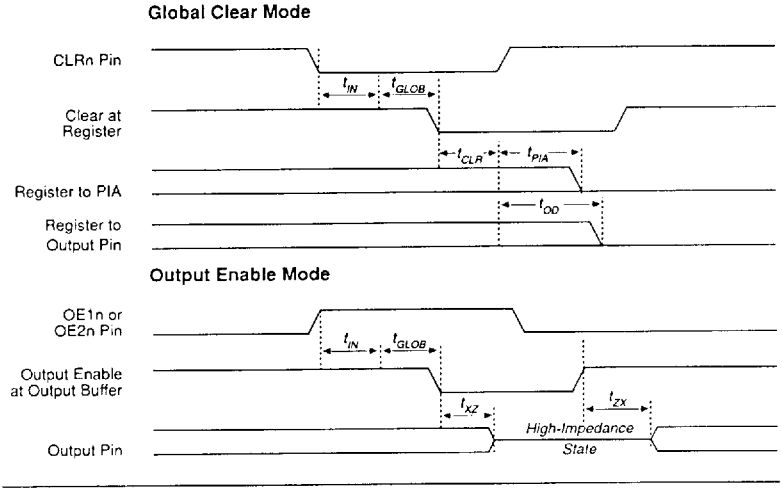
Figure 6. Switching Waveforms (Part 2 of 2)



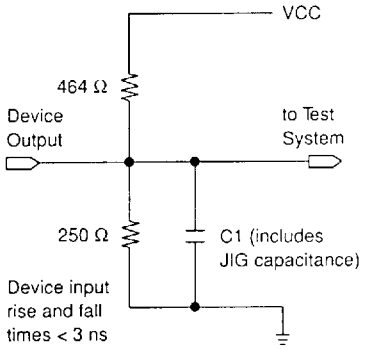
Generic Testing

The EPM7032 EPLD is functionally tested and guaranteed. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are made under the conditions shown in Figure 7.

Test patterns can be used and then erased during all stages of the production flow. This facility to use application-independent, general-purpose tests, called generic testing, is unique among user-configurable logic devices.

Figure 7. EPM7032 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



MAX+PLUS II Development System

The EPM7032 EPLD is supported by Altera's MAX+PLUS II development system and software. MAX+PLUS II supports Altera's Classic, MAX 5000, MAX 7000, and STG EPLDs.

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Designs can be entered as logic schematics with the Graphic Editor; as state machines, truth tables, and Boolean equations with the Altera Hardware Description Language (AHDL); or as waveforms with the Waveform Editor. Logic synthesis and minimization automatically optimize the logic of a design. MAX+PLUS II also provides automatic design partitioning into multiple EPLDs from the same family. Design verification and timing analysis are performed with the built-in Simulator and Timing Analyzer. Errors in a design are automatically located and highlighted in the original design files.

MAX+PLUS II runs on IBM PC-AT, PS/2, and compatible computers, as well as Sun and HP/Apollo workstations. The software gives designers the tools to quickly and efficiently create complex logic designs. MAX+PLUS II also provides an EDIF netlist interface for additional design entry and simulation support with popular CAE tools from Mentor Graphics, Valid Logic, Viewlogic, Synopsys, and others. Further details about the MAX+PLUS II development system are available in the *PLDS-HPS, PLS-HPS, PLS-OS & PLS-ES: MAX+PLUS II Programmable Logic Development System & Software Data Sheet*, the *PLS-WS/SN: MAX+PLUS II Programmable Logic Development Software for Sun Workstations Data Sheet*, and the *PLS-WS/HP: MAX+PLUS II Programmable Logic Development Software for HP/Apollo Workstations Data Sheet* in the 1992 *Data Book*.

Device Programming

The EPM7032 EPLD can be programmed on an IBM PS/2, PC-AT, or compatible computer with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the PLMJ7032 or PLMQ7032 device adapter. The MPU supports device open- and short-circuit testing and performs continuity checking to ensure adequate electrical contact between the programming adapter and the EPLD.

MAX+PLUS II software uses test vectors developed with the Waveform Editor to functionally test the programmed device. For added design verification, designers can compare the functional behavior of the EPM7032 EPLD with the results of timing simulation.

In addition, Data I/O and a variety of third-party manufacturers provide programming support for Altera EPLDs.

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in the 1992 ***Data Book***.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	V_{CC} + 0.3	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load		25		mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *See Note (4)*		30		mA

Capacitance

See Note (4)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

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AC Operating Conditions *See Note (3)*

External Timing Parameters			EPM7032-1 *(8)*		EPM7032-2		EPM7032-3		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12		15	ns
t_{PD2}	I/O input to non-registered output			10		12		15	ns
t_{SU}	Global clock setup time				9		11		ns
t_{H}	Global clock hold time				0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF				6		8	ns
t_{CH}	Global clock high time				4		5		ns
t_{CL}	Global clock low time				4		5		ns
t_{ASU}	Array clock setup time				3		4		ns
t_{AH}	Array clock hold time				3		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF				12		15	ns
t_{ACH}	Array clock high time				5		6		ns
t_{ACL}	Array clock low time				5		6		ns
t_{CNT}	Minimum global clock period				12		13		ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*				83.3		76.9	MHz
t_{ACNT}	Minimum array clock period				12		13		ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*				83.3		76.9	MHz
f_{MAX}	Maximum clock frequency	*See Note (6)*				125		100	MHz

Internal Timing Parameters			EPM7032-1 *(8)*		EPM7032-2		EPM7032-3		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay					2		2	ns
t_{IO}	I/O input pad and buffer delay					2		2	ns
t_{SEXP}	Shared expander delay					7		9	ns
t_{PEXP}	Parallel expander delay					2		2	ns
t_{LAD}	Logic array delay					5		6	ns
t_{LAC}	Logic control array delay					5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF				3		4	ns
t_{ZX}	Output buffer enable delay					6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF				6		6	ns
t_{SU}	Register setup time					3		4	ns
t_{H}	Register hold time					3		4	ns
t_{RD}	Register delay					1		1	ns
t_{COMB}	Combinatorial delay					1		1	ns
t_{IC}	Array clock delay					5		6	ns
t_{EN}	Register enable time					5		6	ns
t_{GLOB}	Global control delay					1		2	ns
t_{PRE}	Register preset time					3		4	ns
t_{CLR}	Register clear time					3		4	ns
t_{PIA}	Prog. Interconnect Array delay					1		2	ns
t_{LPA}	Low power adder	*See Note (7)*				5		5	ns

Notes to tables:

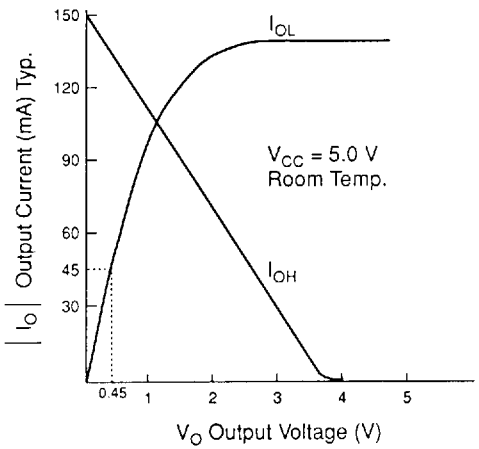
(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(4) Capacitance measured at 25° C. Sample tested only. Pin 44 (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.
(8) This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7032LC44-2, EPM7032LC44-3
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Figure 8 shows output drive characteristics of EPM7032 I/O pins.

Figure 8. Typical EPM7032 Output Drive Characteristics



Package Outlines

Figures 9 and 10 show the package outline for the 44-pin PQFP and the 44-pin PLCC package, respectively.

T-90-01

Figure 9. EPM7032 Plastic Quad Flat Pack (PQFP)

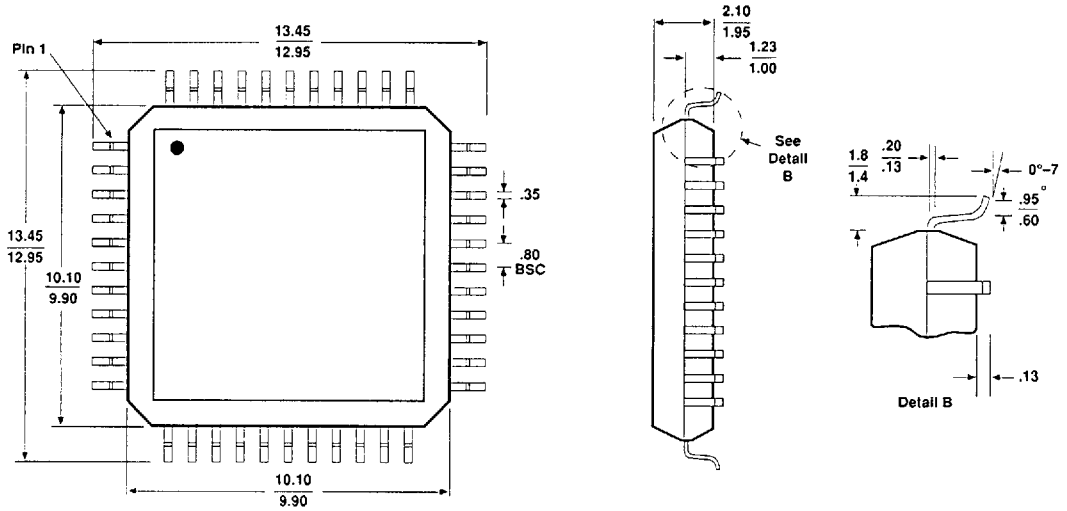


Figure 10. EPM7032 Plastic J-Lead Chip Carrier (PLCC)