NEC
NEC Electronics Inc.

μPD28C256 32,768 x 8-Bit CMOS EEPROM

Description

The μPD28C256 is a 262,144-bit electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C256 provides $\overline{\text{DATA}}$ polling and toggle bit functions to indicate the precise end of write cycles. Additional features include software data protection, software chip erase, auto erase and programming, and 64-byte page write operation using automatic write timing and internal address and data latches.

The μPD28C256 is available in standard 28-pin plastic DIP packaging.

Features

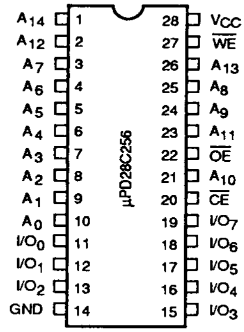
- Single +5-volt power supply
- Fast access time of 200 ns (max)
- Software chip erase cycles
- Auto erase and programming at 10 ms (max)
- 64-byte page programming cycles
- End of write detection
  - — $\overline{\text{DATA}}$ polling
  - — Toggle bit
- Software data protection
- Low power dissipation
  - — 50 mA max (active)
  - — 100 μA max (standby)
- 10,000 erase/write cycles per byte
- Silicon signature included
- Advanced CMOS technology
- 28-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C256CZ-20	200 ns	28-pin plastic DIP
CZ-25	250 ns	

Pin Configuration

28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{CC}	–0.6 to +7.0 V
Input voltage, V_{IN}	–0.6 to V_{CC} + 0.3 V
Input voltage (A_9)	–0.6 to +13.5 V
Output voltage, V_{OUT}	–0.6 to +7.0 V
Operating temperature, T_{OPR}	–10 to +85°C
Storage temperature, T_{STG}	–65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	– 0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			12	pF
Output capacitance	C_O			10	pF

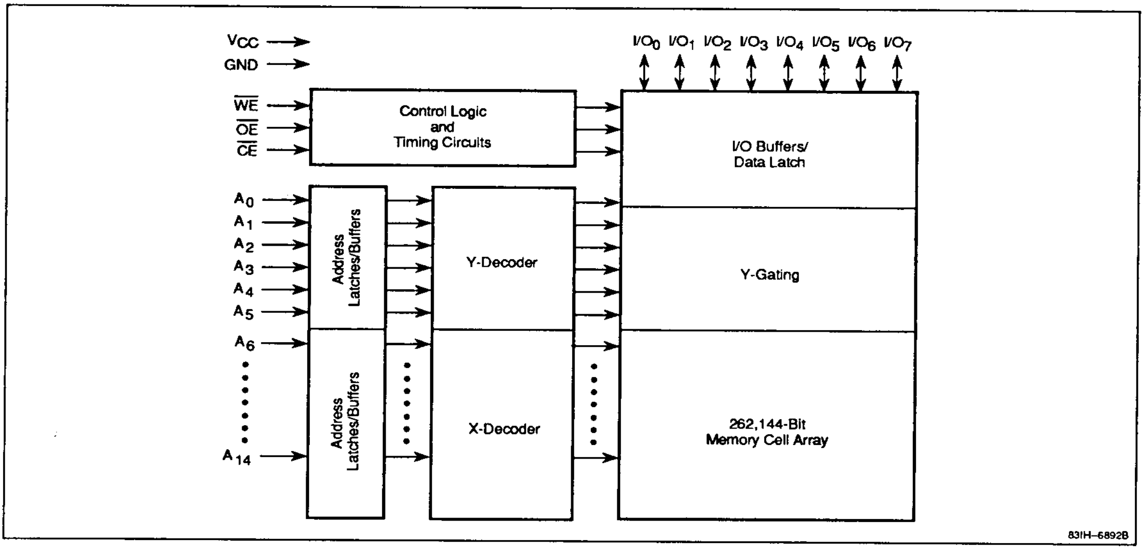
Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Write Inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	−10		10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CE}$ or $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD28C256-20		μPD28C256-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	60	0	80	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Output hold from address, $\overline{OE}$ or $\overline{CE}$, whichever transition occurs first	t_{OH}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Write Operation							
Write cycle time	t_{WC}	10		10		ms	
Address setup time	t_{AS}	10		10		ns	
Address hold time	t_{AH}	200		200		ns	
Write setup time	t_{CS}	0		0		ns	
Write hold time	t_{CH}	0		0		ns	
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
$\overline{OE}$ high hold time	t_{OEH}	50		50		ns	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
$\overline{WE}$ high pulse width	t_{WPH}	2		2		μs	
$\overline{WE}$ high hold time	t_{WEH}	9.9		9.9		ms	
$\overline{CE}$ high hold time	t_{CEH}	9.9		9.9		ms	
Data setup time	t_{DS}	100		100		ns	
Data hold time	t_{DH}	50		50		ns	
Byte load cycle time	t_{BLC}	3	100	3	100	μs	

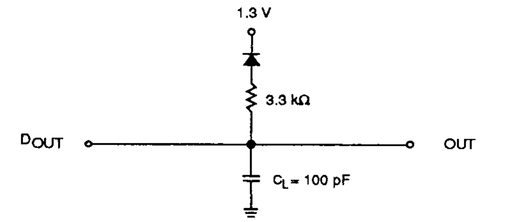
AC Characteristics (cont)

Parameter	Symbol	μPD28C256-20 Min	μPD28C256-20 Max	μPD28C256-25 Min	μPD28C256-25 Max	Unit	Test Conditions
Software Chip Erase Operation							
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	
$\overline{CE}$ hold time	t_{ECH}	20		20		μs	

Notes:

(1) See figure 1 for the output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

Figure 1. Output Load



Read Cycles

Both $\overline{CE}$ and $\overline{OE}$ must be at V_{IL} to enable stored data to be read. While the device is executing read cycles, bringing either of these inputs to V_{IH} will place the outputs in high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Cycles

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C256 in write operation. Write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. Data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuits assume all timing control and the byte being addressed is automatically erased and then programmed within the write cycle time (t_{WC}) of 10 ms.

Page Write Cycles

This option allows the μPD28C256 to be completely programmed in a much shorter time than is required by byte write cycles. Page write cycles can program up to 64 bytes simultaneously, enabling the μPD28C256 to be completely written within a maximum of 5.2 seconds. The page address is specified by the inputs A_6 through A_{14}; once set, this address cannot be changed. Within the page, address inputs A_0 through A_5 can be used sequentially or in random order to specify individual bytes.

The beginning of a page write cycle is the same as a $\overline{WE}$-controlled byte write cycle. If the next falling edge of $\overline{WE}$ occurs within a byte load cycle time of 100 μs, the internal byte register will be loaded with another byte of input data. This cycle can be repeated to load a maximum of 64 bytes of data. At any point in the sequence, if $\overline{WE}$ does not have a new falling edge within the cycle time of 100 μs, byte loading will terminate and automatic erasing and programming operations will begin.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write and page write cycles. $\overline{DATA}$ polling can be used to reduce total programming time of the μPD28C256 to a minimum value, which varies with the system environment.

While internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O_7.

Toggle Bit Feature

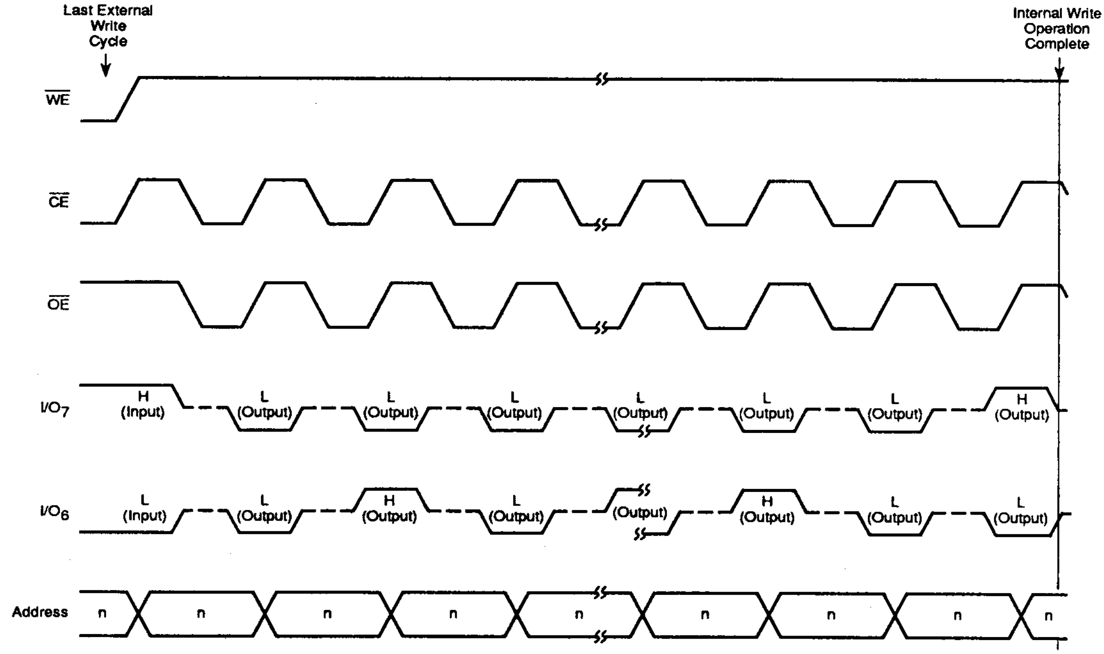
The feature provides another method for indicating the end of write cycles. During the internal automatic write operation, I/O_6 will toggle from 0 to 1 and back on successive attempts to read data. When the write cycle is complete, the toggling stops; a read cycle results in true data being output on I/O_6 (figure 2).

Hardware Data Protection

The μPD28C256 provides three features to prevent invalid write cycles:

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage level detection, where write operation is inhibited when V_{CC} is 2.5 V or less.
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power on or off of the V_{CC} supply voltage.

Figure 2. Data Polling and Toggle Bit Operation



Notes:

[1] The dashed portions of the output waveforms indicate high impedance.

[2] Address n is the address supplied in the last external write cycle.

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Software Data Protection

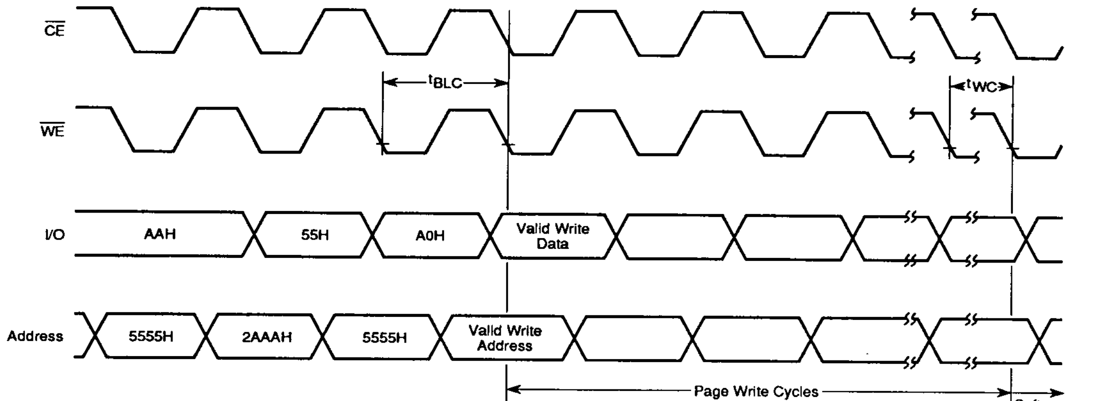
Additional protection of data is available using software control. Standard, unprotected write cycles are illustrated in the timing waveforms. Additional software-controlled protection is enabled or reset with two special sequences of write cycles. To enable software data protection, or to execute additional write cycles after the µPD28C256 is in a protected state, use the address and data sequence shown in table 1. All three byte write cycles must be issued in sequence and must meet the timing illustrated in figure 3.

Table 1. Sequence to Enable Software Data Protection

Address Input (Hex)	Write Data (Hex)
5555H	AAH
2AAAH	55H
5555H	A0H

Under software protection, no write cycles will be executed unless preceded by the above sequence. The protection circuit is nonvolatile and continues to protect the data during power-down and power-up.

Figure 3. Sequence to Initiate or Continue Software Data Protection



Notes:

[1] The software sequence is complete at the end of the first t_{WC} following all of the page write data inputs (from one to 64 bytes).

[2] $\overline{OE}$ is held at a high level.

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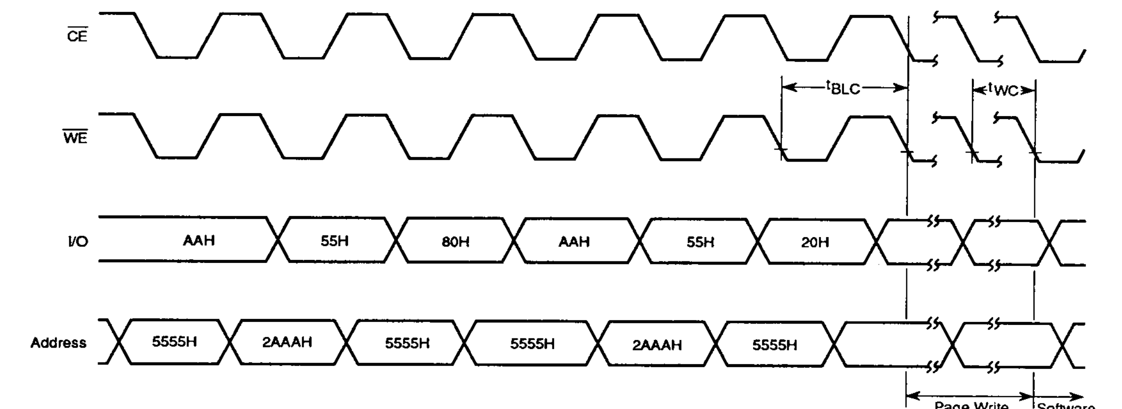
To disable software protection for ease in testing or reprogramming of the μPD28C256, the byte reset sequence shown in table 2 must be issued. The timing is illustrated in figure 4.

Table 2. Sequence to Disable Software Data Protection

Address Input (Hex)	Write Data (Hex)
5555H	AAH
2AAAH	55H
5555H	80H
5555H	AAH
2AAAH	55H
5555H	20H

At the end of this sequence, and after a minimum delay of t_{WC} to reset the nonvolatile protection circuit, the μPD28C256 is in an unprotected state. Any standard write cycle can be executed as desired. In this state, the hardware features provide all data protection.

Figure 4. Reset Sequence for Software Data Protection



Notes:

[1] The software sequence is complete at the end of the first t_{WC} following all of the page write data inputs (from one to 64 bytes).

[2] $\overline{OE}$ is held at a high level.

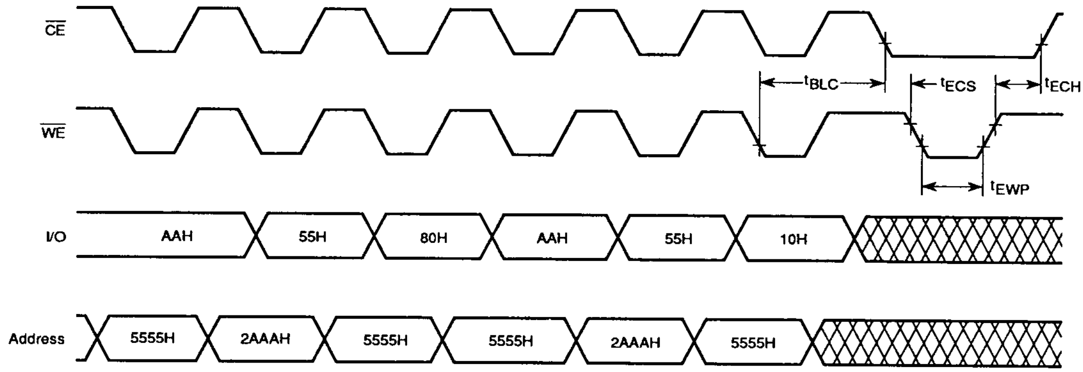
Software Chip Erase Feature

All bytes of the µPD28C256 can be erased simultaneously by making $\overline{CE}$ and then $\overline{WE}$ fall to V_{IL} using the address and data sequence shown in table 3. The required timing is illustrated in figure 5.

Table 3. Sequence to Set Up Software Chip Erase

Address Input (Hex)	Write Data (Hex)
5555H	AAH
2AAAH	55H
5555H	80H
5555H	AAH
2AAAH	55H
5555H	10H

Figure 5. Sequence for Software Chip Erase



Notes:

[1] The software sequence is complete at the end of t_{ECH} following the special address and data sequence and the erase pulse on $\overline{WE}$.

[2] $\overline{OE}$ must be held at a high level.

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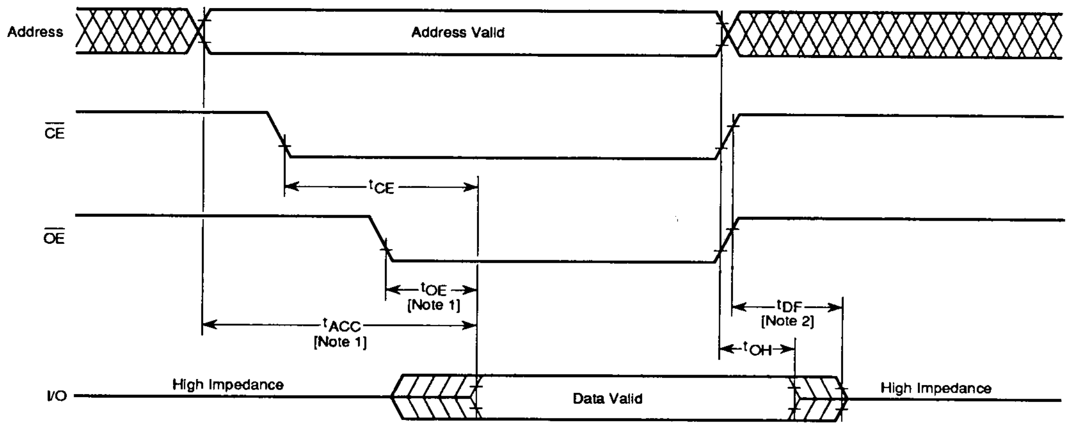
Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

[3] $\overline{WE} = V_{IH}$.

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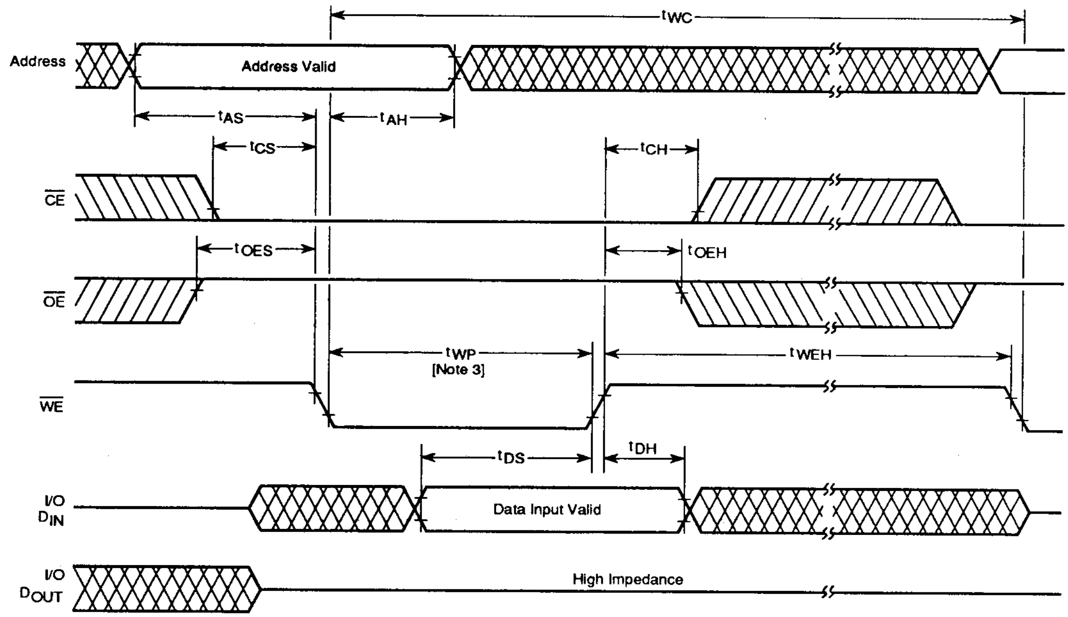
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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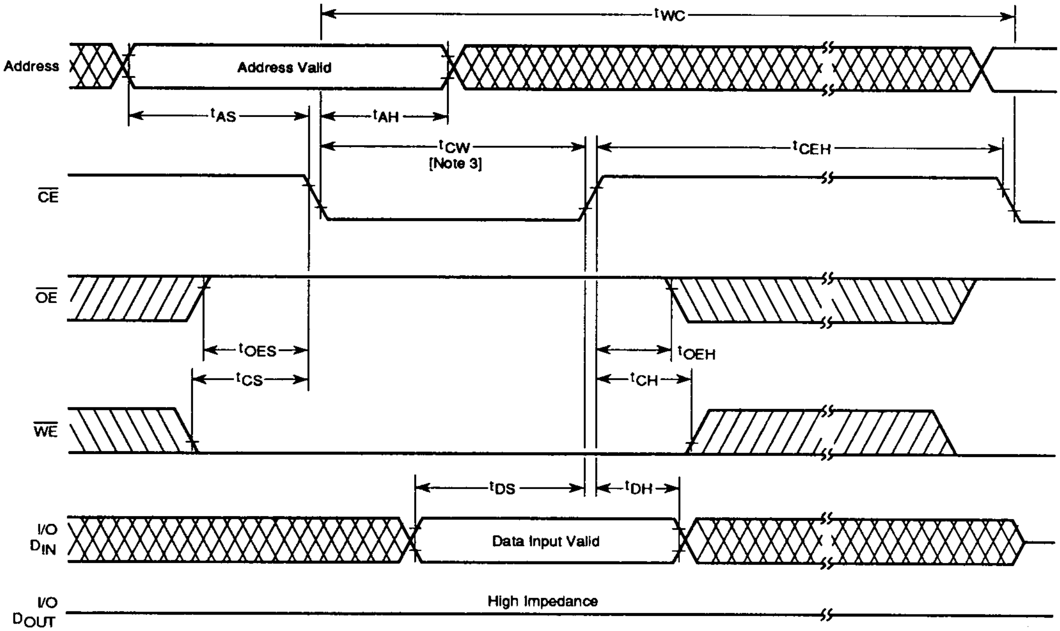
Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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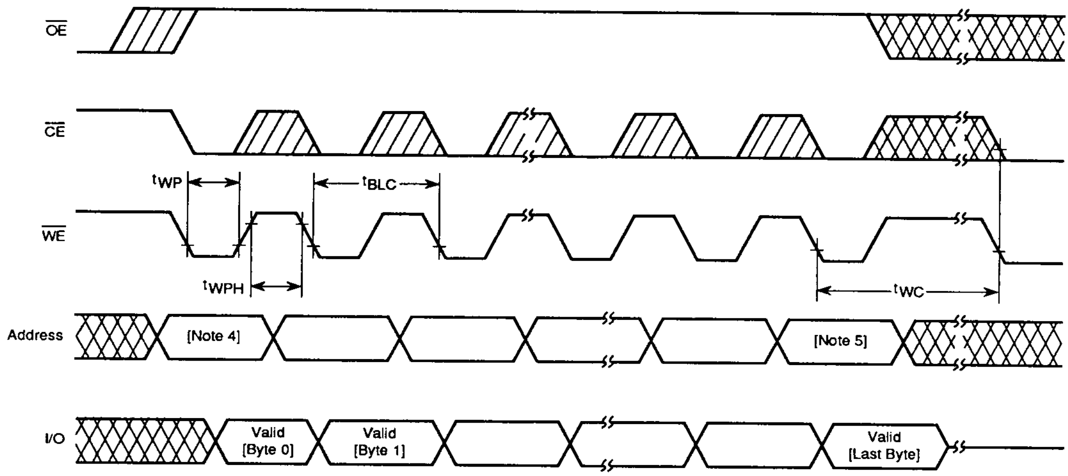
Timing Waveforms (cont)

Page Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page write cycle. Address inputs $A_6 - A_{14}$ must be supplied for every byte load cycle and must remain the same throughout the page write cycle to prevent writing to an unknown address location. Address inputs $A_0 - A_5$ are altered for each byte load cycle and determine the individual byte to be written within the page.

[5] A maximum of 64 bytes may be loaded in a single page write cycle.

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