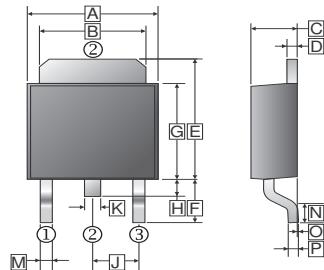
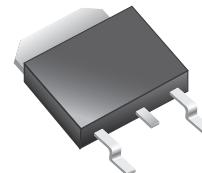


RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD55N03 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The TO-252 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

TO-252(D-Pack)



FEATURES

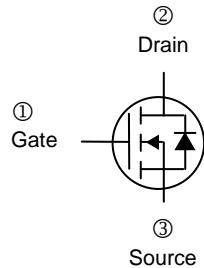
- Dynamic dv/dt Rating
- Simple Drive Requirement
- Repetitive Avalanche Rated
- Fast Switching

MARKING



PACKAGE INFORMATION

Package	MPQ	LeaderSize
TO-252	2.5K	13' inch



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30	REF.
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V _{DS}	25	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current T _C =25°C	I _D	55	A
T _C =100°C		35	A
Pulsed Drain Current ¹	I _{DM}	215	A
Total Power Dissipation	P _D	62.5	W
Linear Derating Factor		0.5	W / °C
Single Pulse Avalanche Energy ²	E _{AS}	240	mJ
Single Pulse Avalanche Current	I _{AS}	31	A
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Ambient	R _{θJA}	110	°C / W
Maximum Thermal Resistance Junction-Case	R _{θJC}	2.0	°C / W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	25	-	-	V	$V_{GS}=0$, $I_D=250\mu\text{A}$
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	-	0.037	-	V/°C	Reference to 25°C, $I_D=1\text{mA}$
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	3.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
Forward Transconductance	g_{fs}	-	30	-	S	$V_{DS}=10\text{V}$, $I_D=28\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}= \pm 20\text{V}$
Drain-Source Leakage Current	$T_J = 25^\circ\text{C}$	I_{DSS}	-	-	1	μA
			-	-	25	μA
Static Drain-Source On-Resistance ³	$R_{DS(ON)}$	-	4.5	6	mΩ	$V_{GS}=10\text{V}$, $I_D=30\text{A}$
		-	7	9		$V_{GS}=4.5\text{V}$, $I_D=30\text{A}$
Total Gate Charge ³	Q_g	-	16.8	-	nC	$I_D=28\text{A}$ $V_{DS}=20\text{V}$ $V_{GS}=5\text{V}$
Gate-Source Charge	Q_{gs}	-	6.0	-		
Gate-Drain ("Miller") Change	Q_{gd}	-	4.9	-		
Turn-on Delay Time ³	$T_{d(on)}$	-	15.1	-	nS	$V_{DS}=15\text{ V}$ $I_D=28\text{ A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$ $R_D=0.53\Omega$
Rise Time	T_r	-	4	-		
Turn-off Delay Time	$T_{d(off)}$	-	45.2	-		
Fall Time	T_f	-	7.6	-		
Input Capacitance	C_{iss}	-	2326	-	pF	$V_{GS}=0$ $V_{DS}=25\text{ V}$ $f=1.0\text{MHz}$
Output Capacitance	C_{oss}	-	331	-		
Reverse Transfer Capacitance	C_{rss}	-	174	-		
Source-Drain Diode						
Diode Forward Voltage ³	V_{SD}	-	-	1.5	V	$I_S=20\text{A}$, $V_{GS}=0$, $T_J=25^\circ\text{C}$
Continuous Source Current (Body Diode)	I_S	-	-	55	A	$V_D=V_G=0$, $V_S=1.5\text{V}$

Notes:

1. Pulse width limited by safe operating area.
2. Starting $T_J=25^\circ\text{C}$, $V_{DD}=20\text{V}$, $L=0.1\text{mH}$, $R_G=25$, $I_{AS}=10\text{A}$.
3. Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

CHARACTERISTIC CURVES

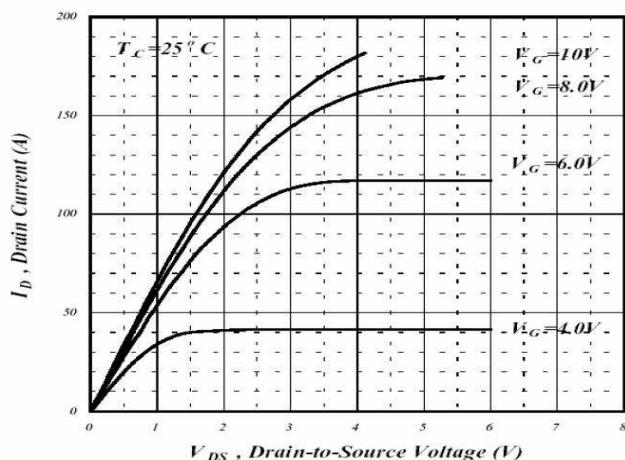


Fig 1. Typical Output Characteristics

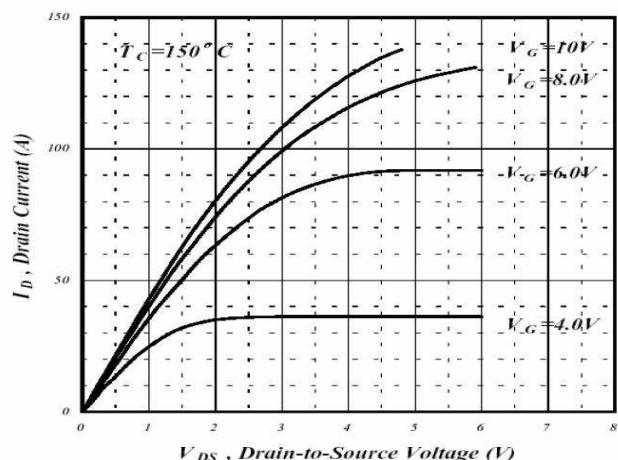


Fig 2. Typical Output Characteristics

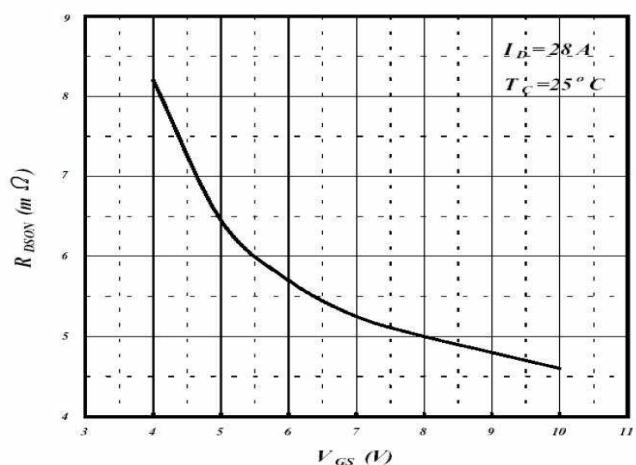


Fig 3. On-Resistance v.s. Gate Voltage

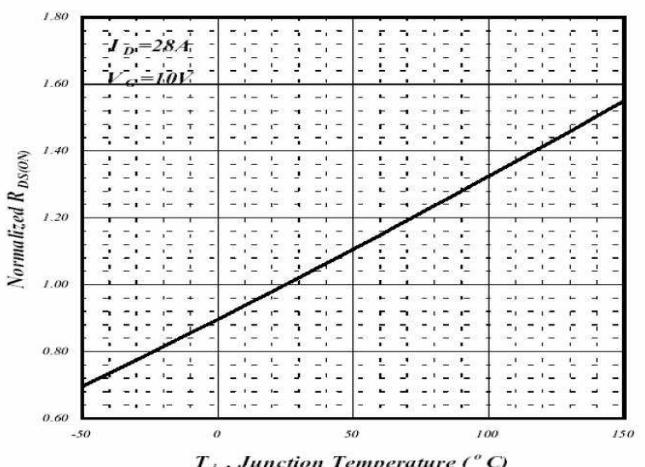


Fig 4. Normalized On-Resistance v.s. Junction Temperature

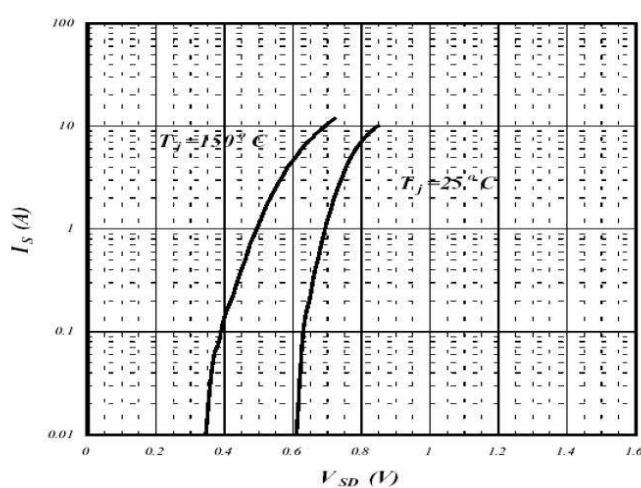


Fig 5. Forward Characteristics of Reverse Diode

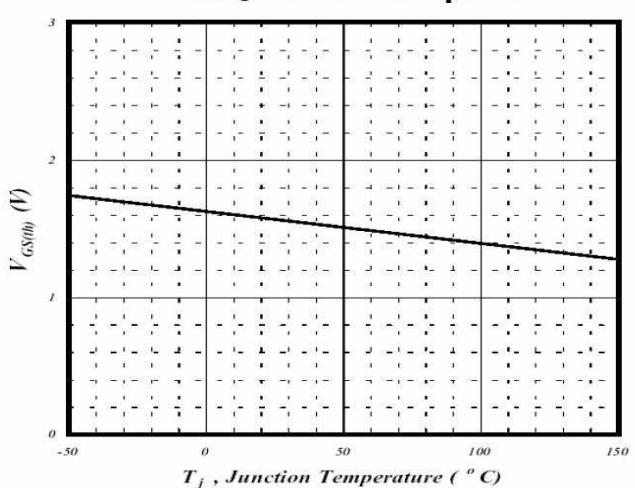


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTIC CURVES

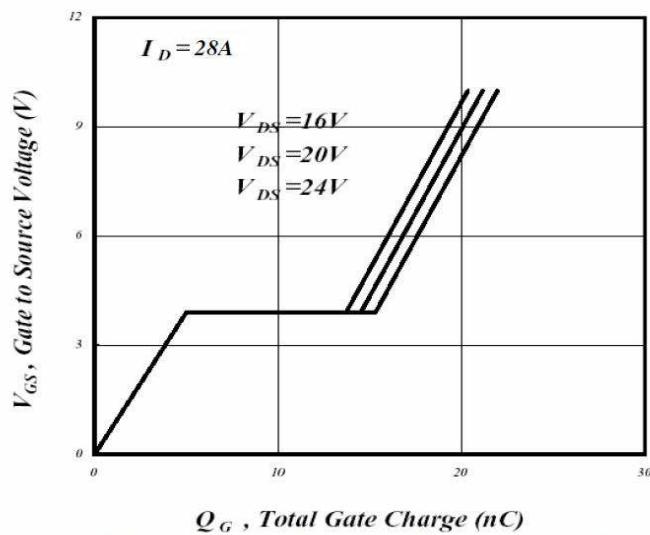


Fig 7. Gate Charge Characteristics

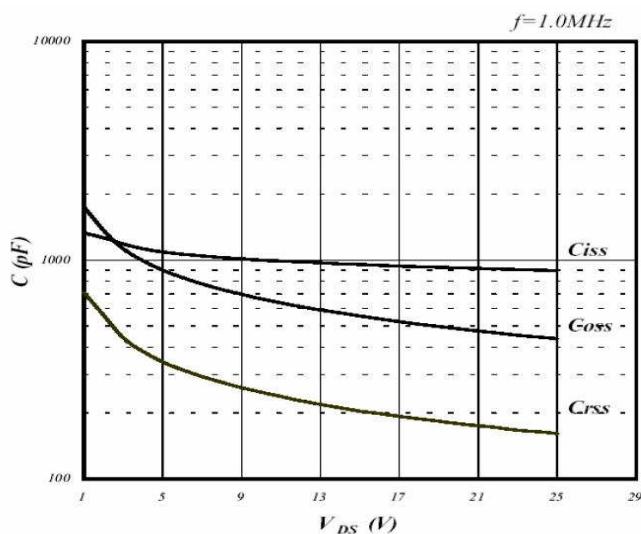


Fig 8. Typical Capacitance Characteristics

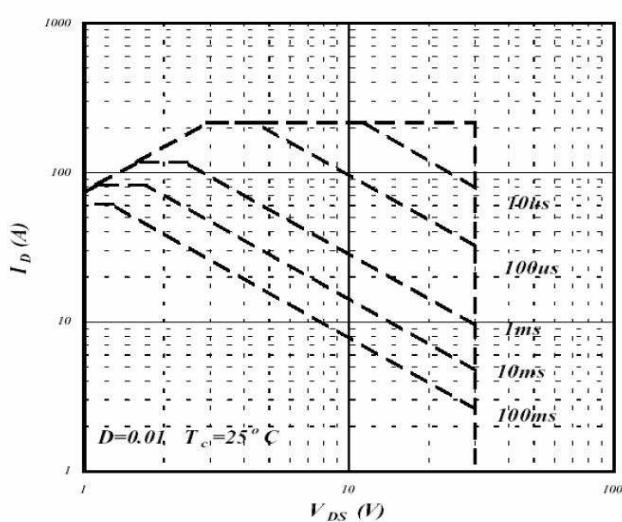


Fig 9. Maximum Safe Operating Area

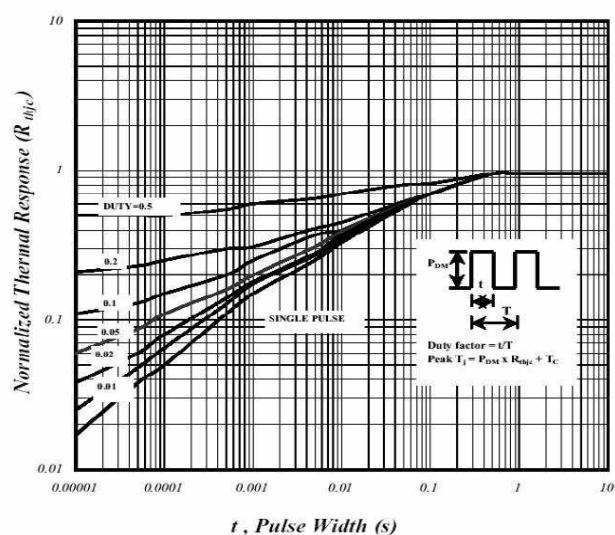


Fig 10. Effective Transient Thermal Impedance

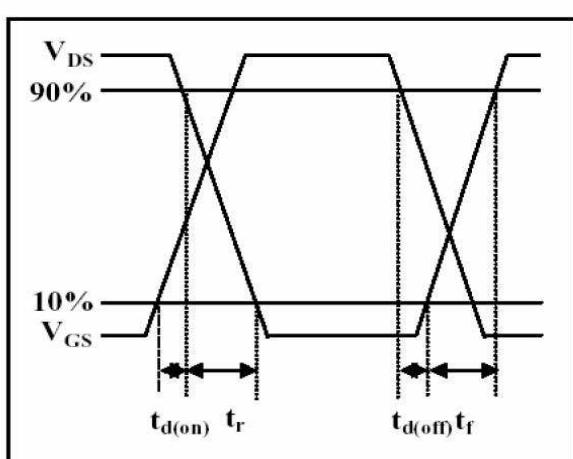


Fig 11. Switching Time Waveform

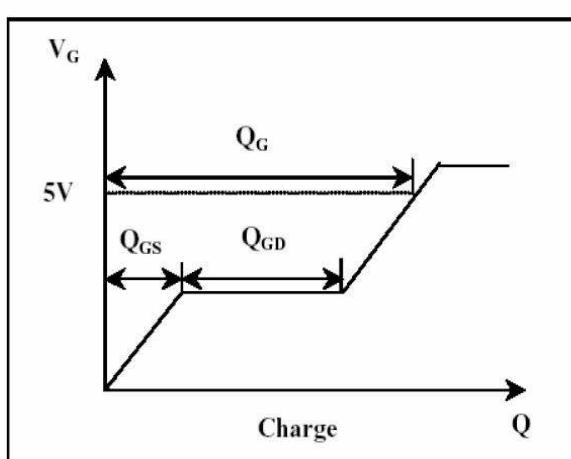


Fig 12. Gate Charge Waveform