Latch

FAST 74F1604

FEATURES

- High impedance NPN base inputs for reduced loading (20µA in high and low state)
- Stores 16–bit wide data inputs, multiplexed 8–bit outputs
- Propagation delay 7.0ns typical
- Power supply current 70mA typical

DESCRIPTION

The 74F1604 is a dual octal transparent latch. Organized as 8–bit A and B latches, the latch outputs are connected by pairs to eight 2–input multiplexers. A select (SELECT A/B) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data from the B inputs are selected when SELECT A/B is low; data from the A inputs are selected when SELECT A/B is high. Data enters the latch on the falling edge of the latch enable (LE) input. The latch remains transparent to the data inputs while LE is low, and stores the data that is present one setup time before the low–to–high latch enable transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F1604	7.0ns	70mA

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0°C$ to $+70°C$
28–pin plastic DIP	N74F1604N
28–pin plastic SOL	N74F1604D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

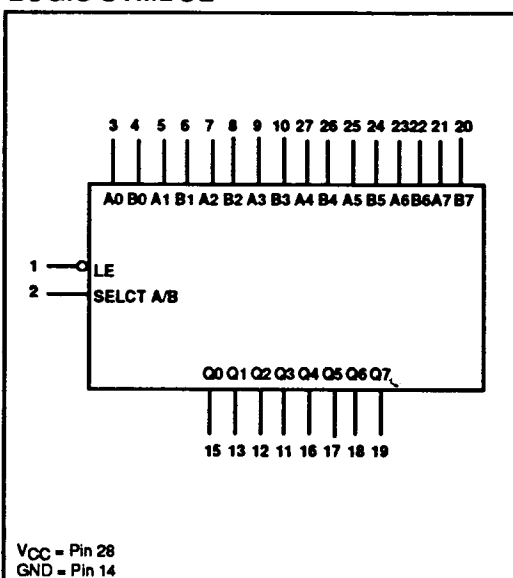| PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	Data inputs	1.0/0.033	20µA/20µA
B0 – B7	Data inputs	1.0/0.033	20µA/20µA
SELECT A/B	Select input	1.0/0.033	20µA/20µA
LE	Latch enable input (active low)	1.0/0.033	20µA/20µA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

Note to input and output loading and fan out table
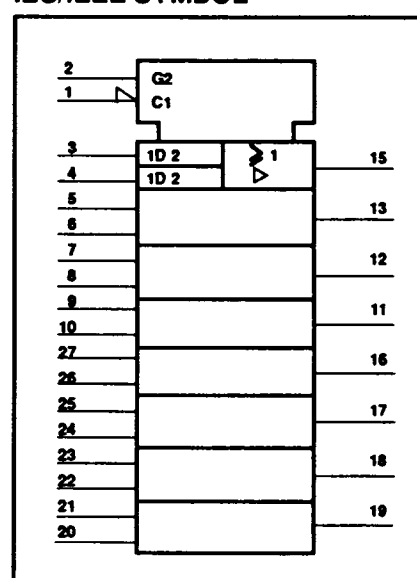1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

PIN CONFIGURATION

LE	1	28	VCC
SELECT A/B	2	27	A4
A0	3	26	B4
B0	4	25	A5
A1	5	24	B5
B1	6	23	A6
A2	7	22	B6
B2	8	21	A7
A3	9	20	B7
B3	10	19	Q7
Q3	11	18	Q6
Q2	12	17	Q5
Q1	13	16	Q4
GND	14	15	Q0

LOGIC SYMBOL

3 4 5 6 7 8 9 10 27 26 25 24 23 22 21 20

A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7

1 — LE
2 — SELCT A/B

Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7

15 13 12 11 16 17 18 19

VCC = Pin 28
GND = Pin 14
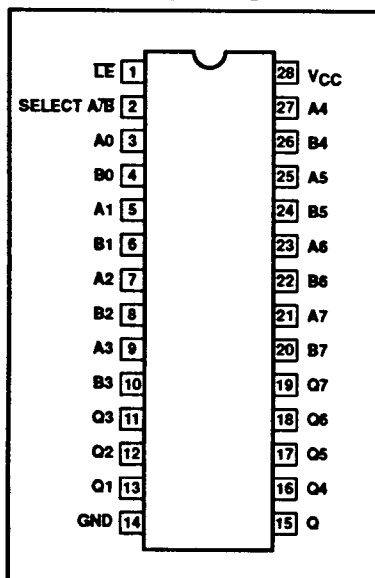
IEC/IEEE SYMBOL

Latch

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LOGIC DIAGRAM

Vcc = Pin 28
GND = Pin 14
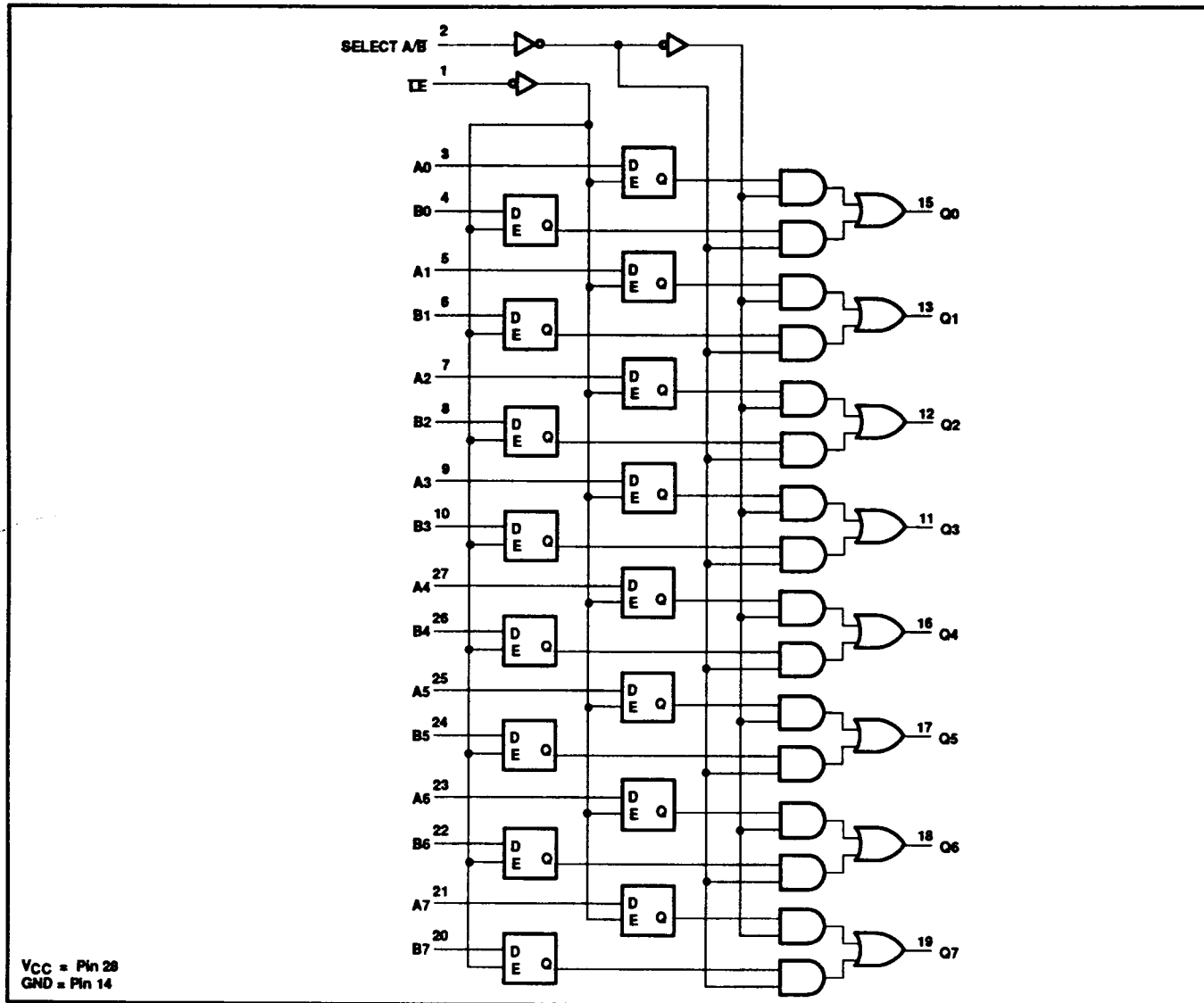
FUNCTION TABLE

INPUTS19				OUTPUTS	OPERATING MODE
A0 – A7	B0 –B7	SELECT A/B̄	L̄E	Q0 – Q7	
A data	B data	L	L	B data	Enable and read register
A data	B data	H	L	A data	
X	X	X	H	NC	Hold
A data	B data	l	↑	B data	Latch and read register
A data	B data	h	↑	A data	

Notes to function table

1. H = High–voltage level
2. h = High–voltage level one setup time before the low–to–high latch enable transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time before the low–to–high latch enable transition
5. NC= No change (If SELECT A/B̄ is toggled and the A latched data is different from B latched data then the output will change accordingly.)
6. X = Don't care
7. ↑ = Low–to–high latch enable transition

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = –3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OS}	Short–circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			60	80	mA
		I_{CCL}				75	100	mA

Notes to DC electrical characteristics
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
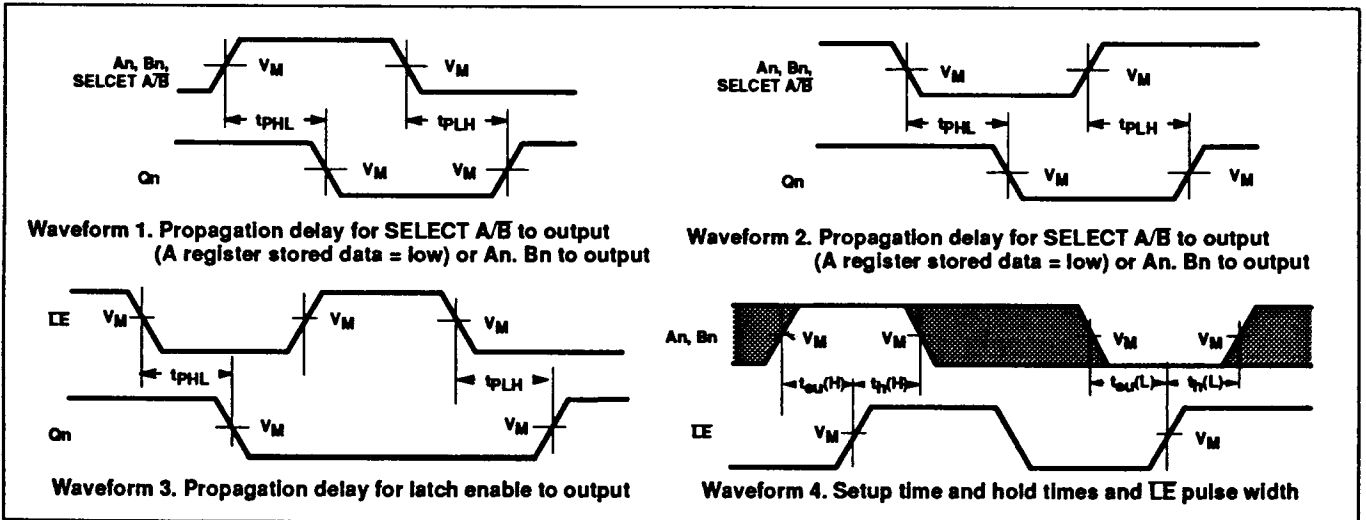
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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay SELECT A/B to Qn (non–inverting)	Waveform 2	3.0 3.5	5.5 6.5	8.5 10.0	2.5 3.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/B to Qn (inverting)	Waveform 1	4.0 2.5	7.0 4.5	10.5 7.5	3.5 2.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	Waveform 3	6.5 6.0	9.5 9.0	13.0 12.5	5.5 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Qn	Waveform 1, 2	4.0 4.0	6.5 7.0	9.5 10.5	3.5 3.5	10.5 12.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An, Bn to LE	Waveform 4	0.0 1.0			0.0 3.5		ns
t_h (H) t_h (L)	Hold time, high or low An, Bn to LE	Waveform 4	1.5 3.0			2.0 3.5		ns
t_w (L)	LE Pulse width, low	Waveform 4	6.5			7.5		ns

AC WAVEFORMS

Waveform 1. Propagation delay for SELECT A/B to output (A register stored data = low) or An. Bn to output

Waveform 2. Propagation delay for SELECT A/B to output (A register stored data = low) or An. Bn to output

Waveform 3. Propagation delay for latch enable to output

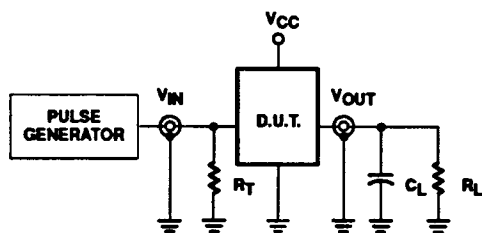Waveform 4. Setup time and hold times and LE pulse width

Note to AC waveforms
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

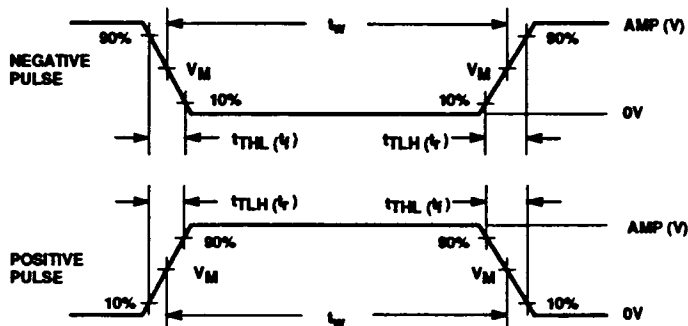## TEST CIRCUIT AND WAVEFORMS

Test circuit for totem-pole outputs

DEFINITIONS:
R_L = Load resistor;
see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of
pulse generators.

Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns