Ordering number : ENN7695

CMOS IC

LC78684NE

Compact Disc Player MP3 Decoder

Overview

The LC78684NE integrates CD-ROM signal-processing functions, MP3 signal-processing functions, and CD-DA anti-shock signal-processing functions on a single chip.
The LC78684NE achieves lower power consumption than other approaches by implementing these signal-processing functions with hardwired structures.
A CD player that supports MPEG audio (MP3) playback from CD media as well as CD-DA anti-shock (prevents audio skipping due to mechanical shock) playback can be implemented by combining this IC with CD DSP, DRAM, audio D/A converter, and other components.

Features

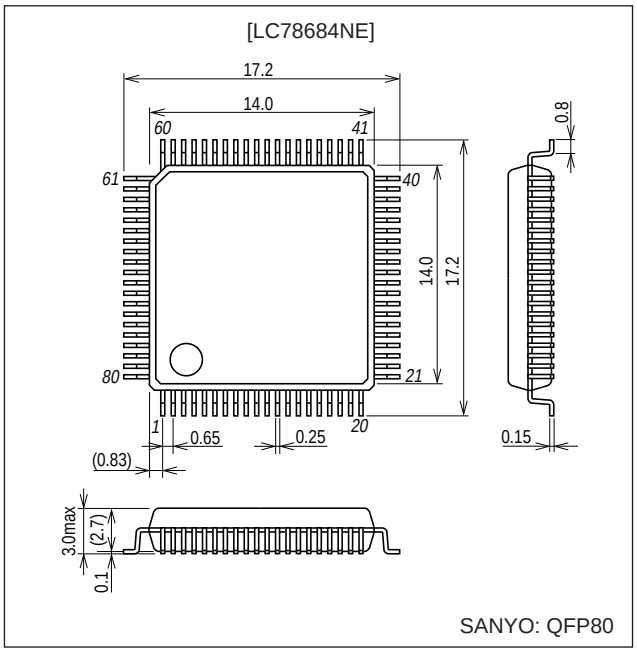
1. MP3 (MPEG audio standard (ISO/IEC 11172-3) layer 3) decoding function
   - Decodes MP3 data decoded from the CD-ROM decoder to the original (digital) audio signal and outputs that signal.
   - Supports all bit rates including variable bit rate
   - Supports the following sampling rates
     MPEG1 (Fs = 32K, 44.1K, 48K)
     MPEG2 (Fs = 16K, 22.05K, 24K)
     MPEG2.5 (Fs = 8K, 11.025K, 12K)
   - Can read out the MPEG header information and the ancillary information
   - Supports automatic muting when CRC errors occur using an MP3 CRC check function
   - MPEG data external serial input function supports playback from memory cards
2. CD-ROM decoding function
   - Supports CD-ROM mode 1 and mode 2 (forms 1 and 2)
   - CD-ROM error correction function provides faithful and accurate decoding of data written to the CD-ROM disc.
   - Header and sector management
   - Supports up to 4×-speed playback
   - In addition to data buffering, also supports C2 error flag buffering
   - External serial output of CD-ROM decoded data
3. CD-DA playback function (with anti-shock support)
   - Provides about 180 seconds of anti-shock play when a 64M DRAM is used (when data compression is used).
   - Supports both compressed and uncompressed, and also provides a data through output
   - Supports VCEC (variable speed) playback up to 4× speed
4. Audio signal processing
   - Audio signal output is provided as a serial output signal from the LRCK, BCK, and DATA pins
     (I^2S format and PCM output data have a precision of 16 or 20 bits, and 16, 24, and 32 bit output modes are supported for data slot output.)
   - Digital bass boost (4 modes), attenuator, and muting (–∞, –12 dB) functions
   - Base clock (384 fs) output pin for use with external digital filter or D/A converter circuits
5. DRAM interface
   - Supports EDO DRAM (1 to 64 Mb, 2 CAS, 16-bit data path) or SDRAM (16 or 64 Mb, 16-bit data path, CAS latency: 2, burst length: full) as external memory
   - Supports allocation of a DRAM user area during CD-ROM (MP3) playback
6. Package and supply voltage specifications
   - Package (units: mm): Sanyo QFP80 (14 × 14 mm)
   - Supply voltages:
     Internal power supply: 1.8 V (typical)
     I/O power supply: 3.3 V (typical)
     Analog system power supply: 3.3 V (typical)

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

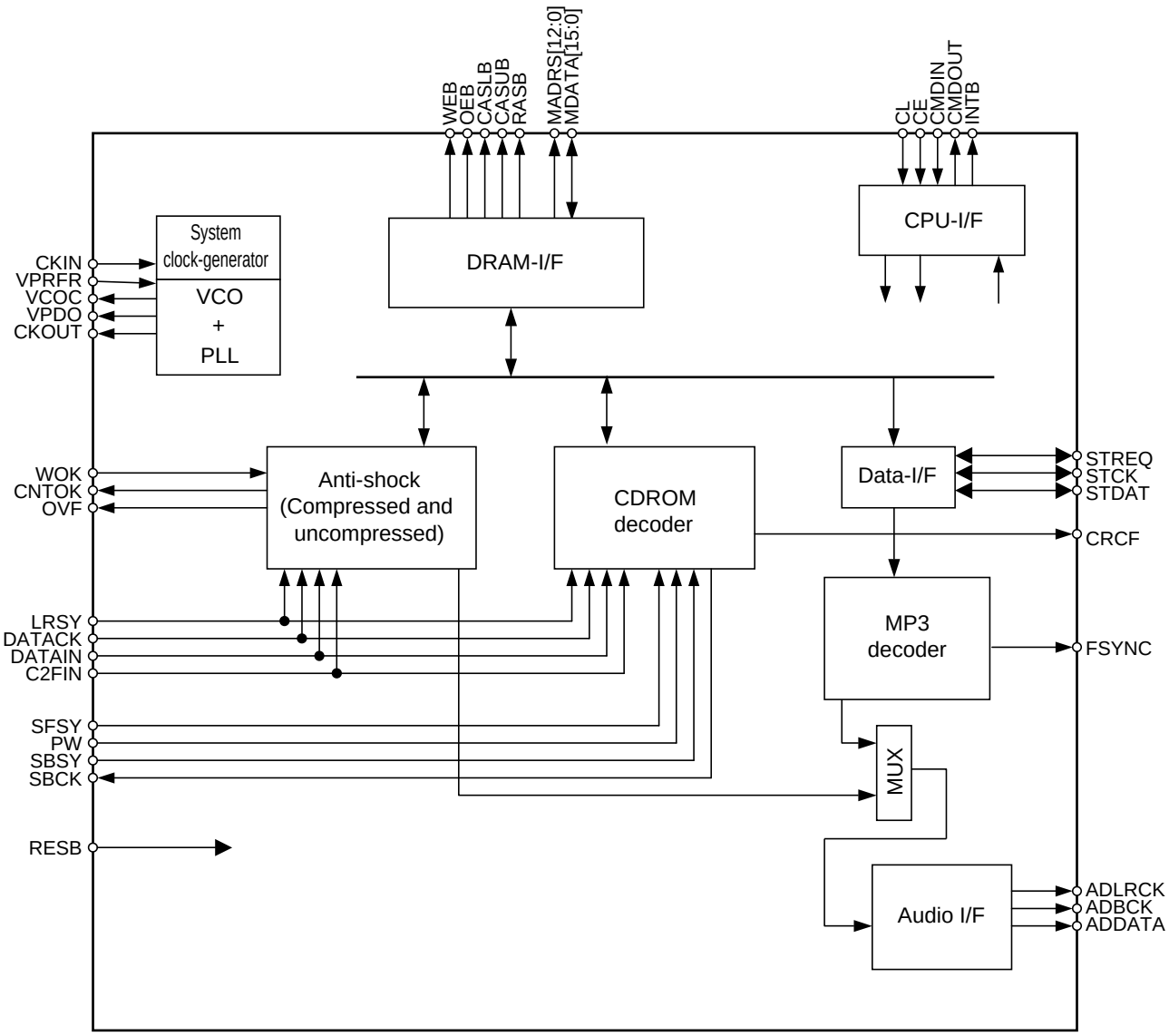
Package Dimensions

unit: mm

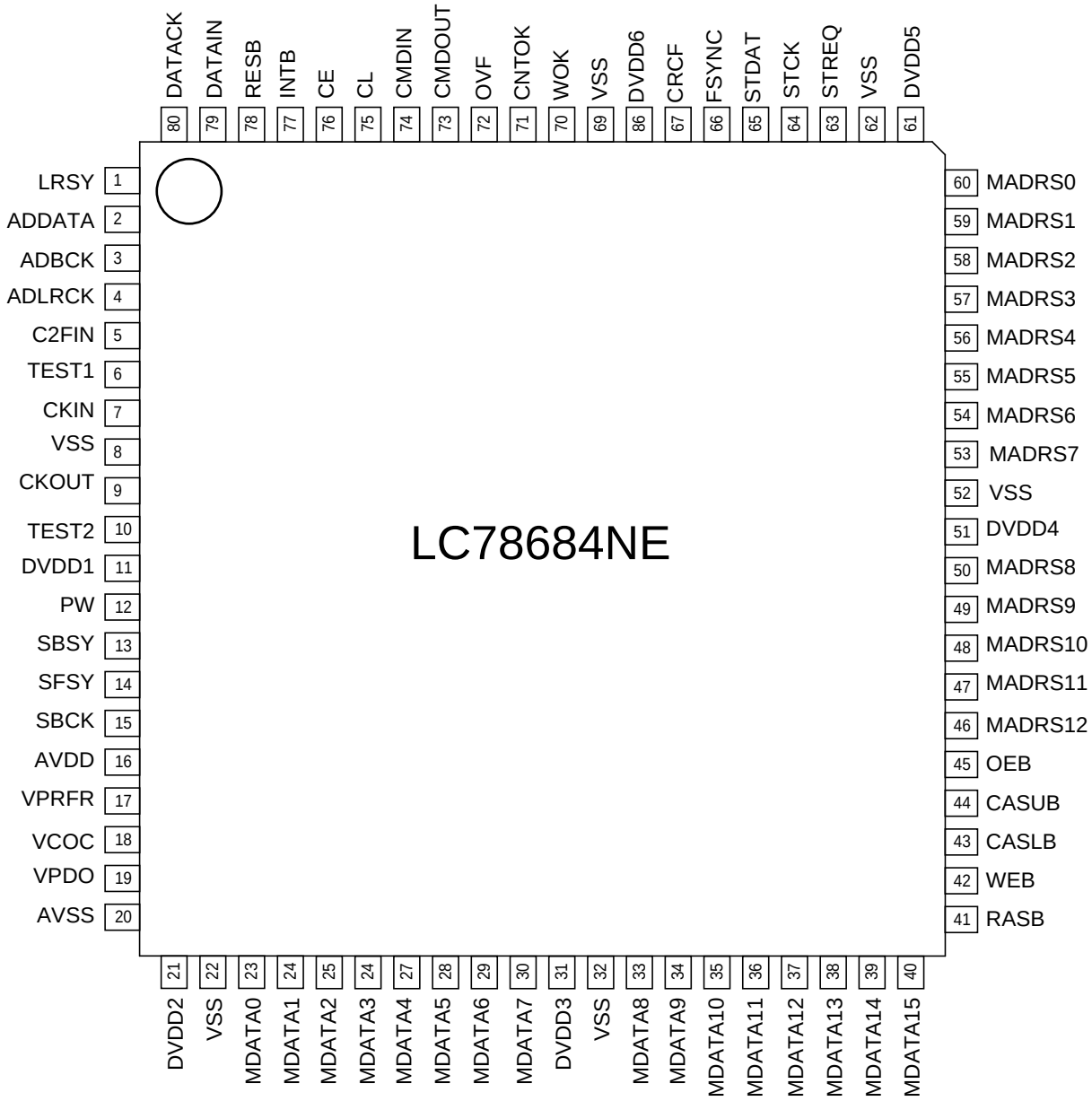
3255-QFP80



Block Diagram



Pin Assignment



Top view

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V, AV_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}1$ max		–0.3 to V_{SS} + 4.0	V
	$V_{DD}2$ max		–0.3 to V_{SS} + 2.2	V
Input voltage	VIN		–0.3 to $V_{DD}1$ + 0.3	V
Output voltage	VOUT		–0.3 to $V_{DD}1$ + 0.3	V
Allowable power dissipation	Pdmax		400	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +75°C, V_{SS} = 0 V, AV_{SS} = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	$V_{DD}1$	$DV_{DD}1$, $DV_{DD}3$, $DV_{DD}4$, $DV_{DD}6$, AV_{DD}		3.0	3.3	3.6	V
	$V_{DD}2$	$DV_{DD}2$, $DV_{DD}5$		1.62	1.8	1.98	V
High-level input voltage	VIH	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB		$0.8V_{DD}1$		$V_{DD}1$	V
Low-level input voltage	VIL	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB, TEST1, TEST2		0		$0.2V_{DD}1$	V
Operating frequency range	Fop	CKIN			16.9344		MHz

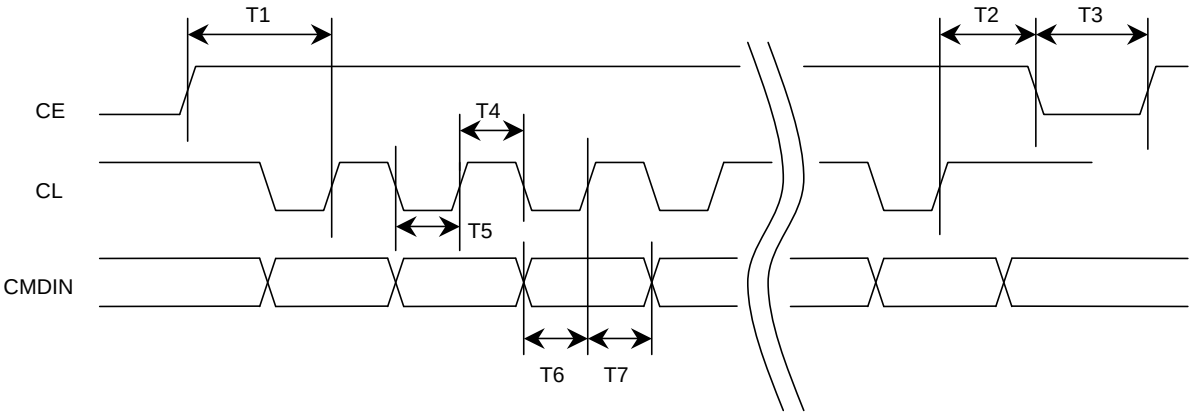
Electrical Characteristics at Ta = –30 to +75°C, $V_{DD}1$ = 3.0 V to 3.6 V, $V_{DD}2$ = 1.62 V to 1.98 V, V_{SS} = 0 V, AV_{SS} = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Current drain	I_{DD} (1)	$DV_{DD}1$, $DV_{DD}3$, $DV_{DD}4$, $DV_{DD}6$, AV_{DD}	$V_{DD}1$ = 3.0 to 3.6 V		10.0	20.0	mA
	I_{DD} (2)	$DV_{DD}2$, $DV_{DD}5$	$V_{DD}2$ = 1.62 to 1.98 V		4.5	10.0	mA
High-level input current	IIH	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB	VIN = $V_{DD}1$			10	µA
Low-level input current	IIL	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB, TEST1, TES2	VIN = 0 V	–10			µA
High-level output voltage	VOH (1)	MDATA0 to 15, STREQ, STCK, STDAT, MADRS0 to 12, RASB, CASUB, CASLB, OEB, WEB, SBCK, ADDATA, ADLRCK, ADBCK, INTB, FSYNC, CRCF, CNTOK, OVF	IOH = –2 mA	$V_{DD}1 - 0.6$			V
	VOH (2)	CKOUT	IOH = –4 mA	$V_{DD}1 - 0.6$			V
	VOH (3)	VPDO	IOH = –0.2 mA	$V_{DD}1 - 0.6$			V
Low-level output voltage	VOL (1)	MDATA0 to 15, STREQ, STCK, STDAT, MADRS0 to 12, RASB, CASUB, CASLB, OEB, WEB, SBCK, ADDATA, ADLRCK, ADBCK, INTB, FSYNC, CRCF, CNTOK, OVF, CMDOUT	IOL = 2 mA			0.4	V
	VOL (2)	CKOUT	IOL = 4 mA			0.4	V
	VOL (3)	VPDO	IOL = 0.2 mA			0.4	V
Output off leakage current	IOFF (1)	MDATA0 to 15, STREQ, STCK, STDAT, CMDOUT	VOUT = $V_{DD}1$			10	µA
	IOFF (2)	MDATA0 to 15, STREQ, STCK, STDAT, CMDOUT	VOUT = 0 V	–10			µA

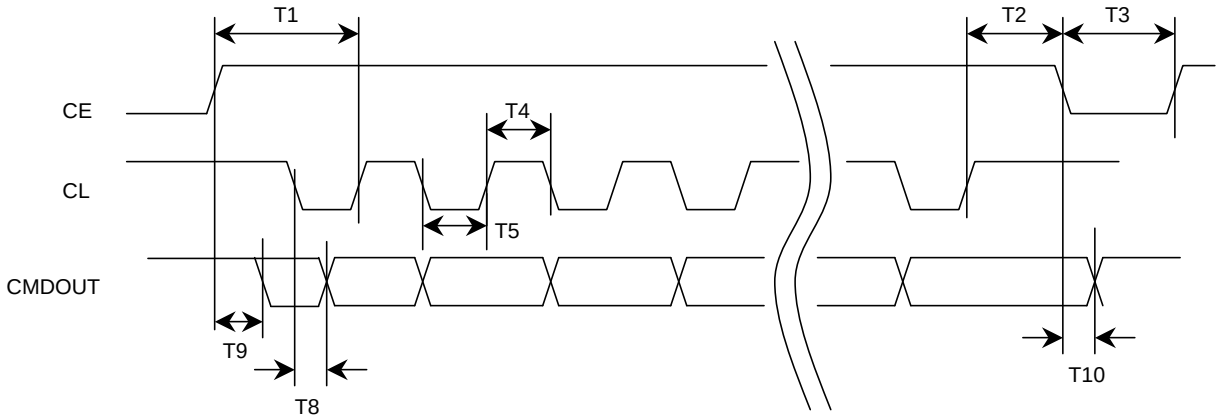
Microcontroller Interface

1. Microcontroller Interface Timing

• Write Cycle



• Read Cycle



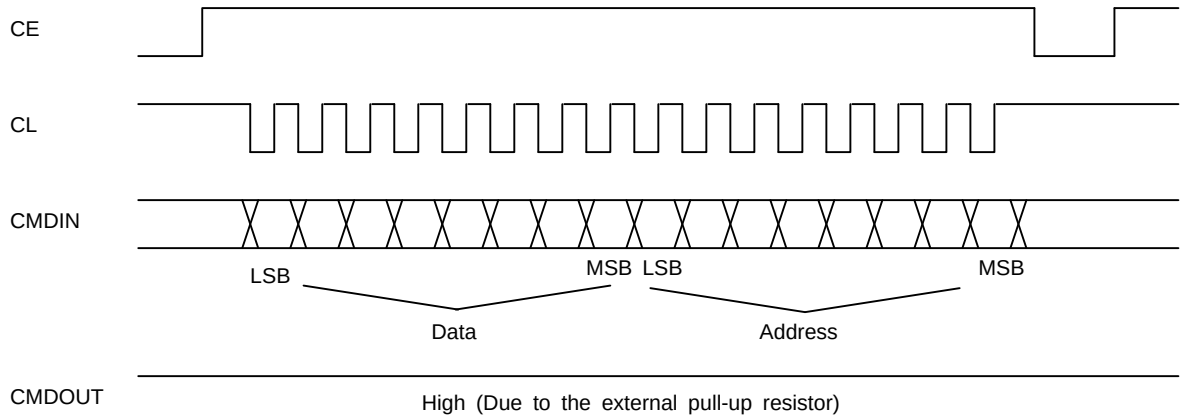
Symbol	Parameter	Ratings			Unit
		min	typ	max	
T1	CE/CL setup time	500			ns
T2	CE/CL hold time	250			ns
T3	Command wait time	1000			ns
T4	CL high-level pulse width	250			ns
T5	CL low-level pulse width	250			ns
T6	Data/CL setup time	150			ns
T7	Data/CL hold time	150			ns
T8	Data-read access time *1	0		240	ns
T9	Data-read turn-on time *1	0		150	ns
T10	Data-read turn-off time *1	0		240	ns

*1: Pull-up register = 1 kΩ, output load = 30 pF.

2. Command Input/Data Output Interface

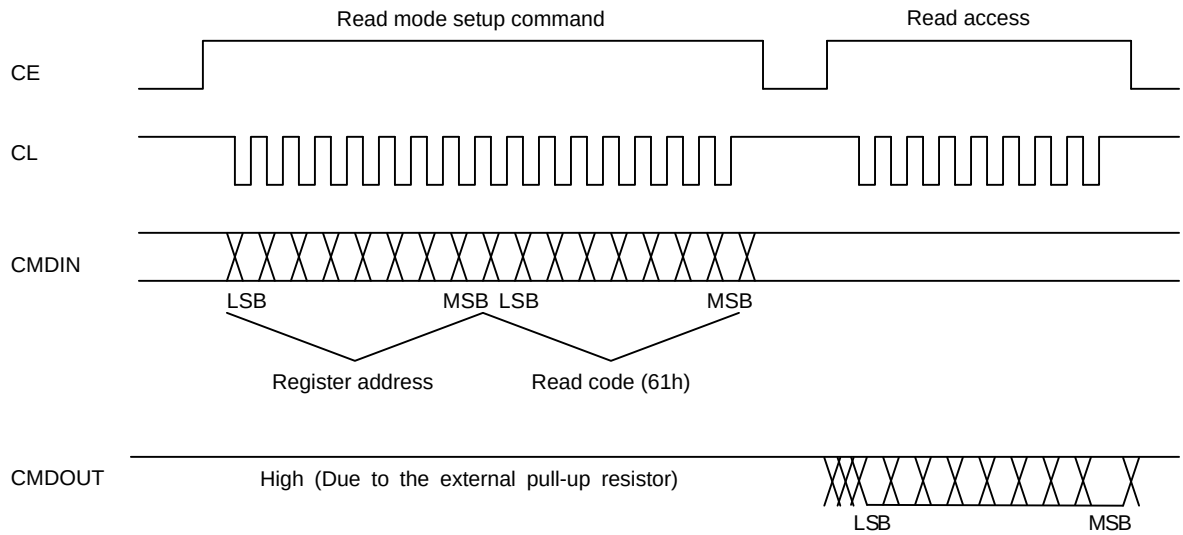
Commands (data write operations) from the microcontroller must be transferred LSB first in the following order: first the data and then the address.
To perform a data output (data read) operation, first issue a read mode setup command and then perform the read access.

• Data Write



• Data Read

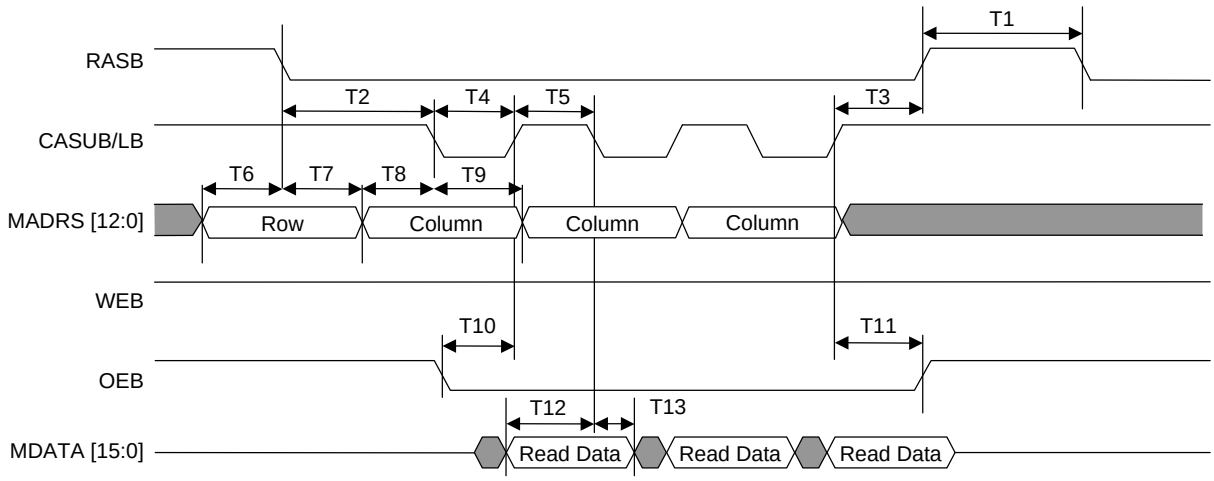
To read the data at address 61h, first write the address and set up read mode by setting CE low temporarily. When CE is set high again and then a CL is issued, the contents of the set register address will be output serially (LSB first) from CMDOUT.
If read mode is set up, a read access must be performed.



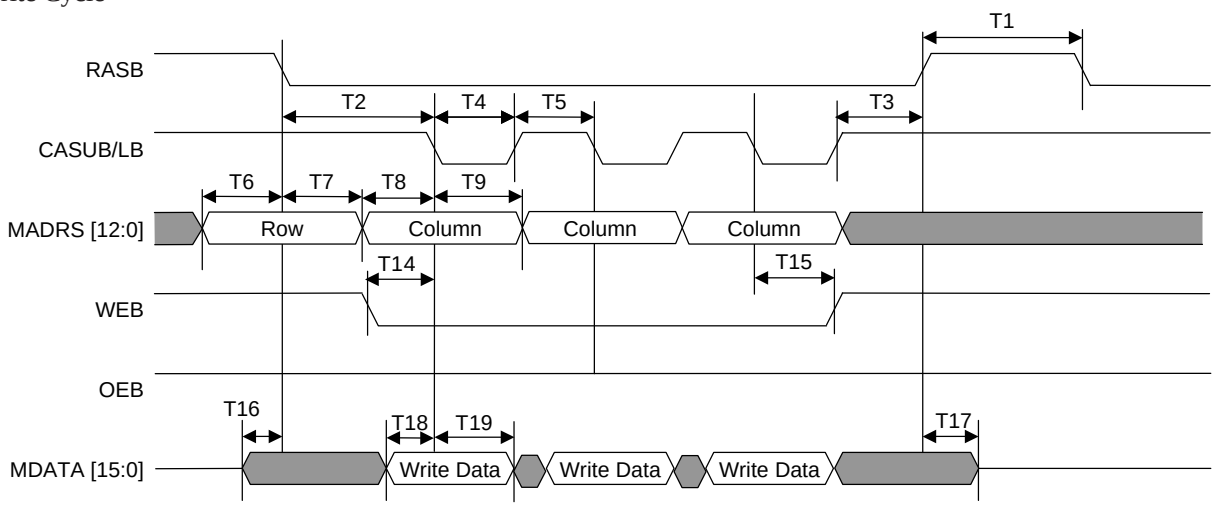
Memory Interface

EDO DRAM Interface Timing

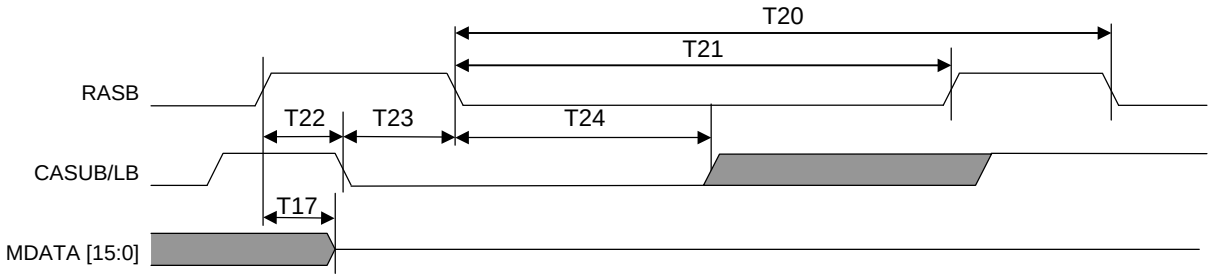
• Read Cycle



• Write Cycle



• Refresh Cycle (CAS before RAS)

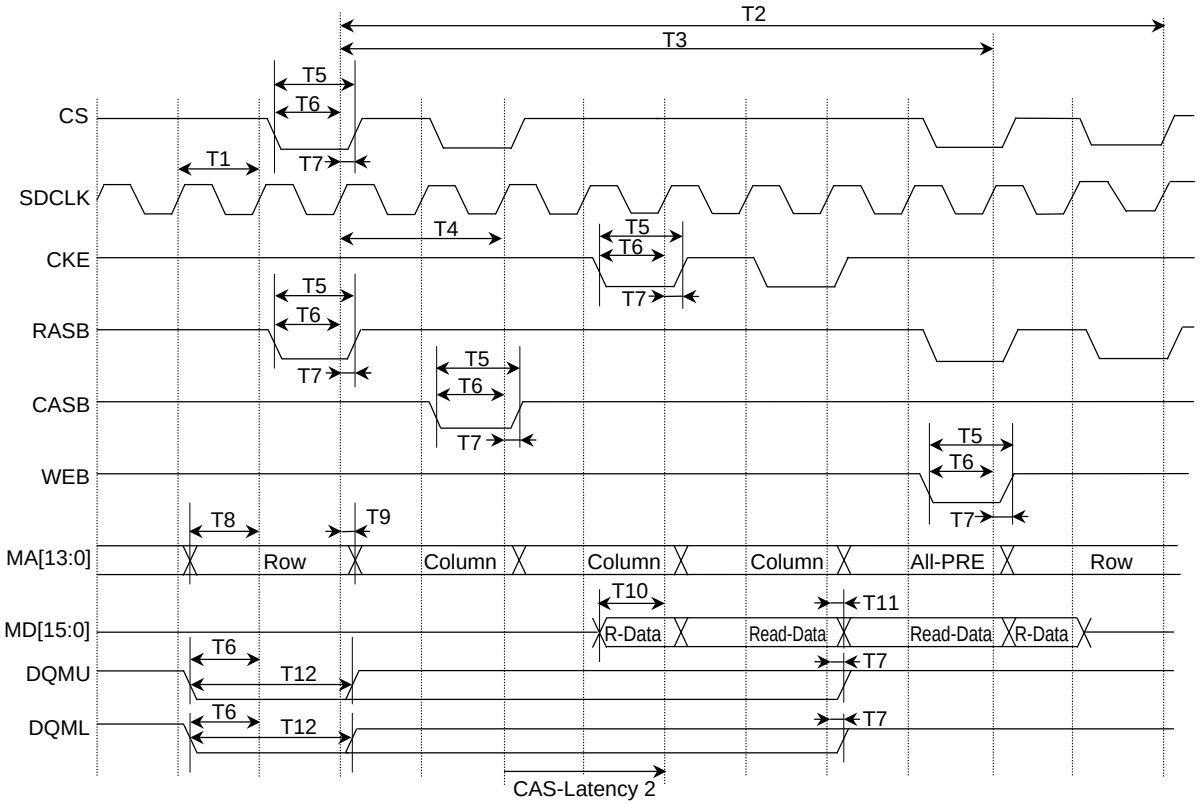


Symbol	Parameter	Ratings			Unit
		min	typ	max	
T1	RASB width high	100			ns
T2	RASB CASB delay	80			ns
T3	CASB RASB delay	40			ns
T4	CASB width low	40			ns
T5	CASB width high	40			ns
T6	Row address setup time	15			ns
T7	Row address hold time	40			ns
T8	Column address setup time	15			ns
T9	Column address hold time	40			ns
T10	OEB ready time	30			ns
T11	OEB hold time	10			ns
T12	Read data setup time	30			ns
T13	Read data hold time	0			ns
T14	WEB ready time	30			ns
T15	WEB hold time	40			ns
T16	Write data turn on time			60	ns
T17	Write data turn off time			80	ns
T18	Write data setup time	15			ns
T19	Write data hold time	40			ns
T20	Refresh cycle	300			ns
T21	RASB low width (Refresh)	200			ns
T22	RASB CASB delay (Refresh)	50			ns
T23	CASB setup time (Refresh)	40			ns
T24	CASB hold time (Refresh)	100			ns

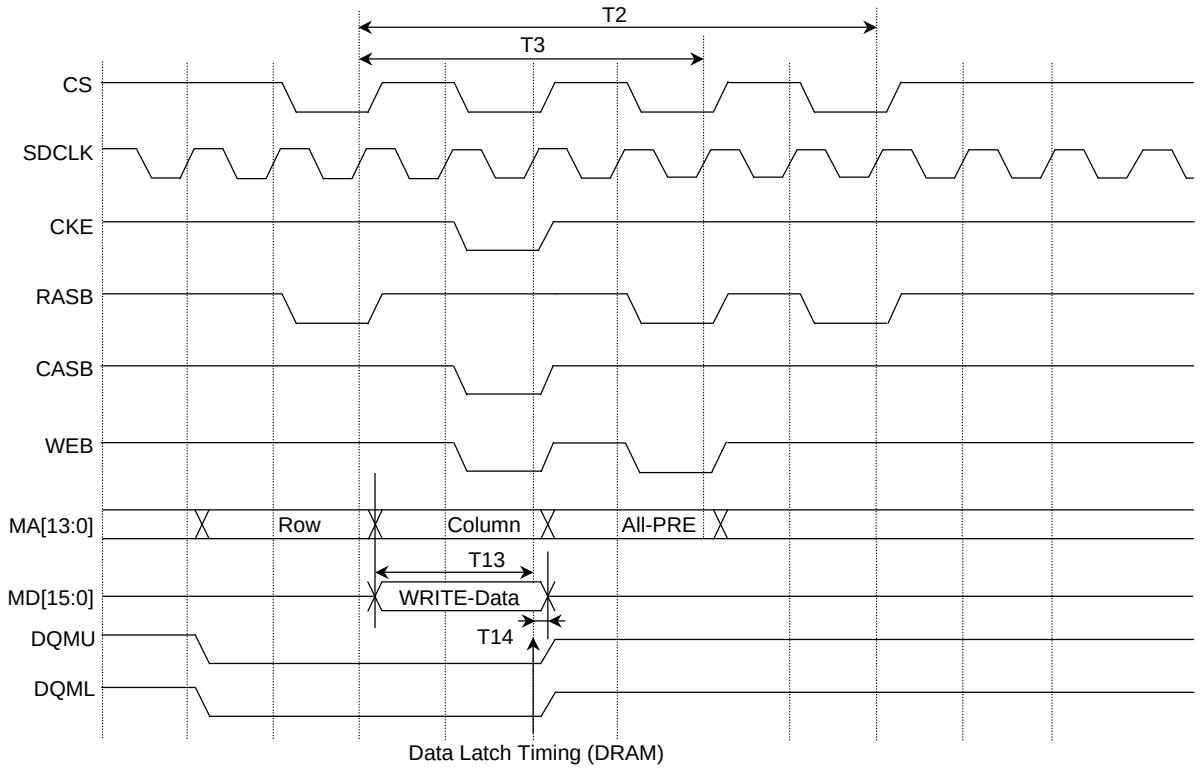
*: These values apply when the frequency of the clock input to the CKIN pin is 16.9344 MHz.

SDRAM Interface Timing

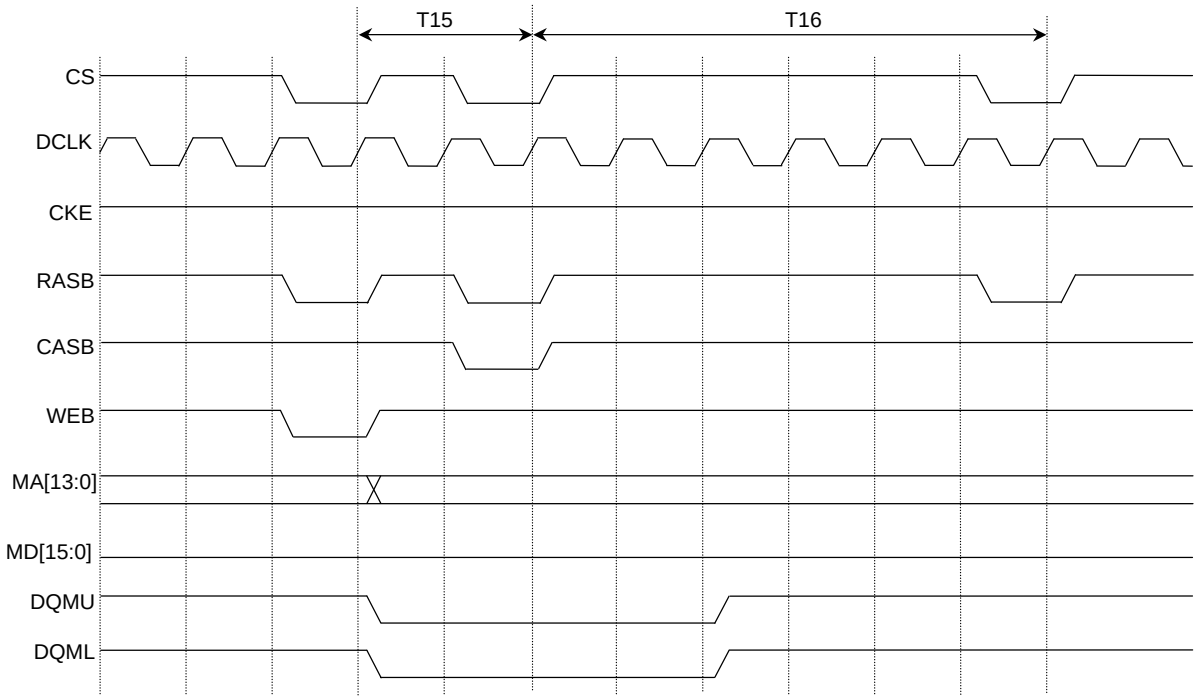
• Read Cycle



• Write Cycle



• Refresh Cycle (Auto Refresh)



*: The correspondence between the signal names used in the above diagrams (Read Cycle, Write Cycle, and Refresh Cycle) and the actual LC78684NE pin names is shown in the table below.

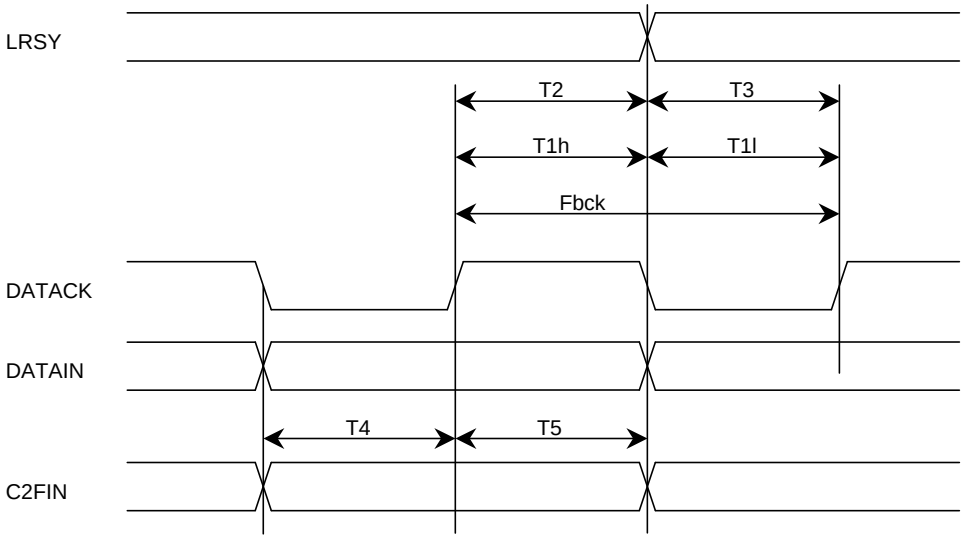
Signal name in figure	LC78684NE pin	Signal name in figure	LC78684NE pin
CS	OEB	MA [13]	CRCF
SDCLK	CASLB	MA [12:0]	MADRS [12:0]
CKE	STREQ	MD [15:0]	MDAT [15:0]
RASB	RASB	DQMU	STDAT
CASB	CASUB	DQML	STCK
WEB	WEB		

Symbol	Parameter	Ratings			Unit
		min	typ	max	
T1	SDRAM clock frequency		59		ns
T2	Active to active command period	(T1) × 6	—	—	ns
T3	Active to precharge command period (RAS to CAS delay)	(T1) × 4	—	—	ns
T4	Active to read or write delay	(T1) × 2	—	—	ns
T5	Command low-level width (CKE, RAS, CAS, WEB)	40	—	—	ns
T6	Command setup time (CKE, RAS, CAS, WEB, DQMU/L)	30	—	—	ns
T7	Command hold time (CKE, RAS, CAS, WEB, DQMU/L)	2.5	—	—	ns
T8	Address setup time	30	—	—	ns
T9	Address hold time	2.5	—	—	ns
T10	READ data setup time (DRAM: read / LC78684: input)	30	—	—	ns
T11	READ data hold time (DRAM: read / LC78684: input)	0	—	—	ns
T12	DQM low-level width (Bite-access mode)	90	—	—	ns
T13	WRITE data setup time (DRAM: write / LC78684E: output)	80	—	—	ns
T14	WRITE data hold time (DRAM: write / L78684E output)	2.5	—	—	ns
T15	Precharge to refresh command period	(T1) × 2	—	—	ns
T16	Refresh to active command period	(T1) × 6	—	—	ns

Notes: 1. These values apply when the frequency of the clock input to the CKIN pin is 16.9344 MHz.
2. The setup time and hold time values shown above are times relative to the rise of the SDCLK signal.
3. The above times are common to all of the read, write and refresh operation modes.

CD DSP Interface

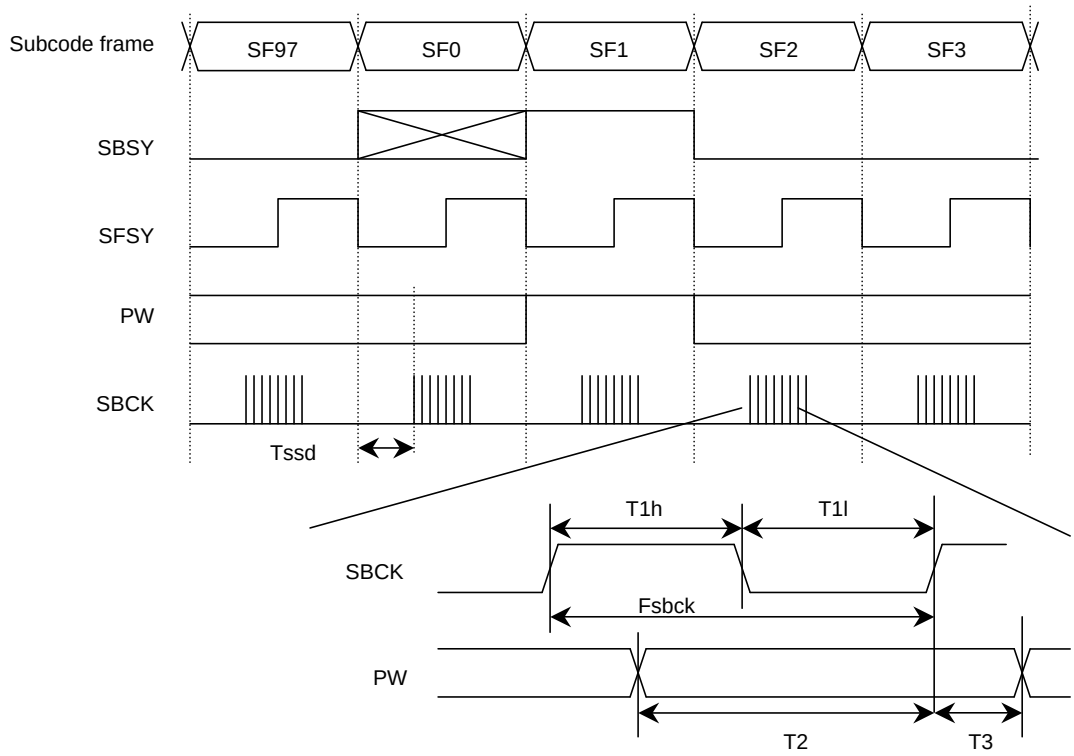
• CD DSP Interface Timing



Symbol	Parameter	Ratings			Unit
		min	typ	max	
Fbck	DATACK frequency			14.5	MHz
T1h	DATACK high-level pulse width	30			ns
T1l	DATACK low-level pulse width	30			ns
T2	LRSY setup time	30			ns
T3	LRSY hold time	30			ns
T4	DATAIN, C2FIN setup time	30			ns
T5	DATAIN, C2FIN hold time	25			ns

*: The figure above shows the timings relative to the rise of the DATACK signal. When data is latched on the fall of the DATACK signal, the setup and hold times are the same as those shown in the table above.

• Subcode Interface Timing

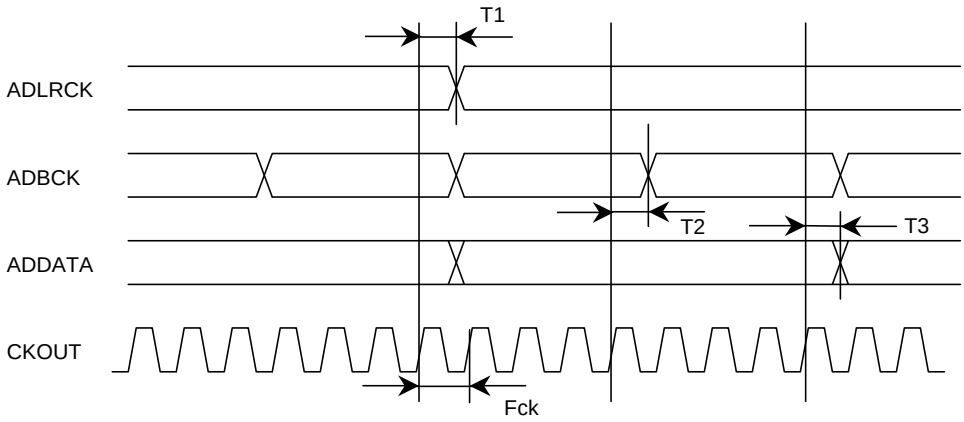


Symbol	Parameter	Ratings			Unit
		min	typ	max	
Tssd	SFSY–SBCK delay time	235		7150	ns
Fsbck	SBCK frequency *		1.0584		MHz
T1h	SBCK high-level pulse width	450			ns
T1l	SBCK low-level pulse width	450			ns
T2	PW setup time	50			ns
T3	PW hold time	0			ns

*: These values apply when the frequency of the clock input to the CKIN pin is 16.9344 MHz.

Audio Output Interface

• Audio Output Interface Timing

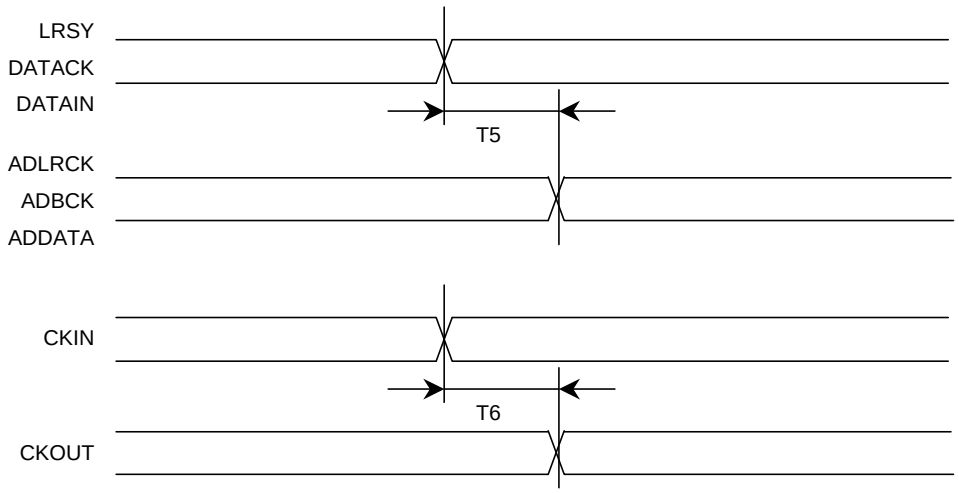


The figure above applies when the audio data output slot is a 48-bit slot.

Symbol	Parameter	Ratings			Unit
		min	typ	max	
T1	CKOUT → ADLRCK delay time	0		35	ns
T2	CKOUT → ADBCK delay time	0		35	ns
T3	CKOUT → ADDATA delay time	0		35	ns
Fck	CKOUT frequency *		16.9344		MHz

*: These values apply in MPEG1 (Fs = 44.1 kHz) playback mode when the PLL is locked normally. These values depend on the playback sampling frequency (Fs). (CKOUT frequency = Fs × 384)

• Supplement: Output Timing in Full Through Mode Playback



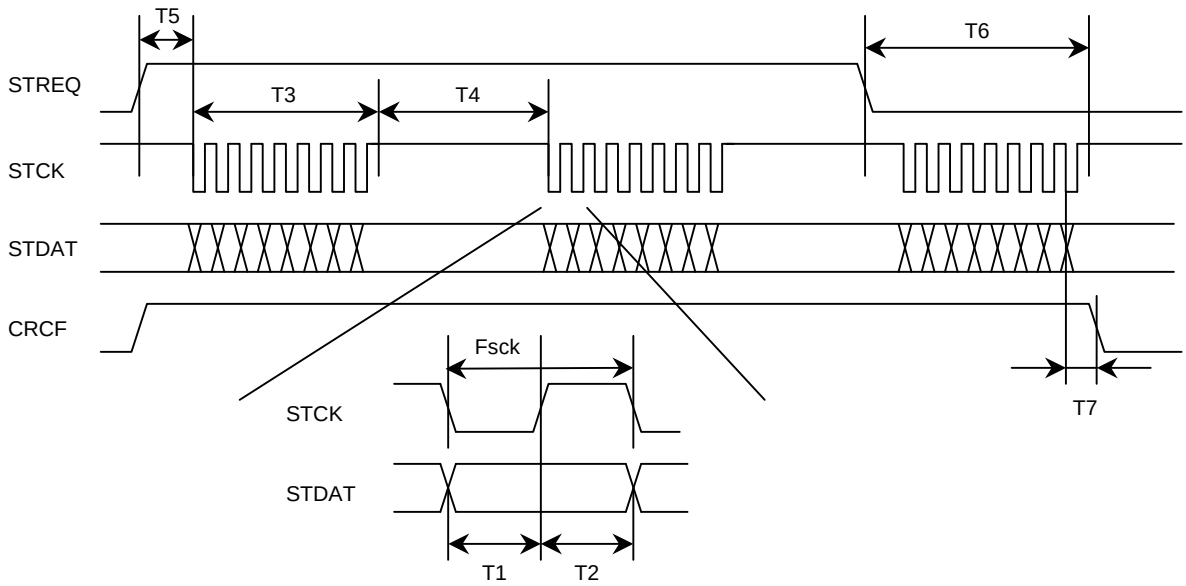
*: Full through mode is the mode where the THROUGH bit (bit 6 in register 60h) is set to 1.

Symbol	Parameter	Ratings			Unit
		min	typ	max	
T5	INPUT → OUTPUT delay time	0		35	ns
T6	CKIN → CKOUT delay time *	0		35	ns

*: These values apply when the CKIN pin input is directly output from the CKOUT pin.

Data Serial I/O Interface

• DRAM Data Serial Output Timing



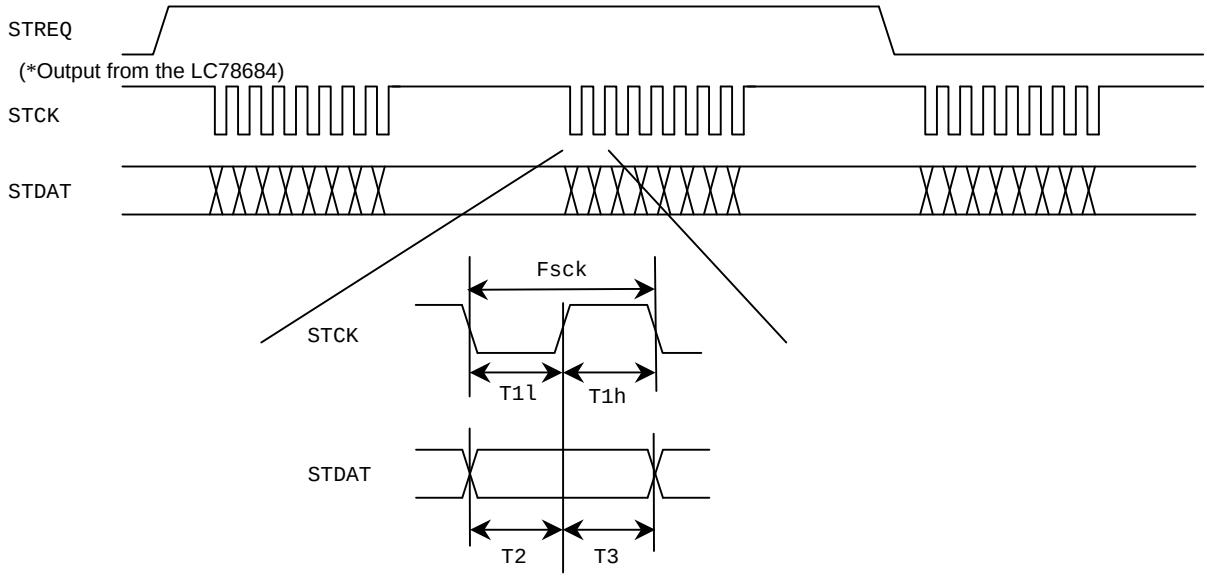
*: When EDO DRAM is used, a transfer data command from DRAM must be issued first to output data from DRAM. (This function cannot be used with SDRAM.)
If this command has not been issued, the clock and data signals will not be output from the STCK and STDAT pins even if STREQ is set high.

Symbol	Parameter	Ratings			Unit
		min	typ	max	
Fsck	Transfer clock frequency		4.2336		MHz
T1	STDAT/STCK setup time	30			ns
T2	STDAT/STCK hold time	30			ns
T3	Data (1 byte) transfer time		1.89		µs
T4	Data transfer wait time		1.89		µs
T5	Data transfer start time	1.89		15.2	µs
T6	Data transfer stop time	0		15.2	µs
T7	Enable flag turn off time	210	236.2	270	ns

*1: The typical values apply when the frequency of the clock signal input to the CKIN pin is 16.9344 MHz.
*2: There are cases in data transfer operations where between a minimum of 0 bytes and a maximum of 4 bytes of data are output from the STDAT pin after the STREQ pin goes low. The period T6 in the figure above stipulates this time.
*3: The T7 stipulation in the figure above applies when one or more bytes of data are output from the STDAT pin after the STREQ pin goes low. The timing with which the CRCF pin goes low when data output from the STDAT does not occur is the same as the timing with which STREQ goes low.

- The Fsck clock frequency can also be set to 2.1168 MHz (typical), 1.084 MHz (typical).
  In these cases, the values for T3 to T7 will be 2 times or 4 times the listed values.
- The WOK, OVF, and CNTOK pins can be used in place of STREQ (input mode), STCK, and STDAT. The above timing specifications apply in this case as well.

• MP3 Data Serial Input Timing



*: For data serial input, if EDO DRAM is used, a serial input command must have been issued. (This function cannot be used with SDRAM.)
If this command has not been issued, the MP3 decoder will not operate, even if clock and data signals are input to the STCK and STDAT pins.

Symbol	Parameter	Ratings			Unit
		min	typ	max	
Fsck	Transfer clock frequency *			9.216	MHz
T1h	STCK high-level pulse width	45			ns
T1l	STCK low-level pulse width	45			ns
T2	STDAT / STCK setup time	30			ns
T3	STDAT / STCK hold time	30			ns

*: The maximum frequencies of the transfer clock signal during serial input are listed in the following table.

MODE	Fs (KHz)	Maximum serial transfer clock frequency (MHz)
MPEG1	48	9.216
	44.1	8.4672
	32	6.144
MPEG2 (MPEG2.5)	24 (12)	4.608
	22.05 (11.025)	4.2336
	16 (8)	3.072

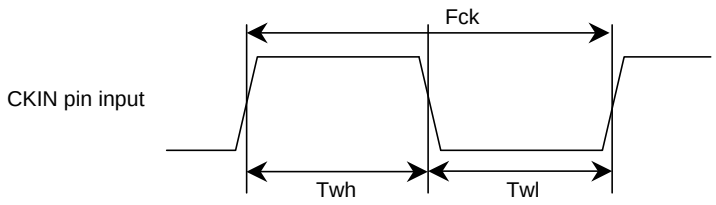
Determine the frequency of the transfer clock such that the frequency is below the maximum frequency listed above and the MP3 decoding processing is performed in time.

Note that the values in the table above apply when MP3DSET (bit 0 in register 41h) is set to 1 (high-speed transfer mode).
If MP3DSET is set to 0 (low-speed transfer mode) the following timings apply.

Symbol	Parameter	Ratings			Unit
		min	typ	max	
Fsck	Transfer clock frequency			3.072	MHz
T1h	STCK high-level pulse width	150			ns
T1l	STCK low-level pulse width	150			ns
T2	STDAT / STCK setup time	125			ns
T3	STDAT / STCK hold time	125			ns

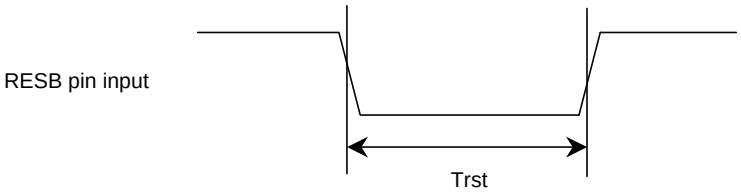
*2: The LC78684NE can receive up to a maximum of 3 bytes of data even after the STREQ pin has gone low.

System Clock Input



Symbol	Parameter	Ratings			Unit
		min	typ	max	
Fck	CKIN input frequency		16.9344	18.0	MHz
Twh	CKIN high-level pulse width	20			ns
Twl	CKIN low-level pulse width	20			ns

System Reset Input



Symbol	Parameter	Ratings			Unit
		min	typ	max	
Trst	System reset pulse width	1			µs

*: A system reset must be applied after power is first applied.
The reset line must be designed so that noise does not occur on the reset signal.

Pin Functions

Block	No.	Pin	I/O	Supplement
CD IF	1	LRSY	I	CD left/right clock input
Audio interface	2	ADDATA	O	Audio data output
	3	ADBCK	O	Audio bit clock output
	4	ADLRCK	O	Audio left/right clock output
CD IF	5	C2FIN	I	CD C2 error flag input
Test	6	TEST1	I	Test input 1 (This pin must be connected to ground.)
CLOCK	7	CKIN	I	System clock (16.9344 MHz) input
Power supply	8	VSS	—	Ground
CLOCK	9	CKOUT	O	External digital filter and D/A converter clock output (384 Fs)
Test	10	TEST2	I	Test input 2 (This pin must be connected to ground.)
Power supply	11	DVDD1	—	Digital system power supply (I/O)
Subcode interface	12	PW	I	CD subcode data serial input
	13	SBSY	I	CD subcode block sync signal input
	14	SFSY	I	CD subcode frame sync signal input
	15	SBCK	O	CD subcode transfer serial clock output
Power supply	16	AVDD	—	Analog system power supply (PLL)
PLL	17	VPRFR	—	VCO oscillator range setting
	18	VCOC	I	VCO control voltage input
	19	VPDO	O	VCO charge pump output
Power supply	20	AVSS	—	Analog system ground
	21	DVDD2	—	Internal logic system power supply
	22	VSS	—	Ground
Memory interface	23	MDATA0	I/O	DRAM data bus0
	24	MDATA1	I/O	DRAM data bus1
	25	MDATA2	I/O	DRAM data bus2
	26	MDATA3	I/O	DRAM data bus3
	27	MDATA4	I/O	DRAM data bus4
	28	MDATA5	I/O	DRAM data bus5
	29	MDATA6	I/O	DRAM data bus6
	30	MDATA7	I/O	DRAM data bus7
Power supply	31	DVDD3	—	Digital system power supply (I/O)
	32	VSS	—	Ground
Memory interface	33	MDATA8	I/O	DRAM data bus8
	34	MDATA9	I/O	DRAM data bus9
	35	MDATA10	I/O	DRAM data bus10
	36	MDATA11	I/O	DRAM data bus11
	37	MDATA12	I/O	DRAM data bus12
	38	MDATA13	I/O	DRAM data bus13
	39	MDATA14	I/O	DRAM data bus14
	40	MDATA15	I/O	DRAM data bus15
	41	RASB	O	RAS output for EDO DRAM or SDRAM (active low)
	42	WEB	O	WE output for EDO DRAM or SDRAM (active low)
	43	CASLB	O	When EDO DRAM is used: CAS output (lower byte, active low)
				When SDRAM is used: DRAM clock output
	44	CASUB	O	When EDO DRAM is used: CAS output (upper byte, active low)
				When SDRAM is used: CAS output (active low)
	45	OEB	O	When EDO DRAM is used: OE output (active low)
				When SDRAM is used: CS output (active low)
	46	MADRS12	O	DRAM address output 12
	47	MADRS11	O	DRAM address output 11
	48	MADRS10	O	DRAM address output 10
	49	MADRS9	O	DRAM address output 9
	50	MADRS8	O	DRAM address output 8
Power supply	51	DVDD4	—	Digital system power supply (I/O)
	52	VSS	—	Ground

Continued on next page.

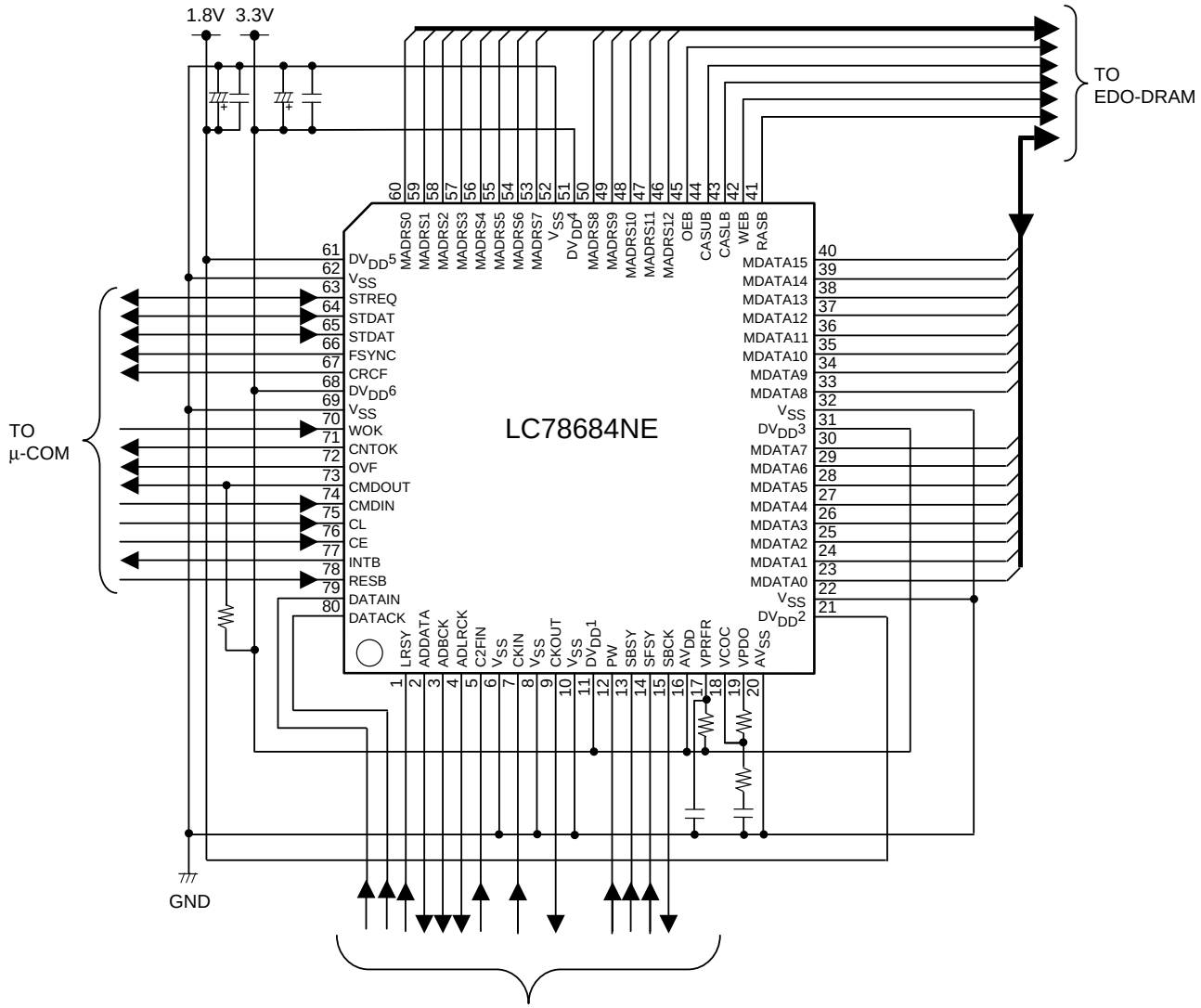
Continued from preceding page.

Block	No.	Pin	I/O	Supplement
Memory interface	53	MADRS7	O	DRAM address output 7
	54	MADRS6	O	DRAM address output 6
	55	MADRS5	O	DRAM address output 5
	56	MADRS4	O	DRAM address output 4
	57	MADRS3	O	DRAM address output 3
	58	MADRS2	O	DRAM address output 2
	59	MADRS1	O	DRAM address output 1
	60	MADRS0	O	DRAM address output 0
Power supply	61	DVDD5	—	Internal logic system power supply
	62	VSS	—	Ground
MP3 stream	63	STREQ	I/O	When EDO DRAM is used: MP3 data request flag output (active high)/DRAM data request flag input (in CD ROM mode: active high)
				When SDRAM is used: CKE output (active low)
I/O	64	STCK	I/O	When EDO DRAM is used: MP3 data transfer clock input/DRAM data transfer clock output
				When SDRAM is used: DQML output (active low)
	65	STDAT	I/O	When EDO DRAM is used: MP3 data serial input/DRAM data serial output
				When SDRAM is used: DQMH output (active low)
MP3 decoder	66	FSYNC	O	MP3 frame sync signal (active high) Data continuity point detection complete flag (CD-DA mode, active high)
CD monitor	67	CRCF	O	When EDO DRAM is used: CRC check (CD ROM data/CD-DA subcode data) result output (active high)/DRAM data output enable flag (active high)
				When SDRAM is used: ADRS13 output
Power supply	68	DVDD6	—	Digital system power supply (I/O)
	69	VSS	—	Ground
Anti-shock/MP3 I/O	70	WOK	I	DRAM write enable input (CD-DA mode, active high) DRAM data request flag input (only when EDO DRAM is used)
	71	CNTOK	O	Data continuity point detection complete flag (CD-DA mode, active high) SYNC error monitor flag (MP3 mode, active high) DRAM data serial output (only when EDO DRAM is used:)
	72	OVF	O	DRAM write interrupted flag (CD-DA mode, active high) Emphasis output flag (CD-DA and MP3 modes, active high) DRAM data transfer clock output (only when EDO DRAM is used)
Microcontroller interface	73	CMDOUT	O	Command serial data output (This is an n-channel open-drain output.)
	74	CMDIN	I	Command serial data input
	75	CL	I	Command serial clock input
	76	CE	I	Command enable input (active high)
	77	INTB	O	Interrupt signal output (active low) DRAM write interrupted flag (CD-DA mode, active high)
	78	RESB	I	System reset (active low)
CD IF	79	DATAIN	I	CD serial data input
	80	DATACK	I	CD bit clock input

Note: 1. Notes on unused ports
Unused input pins must be connected to ground (0 V).
Unused output pins must be left open. Do not connect anything to these pins.
Unused I/O pins must either be connected to ground (0 V) or be left open.
2. The same potential must be supplied to all of the DVDD1, DVDD3, DVDD4, DVDD6, and AVDD pins. The same potential must also be supplied to the DVDD2 and DVDD5 pins.
(See the Allowable Operating Ranges section for details on the voltage supplied.)
3. The input pins TEST1 and TEST2 must be connected to ground (0 V).
4. The I/O pins (MDATA0 to MDATA15, STREQ, STCK, and STDAT) are set to input mode by the initial system reset.
5. Applications must apply a low level (of at least 1 µs) to the RESB after power is first applied.
6. A clock signal with a frequency of 16.9344 MHz must applied to the CKIN pin from the CD DSP IC or other source.
An oscillator circuit cannot be formed with just this IC and an oscillator element.

Application Circuit Examples

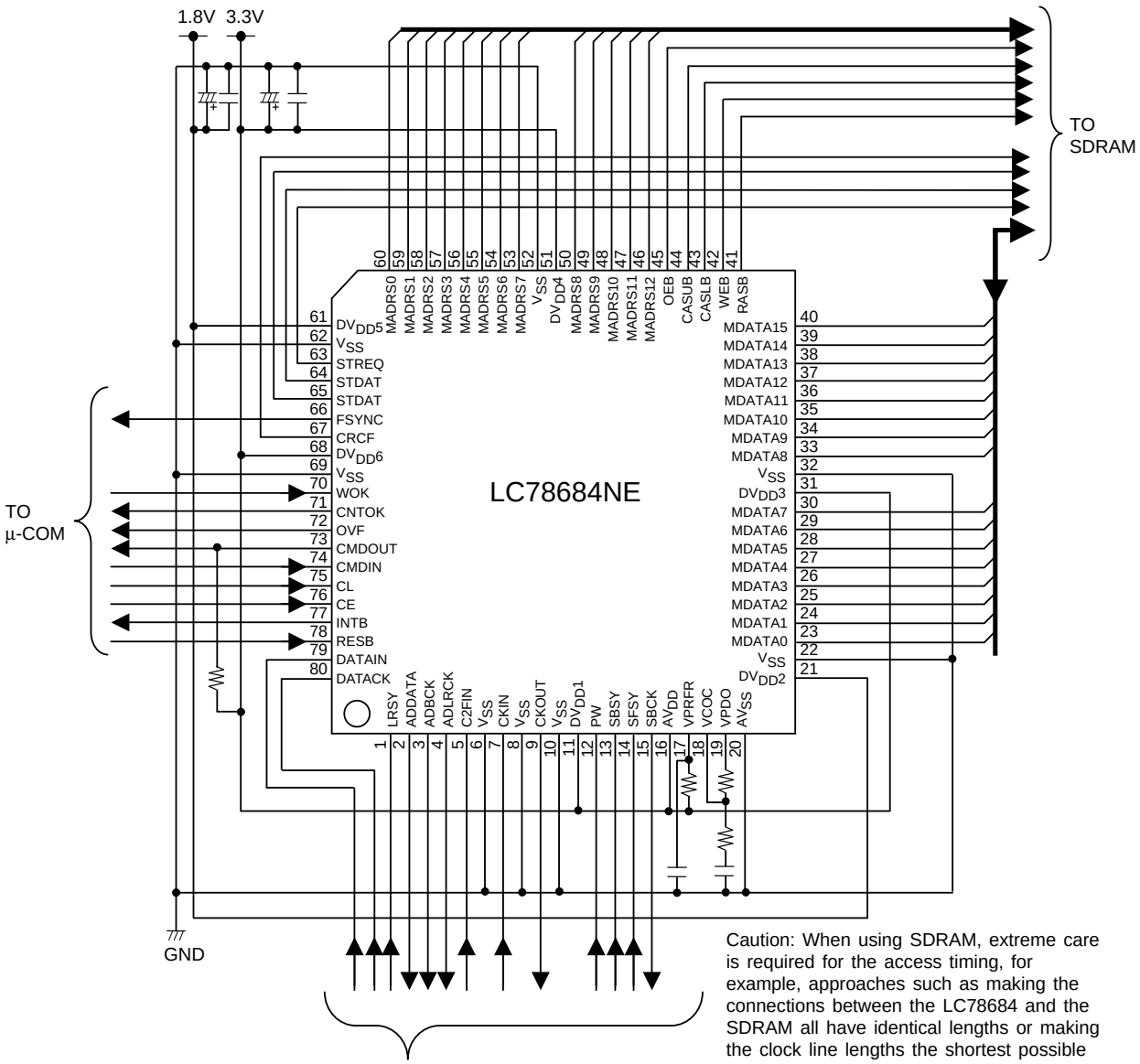
(1) Using EDO DRAM



To the CD DSP

*: The CKOUT, ADLRCK, ADBCK, and ADDATA pins must be connected to a CD DSP that supports D/A converter external input.
An external D/A converter is required if the CD DSP does not provide this support.

(2) Using SDRAM



Application Design Notes

While it goes without saying that strictly observing the absolute maximum ratings and allowable operating ranges (recommended operating conditions) for this IC is necessary for application reliability, careful consideration must also be given to the ambient temperature, static discharge, and other environmental conditions as well as the mounting conditions. This section presents notes regarding application design and circuit board mounting for this IC.

1. Handling unused pins
   If any unused input pins on this IC are left open, internal circuits may become unstable. The instructions on handling unused pins for specific pins given in the technical documentation must be followed. Also note that unused output pins must not be shorted to power, ground, or other outputs.

2. Latchup prevention
   (1) The voltages stipulated in the specifications must be applied to the power supply pins. If there are multiple power supply pins that are stipulated to have the same voltage, the identical potential must be applied to all those pins.
   (2) The voltage levels on I/O pins must not exceed the peripheral 3 V system block supply voltage, and must not go below the ground level.
   (3) Design applications so that overvoltages and abnormal noise are not applied to this IC.
   (4) In general, latchup can be prevented by holding unused input pins fixed at either VDD or VSS. However, the handling of each pin must follow an specific instruction in the pin functions documentation.
   (5) The outputs must not be shorted.

3. Interface
   When connected to other devices, this IC may not operate correctly if the input VIL/VIH and output VOL/VOH levels do not match. When connecting this IC to other devices in dual power supply systems, level shifters must be inserted to prevent the device from being destroyed.

4. Load capacitance and output current
   (1) When connected to high capacitance loads, lines may be melted since the effect of such loads is the same as the load being shorted for an extended period. Also, large charge/discharge currents may result in noise that may degrade equipment performance and cause malfunctions. The recommended load capacitance ratings must be observed.
   (2) Excessive output sink or source current can cause problems. Observe the maximum allowable power dissipation ratings and use this IC within the recommended current value range.

5. Notes on power application and power-on reset
   (1) There are cases where special care is required at power on, during a reset, and after a reset is cleared. Refer to spec sheets and other documentation and design applications taking these concerns into account.
   (2) This IC's output pin states, I/O settings, and register values are not guaranteed when power is first applied. The operation of items that are defined by a reset operation or mode settings is only guaranteed after the corresponding reset or setting operation. A reset must be applied to this IC after power is first applied. The states immediately after power on of pins and registers that are not explicitly defined cannot be relied on: they may differ either due to long-term variations in a given device or due to design changes in later versions of the same product.

6. Notes on thermal design
   The failure rate of semiconductor devices is accelerated greatly by increases in ambient temperature or power consumption. To assure high reliability, design the application heat dissipation systems to provide adequate margin for variations in ambient conditions.

7. Notes on PWB pattern design
   (1) Ideally, there should be separate power supply and ground lines for each system to reduce the influence of shared impedances.
   (2) The power supply and ground lines should be as wide and as short as possible, and the impedance to high frequencies should be as small as possible.
   Insert both decoupling capacitors (of about 0.01 to 1 μF) and capacitors of about 100 to 200 μF between each power supply/ground pair. However, note that if these capacitors are too large, latchup may occur.

8. Other notes
   If there are any points that are unclear, or if you have any questions, contact your Sanyo representative during the design phase.
   This IC is a special-purpose device designed for CD player applications, and has specifications that differ from those of general-purpose logic devices. End products must be designed to operate in a failsafe manner appropriate for the application, and application operation must be verified using test equipment.