

# NLX1G99

## Configurable Multifunction Gate

The NLX1G99 MiniGate™ is an advanced high-speed CMOS multifunction gate with a 3-state output. With the output enable input ( $\overline{OE}$ ) at High, the output is disabled and is kept at high impedance. With the output enable input ( $\overline{OE}$ ) at Low, the device can be configured for logic functions such as MUX, AND, OR, NAND, NOR, XOR, XNOR, INVERT and BUFFER, depending on the combination of the 4-bit input. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

The NLX1G99 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

### Features

- High Speed:  $t_{PD} = 6.7$  ns (Max) @  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 1$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

### PIN ASSIGNMENT

1	$\overline{OE}$
2	A
3	B
4	GND
5	C
6	D
7	Y
8	$V_{CC}$



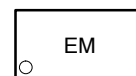
**ON Semiconductor®**

<http://onsemi.com>

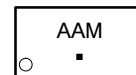
### MARKING DIAGRAMS



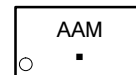
**ULLGA8**  
1.45 x 1.0  
CASE 613AA



**ULLGA8**  
1.6 x 1.0  
CASE 613AB

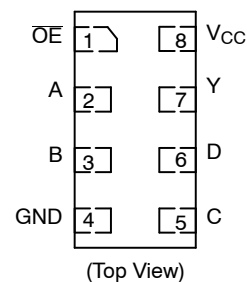


**ULLGA8**  
1.95 x 1.0  
CASE 613AC



AA or E = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

### PIN ASSIGNMENTS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

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## FUNCTION DIAGRAM

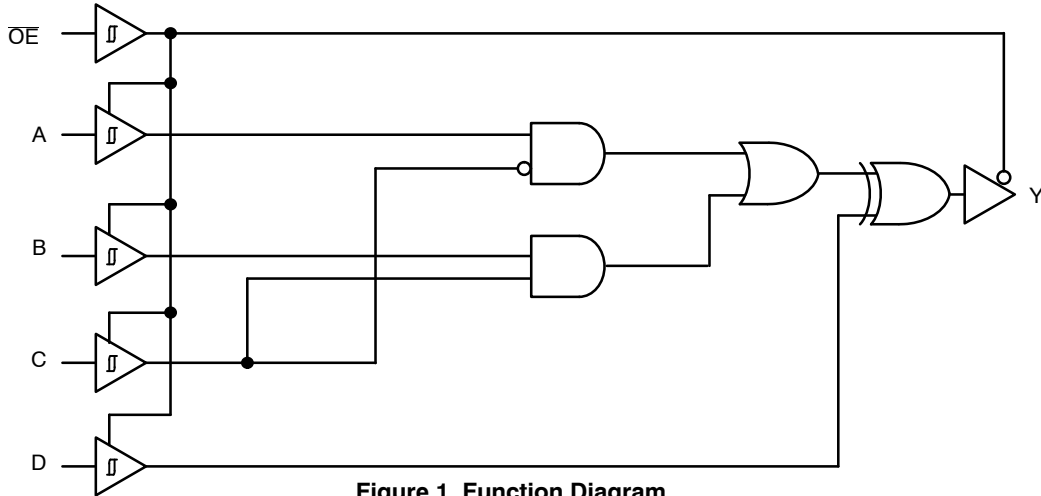


Figure 1. Function Diagram

## FUNCTION TABLE\*

INPUT					OUTPUT
OE	D	C	B	A	Y
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	L
H	H or L	H or L	H or L	H or L	Z

\*To select a logic function, please refer to "Logic Configurations" section.

FUNCTION SELECTION	LOGIC CONFIGURATION PAGE
3-State Buffers	3
3-State Inverters	3
3-State MUXes	3
3-State AND / OR / NOR	4
3-State NAND / OR	5
3-State XOR/XNOR	6

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## LOGIC CONFIGURATIONS

### 3-State Buffer Functions Available

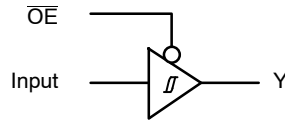


Figure 2.

Function	$\overline{OE}$	A	B	C	D
3-State Buffer	L	Input H or L L H H H or L L	H or L Input H L H or L L L	L H Input Input L H H or L	L L L H Input Input Input

### 3-State Inverter Functions Available

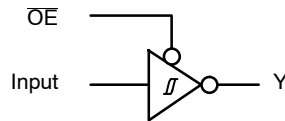


Figure 3.

Function	$\overline{OE}$	A	B	C	D
3-State Buffer	L	Input X L H H H or L H	H or L Input H L H or L H H	L H Input Input L H H or L	H H H L Input Input Input

### 3-State MUX Functions Available

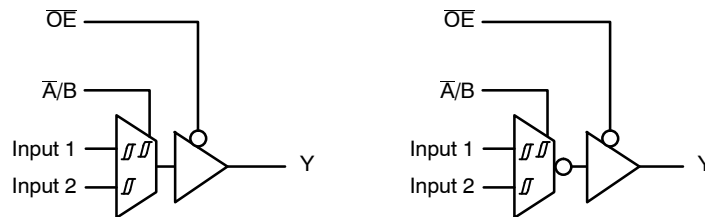


Figure 4.

Function	$\overline{OE}$	A	B	C	D
3-State 2-to-1	L	Input 1	Input 2	$\overline{\text{Input 1}}$ or Input 2	L
3-State 2-to-1		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	L
3-State 2-to-1, Inverted Out		Input 1	Input 2	$\overline{\text{Input 1}}$ or Input 2	H
3-State 2-to-1, Inverted Out		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	H

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## 3-State AND/NOR/OR Function Available

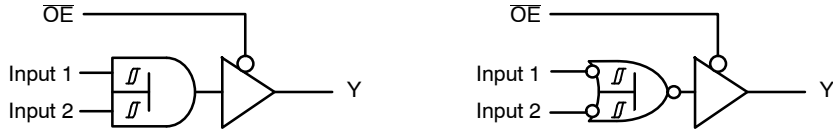


Figure 5.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	L	Input 1	Input 2	L
2	3-State AND	3-State NOR		L	Input 2	Input 1	L

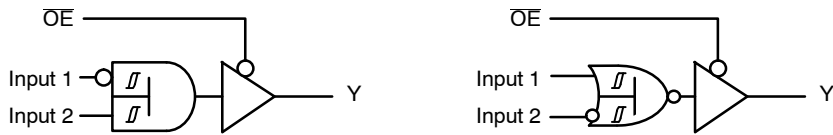


Figure 6.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	Input 2	L	Input 1	L
2	3-State AND	3-State NOR		H	Input 1	Input 2	H

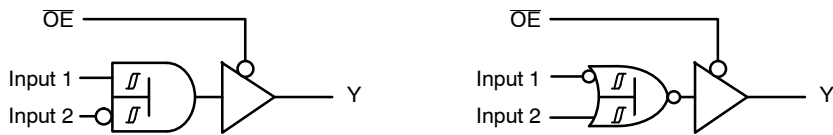


Figure 7.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	Input 1	L	Input 2	L
2	3-State AND	3-State NOR		H	Input 2	Input 1	H

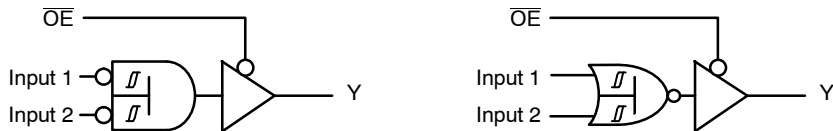


Figure 8.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State OR	L	Input 1	H	Input 2	L
2	3-State AND	3-State OR		Input 2	H	Input 1	L

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## 3-State NAND/OR Function Available

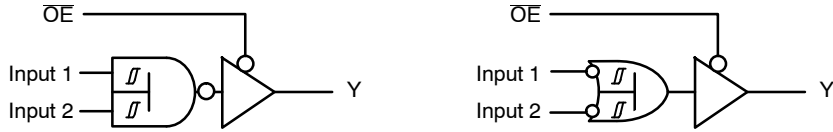


Figure 9.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	L	Input 1	Input 2	H
2	3-State NAND	3-State OR		L	Input 2	Input 1	H

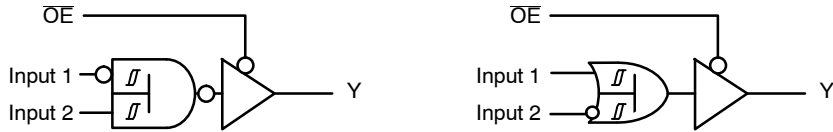


Figure 10.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	Input 2	L	Input 1	H
2	3-State NAND	3-State OR		H	Input 1	Input 2	L

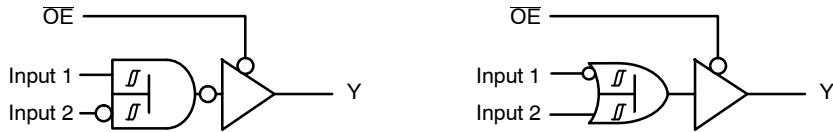


Figure 11.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	Input 1	L	Input 2	H
2	3-State NAND	3-State OR		H	Input 2	Input 1	L

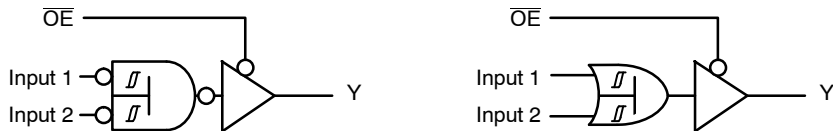


Figure 12.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State OR	L	Input 1	H	Input 2	L
2	3-State AND	3-State OR		Input 2	H	Input 1	L

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## 3-State XOR/XNOR Function Available

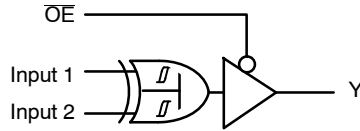


Figure 13.

Function	OE	A	B	C	D
3-State XOR	L	Input 1 Input 2 H or L H or L L L	H or L H or L Input 1 Input 2 H H	L L H H Input 1 Input 2	Input 2 Input 1 Input 2 Input 1 Input 2 Input 1

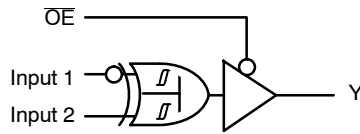


Figure 14.

Function	OE	A	B	C	D
3-State XOR	L	H	L	Input 1	Input 2

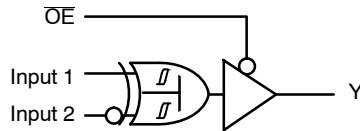


Figure 15.

Function	OE	A	B	C	D
3-State XOR	L	H	L	Input 1	Input 2

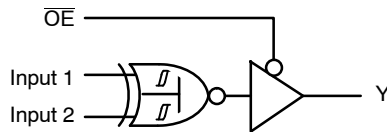


Figure 16.

Function	OE	A	B	C	D
3-State XNOR	L	H	L	Input 1	Input 2
3-State XNOR	L	H	L	Input 1 Input 2	Input 2 Input 1

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>OUT</sub>	DC Output Voltage	-0.5 to +7.0	V
I <sub>IK</sub>	DC Input Diode Current V <sub>IN</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current V <sub>OUT</sub> < GND	-50	mA
I <sub>O</sub>	DC Output Source/Sink Current	± 50	mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	± 100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	± 100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I <sub>LATCHUP</sub>	Latchup Performance Above V <sub>CC</sub> and Below GND at 125°C (Note 5)	± 500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage	1.65	5.5	V
V <sub>IN</sub>	Digital Input Voltage	0	5.5	V
V <sub>OUT</sub>	Output Voltage	0	5.5	V
T <sub>A</sub>	Operating Free-Air Temperature	-55	+125	°C
Δt / ΔV	Input Transition Rise or Fall Rate V <sub>CC</sub> = 2.5 V ± 0.2 V V <sub>CC</sub> = 3.3 V ± 0.3 V V <sub>CC</sub> = 5.0 V ± 0.5 V	0 0 0	No Limit No Limit No Limit	nS/V

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		T <sub>A</sub> ≤ +85°C		T <sub>A</sub> = -55°C to +125°C		Unit	
				Min	Max	Min	Max	Min	Max		
				V <sub>T+</sub>	Positive Threshold Voltage		1.65 2.3 3.0 4.5 5.5	0.79 1.11 1.5 2.16 2.61	1.16 1.56 1.87 2.74 3.33		
V <sub>T-</sub>	Negative Threshold Voltage		1.65 2.3 3.0 4.5 5.5	0.35 0.58 0.84 1.41 1.78	0.62 0.87 1.19 1.9 2.29	0.35 0.58 0.84 1.41 1.78		0.35 0.58 0.84 1.41 1.78		0.35 0.58 0.84 1.41 1.78	V
V <sub>H</sub>	Hysteresis Voltage		1.65 2.3 3.0 4.5 5.5	0.30 0.40 0.53 0.71 0.8	0.62 0.8 0.87 1.04 1.2	0.30 0.40 0.53 0.71 0.8	0.62 0.8 0.87 1.04 1.2	0.30 0.40 0.53 0.71 0.8	0.62 0.8 0.87 1.04 1.2	V	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OH</sub> = -50 μA	1.65-5.5	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		V	
		V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA I <sub>OH</sub> = -16 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -32 mA	1.65 2.3 3.0 3.0 4.5	1.2 1.9 2.4 2.3 3.8		1.2 1.9 2.4 2.3 3.8		1.2 1.9 2.4 2.3 3.8		V	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OL</sub> = 50 μA	1.65-5.5		0.1		0.1		0.1	V	
		V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 32 mA	1.65 2.3 3.0 3.0 4.5	0.45 0.3 0.4 0.55 0.55		0.45 0.3 0.4 0.55 0.55		0.45 0.3 0.4 0.55 0.55		0.45 0.3 0.4 0.55 0.55	V
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0 - 5.5		±0.1		±1.0		±1.0	μA	
I <sub>off</sub>	Power off Leakage Current	V <sub>IN</sub> or V <sub>O</sub> = 5.5 V	0		±1.0		±10		±10	μA	
I <sub>OZ</sub>	Tri-state Output Leakage Current	V <sub>O</sub> = V <sub>CC</sub> or GND	1.65-5.5		±1.0		±10		±10	μA	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	1.65-5.5		1.0		10		10	μA	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> Per Input	One input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND	3 - 5.5		10		100		100	μA	



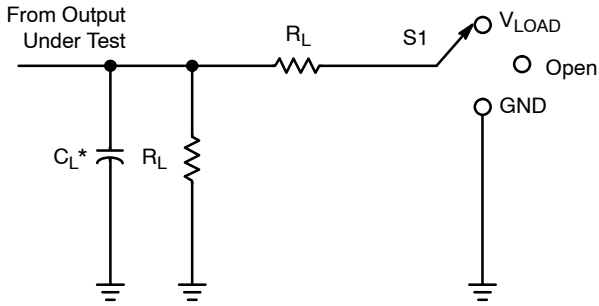
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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V <sub>CC</sub> (V)	Test Condition	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.3	12.8	25.1	4.3	25.1	4.3	25.1	ns
				2.4	7.1	10.2	2.4	10.2	2.4	10.2	
				1.7	5.2	6.7	1.7	6.9	1.7	7.0	
				1.3	4.0	4.5	1.3	4.9	1.3	5.0	
t <sub>EN</sub>	Output Enable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	3.4		24.7	3.4	24.7	3.4	24.7	ns
				2.1		11	2.1	12	2.1	12.2	
				1.3		7.5	1.3	8.0	1.3	8.3	
				1.0		5.7	1.0	6.2	1.0	6.5	
t <sub>DIS</sub>	Output Disable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.0		15.5	4.0	15.5	4.0	15.5	ns
				2.7		7.5	2.7	7.5	2.7	7.5	
				3.5		7.0	3.5	7.0	3.5	7.0	
				2.0		5.5	2.0	5.5	2.0	5.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.3	13.6	25.7	4.3	25.7	4.3	25.7	ns
				2.5	7.8	10.7	2.5	10.7	2.5	10.7	
				2.3	5.6	7.6	2.3	7.6	2.3	7.6	
				1.6	4.4	5.2	1.6	5.2	1.6	5.2	
t <sub>EN</sub>	Output Enable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.2		25.2	4.2	25.2	4.2	25.2	ns
				2.4		11.3	2.4	12.2	2.4	13	
				2.0		8.0	2.0	8.5	2.0	8.7	
				1.7		6.0	1.7	6.5	1.7	6.7	
t <sub>DIS</sub>	Output Disable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	3.7		15	3.7	15	3.7	15	ns
				2.0		6.5	2.0	6.7	2.0	6.9	
				2.1		5.6	2.1	5.8	2.1	5.9	
				1.0		4.5	1.0	4.7	1.0	4.9	
C <sub>IN</sub>	Input Capacitance	3.3			3.5					pF	
C <sub>O</sub>	Output Capacitance	3.3			6.0					pF	
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	3.3	f = 10 MHz		22					pF	

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ . C<sub>PD</sub> is used to determine the no-load dynamic power consumption:  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

TEST CIRCUIT AND VOLTAGE WAVEFORMS



\* $C_L$  includes probes and jig capacitance.

Figure 17. Load Circuit

Test	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	Inputs		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
$5.5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.3 V

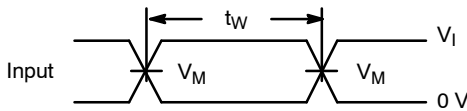


Figure 18. Voltage Waveforms Pulse Duration

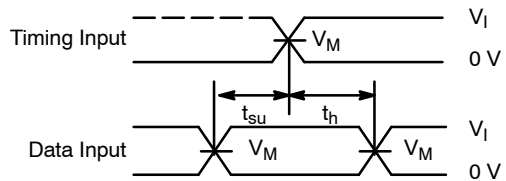


Figure 19. Voltage Waveforms Setup and Hold Times

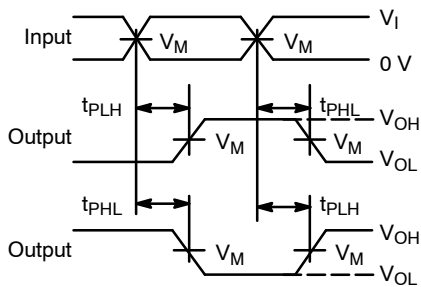


Figure 20. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

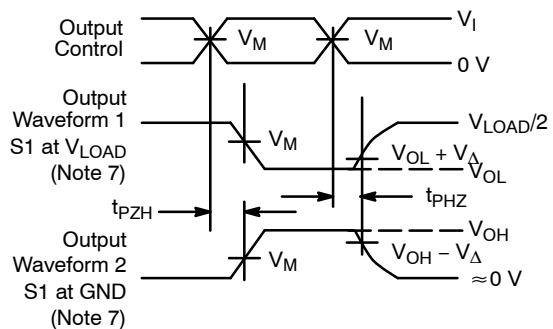
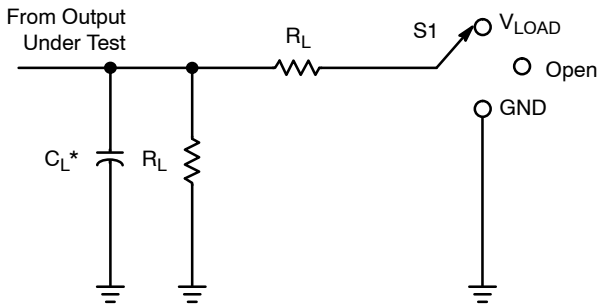


Figure 21. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

7. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
8. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
9. The outputs are measured one at a time, with one transition per measurement.
10. All parameters are waveforms are not applicable to all devices.

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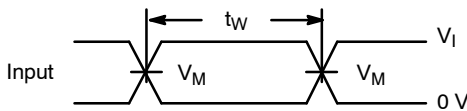


\*C<sub>L</sub> includes probes and jig capacitance.

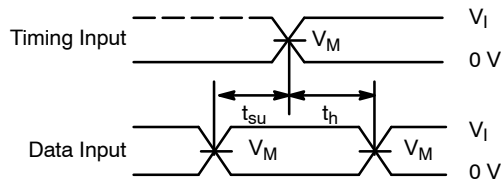
**Figure 22. Load Circuit**

Test	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

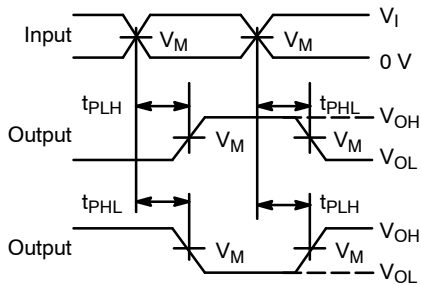
V <sub>CC</sub>	Inputs		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>					
1.8 V ± 0.15 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 x V <sub>CC</sub>	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 x V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5.5 V ± 0.5 V	V <sub>CC</sub>	≤ 2.5 ns	V <sub>CC</sub> /2	2 x V <sub>CC</sub>	50 pF	500 Ω	0.3 V



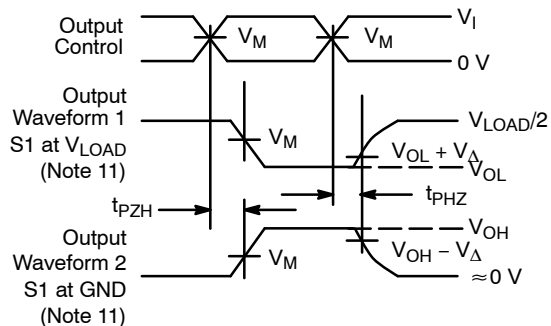
**Figure 23. Voltage Waveforms Pulse Duration**



**Figure 24. Voltage Waveforms Setup and Hold Times**



**Figure 25. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs**



**Figure 26. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling**

- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
- The outputs are measured one at a time, with one transition per measurement.
- All parameters are waveforms are not applicable to all devices.

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## ORDERING INFORMATION

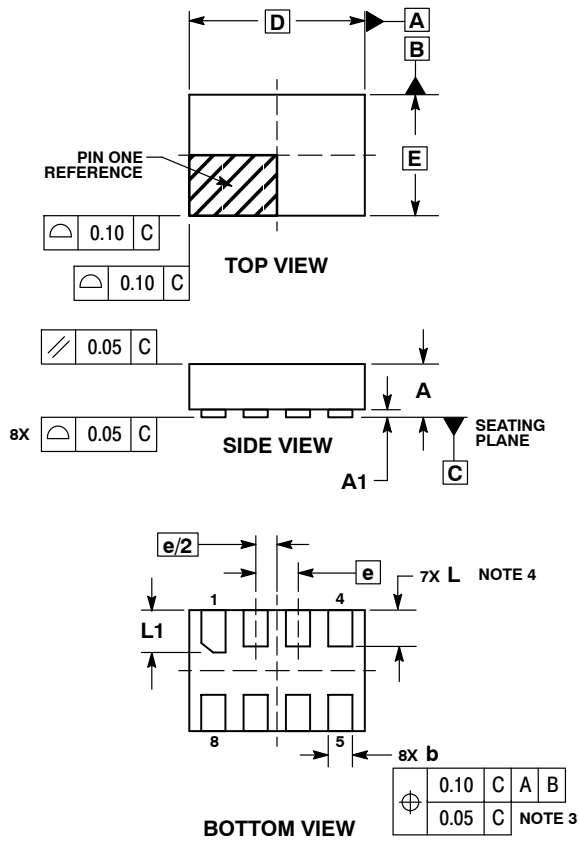
Device	Package	Shipping <sup>†</sup>
NLX1G99AMX1TCG	ULLGA8 – 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G99BMX1TCG	ULLGA8 – 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G99CMX1TCG	ULLGA8 – 0.35P (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

ULLGA8 1.45x1.0, 0.35P  
CASE 613AA-01  
ISSUE A

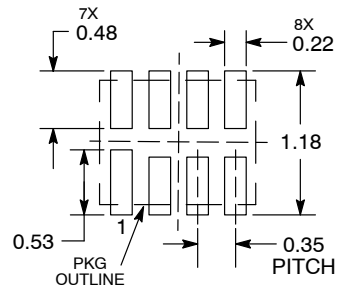


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT  
SOLDERMASK DEFINED\***



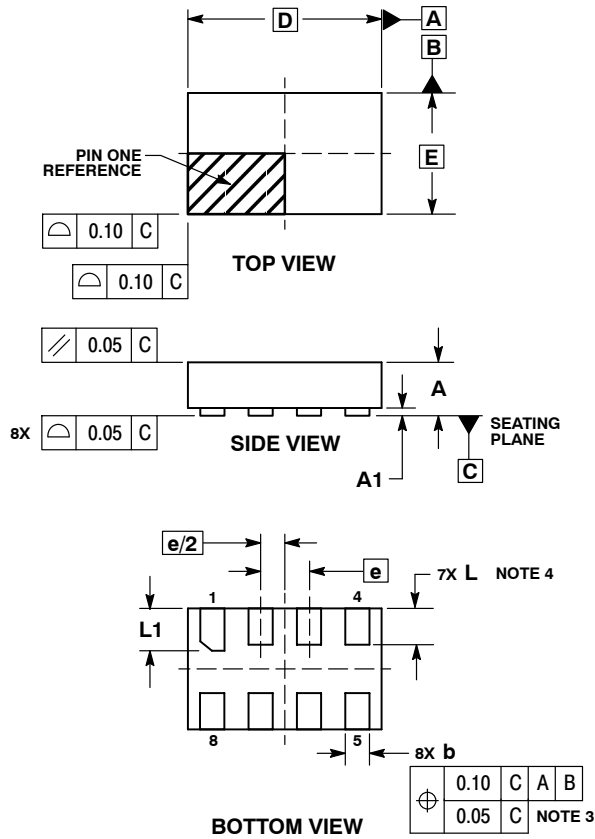
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G99

## PACKAGE DIMENSIONS

ULLGA8 1.6x1.0, 0.4P  
CASE 613AB-01  
ISSUE A

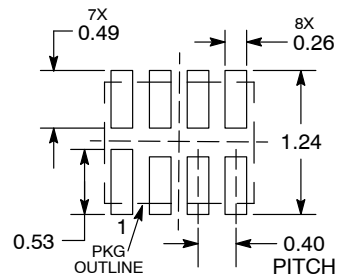


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.60 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT  
SOLDERMASK DEFINED\***



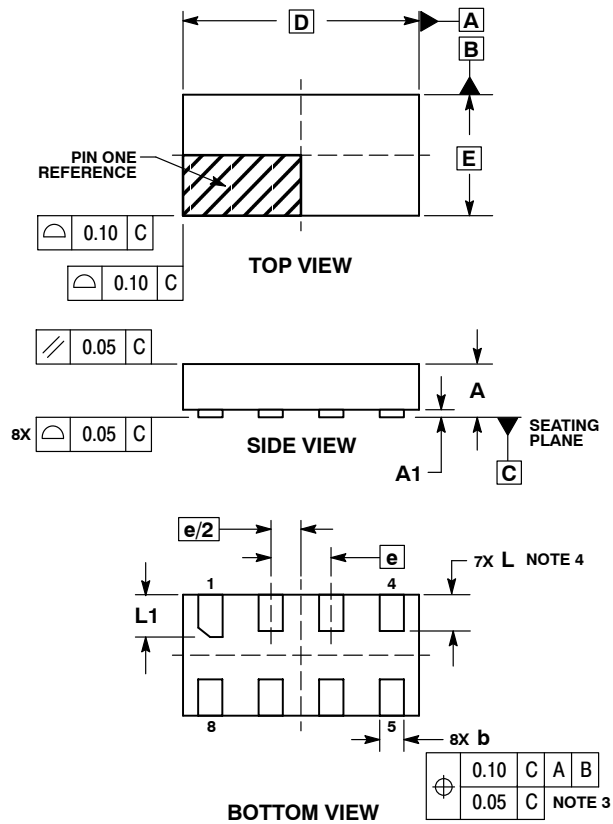
DIMENSIONS: MILLIMETERS

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## PACKAGE DIMENSIONS

ULLGA8 1.95x1.0, 0.5P  
CASE 613AC-01  
ISSUE A

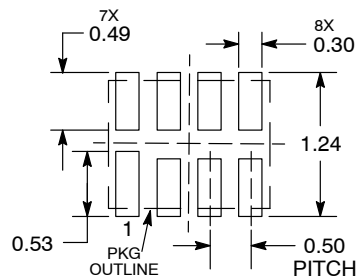


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.95 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT  
SOLDERMASK DEFINED\***



DIMENSIONS: MILLIMETERS

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