HARRIS SEMICONDUCTOR

HS-65643RH

Radiation Hardened 64K x 1 SOS CMOS Static RAM

September 1995

Features

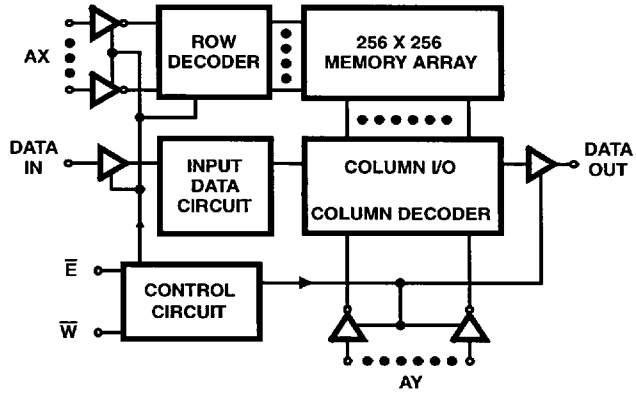
- 1.2 Micron Radiation Hardened SOS CMOS
  - Total Dose 3 x 10^5 RAD (Si)
  - Transient Upset >1 x 10^{11} RAD (Si)/s
  - Single Event Upset < 1 x 10^{-12} Errors/Bit-Day
- Latch-up Free
- LET Threshold >250 MeV/mg/cm2
- Low Standby Supply Current 10mA (Max)
- Low Operating Supply Current 35mA (Max)
- Fast Access Time 50ns (Max), 35ns (Typ)
- High Output Drive Capability ±8mA
- Gated Input Buffers
- Six Transistor Memory Cell
- Fully Static Design
- Asynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Military Temperature Range -55°C to +125°C

Description

The Harris HS-65643RH is a fully asynchronous 64K x 1 radiation hardened static RAM. This RAM is fabricated using the Harris 1.2 micron silicon-on-sapphire CMOS technology. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, high intensity ionizing dose rates, and cosmic rays.

Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Functional Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HS1-65643RH-Q	-55°C to +125°C	24 Lead SBDIP
HS1-65643RH-8	-55°C to +125°C	24 Lead SBDIP
HS1-65643RH/Sample	+25°C	24 Lead SBDIP
HS9-65643RH-Q	-55°C to +125°C	24 Lead Ceramic Flatpack
HS9-65643RH-8	-55°C to +125°C	24 Lead Ceramic Flatpack
HS9-65643RH/Sample	+25°C	24 Lead Ceramic Flatpack
HS9A-65643RH-Q	-55°C to +125°C	28 Lead Ceramic Flatpack
HS9A-65643RH-8	-55°C to +125°C	28 Lead Ceramic Flatpack
HS9A-65643RH/Sample	+25°C	28 Lead Ceramic Flatpack

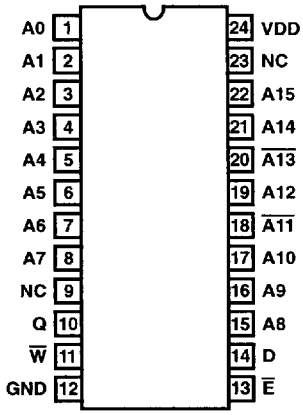
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Spec Number **518730**

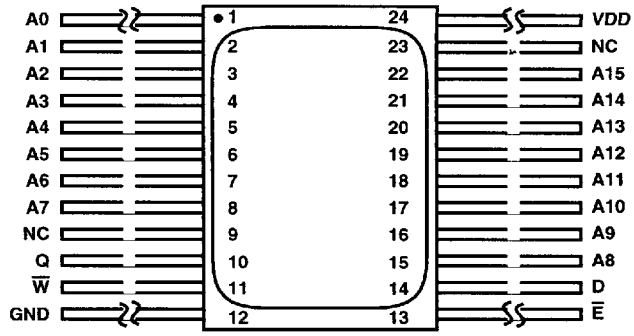
File Number **2794.3**

Pinouts

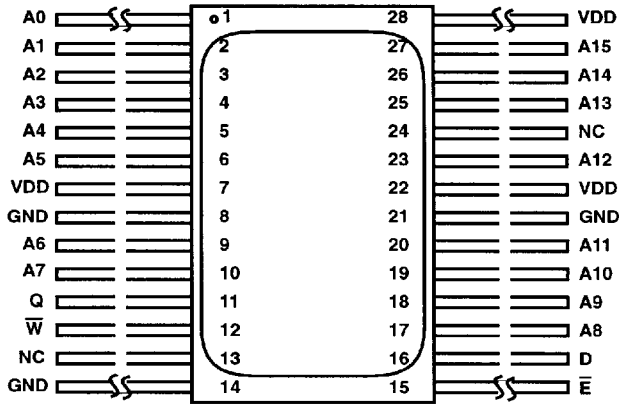
HS1-65643RH 24 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T24
TOP VIEW



HS9-65643RH 24 LEAD CERAMIC
METAL SEAL FLATPACK PACKAGE (FLATPACK)
HARRIS OUTLINE K24.B
TOP VIEW



HS9A-65643RH 28 LEAD CERAMIC METAL
SEAL FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP3-F28
TOP VIEW



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
Typical Derating Factor . . . . . 3mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
24 Lead SBDIP Package	45°C/W	8.0°C/W
24/28 Lead Ceramic Flatpack Package	64°C/W	8.8°C/W

Maximum Package Power Dissipation at +125°C Ambient
24 Lead SBDIP Package 1.11W
24/28 Lead Ceramic Flatpack Package 0.78W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
24 Lead SBDIP Package 22.2mW/C
24/28 Lead Ceramic Flatpack Package 15.6mW/C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VDD) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0V to +0.2VDD
Input High Voltage (VIH) . . . . . 0.8VDD to VDD
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time . . . . . 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -8.0mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	2.4	-	V
	VOH2	VDD = 4.5V, IO = -100µA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	VDD-0.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VO = GND or VDD, VI = VDD or GND $\overline{E}$ = VDD	1, 3	-55°C, +25°C	-10	10	µA
			2	+85°C	-30	30	µA
			2	+125°C	-60	60	µA
Input Leakage Current	IIH or IIL	VDD = 5.5V, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E}$ = VDD	1, 3	-55°C, +25°C	-	500	µA
			2	+85°C	-	4	mA
			2	+125°C	-	10	mA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E}$ = 0.0V	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	30	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E}$ = 0.0V, f = 1MHz	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	35	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, VI = VDD or GND $\overline{E}$ = VDD	1, 3	-55°C, +25°C	-	50	µA
			2	+85°C	-	1	mA
			2	+125°C	-	4	mA
Functional Tests	FT	VDD = 4.5V and 5.5V VI = VDD or GND, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 4.5, VIL = 0.2 VDD VIH = 0.8 VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Chip Enable Access Time	TELQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Write Recovery Time	TWHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Address Hold Time	TEHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Chip Enable to End-of-Write	TELWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Address Valid to End-of-Write	TAVEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	35	-	ns
Chip Enable Pulse Width	TELEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Address Setup Time	TAVWL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	10	-	ns
	TAVEL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	5	-	ns
Write to End-of-Write	TWLEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	25	-	ns
Data Setup Time	TDVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
	TDVEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Address Valid to End-of-Write	TAVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Data Hold Time	TWHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
	TEHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns

NOTES:

1. AC measurements tested at worst case VDD. Guaranteed over full operating range.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD; timing reference levels = 2.0V; output load = 1 TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
I/O Capacitance	COUT	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
Write Enable to Output in High Z	TWLQZ	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	15	ns
Write Enable High to Output ON	TWHQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable to Output ON	TELQX	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	0	-	ns
Chip Enable to Output High Z	TEHQZ	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	15	ns
Read/Write/Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	50	-	ns
Output Hold from Address Change	TAXQX	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	0	-	ns

NOTES:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device GND.

TABLE 4. POST 300K RAD DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD, VI = VDD or GND	+25°C	-	10	mA
Enabled Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 0.0V, VI = VDD or GND	+25°C	-	30	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, f = 1MHz, $\overline{E}$ = 0.0V, VI = VDD or GND	+25°C	-	35	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, $\overline{E}$ = VDD	+25°C	-	6	mA

NOTES:

1. DC parameters not listed in this table are tested at the +25°C pre-irradiation test limits. All AC parameters are tested at the +25°C pre-irradiation test limits.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) GROUP B, SUBGROUP 5

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±150µA
High Impedance Output Leakage Current	IOZH	± 2µA
	IOZL	±2µA
Input Leakage Current	IIH	± 150nA
	IIL	±150nA
Low Level Output Voltage	VOL	± 60mV
Output High Voltage	VOH1	± 400mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100% 5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA	100% 5004	1, 7, Δ	-	1, 7	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	-	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)	N/A	
Subgroup B6	Sample 5005	1, 7, 9	-	N/A	
Group C	Sample 5005	N/A	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9	-	1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9	-	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.
2. Table 5 parameters only

Harris Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 72 Hours Min, +125°C Min, Method 1015

100% Static Burn-In 2, Condition A or B, 72 Hours Min, +125°C Min, Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 1)

100% Dynamic Burn-In, Condition D, 240 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test 2(T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 2)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 3)

Sample - Group B, Method 5005 (Note 4)

Sample - Group D, Method 5005 (Notes 4 and 5)

100% Data Package Generation (Note 6)

NOTES:

1. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
2. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
3. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
4. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group Samples, Group D Test and Group D Samples.
5. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
6. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Harris Space Level Product Flow -8

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

Periodic- Wire Bond Pull Monitor, Method 2011

Periodic- Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition B

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% External Visual

100% Initial Electrical Test

100% Dynamic Burn-In, Condition D, 160 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test

100% PDA, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 2)

Sample - Group B, Method 5005 (Note 3)

Sample - Group C, Method 5005 (Notes 3 and 4)

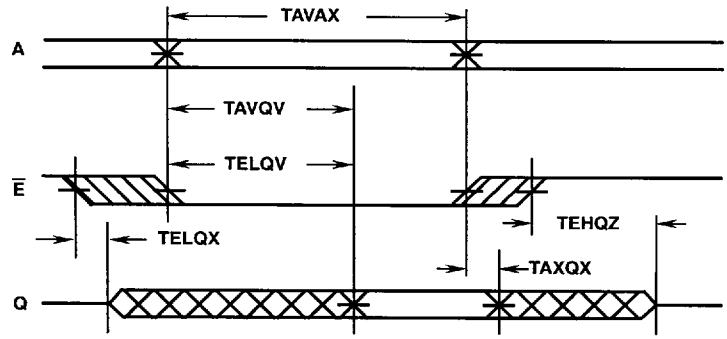
Sample - Group D, Method 5005 (Notes 3 and 4)

100% Data Package Generation (Note 5)

NOTES:

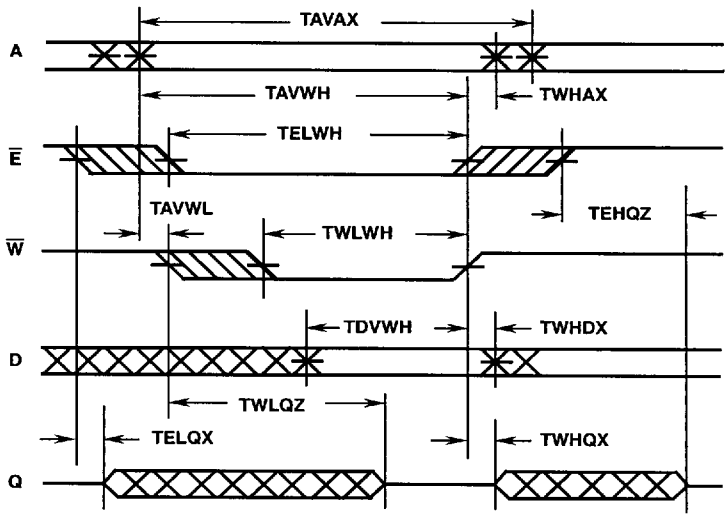
1. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5%.
2. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
3. Group B, C and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.
4. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group C Generic Data and/or Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
5. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Group B, C and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Timing Waveforms



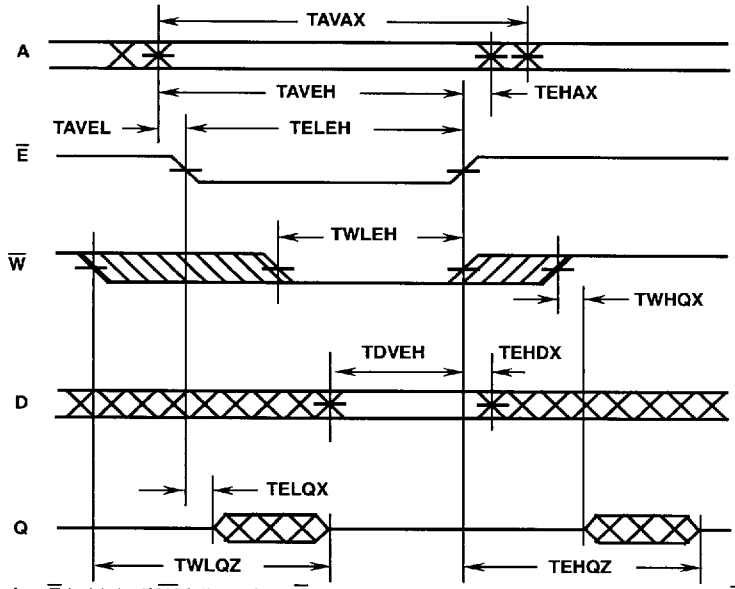
NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

FIGURE 1. READ CYCLE



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

FIGURE 2. WRITE CYCLE I: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$ is high. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ and rises after $\overline{E}$ by a time exceeding TEHQZ then the output will remain in the high impedance state throughout the write cycle.

FIGURE 3. WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E}$ (EARLY WRITE)

Performance Curves

HS-65643RH TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, Unless Otherwise Specified

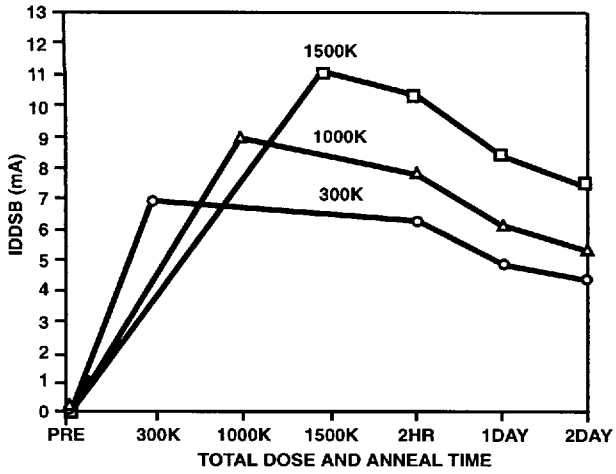


FIGURE 4

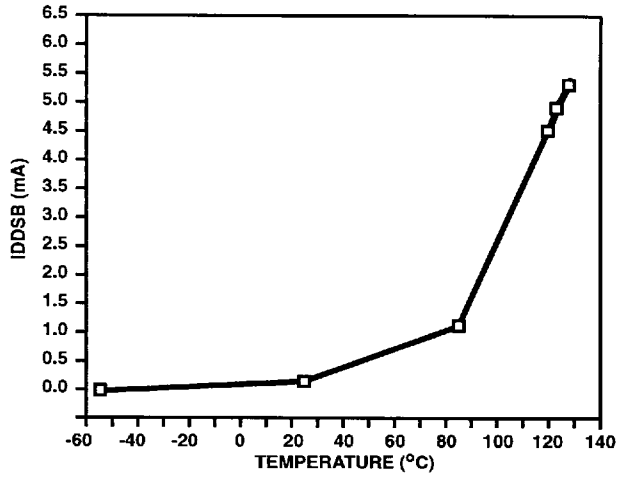


FIGURE 5

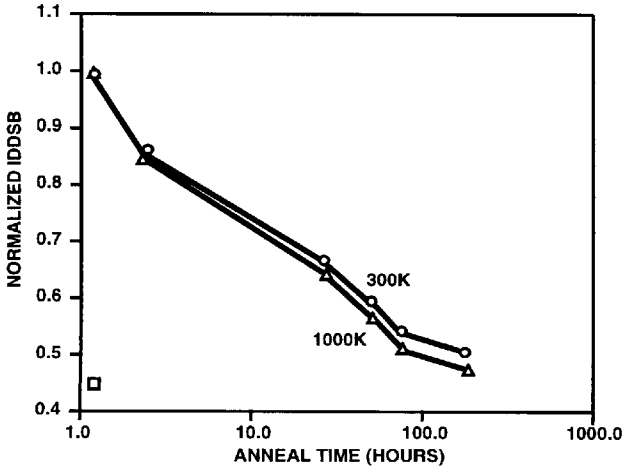


FIGURE 6

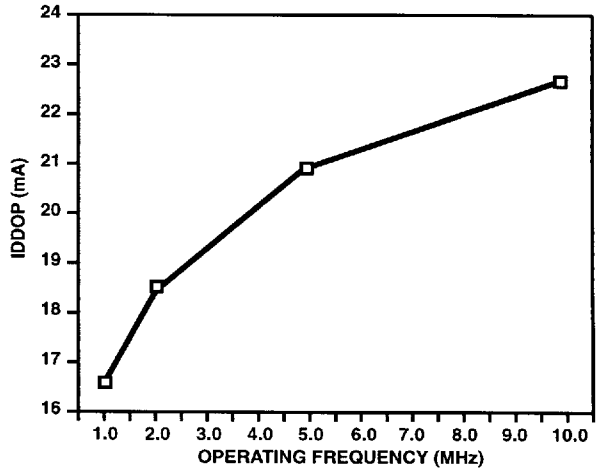


FIGURE 7

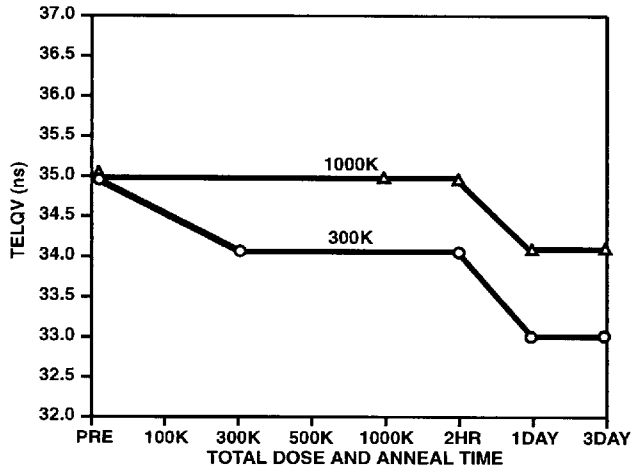
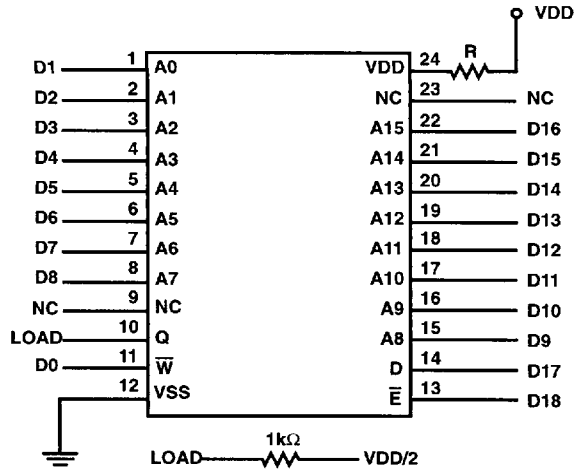


FIGURE 8

Burn-In Circuits

HS-65643RH 24 PIN FLATPACK AND CERAMIC DIP

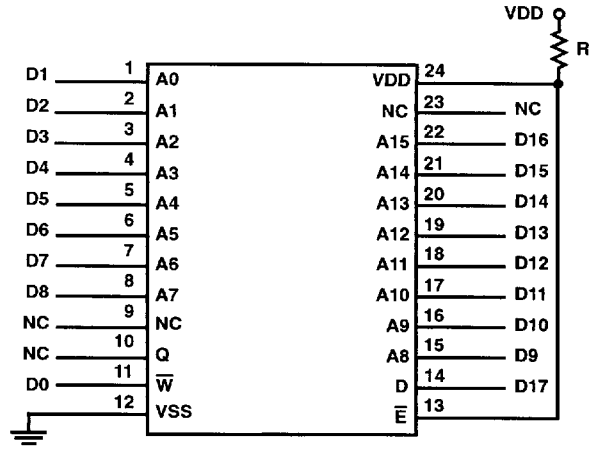


DYNAMIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10Ω ± 10%
3. D0 - D18 are signals from the driver EPROM
4. F = 100kHz

HS-65643RH 24 PIN FLATPACK AND CERAMIC DIP

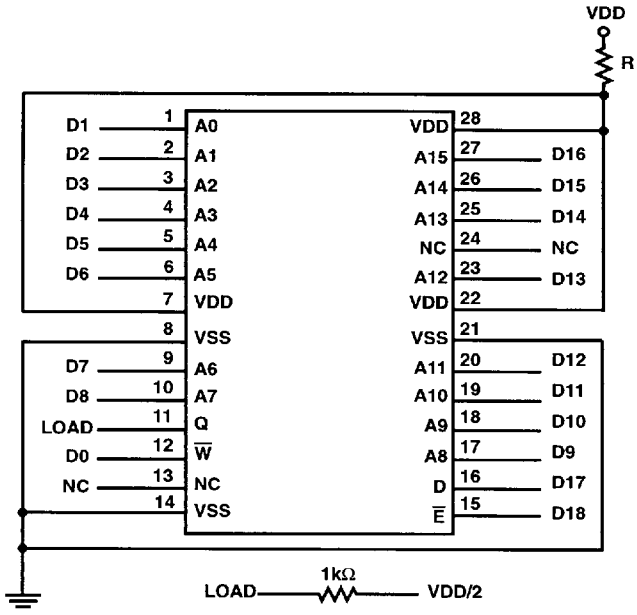


STATIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10Ω ± 10%
3. Static 1: Checkerboard patterns are loaded into the memory for static burn-in. After the pattern is written, $\overline{E}$ is raised to VDD and a random address selected with inputs at either VDD or VSS
4. Static 2: Repeat above except with inverse pattern.

HS-65643RH 28 PIN FLATPACK

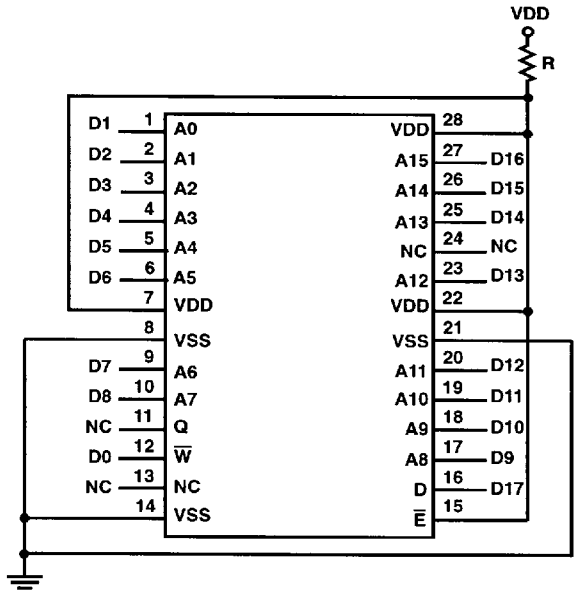


DYNAMIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10Ω ± 10%
3. D0 - D18 are signals from the driver EPROM
4. F = 100kHz

HS-65643RH 28 PIN FLATPACK



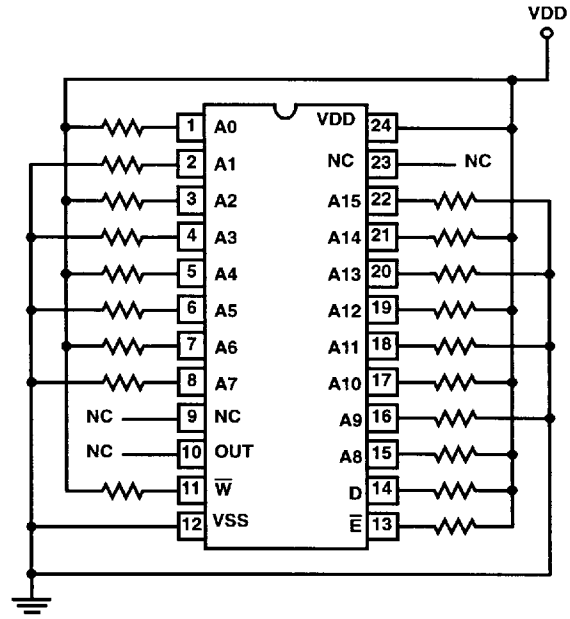
STATIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10Ω ± 10%
3. Static 1: Checkerboard patterns are loaded into the memory for static burn-in. After the pattern is written, $\overline{E}$ is raised to VDD and a random address selected with inputs at either VDD or VSS
4. Static 2: Repeat above except with inverse pattern.

Irradiation Circuit

HS-65643RH (64K x 1 TSOS4 SRAM) 24 PIN CERAMIC DIP



NOTE:

1. VDD = 5.5V ± 0.5V
   R = 10kΩ ± 10%

Test Patterns

MARCH (II)PATTERN

After a background of zeros is written, each cell (from beginning to end in sequence) is read, written to a one and reread. When the array is full of ones each cell (from the end to the beginning) is read, restored to a zero and reread.

After this the pattern is repeated but with complemented data.

MASEST PATTERN (Multiple Address Select Pattern)

A checkerboard pattern is written into the memory. Then the first cell is read, then its binary address complement is read. The second cell is read and then its binary address complement is read. This pattern of incrementing the address and then reading its binary address complement is repeated until the entire memory is read.

This is then repeated but using a checkerboard bar pattern.

GALROW PATTERN (Row Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the row. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

GALCOL PATTERN (Column Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the column. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

CHECKERBOARD PATTERN and CHECKERBOARD BAR

A checkerboard is written (101010) into the memory and then the pattern is read back. This is then repeated but using complemented data.

Metallization Topology

DIE DIMENSIONS:
297 x 310 x 21 ±1mils

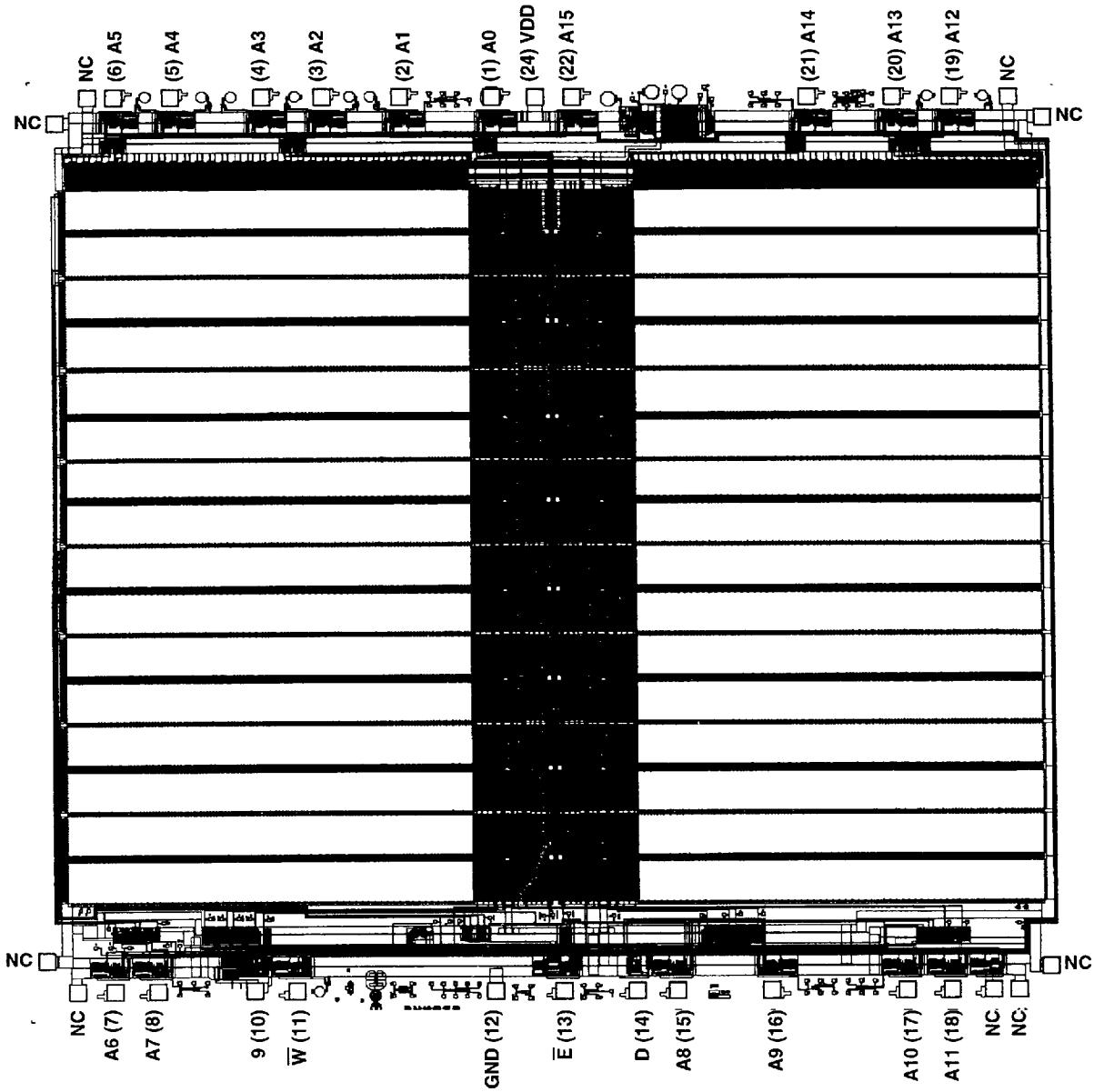
METALLIZATION:
Type: Al/Si/Cu
Metal 1 Thickness: 7500Å ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

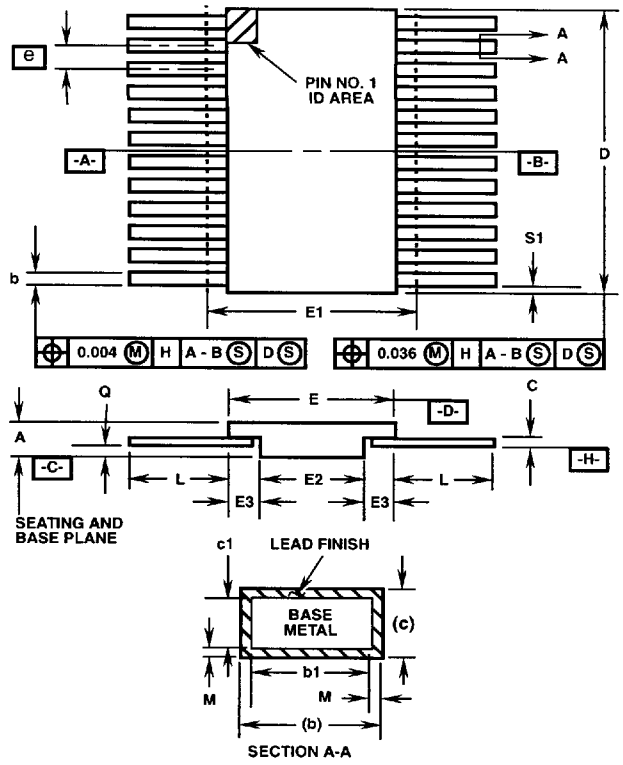
WORST CASE CURRENT DENSITY:
1.5 x 10^5 Amps/cm^2

Metallization Mask Layout

HS-65643RH



Packaging



K24.B

24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.070	0.115	1.78	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	0.590	0.610	14.99	15.49	3
E	0.490	0.510	12.45	12.95	-
E1	-	0.520	-	13.20	3
E2	0.370	0.390	9.40	9.91	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	-	-	-	-	-
L	0.330	0.350	8.38	8.89	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	24		24		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.