

### Low Noise, Low Power I<sup>2</sup>C® Bus, 256 Taps

The ISL90840 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I<sup>2</sup>C bus interface. Each potentiometer has an associated Wiper Register (WR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper.

The DCPs can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

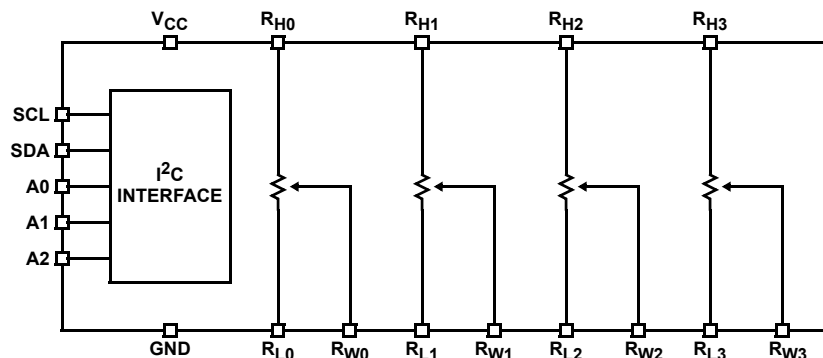
### Ordering Information

| PART NUMBER                       | PACKAGE                  | TEMP RANGE (°C) | RESISTANCE OPTION (Ω) |
|-----------------------------------|--------------------------|-----------------|-----------------------|
| ISL90840UIV2027                   | 20 Ld TSSOP              | -40 to +85      | 50K                   |
| ISL90840UIV2027Z<br>(Notes 1 & 2) | 20 Ld TSSOP<br>(Pb-Free) | -40 to +85      | 50K                   |
| ISL90840WIV2027                   | 20 Ld TSSOP              | -40 to +85      | 10K                   |
| ISL90840WIV2027Z<br>(Notes 1 & 2) | 20 Ld TSSOP<br>(Pb-Free) | -40 to +85      | 10K                   |

#### NOTES:

- Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- Contact factory for availability.

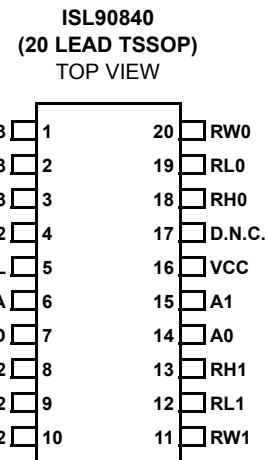
### Functional Diagram



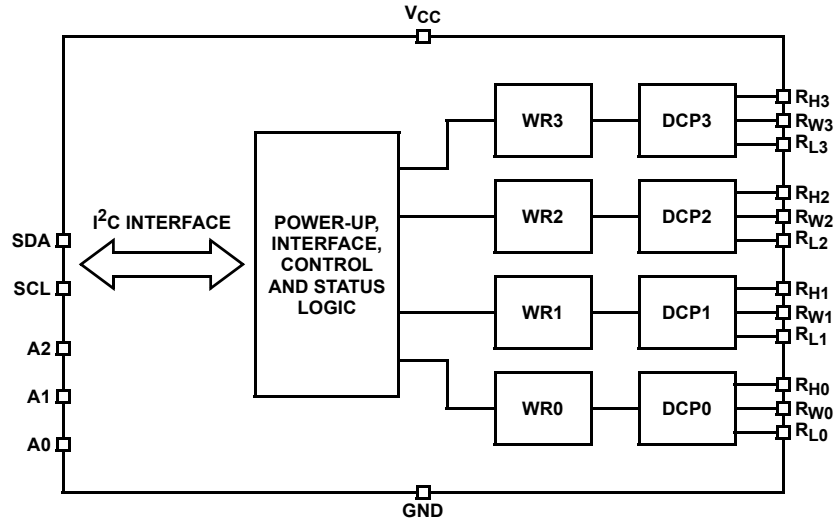
### Features

- Four potentiometers in one package
- 256 resistor taps - 0.4% resolution
- I<sup>2</sup>C serial interface
  - Three address pins, up to eight devices/bus
- Wiper resistance: 70Ω typical @ 3.3V
- Standby current <5μA max
- Power supply: 2.7V to 5.5V
- 50kΩ, 10kΩ total resistance
- 20 Lead TSSOP
- Pb-free plus anneal available (RoHS compliant)

### Pinout



## Block Diagram



## Pin Descriptions

| TSSOP PIN | SYMBOL | DESCRIPTION  |
|-----------|--------|--|
| 1         | RH3    | "High" terminal of DCP3                            |
| 2         | RL3    | "Low" terminal of DCP3                             |
| 3         | RW3    | "Wiper" terminal of DCP3                           |
| 4         | A2     | Device address for the I <sup>2</sup> C interface  |
| 5         | SCL    | I <sup>2</sup> C interface clock                   |
| 6         | SDA    | Serial data I/O for the I <sup>2</sup> C interface |
| 7         | GND    | Device ground pin                                  |
| 8         | RW2    | "Wiper" terminal of DCP2                           |
| 9         | RL2    | "Low" terminal of DCP2                             |
| 10        | RH2    | "High" terminal of DCP2                            |
| 11        | RW1    | "Wiper" terminal of DCP1                           |
| 12        | RL1    | "Low" terminal of DCP1                             |
| 13        | RH1    | "High" terminal of DCP1                            |
| 14        | A0     | Device address for the I <sup>2</sup> C interface  |
| 15        | A1     | Device address for the I <sup>2</sup> C interface  |
| 16        | VCC    | Power supply pin                                   |
| 17        | D.N.C. | Do not connect                                     |
| 18        | RH0    | "High" terminal of DCP0                            |
| 19        | RL0    | "Low" terminal of DCP0                             |
| 20        | RW0    | "Wiper" terminal of DCP0                           |

**Absolute Maximum Ratings**

Storage temperature .....-65°C to +150°C  
 Voltage at any digital interface pin  
 with respect to GND ..... -0.3V to  $V_{CC}+0.3$   
 $V_{CC}$  ..... -0.3V to +6V  
 Voltage at any DCP pin with  
 respect to GND ..... -0.3V to  $V_{CC}$   
 Lead temperature (soldering, 10s) ..... 300°C  
 $I_W$  (10s) ..... ±6mA  
 Latchup ..... Class II, Level B at +85°C  
 ESD ..... >2kV Human Body Model

**Recommended Operating Conditions**

Industrial .....-40°C to +85°C  
 $V_{CC}$  ..... 2.7V to 5.5V  
 Power rating of each DCP ..... 5mW  
 Wiper current of each DCP ..... ±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**Analog Specifications** Over recommended operating conditions unless otherwise stated.

| SYMBOL  | PARAMETER   | TEST CONDITIONS   | MIN  | TYP (NOTE 1) | MAX | UNIT         |
|---|---|---|------|--------------|-----|--------------|
| R <sub>TOTAL</sub>  | R <sub>H</sub> to R <sub>L</sub> resistance           | W option  |      | 10           |     | kΩ           |
|   |   | U option  |      | 50           |     | kΩ           |
|   | R <sub>H</sub> to R <sub>L</sub> resistance tolerance |   | -20  |              | +20 | %            |
| R <sub>W</sub>  | Wiper resistance                                      | $V_{CC} = 3.3V @ 25°C$ , wiper current = $V_{CC}/R_{TOTAL}$   |      | 70           | 200 | Ω            |
| C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub>  | Potentiometer capacitance (Note 15)                   |   |      | 10/10/25     |     | pF           |
| I <sub>LkgDCP</sub>   | Leakage on DCP pins (Note 15)                         | Voltage at pin from GND to $V_{CC}$   |      | 0.1          | 1   | μA           |
| <b>VOLTAGE DIVIDER MODE</b> (0V @ R <sub>Li</sub> ; $V_{CC}$ @ R <sub>Hi</sub> ; measured at R <sub>Wi</sub> , unloaded; i = 0, 1, 2, or 3)   |   |   |      |              |     |              |
| INL (Note 6)  | Integral non-linearity                                |   | -1   |              | 1   | LSB (Note 2) |
| DNL (Note 5)  | Differential non-linearity                            | Monotonic over all tap positions  | -0.5 |              | 0.5 | LSB (Note 2) |
| ZSerror (Note 3)  | Zero-scale error                                      | W option  | 0    | 1            | 7   | LSB (Note 2) |
|   |   | U option  | 0    | 0.5          | 2   |              |
| FSerror (Note 4)  | Full-scale error                                      | W option  | -7   | -1           | 0   | LSB (Note 2) |
|   |   | U option  | -2   | -1           | 0   |              |
| V <sub>MATCH</sub> (Note 7)   | DCP to DCP matching                                   | Any two DCPs at same tap position, same voltage at all R <sub>H</sub> terminals, and same voltage at all R <sub>L</sub> terminals | -2   |              | 2   | LSB (Note 2) |
| TC <sub>V</sub> (Note 8)  | Ratiometric temperature coefficient                   | DCP register set to 80 hex  |      | ±4           |     | ppm/°C       |
| <b>RESISTOR MODE</b> (Measurements between R <sub>Wi</sub> and R <sub>Li</sub> with R <sub>Hi</sub> not connected, or between R <sub>Wi</sub> and R <sub>Hi</sub> with R <sub>Li</sub> not connected. i = 0, 1, 2 or 3) |   |   |      |              |     |              |
| RINL (Note 12)  | Integral non-linearity                                | DCP register set between 20 hex and FF hex; monotonic over all tap positions  | -1   |              | 1   | MI (Note 9)  |
| RDNL (Note 11)  | Differential non-linearity                            |   | -0.5 |              | 0.5 | MI (Note 9)  |
| R <sub>offset</sub> (Note 10)   | Offset  | W option  | 0    | 1            | 7   | MI (Note 9)  |
|   |   | U option  | 0    | 0.5          | 2   | MI (Note 9)  |
| R <sub>MATCH</sub> (Note 13)  | DCP to DCP matching                                   | Any two DCPs at the same tap position with the same terminal voltages   | -2   |              | 2   | MI (Note 9)  |
| TC <sub>R</sub> (Note 14)   | Resistance temperature coefficient                    | DCP register set between 20 hex and FF hex  |      | ±45          |     | ppm/°C       |

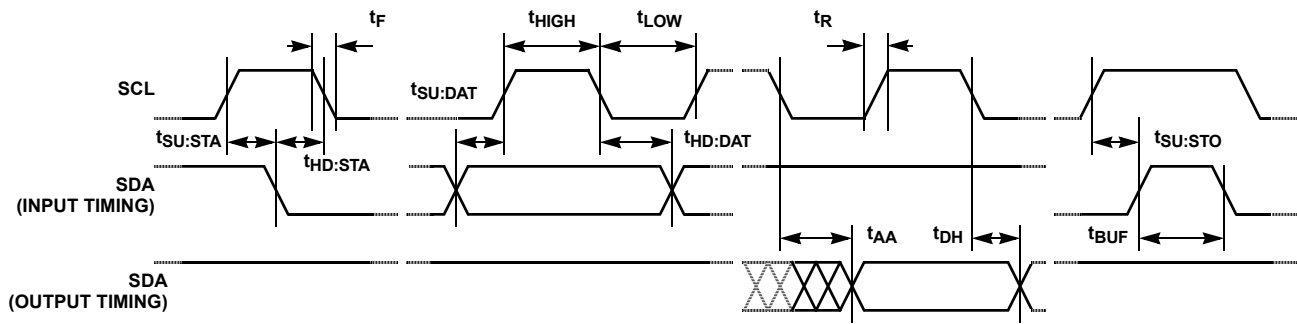
**Operating Specifications** Over the recommended operating conditions unless otherwise specified.

| SYMBOL                        | PARAMETER  | TEST CONDITIONS  | MIN                          | TYP<br>(NOTE 1) | MAX                  | UNIT |
|-------------------------------|--|--|------------------------------|-----------------|----------------------|------|
| I <sub>CC1</sub>              | V <sub>CC</sub> supply current (volatile write/read)             | f <sub>SCL</sub> = 400kHz; SDA = Open; (for I <sup>2</sup> C, active, read and write states)   |                              |                 | 1                    | mA   |
| I <sub>SB</sub>               | V <sub>CC</sub> current (standby)                                | V <sub>CC</sub> = +5.5V, I <sup>2</sup> C interface in standby state   |                              |                 | 5                    | μA   |
|                               |  | V <sub>CC</sub> = +3.6V, I <sup>2</sup> C interface in standby state   |                              |                 | 2                    | μA   |
| I <sub>LkgDig</sub>           | Leakage current, at pins A0, A1, A2, SDA, and SCL                | Voltage at pin from GND to V <sub>CC</sub>   | -10                          |                 | 10                   | μA   |
| t <sub>DCP</sub><br>(Note 15) | DCP wiper response time  | SCL falling edge of last bit of DCP data byte to wiper change  |                              |                 | 1                    | μs   |
| <b>SERIAL INTERFACE SPECS</b> |  |  |                              |                 |                      |      |
| V <sub>IL</sub>               | A2, A1, A0, SDA, and SCL input buffer LOW voltage                |  | -0.3                         |                 | 0.3*V <sub>CC</sub>  | V    |
| V <sub>IH</sub>               | A2, A1, A0, SDA, and SCL input buffer HIGH voltage               |  | 0.7*V <sub>CC</sub>          |                 | V <sub>CC</sub> +0.3 | V    |
| Hysteresis<br>(Note 15)       | SDA and SCL input buffer hysteresis                              |  | 0.05*<br>V <sub>CC</sub>     |                 |                      | V    |
| V <sub>OL</sub><br>(Note 15)  | SDA output buffer LOW voltage, sinking 4mA                       |  | 0                            |                 | 0.4                  | V    |
| C <sub>pin</sub><br>(Note 15) | A2, A1, A0, SDA, and SCL pin capacitance                         |  |                              |                 | 10                   | pF   |
| f <sub>SCL</sub>              | SCL frequency  |  |                              |                 | 400                  | kHz  |
| t <sub>IN</sub><br>(Note 15)  | Pulse width suppression time at SDA and SCL inputs               | Any pulse narrower than the max spec is suppressed   |                              |                 | 50                   | ns   |
| t <sub>AA</sub><br>(Note 15)  | SCL falling edge to SDA output data valid                        | SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA exits the 30% to 70% of V <sub>CC</sub> window                              |                              |                 | 900                  | ns   |
| t <sub>BUF</sub><br>(Note 15) | Time the bus must be free before the start of a new transmission | SDA crossing 70% of V <sub>CC</sub> during a STOP condition, to SDA crossing 70% of V <sub>CC</sub> during the following START condition | 1300                         |                 |                      | ns   |
| t <sub>LOW</sub>              | Clock LOW time   | Measured at the 30% of V <sub>CC</sub> crossing  | 1300                         |                 |                      | ns   |
| t <sub>HIGH</sub>             | Clock HIGH time  | Measured at the 70% of V <sub>CC</sub> crossing  | 600                          |                 |                      | ns   |
| t <sub>SU:STA</sub>           | START condition setup time                                       | SCL rising edge to SDA falling edge; both crossing 70% of V <sub>CC</sub>  | 600                          |                 |                      | ns   |
| t <sub>HD:STA</sub>           | START condition hold time  | From SDA falling edge crossing 30% of V <sub>CC</sub> to SCL falling edge crossing 70% of V <sub>CC</sub>                                | 600                          |                 |                      | ns   |
| t <sub>SU:DAT</sub>           | Input data setup time  | From SDA exiting the 30% to 70% of V <sub>CC</sub> window, to SCL rising edge crossing 30% of V <sub>CC</sub>                            | 100                          |                 |                      | ns   |
| t <sub>HD:DAT</sub>           | Input data hold time   | From SCL rising edge crossing 70% of V <sub>CC</sub> to SDA entering the 30% to 70% of V <sub>CC</sub> window                            | 0                            |                 |                      | ns   |
| t <sub>SU:STO</sub>           | STOP condition setup time  | From SCL rising edge crossing 70% of V <sub>CC</sub> , to SDA rising edge crossing 30% of V <sub>CC</sub>                                | 600                          |                 |                      | ns   |
| t <sub>HD:STO</sub>           | STOP condition hold time for read, or volatile only write        | From SDA rising edge to SCL falling edge; both crossing 70% of V <sub>CC</sub>   | 600                          |                 |                      | ns   |
| t <sub>DH</sub><br>(Note 15)  | Output data hold time  | From SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA enters the 30% to 70% of V <sub>CC</sub> window                        | 0                            |                 |                      | ns   |
| t <sub>R</sub><br>(Note 15)   | SDA and SCL rise time  | From 30% to 70% of V <sub>CC</sub>   | 20 +<br>0.1 * C <sub>b</sub> |                 | 250                  | ns   |

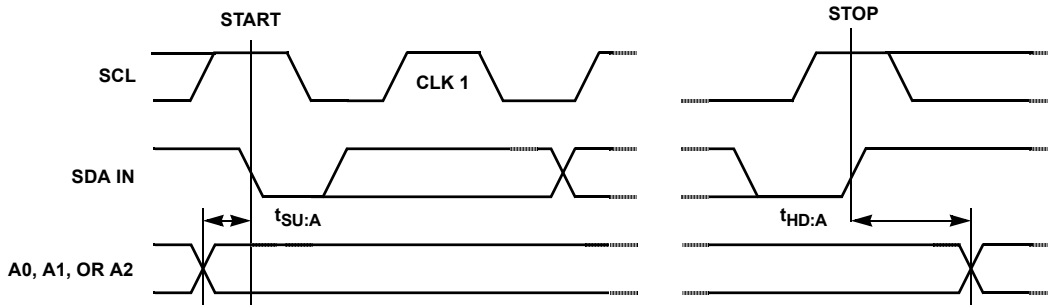
**Operating Specifications** Over the recommended operating conditions unless otherwise specified. (Continued)

| SYMBOL                | PARAMETER                                 | TEST CONDITIONS   | MIN              | TYP (NOTE 1) | MAX | UNIT       |
|-----------------------|---|---|------------------|--------------|-----|------------|
| $t_F$<br>(Note 15)    | SDA and SCL fall time                     | From 70% to 30% of $V_{CC}$   | $20 + 0.1 * C_b$ |              | 250 | ns         |
| $C_b$<br>(Note 15)    | Capacitive loading of SDA or SCL          | Total on-chip and off-chip  | 10               |              | 400 | pF         |
| $R_{pu}$<br>(Note 15) | SDA and SCL bus pull-up resistor off-chip | Maximum is determined by $t_R$ and $t_F$<br>For $C_b = 400\text{pF}$ , max is about 2~2.5k $\Omega$ .<br>For $C_b = 40\text{pF}$ , max is about 15~20k $\Omega$ | 1                |              |     | k $\Omega$ |
| $t_{SU:A}$            | A2, A1 and A0 setup time                  | Before START condition  | 600              |              |     | ns         |
| $t_{HD:A}$            | A2, A1 and A0 hold time                   | After STOP condition  | 600              |              |     | ns         |

**SDA vs SCL Timing**



**A0, A1, and A2 Pin Timing**



NOTES:

1. Typical values are for  $T_A = 25^\circ\text{C}$  and 3.3V supply voltage.
2. LSB:  $[V(R_W)_{255} - V(R_W)_0]/255$ .  $V(R_W)_{255}$  and  $V(R_W)_0$  are  $V(R_W)$  for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error =  $V(R_W)_0/\text{LSB}$ .
4. FS error =  $[V(R_W)_{255} - V_{CC}]/\text{LSB}$ .
5. DNL =  $[V(R_W)_i - V(R_W)_{i-1}]/\text{LSB} - 1$ , for  $i = 1$  to 255.  $i$  is the DCP register setting.
6. INL =  $V(R_W)_i - i \cdot \text{LSB} - V(R_W)$  for  $i = 1$  to 255.
7.  $V_{\text{MATCH}} = [V(R_W)_x - V(R_W)_y]/\text{LSB}$ , for  $i = 0$  to 255,  $x = 0$  to 3 and  $y = 0$  to 3.
8.  $TC_V = \frac{\text{Max}(V(R_W)_i) - \text{Min}(V(R_W)_i)}{[\text{Max}(V(R_W)_i) + \text{Min}(V(R_W)_i)]/2} \times \frac{10^6}{125^\circ\text{C}}$  for  $i = 16$  to 240 decimal,  $T = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  $\text{Max}()$  is the maximum value of the wiper voltage and  $\text{Min}()$  is the minimum value of the wiper voltage over the temperature range.
9.  $MI = |R_{255} - R_0|/255$ .  $R_{255}$  and  $R_0$  are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
10.  $R_{\text{offset}} = R_0/MI$ , when measuring between  $R_W$  and  $R_L$ .  
 $R_{\text{offset}} = R_{255}/MI$ , when measuring between  $R_W$  and  $R_H$ .
11.  $RDNL = (R_i - R_{i-1})/MI$ , for  $i = 32$  to 255.
12.  $RINL = [R_i - (MI \cdot i) - R_0]/MI$ , for  $i = 32$  to 255.
13.  $R_{\text{MATCH}} = (R_{i,x} - R_{i,y})/MI$ , for  $i = 0$  to 255,  $x = 0$  to 3 and  $y = 0$  to 3.
14.  $TC_R = \frac{[\text{Max}(R_i) - \text{Min}(R_i)]}{[\text{Max}(R_i) + \text{Min}(R_i)]/2} \times \frac{10^6}{125^\circ\text{C}}$  for  $i = 32$  to 255,  $T = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  $\text{Max}()$  is the maximum value of the resistance and  $\text{Min}()$  is the minimum value of the resistance over the temperature range.
15. This parameter is not 100% tested.

Typical Performance Curves

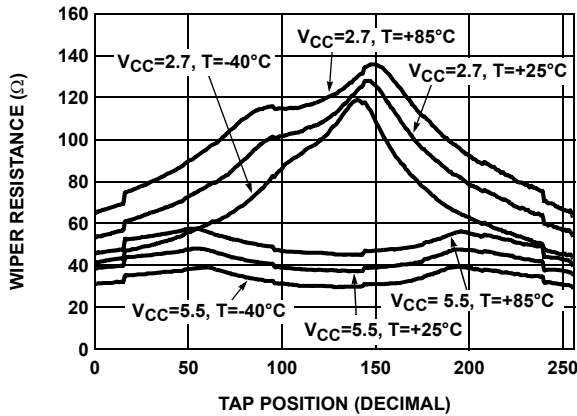


FIGURE 1. WIPER RESISTANCE vs TAP POSITION  
 $[I(R_W) = V_{CC} / R_{\text{TOTAL}}]$  FOR 50kΩ (U)

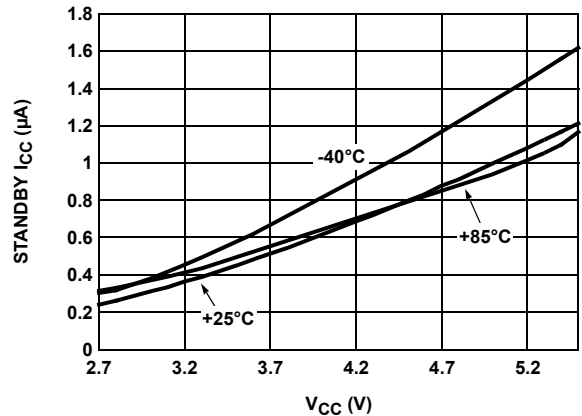


FIGURE 2. STANDBY  $I_{CC}$  vs  $V_{CC}$

Typical Performance Curves (Continued)

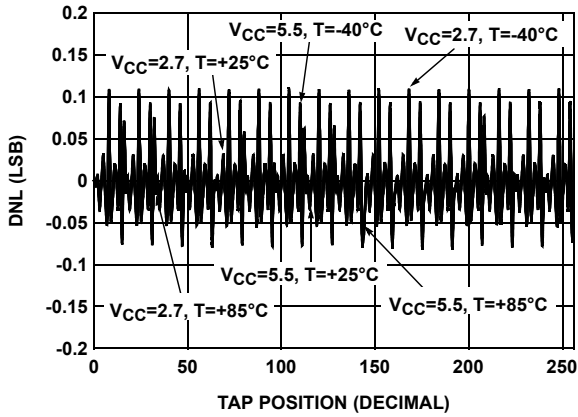


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

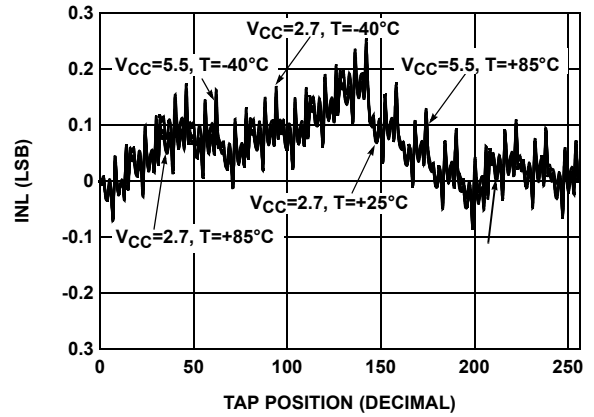


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

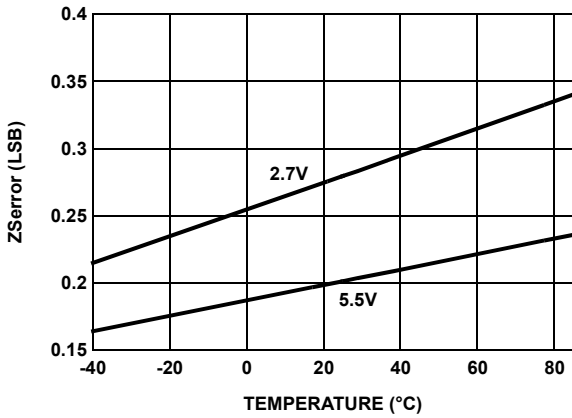


FIGURE 5. ZSerror vs TEMPERATURE FOR 50kΩ (W)

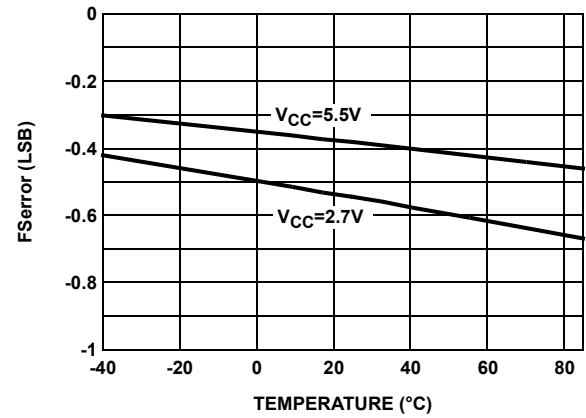


FIGURE 6. FSerror vs TEMPERATURE FOR 50kΩ (W)

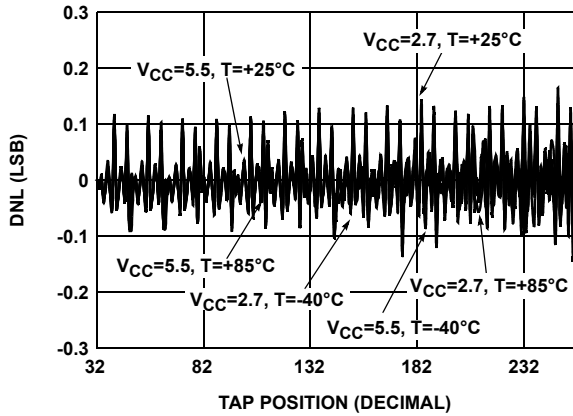


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

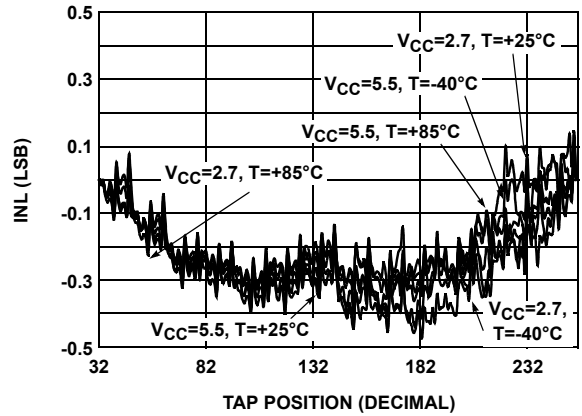


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

Typical Performance Curves (Continued)

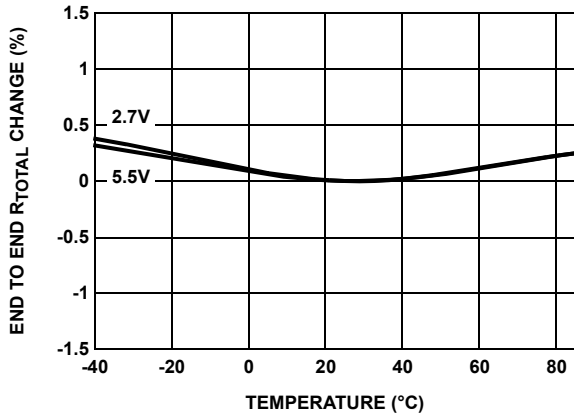


FIGURE 9. END TO END  $R_{TOTAL}$  % CHANGE vs TEMPERATURE FOR 50k $\Omega$  (W)

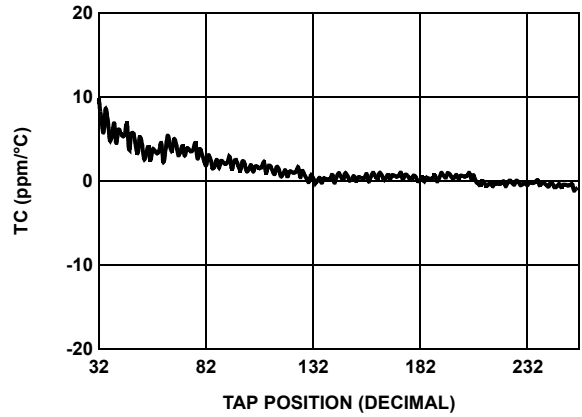


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm FOR 50k $\Omega$  (W)

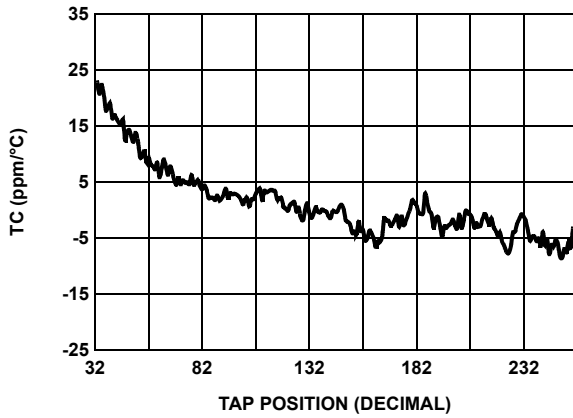


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm FOR 50k $\Omega$  (W)

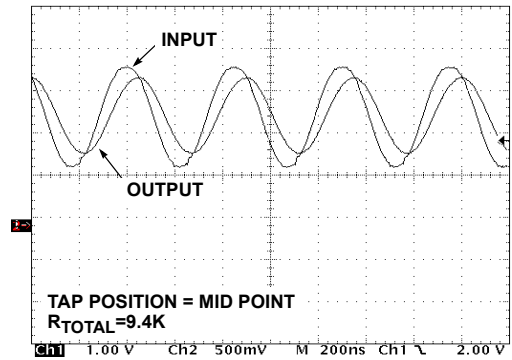


FIGURE 12. FREQUENCY RESPONSE (2.2MHz)

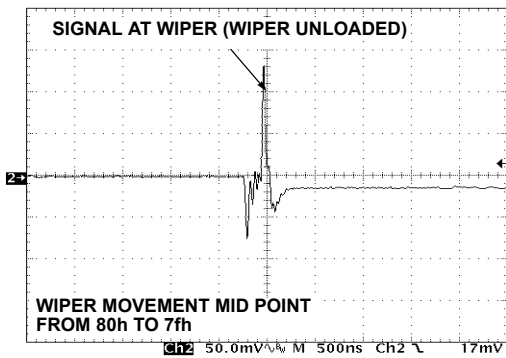


FIGURE 13. MIDSACLE GLITCH, CODE 80h TO 7fh (WIPER 0)

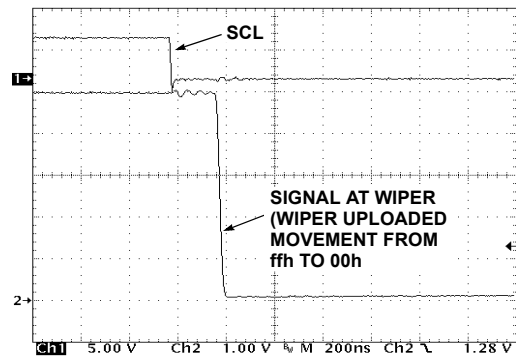


FIGURE 14. LARGE SIGNAL SETTLING TIME



## Principles of Operation

The ISL90840 is an integrated circuit incorporating four DCPs with their associated registers, and an I<sup>2</sup>C serial interface providing direct communication between a host and the potentiometers.

### DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (R<sub>H</sub> and R<sub>L</sub> pins). The R<sub>W</sub> pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR<7:0>: 00h), its wiper terminal (R<sub>W</sub>) is closest to its “Low” terminal (R<sub>L</sub>). When the WR of a DCP contains all ones (WR<7:0>: FFh), its wiper terminal (R<sub>W</sub>) is closest to its “High” terminal (R<sub>H</sub>). As the value of the WR increases from all zeroes (00h) to all ones (255 decimal), the wiper moves monotonically from the position closest to R<sub>L</sub> to the closest to R<sub>H</sub>. At the same time, the resistance between R<sub>W</sub> and R<sub>L</sub> increases monotonically, while the resistance between R<sub>H</sub> and R<sub>W</sub> decreases monotonically.

While the ISL90840 is being powered up, all four WRs are reset to 80h (128 decimal), which locates R<sub>W</sub> roughly at the center between R<sub>L</sub> and R<sub>H</sub>.

The WRs can be read or written to directly using the I<sup>2</sup>C serial interface as described in the following sections. The I<sup>2</sup>C interface Address Byte has to be set to 00h, 01h, 02h, and 03h to access the WR of DCP0, DCP1, DCP2, and DCP3 respectively

## I<sup>2</sup>C Serial Interface

The ISL90840 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL90840 operates as a slave device in all applications.

All communication over the I<sup>2</sup>C interface is conducted by sending the MSB of each byte of data first.

### Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 15). On power-up of the ISL90840 the SDA pin is in the input mode.

All I<sup>2</sup>C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL90840 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 15). A START condition is ignored during the power-up of the device.

All I<sup>2</sup>C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 15). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 16).

The ISL90840 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL90840 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 0101 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB is the Read/Write bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 1).

**TABLE 1. IDENTIFICATION BYTE FORMAT**

Logic values at pins A2, A1, and A0 respectively

|       |   |   |   |    |    |    |                |
|-------|---|---|---|----|----|----|----------------|
| 0     | 1 | 0 | 1 | A2 | A1 | A0 | R <sub>W</sub> |
| (MSB) |   |   |   |    |    |    | (LSB)          |

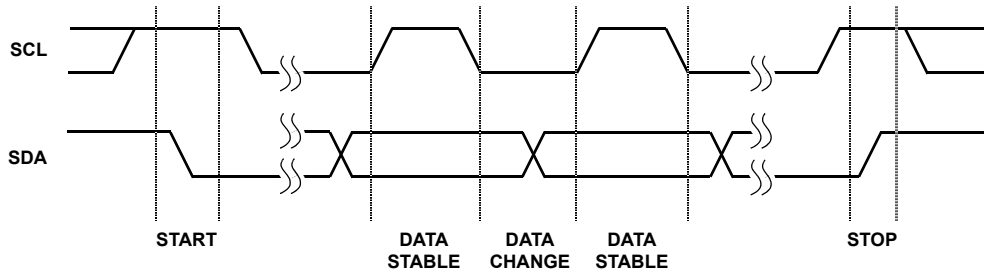


FIGURE 15. VALID DATA CHANGES, START, AND STOP CONDITIONS

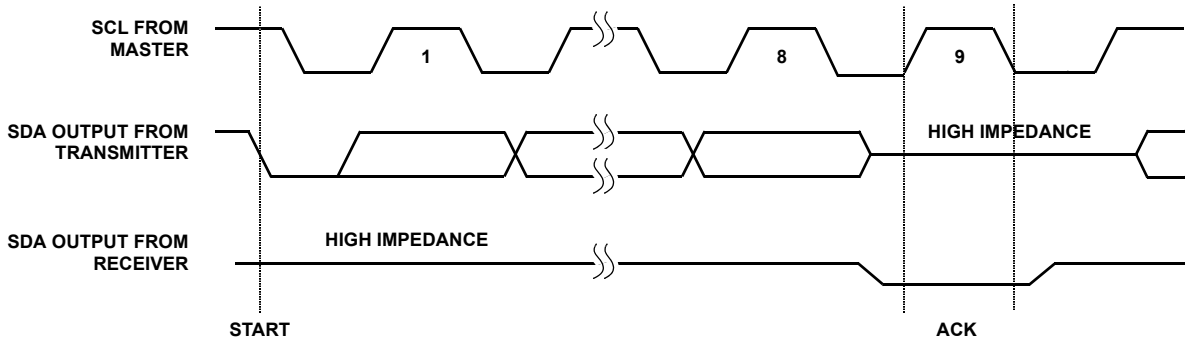


FIGURE 16. ACKNOWLEDGE RESPONSE FROM RECEIVER

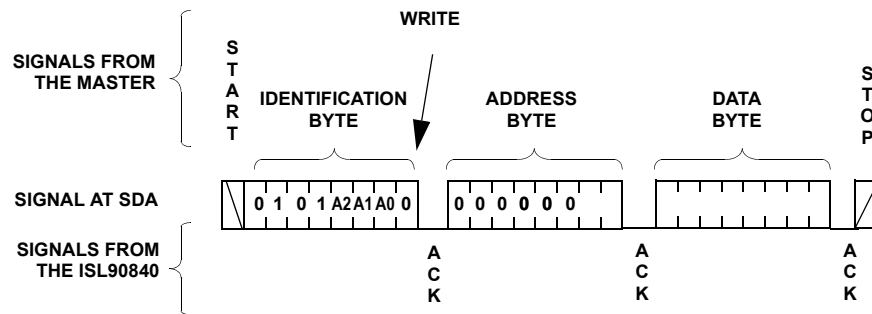


FIGURE 17. BYTE WRITE SEQUENCE

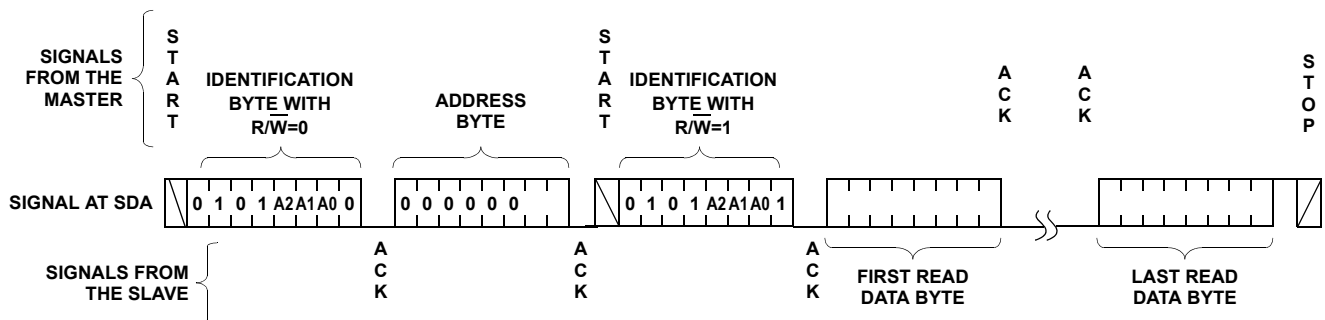


FIGURE 18. READ SEQUENCE

### **Write Operation**

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL90840 responds with an ACK. At this time, the device enters its standby state (See Figure 17).

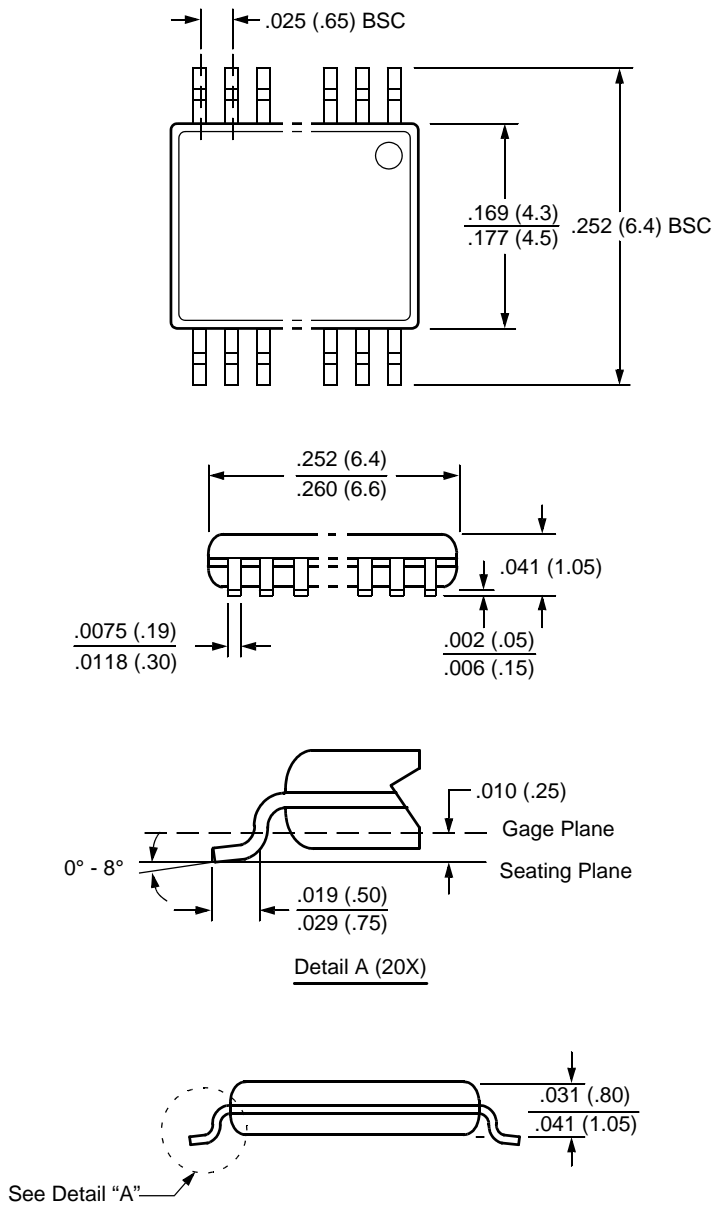
### **Read Operation**

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification byte with the  $\overline{R/W}$  bit set to "0", an Address Byte, a second START, and a second Identification byte with the  $\overline{R/W}$  bit set to "1". After each of the three bytes, the ISL90840 responds with an ACK. Then the ISL90840 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 18).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 03h, the pointer "rolls over" to 00h, and the device continues to output data for each ACK received.

Packaging Information

20-Lead Plastic, TSSOP, Package Code V20



NOTE: All dimensions in inches (in parentheses in millimeters).

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