

## DUAL 4-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER



The HEF4052B is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs ( $Y_0$  to  $Y_3$ ) and a common input/output ( $Z$ ). The common channel select logic includes two address inputs ( $A_0$  and  $A_1$ ) and an active LOW enable input ( $\bar{E}$ ).

Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output ( $Y_0$  to  $Y_3$ ) and the other side connected to a common input/output ( $Z$ ).

With  $\bar{E}$  LOW, one of the four switches is selected (low impedance ON-state) by  $A_0$  and  $A_1$ . With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of  $A_0$  and  $A_1$ .

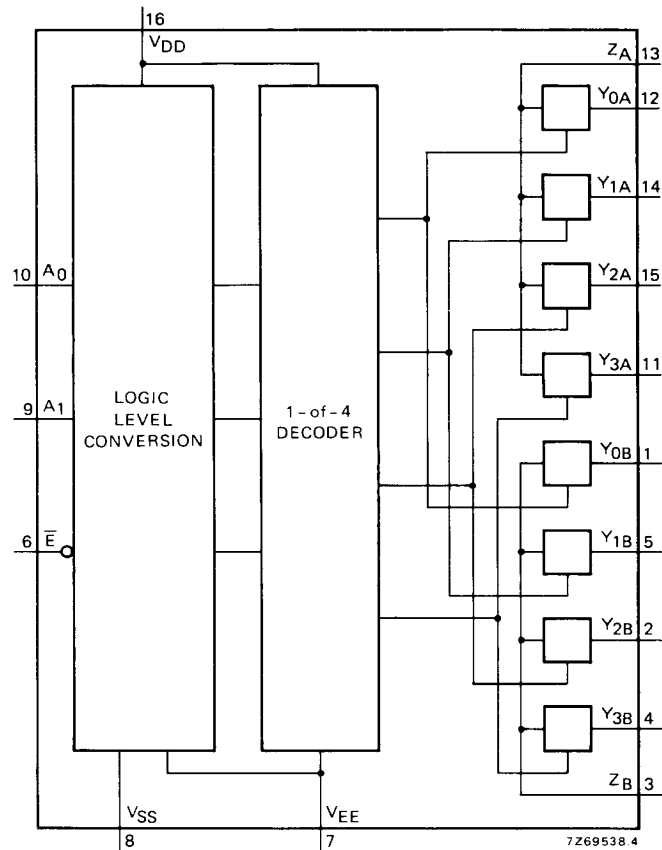
$V_{DD}$  and  $V_{SS}$  are the supply voltage connections for the digital control inputs ( $A_0$ ,  $A_1$  and  $\bar{E}$ ). The  $V_{DD}$  to  $V_{SS}$  range is 3 to 15 V. The analogue inputs/outputs ( $Y_0$  to  $Y_3$ , and  $Z$ ) can swing between  $V_{DD}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{DD} - V_{EE}$  may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to  $V_{SS}$  (typically ground).

Fig. 1 Functional diagram.

### FAMILY DATA

$I_{DD}$  LIMITS category MSI  
see Family Specifications



# HEF4052B

MSI

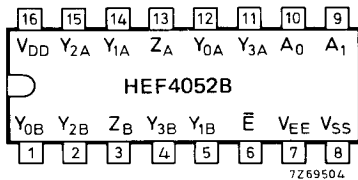


Fig. 2 Pinning diagram.

## PINNING

- Y0A to Y3A independent inputs/outputs
- Y0B to Y3B independent inputs/outputs
- A0, A1 address inputs
- $\bar{E}$  enable input (active LOW)
- Z<sub>A</sub>, Z<sub>B</sub> common inputs/outputs

HEF4052BP : 16-lead DIL; plastic (SOT-38Z).  
 HEF4052BD: 16-lead DIL; ceramic (cerdip) (SOT-74).  
 HEF4052BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

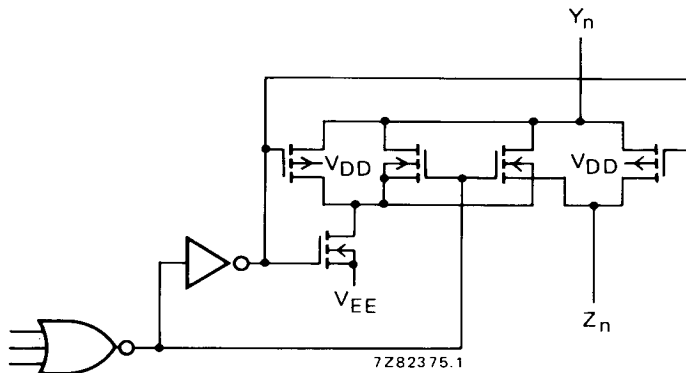


Fig. 3 Schematic diagram (one switch).

## FUNCTION TABLE

inputs			channel ON
$\bar{E}$	A <sub>1</sub>	A <sub>0</sub>	
L	L	L	Y <sub>0A</sub> -Z <sub>A</sub> ; Y <sub>0B</sub> -Z <sub>B</sub>
L	L	H	Y <sub>1A</sub> -Z <sub>A</sub> ; Y <sub>1B</sub> -Z <sub>B</sub>
L	H	L	Y <sub>2A</sub> -Z <sub>A</sub> ; Y <sub>2B</sub> -Z <sub>B</sub>
L	H	H	Y <sub>3A</sub> -Z <sub>A</sub> ; Y <sub>3B</sub> -Z <sub>B</sub>
H	X	X	none

H = HIGH state (the more positive voltage)  
 L = LOW state (the less positive voltage)  
 X = state is immaterial

## RATINGS

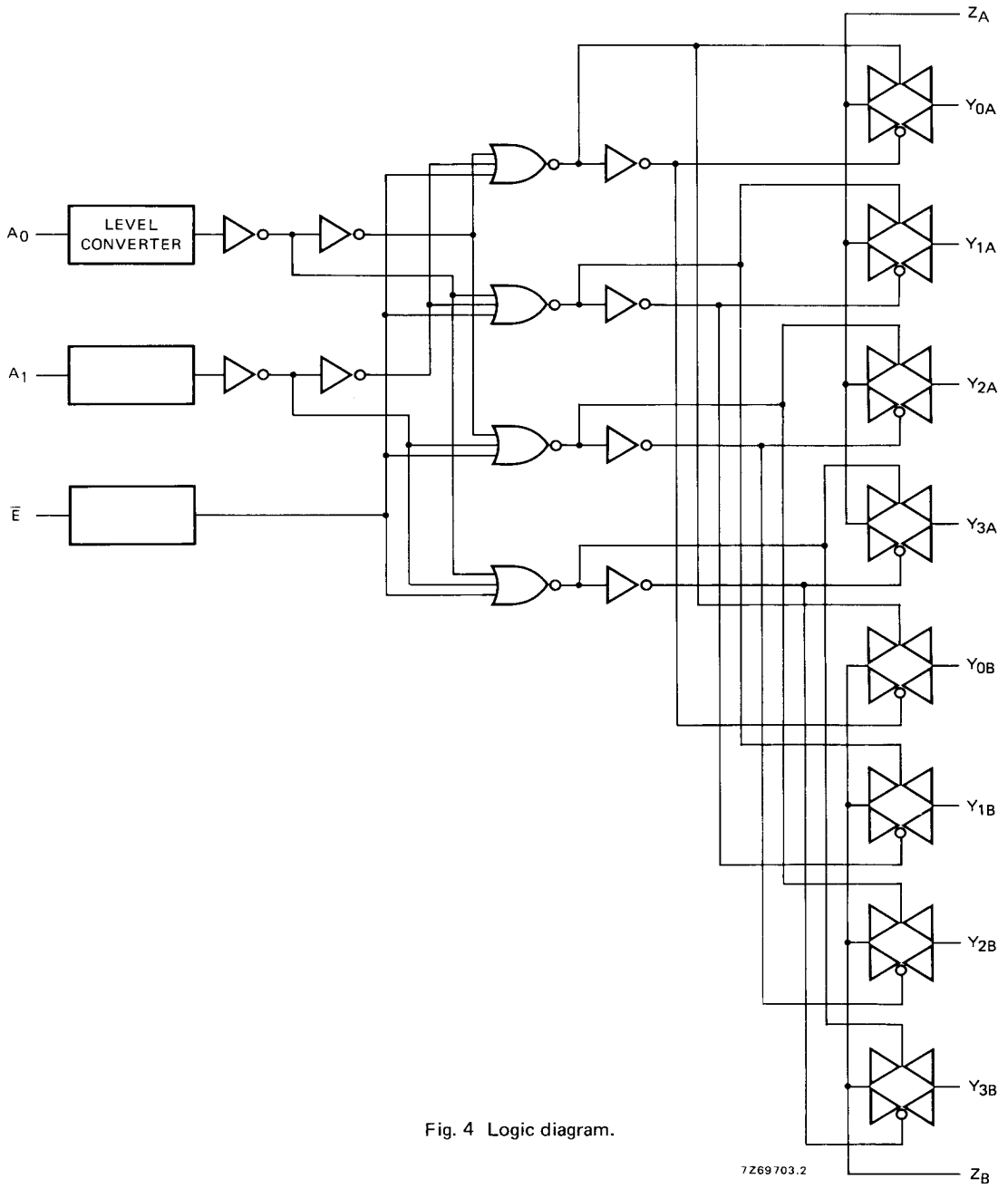
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V<sub>DD</sub>)

V<sub>EE</sub> -18 to +0,5 V

## NOTE

To avoid drawing V<sub>DD</sub> current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V<sub>DD</sub> current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V<sub>DD</sub> or V<sub>EE</sub>.



## D.C. CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.	conditions
ON resistance	5	$R_{ON}$	350	2500	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	
	15		60	175	
ON resistance	5	$R_{ON}$	115	340	} $V_{is} = 0$ see Fig. 6
	10		50	160	
	15		40	115	
ON resistance	5	$R_{ON}$	120	365	} $V_{is} = V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	
	15		50	155	
' $\Delta$ ' ON resistance between any two channels	5	$\Delta R_{ON}$	25	—	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	—	
	15		5	—	
OFF-state leakage current, all channels OFF	5	$I_{OZZ}$	—	—	} $\bar{E}$ at $V_{DD}$
	10		—	—	
	15		—	1000	
OFF-state leakage current, any channel	5	$I_{OZY}$	—	—	} $\bar{E}$ at $V_{SS}$
	10		—	—	
	15		—	200	

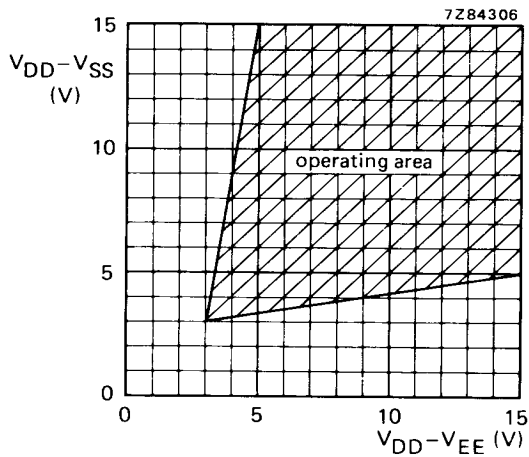


Fig. 5 Operating area as a function of the supply voltages.

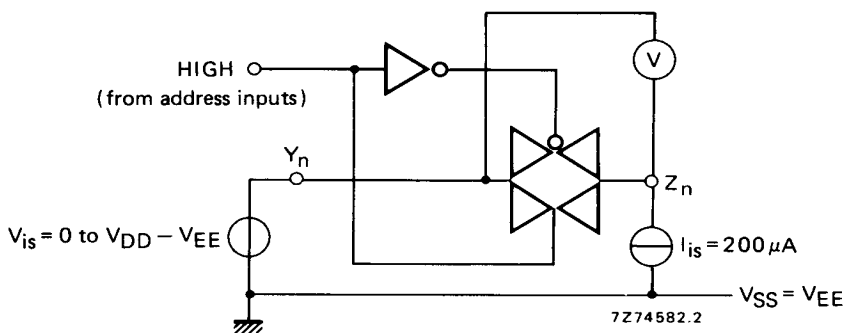


Fig. 6 Test set-up for measuring  $R_{ON}$ .

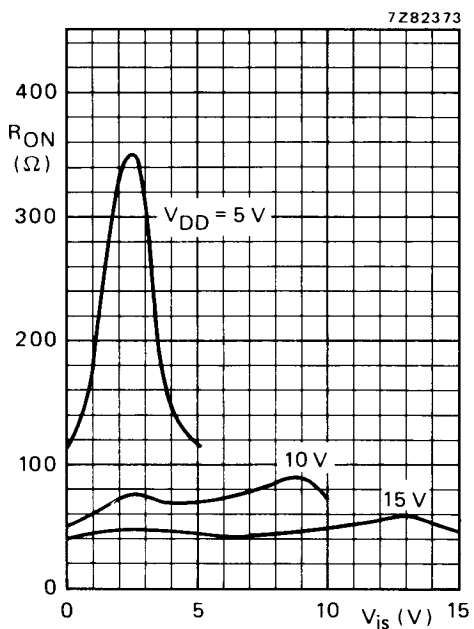


Fig. 7 Typical  $R_{ON}$  as a function of input voltage.  
 $I_{is} = 200 \mu A$   
 $V_{SS} = V_{EE} = 0 V$

## A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; input transition times  $\leq 20 \text{ ns}$ 

	$V_{DD}$ V	typical formula for P ( $\mu\text{W}$ )	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$6\,100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

## A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; input transition times  $\leq 20 \text{ ns}$ 

	$V_{DD}$ V	symbol	typ.	max.		
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	tPHL	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	tPLH	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
$A_n \rightarrow V_{os}$ HIGH to LOW	5	tPHL	150	305	ns	} note 2
	10		65	135	ns	
	15		50	100	ns	
LOW to HIGH	5	tPLH	150	300	ns	} note 2
	10		75	150	ns	
	15		50	100	ns	
Output disable times $\bar{E} \rightarrow V_{os}$ HIGH	5	tPHZ	95	190	ns	} note 3
	10		90	180	ns	
	15		90	180	ns	
LOW	5	tPLZ	100	205	ns	} note 3
	10		90	180	ns	
	15		90	180	ns	
Output enable times $\bar{E} \rightarrow V_{os}$ HIGH	5	tPZH	130	260	ns	} note 3
	10		55	115	ns	
	15		45	85	ns	
LOW	5	tPZL	120	240	ns	} note 3
	10		50	100	ns	
	15		35	75	ns	

## A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	} note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		—	MHz	} note 5
	10		1	MHz	
	15		—	MHz	
Crosstalk; enable or address input to output	5		—	mV	} note 6
	10		50	mV	
	15		—	mV	
OFF-state feed-through	5		—	MHz	} note 7
	10		1	MHz	
	15		—	MHz	
ON-state frequency response	5		13	MHz	} note 8
	10		40	MHz	
	15		70	MHz	

## NOTES

 $V_{is}$  is the input voltage at a Y or Z terminal, whichever is assigned as input. $V_{os}$  is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10\text{ k}\Omega$  to  $V_{EE}$ ;  $C_L = 50\text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{SS}$ ;  $V_{is} = V_{DD}$  (square-wave); see Fig. 8.
- $R_L = 10\text{ k}\Omega$ ;  $C_L = 50\text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{SS}$ ;  $A_n = V_{DD}$  (square-wave);  $V_{is} = V_{DD}$  and  $R_L$  to  $V_{EE}$  for  $t_{PLH}$ ;  $V_{is} = V_{EE}$  and  $R_L$  to  $V_{DD}$  for  $t_{PHL}$ ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$ ;  $C_L = 50\text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{DD}$  (square-wave);  $V_{is} = V_{DD}$  and  $R_L$  to  $V_{EE}$  for  $t_{PHZ}$  and  $t_{PZH}$ ;  $V_{is} = V_{EE}$  and  $R_L$  to  $V_{DD}$  for  $t_{PLZ}$  and  $t_{PZL}$ ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$ ;  $C_L = 15\text{ pF}$ ; channel ON;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $f_{is} = 1\text{ kHz}$ ; see Fig. 9.
- $R_L = 1\text{ k}\Omega$ ;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$ ; see Fig. 10.
- $R_L = 10\text{ k}\Omega$  to  $V_{EE}$ ;  $C_L = 15\text{ pF}$  to  $V_{EE}$ ;  $\bar{E}$  or  $A_n = V_{DD}$  (square-wave); crosstalk is  $|V_{os}|$  (peak value); see Fig. 8.
- $R_L = 1\text{ k}\Omega$ ;  $C_L = 5\text{ pF}$ ; channel OFF;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$ ; see Fig. 9.
- $R_L = 1\text{ k}\Omega$ ;  $C_L = 5\text{ pF}$ ; channel ON;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$ ; see Fig. 9.

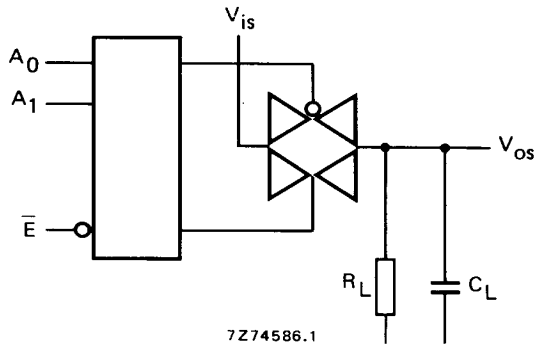


Fig. 8.

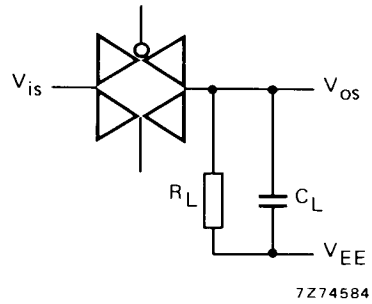


Fig. 9.

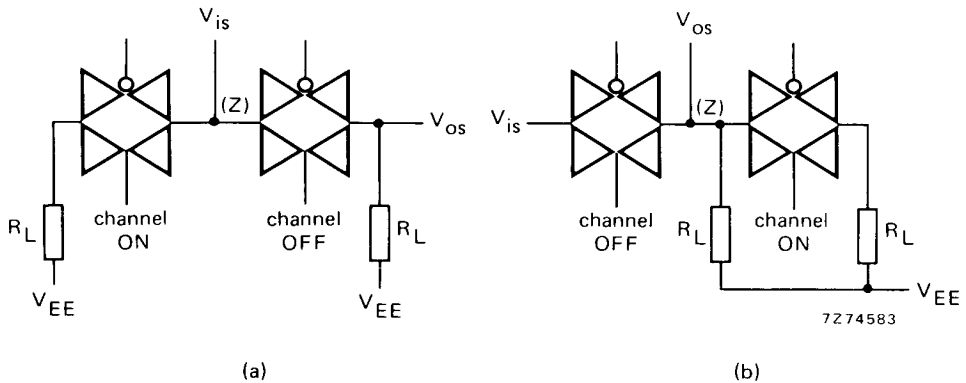


Fig. 10.

**APPLICATION INFORMATION**

Some examples of applications for the HEF4052B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

**NOTE**

If break before make is needed, then it is necessary to use the enable input.