SONY

CXD1186CQ/CR

CD-ROM Decoder

Description

The CXD1186C is a CD-ROM decoder LSI.

Features

- Corresponds to CD-ROM, CD-I and CD-ROM XA formats.
- Real time error correction. (Erasure correction using C2 pointer from CD player.)
- Double speed playback.
- Connection to standard SRAM up to 64 K bytes, as buffer memory, possible.

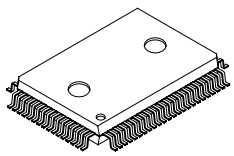
Applications

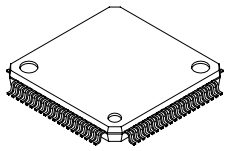
CD-ROM driver

Structure

Silicon gate CMOS IC

CXD1186CQ	CXD1186CR
80 pin QFP (Plastic)	80 pin LQFP (Plastic)





Absolute Maximum Ratings (Ta=25 °C)

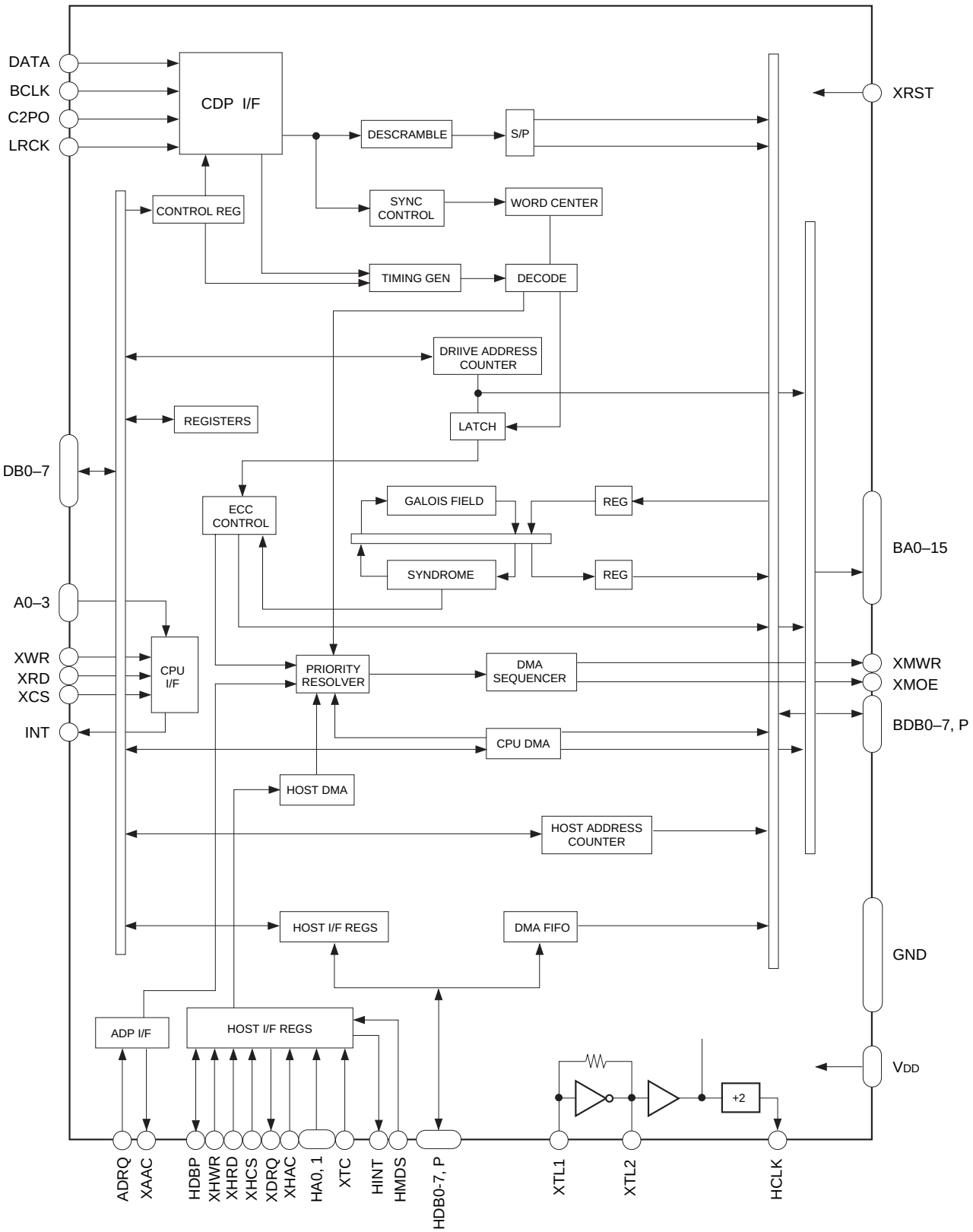
• Supply voltage	V_{DD}	–0.5 to +7.0	V
• Input voltage	V_I	–0.5 to V_{DD} +0.5	V
• Output voltage	V_O	–0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

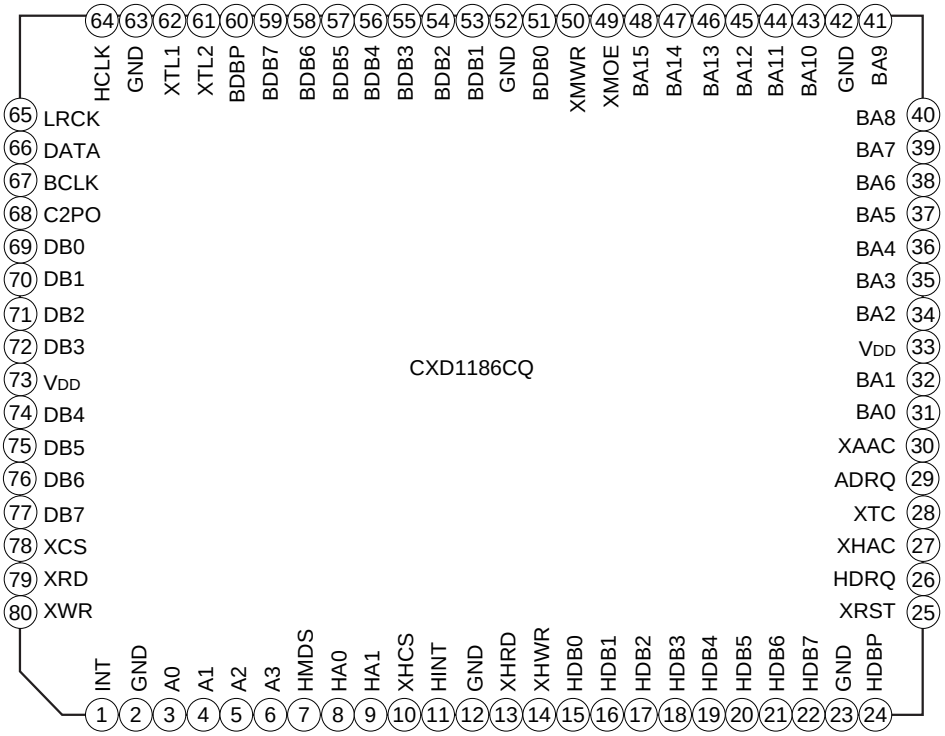
• Supply voltage	V_{DD}	+4.5 to +5.5 (standard +5.0)	V
• Operating temperature	Topr	–20 to +75	°C

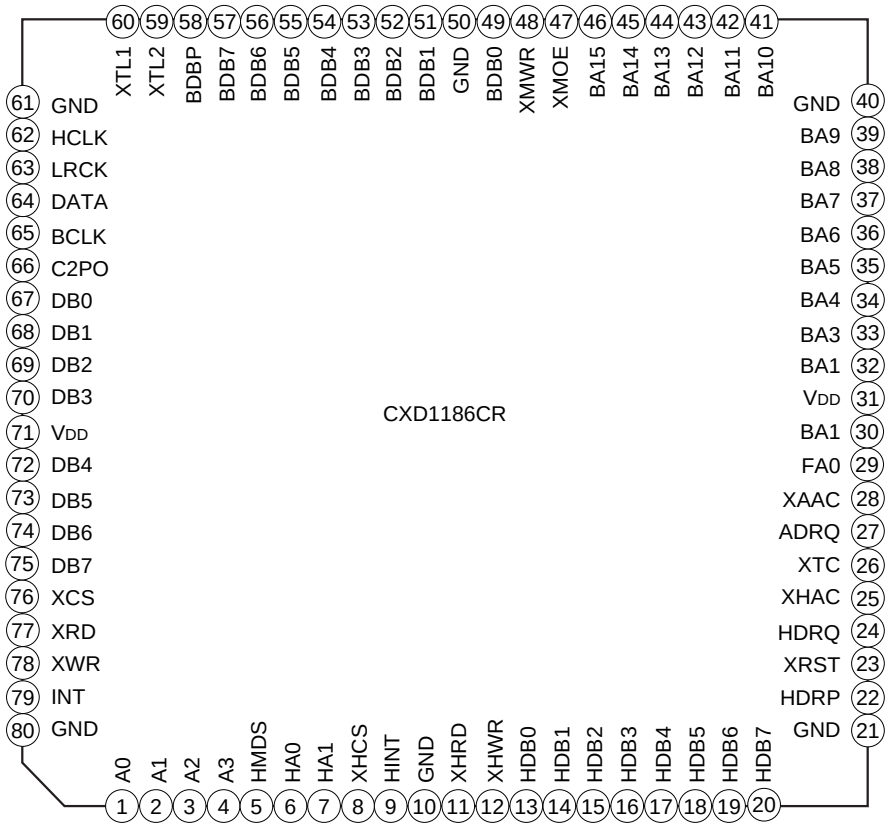
E93512A78-TE

Block Diagram



Pin Configuration





Pin Description

Pin No.		Symbol	I/O	Description
CXD1186CQ	CXD1186CR			
1	79	INT	O	Interrupt request signal to CPU
2	80	GND	—	GND pin
3	1	A0	I	CPU address signal
4	2	A1	I	CPU address signal
5	3	A2	I	CPU address signal
6	4	A3	I	CPU address signal
7	5	HMDS	I	Host mode select signal
8	6	HA0	I	Host address signal
9	7	HA1	I	Host address signal
10	8	XHCS	I	Chip select negative logic signal from host
11	9	HINT	O	Interrupt request negative logic signal to host
12	10	GND	—	GND pin
13	11	XHRD	I/O	Data read strobe signal from host or to SCSI control IC
14	12	XHWR	I/O	Data write strobe signal from host or to SCSI control IC
15	13	HDB0	I/O	Host data bus
16	14	HDB1	I/O	Host data bus
17	15	HDB2	I/O	Host data bus
18	16	HDB3	I/O	Host data bus
19	17	HDB4	I/O	Host data bus
20	18	HDB5	I/O	Host data bus
21	19	HDB6	I/O	Host data bus
22	20	HDB7	I/O	Host data bus
23	21	GND	—	GND pin
24	22	HDBP	I/O	Error flag, Host data bus
25	23	XRST	I	Reset negative logic signal
26	24	HDRQ	O	Data request positive logic signal to host. Or DMA acknowledge negative logic signal to SCSI control IC
27	25	XHAC	I	DMA acknowledge negative logic signal from host. Or data request positive logic signal from SCSI control IC
28	26	XTC	I	Terminal count negative logic signal
29	27	ADRQ	I	DMA request positive logic signal from ADP
30	28	XAAC	O	DMA acknowledge negative logic signal to ADP
31	29	BA0	O	Buffer memory address
32	30	BA1	O	Buffer memory address
33	31	V_{DD}	—	Power (+5 V) supply pin
34	32	BA2	O	Buffer memory address
35	33	BA3	O	Buffer memory address
36	34	BA4	O	Buffer memory address
37	35	BA5	O	Buffer memory address
38	36	BA8	O	Buffer memory address
39	37	BA7	O	Buffer memory address

Pin No.		Symbol	I/O	Description
CXD1186CQ	CXD1186CR			
40	38	BA8	O	Buffer memory address
41	39	BA9	O	Buffer memory address
42	40	GND	—	GND pin
43	41	BA10	O	Buffer memory address
44	42	BA11	O	Buffer memory address
45	43	BA12	O	Buffer memory address
46	44	BA13	O	Buffer memory address
47	45	BA14	O	Buffer memory address
48	46	BA15	O	Buffer memory address
49	47	XMOE	O	Buffer memory output enable negative logic signal
50	48	XMWR	O	Buffer memory write negative logic signal
51	49	BDB0	I/O	Buffer memory data bus
52	50	GND	—	GND pin
53	51	BDB1	I/O	Buffer memory data bus
54	52	BDB2	I/O	Buffer memory data bus
55	53	BDB3	I/O	Buffer memory data bus
56	54	BDB4	I/O	Buffer memory data bus
57	55	BDB5	I/O	Buffer memory data bus
58	56	BDB6	I/O	Buffer memory data bus
59	57	BDB7	I/O	Buffer memory data bus
60	58	BDBP	I/O	Buffer memory pointer data bus
61	59	XTL2	O	Crystal oscillation circuit output pin
62	60	XTL1	I	Crystal oscillation circuit input pin
63	61	GND	—	GND pin
64	62	HCLK	O	1/2 frequency divided clock signal of XTL1
65	63	LRCK	I	LR clock from CD player
66	64	DATA	I	Serial data from CD player
67	65	BCLK	I	Bit clock from CD player
68	66	C2PO	I	C2 pointer from CD player
69	67	DB0	I/O	CPU data bus
70	68	DB1	I/O	CPU data bus
71	69	DB2	I/O	CPU data bus
72	70	DB3	I/O	CPU data bus
73	71	V_{DD}	—	Power (+5 V) supply pin
74	72	DB4	I/O	CPU data bus
75	73	DB5	I/O	CPU data bus
76	74	DB6	I/O	CPU data bus
77	75	DB7	I/O	CPU data bus
78	76	XCS	I	Chip select negative logic signal from CPU
79	77	XRD	I	CPU strobe negative logic signal to read out this IC internal register
80	78	XWR	I	CPU strobe negative logic signal to write in this IC internal register

Electrical Characteristics

DC characteristics

(V_{DD}=5 V±10 %, V_{SS}=0 V, Topr=–20 to +75 °C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH1}		2.2			V
	L level	V_{IL1}				0.8	V
TTL Schmitt hysterisis		$(V_{t+})-(V_{t-})$		0.2	0.4		V
Input current of pull up input		I_{IL}	V_{IL}=0 V	–40	–100	–240	µA
Input current of pull down input		I_{IH}	$V_{IH}=V_{DD}$	40	100	240	µA
Output voltage	H level	V_{OH1}	I_{OH}=–2 mA	V_{DD}–0.8			V
	L level	V_{OL1}	I_{OL}=4 mA			0.4	V
Open drain output L level		V_{OL2}	I_{OL}=4 mA			0.4	V
Oscillation cell input voltage	H level	V_{IH}		0.7 V_{DD}			V
	L level	V_{IL}				0.3 V_{DD}	V
Logic threshold value		LV_{th}			V_{DD}/2		V
Feedback resistance		R_{FB}	$V_{IN}=V_{SS}$ or V_{DD}	250 k	1 M	2.5 M	Ω
Output voltage	H level	V_{OH}	I_{OH}=–1 mA	V_{DD}/2			V
	L level	V_{OL}	I_{OL}=1 mA			V_{DD}/2	V

- Input pin with pull up resistance : XHCS, HA0, HA1, XTC
- Input pin with pull down resistance : C2PO, HMDS, ADRQ
- TTL Schmitt input pin : XRST
- Open drain output pin : HINT
- Two-way data bus always pulled up.
- Oscillation cell

  Input : XTL1

  Output : XTL2

I/O capacitance

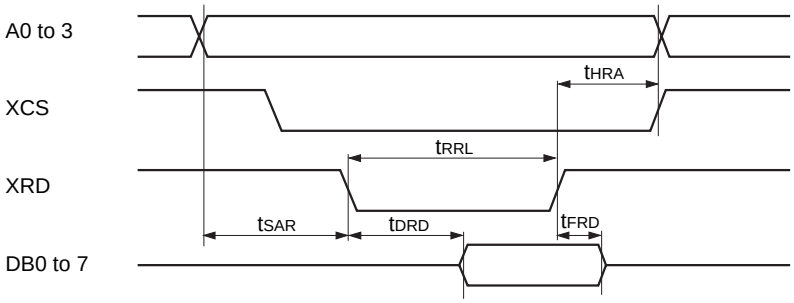
$V_{DD}=V_I$=0 V, f=1 MHz

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
I/O pin	$C_{I/O}$			11	pF

AC characteristics (Ta=–20 to +75 °C, V_{DD}=5 V±10 %, Output Load=50 pF, f≤ 24.576 MHz)

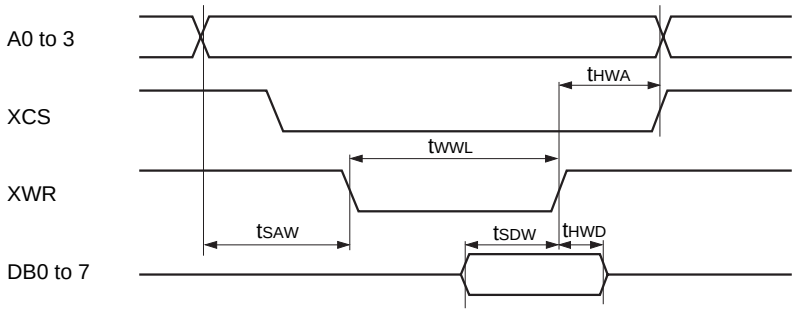
1. CPU interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XCS & XRD ↓)	t_{SAR}	30			n
Address hold time (vs. XCS & XRD ↑)	t_{HRA}	20			n
Data delay time (vs. XCS & XRD ↓)	t_{DRD}			60	n
Data float time (vs. XCS & XRD ↑)	t_{FRD}	0		10	n
Low level XRD pulse width	t_{RRL}	100			n

(2) Write

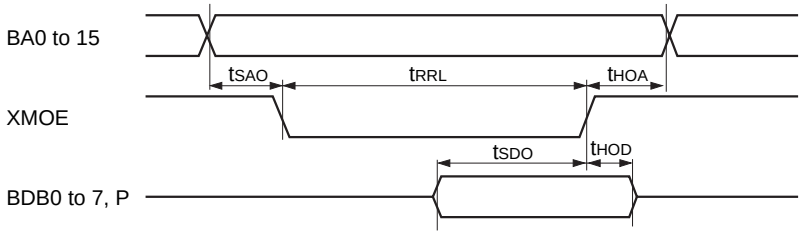


Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XCS & XWR ↓)	t_{SAW}	30			n
Address hold time (vs. XCS & XWR ↑)	t_{HWA}	20			n
Data setup time (vs. XCS & XWR ↑)	t_{SDW}	40			n
Data hold time (vs. XCS & XWR ↑)	t_{HWD}	10			n
Low level XWR pulse width	t_{WWL}	50			n

Where & in the chart indicates logical multiplication.

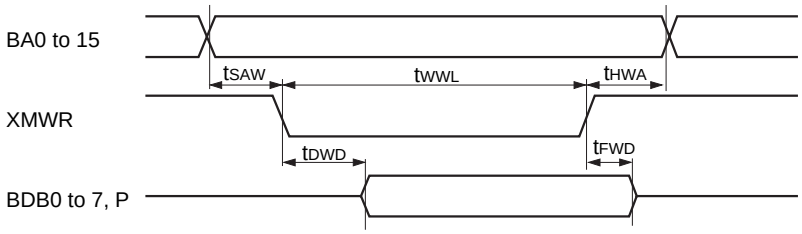
2. Memory interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XMOE ↓)	t_{SAO}	Tw–22			n
Address hold time (vs. XMOE ↑)	t_{HOA}	Tw–9			n
Data setup time (vs. XMOE ↑)	t_{SDO}	45			n
Data hold time (vs. XMOE ↑)	t_{HOD}	0			n
Low level XMOE pulse width	t_{RRL}	2 • Tw		2•Tw+16	n

(2) Write



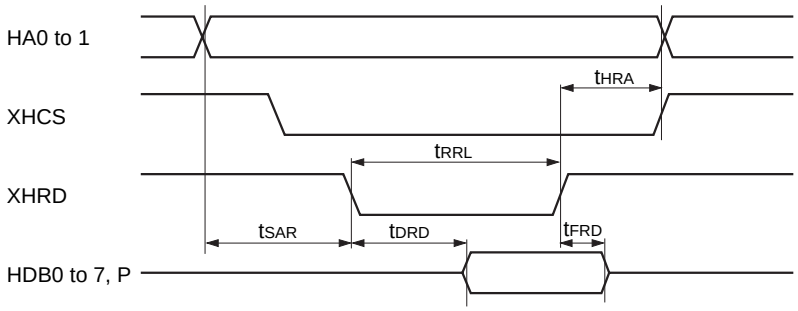
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XMWR ↓)	t_{SAW}	Tw–29			n
Address hold time (vs. XMWR ↑)	t_{HWA}	Tw–9			n
Data delay time (vs. XMWR ↓)	t_{DWD}			0	n
Data float time (vs. XMWR ↑)	t_{FWD}	10			n
Low level XMWR pulse width	t_{WWL}	2 • Tw			n

Where Tw=1/f.

Usually, when f=16.9344 MHz, use a RAM with access time within 120 ns.

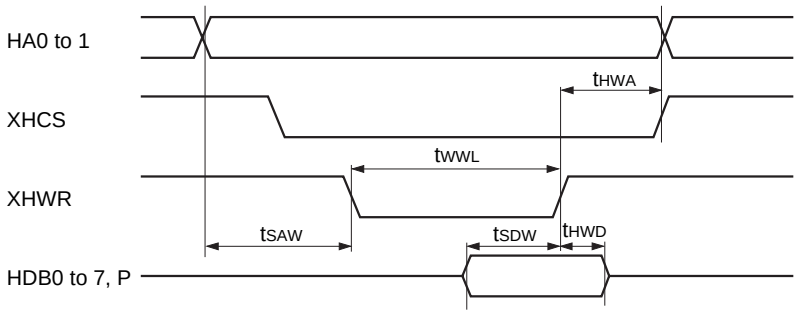
3. Host interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XHCS & XHRD ↓)	t_{SAR}	30			n
Address hold time (vs. XHCS & XHRD ↑)	t_{HRA}	20			n
Data delay time (vs. XHCS & XHRD ↓)	t_{DRD}			60	n
Data float time (vs. XHCS & XHRD ↑)	t_{FRD}	0		10	n
Low level XHRD pulse width	t_{RRL}	100			n

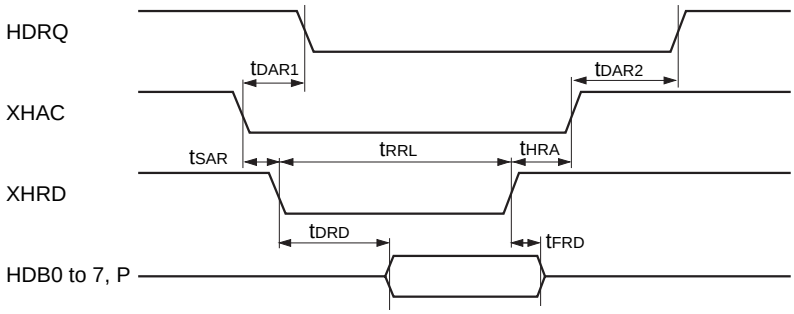
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XHCS & XHWR ↓)	t_{SAW}	30			n
Address hold time (vs. XHCS & XHWR ↑)	t_{HWA}	20			n
Data setup time (vs. XHCS & XHWR ↑)	t_{SDW}	40			n
Data hold time (vs. XHCS & XHWR ↑)	t_{HWD}	10			n
Low level XHWR pulse width	t_{WWL}	50			n

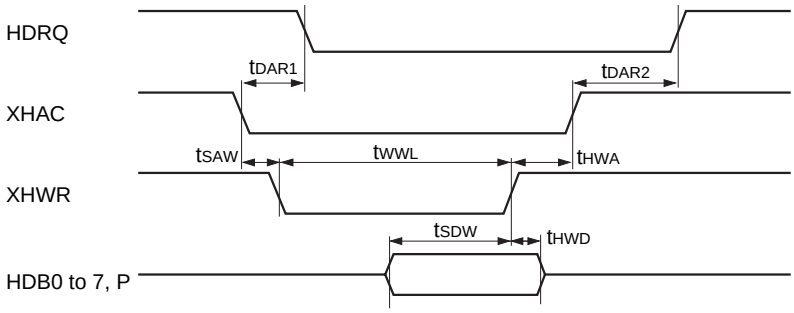
4. HOST DMA cycle (80 type bus)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (vs. XHAC ↓)	t_{DAR1}			35	n
HDRQ rise time (vs. XHAC ↑)	t_{DAR2}			48	n
XHAC setup time (vs. XHRD ↓)	t_{SAR}	5			n
XHAC hold time (vs. XHRD ↑)	t_{HRA}	0			n
Low level XHRD pulse width	t_{RRL}	100			n
Data delay time (vs. XHRD ↓)	t_{DRD}			60	n
Data float time (vs. XHRD ↑)	t_{FRD}	0		10	n

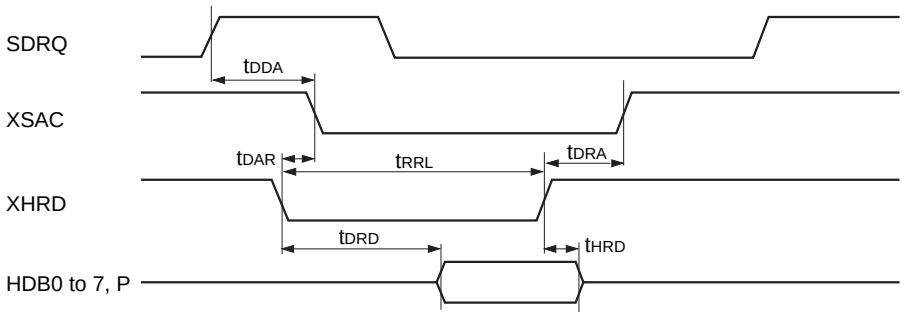
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (vs. XHAC ↓)	t_{DAR1}			35	n
HDRQ rise time (vs. XHAC ↑)	t_{DAR2}			48	n
XHAC setup time (vs. XHWR ↓)	t_{SAW}	5			n
XHAC hold time (vs. XHWR ↑)	t_{HWA}	0			n
Low level XHWR pulse width	t_{WWL}	50			n
Data setup time (vs. XHWR ↑)	t_{SDW}	40			n
Data hold time (vs. XHWR ↑)	t_{HWD}	10			n

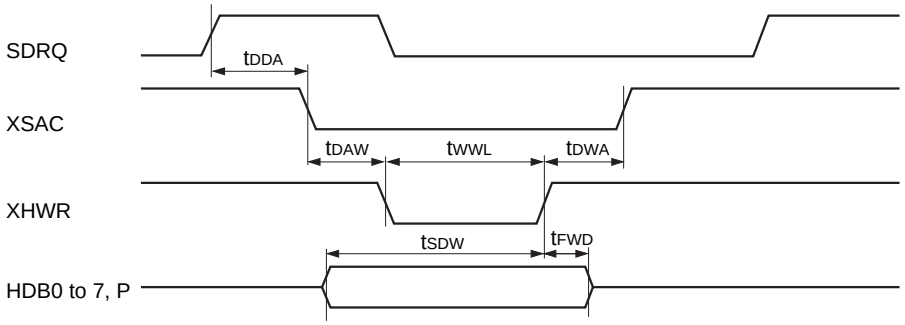
5. HOST DMA cycle (SCSI bus)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall time (vs. SDRQ ↑)	t_{DDA}			Tw	n
XSAC delay time (vs. XHRD ↓)	t_{DAR}	0			n
XSAC delay time (vs. XHRD ↑)	t_{DRA}			Tw	n
Low level XHRD pulse width	t_{RRL}	T+59			n
Data delay time (vs. XHRD ↓)	t_{DRD}			90	n
Data hold time (vs. XHRD ↑)	t_{HRD}	0			n

(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall time (vs. SDRQ ↑)	t_{DDA}			Tw	n
XHWR delay time (vs. XSAC ↓)	t_{DAW}			Tw	n
XSAC delay time (vs. XHWR ↑)	t_{DWA}			Tw	n
Low level XHWR pulse width	t_{WWL}	T			n
Data setup time (vs. XHWR ↓)	t_{SDW}	T+24			n
Data float time (vs. XHWR ↓)	t_{FWD}	27			n

Where T in the chart indicates :

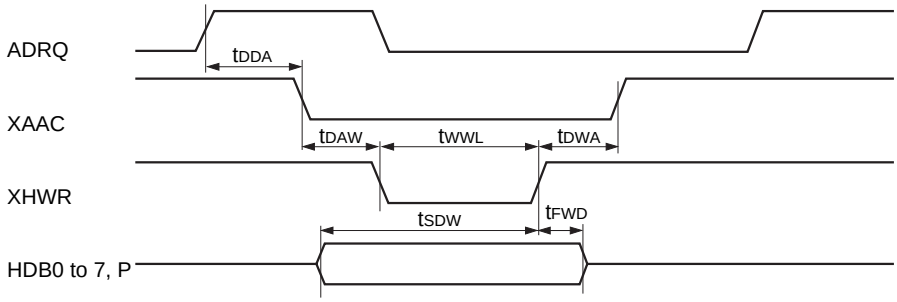
Tw for 3 cycle mode

2 • Tw for 4 cycle mode

3 • Tw for 5 cycle mode

Here Tw=1/f

6. ADPCM DMA cycle



Item	Symbol	Min.	Typ.	Max.	Unit
XAAC fall time (vs. ADRQ ↑)	t_{DDA}			Tw	n
XHWR delay time (vs. XAAC ↓)	t_{DAW}			Tw	n
XAAC delay time (vs. XHWR ↑)	t_{DWA}			Tw	n
Low level XHWR pulse width	t_{WWL}	T			n
Data setup time (vs. XHWR ↓)	t_{SDW}	T+24			n
Data float time (vs. XHWR ↓)	t_{FWD}	27			n

Where T in the chart indicates :

Tw for 3 cycle mode

2 • Tw for 4 cycle mode

3 • Tw for 5 cycle mode

Here Tw=1/f

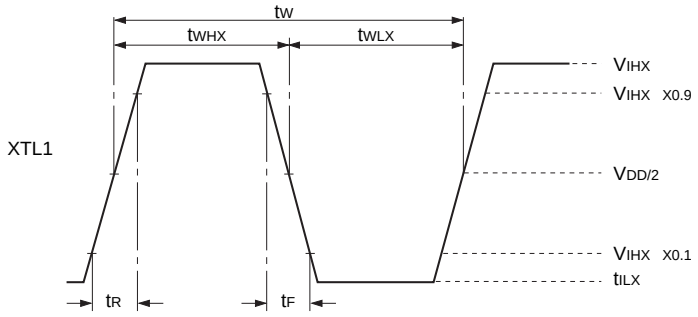
7. XTL1 and XTL2 pins

(1) For self oscillation (Topr=–20 to +75 °C, V_{DD}=5.0 V±10 %)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	16.9344		24.576	MHz

(2) When a pulse is input to XTL1 (Topr=–20 to +75 °C, V_{DD}=5.0 V±10 %)

Item	Symbol	Min.	Typ.	Max.	Unit
“H” level pulse width	t_{WHX}	15			ns
“L” level pulse width	t_{WLX}	15			ns
Pulse period	t_W	40.7			ns
Input “H” level	V_{IHX}	V_{DD}—1.0			V
Input “L” level	V_{ILX}			0.8	V
Rise time, Fall time	t_R, t_F			15	ns



Description of Function

1. Pin description

Below is a description of pins by function.

1.1 CD player interface (4 pins)

(1) DATA (input)
Serial data from CIRC LSI (digital signal processing LSI for CD)

(2) BCLK (input)
Bit clock. Clock for DATA Strobe.

(3) LRCK (input)
LR clock. Indicates LCH and RCH of DATA input.

(4) C2PO (positive logic input)
C2 pointer signal from CIRC. Indicates an error is included in the DATA input.
Interface mode with the CD player is controlled at DRVIF register.

1.2 Buffer memory interface (27 pins)

(1) XMWR (memory write, negative logic output)
Data write strobe signal of the buffer memory.

(2) XMOE (memory output enable, negative logic output)
Data read strobe signal of the buffer memory.

(3) BA0 to 15 (Buffer memory address, output)
Address signal of the buffer memory.

(4) BDB0 to 7 (Buffer data bus, I/O)
Data bus signal of the buffer memory.

(5) BDBP (Buffer data bus, I/O)
Buffer memory data bus signal for error pointer.

1.3 CPU interface (16 pins)

(1) XWR (CPU write, negative logic input)
Write strobe signal of the CPU register.

(2) XRD (CPU read, negative logic input)
Read out strobe signal of the CPU register.

(3) XCS (CPU chip select, negative logic input)
Chip select negative logic signal from the CPU.

(4) A0 to 3 (CPU address, input)
Address signal for the CPU selection of the IC internal register.

(5) DB0 to 7 (CPU data bus, I/O)
CPU data bus signal.

(6) INT (CPU interrupt, output)
Interrupt request output to the CPU. This pin polarity is controlled at the CONFIG register.

1.4 Host interface (19 pins)

(1) HMDS (Host mode select, input)
Signal for the host mode selection. This pin is pulled down inside the IC by means of a resistor at a standard 50 kΩ.
"L" or open : connected to Intel 80 type host Bus.
"H" : connected to SCSI controller IC.

(2) HDRQ/XSAC (Host data request/SCSI acknowledge, output)
When HMDS is at "L", DMA data request positive logic signal to host.
When HMDS is at "H", DMA acknowledge negative logic signal to SCSI control IC.

(3) XHAC/SDRQ (Host DMA acknowledge/SCSI data request, input)
When HMDS is at “L”, DMA acknowledge negative logic signal from host.
When HMDS is at “H”, DMA data request positive logic signal from SCSI control IC.
(4) XHWR (Host write, negative logic I/O)
When HMDS is at “L” and ADMAEN (DMACTL register, bit4) also at “L”, data write strobe input from host.
When HMDS is at “H” and ADMAEN at “L”, data write strobe output to SCSI control IC.
When ADMAEN is at “H”, data write strobe output to audio processor (ADP).
(5) XHRD (Host read, negative logic I/O)
When HMDS is at “L” and ADMAEN also at “L”, data read strobe input from host.
When HMDS is at “H” and ADMAEN at “L”, data read strobe output to SCSI control IC.
When ADMAEN is at “H”, data read strobe output to ADP.
(6) XHCS (Host chip select, negative logic input)
This pin is pulled up inside the IC by means of a resistor at a standard 50 kΩ.
When HMDS is at “L”, chip select input from host.
When HMDS is at “H”, this signal is not used. Either fix to “H” or keep open.
(7) HA0 and 1 (Host address, input)
These pins are pulled up inside the IC by means of a resistor at a standard 50 kΩ.
When HMDS is at “L”, address input from the host.
When HMDS is at “H”, these signals are not used. Either fix to “H” or keep open.
(8) HDB0 to 7 (Host data bus, I/O)
Host data bus signal.
(9) HDBP (Host data bus, I/O)
Host data bus signal for error pointer.
(10) HINT (HOST interrupt, output)
This pin is an open drain output.
When HMDS is at “L”, interrupt request negative logic output to host.
When HMDS is at “H”, this signal is not used.
(11) XTC (Terminal count, negative logic output)
This is pulled up inside the IC by means of a resistor at a standard 50 kΩ.
When HMDS is at “L”, data transfer complete instruction negative logic input from the host.
When HMDS is at “H”, this signal is not used. Either fix to “H” or keep open.

1.5 Audio processor (ADP) interface (2 pins)
(1) ADRQ (audio processor DMA request, positive logic input)
This pin is pulled down inside the IC by means of a resistor at a standard 50 kΩ.
DMA data request signal to ADP. When not connected to ADP and CXD1186Q, either fix to “L” or keep open.
(2) XAAC (audio processor DMA acknowledge, negative logic output)
DMA acknowledge signal from ADP.

1.6 Others (4 pins)
(1) XTL1 (Crystal1, input)
(2) XTL2 (Crystal2, output)
Crystal oscillator connecting pin for master clock oscillation.
(3) HCLK (halfclock, output)
Half frequency divided clock of the master clock.
(4) XRST (Reset, negative logic input)
Chip reset signal.

Pins BDB0 to 7, BDBP, DB0 to 7, HDB0 to 7 and HDBP are pulled up inside the IC by means of a resistor at a standard 25 kΩ.

2. Register function

This IC is controlled from the CPU by means of 19 registers for each of write and read, respectively.

2.1 Write register

2.1.1 Drive Interface (DRVIF) register

bit0 : DIGIN (Digital IN)

"H" ; When Digital In (See fig. 2.1.1) is connected, this bit is set to "H".

"L" ; When connected to CIRC LSI, this bit is set to "L".

bits 2 to 5 are effective only when DIGIN is at "L".

bit1 : LSB1ST (LSB First)

"H" ; When data is connected to CIRC LSI output through LSB first, this bit is set to "H".

"L" ; When data is connected to CIRC LSI output through MSB first, this bit is set to "L".

bits2 and 3 : BCKMD 0, 1 (BCLK mode 0, 1)

These bits are set according to the number of BCLK clocks output during one word by CIRC LSI.

BCKMD 1	BCKMD 0	
"L"	"L"	16BCLKs/Word
"L"	"H"	24BCLKs/Word
"H"	"X"	32BCLKs/Word

Moreover, when there are 24 or 32 clocks within 1 word, the 16 bits of data before LRCK edge, become effective.

bit4 : BCKRED (BCLK Rising Edge)

"H" ; Data is strobed with BCLK rise.

"L" ; Data is strobed with BCLK fall.

bit5 : LCHLOW (LCH LOW)

"H" ; When LRCK is at "L", it is determined to be LCH data.

"L" ; When LRCK is at "H", it is determined to be LCH data.

∗1. When DIGIN="H", We automatically have LSBIST=BCKMD1="H", BCKRED=LCHLOW="L".

bit6 : DBLSPD (Double Speed)

"H" ; At double speed PB, this bit is set to "H".

"L" ; At normal speed PB, this bit is set to "L".

bit7 : C2PLIST (C2PO Lower-byte 1st)

"H" ; When 2 bytes of data are input to C2PO, the Lower-byte and the upper-byte are input in the order.

"L" ; When 2 bytes of data are input to C2PO, the Upper-byte and the lower-byte are input in the order.

Table 2.1.1 indicates the setting value of bits 0 to 7 when Sony-made CIRC LSI is connected. Fig. 2.1.1 (1) to (4) indicates the input timing chart.

Here, the upper byte means the upper 8 bits including MSB from CIRC LSI, Lower byte indicates the lower 8 bits including LSB from CIRC LSI.

Changes in value for the respective bits in this register have to be executed in the decoder disable condition.

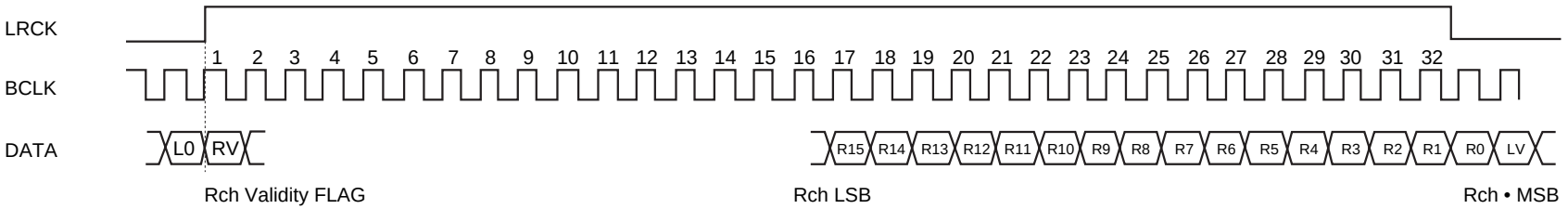


Fig. 2.1.1 (1) Digital In Timing Chart (C2PO don't care, no need for connection)

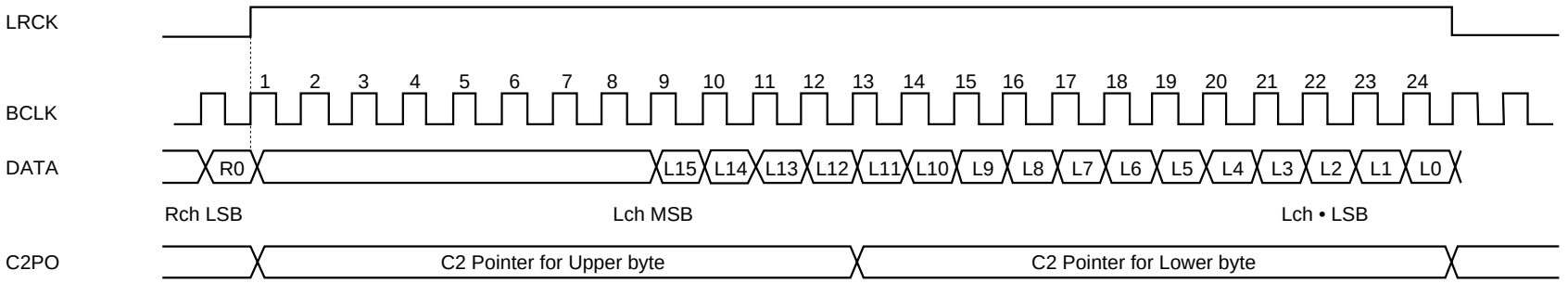


Fig. 2.1.1 (2) CDL30, 35 Series, Timing Chart

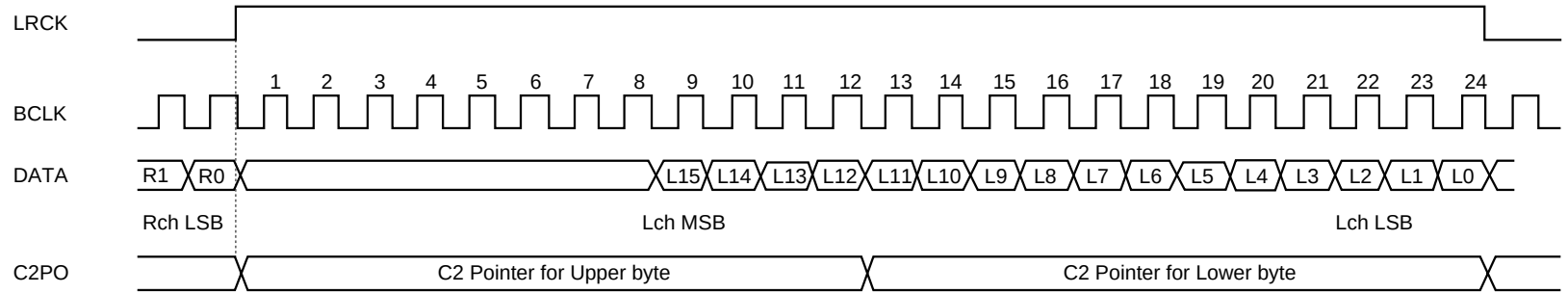


Fig. 2.1.1 (3) CXD2500Q, 48 bit Slot Mode Timing Chart

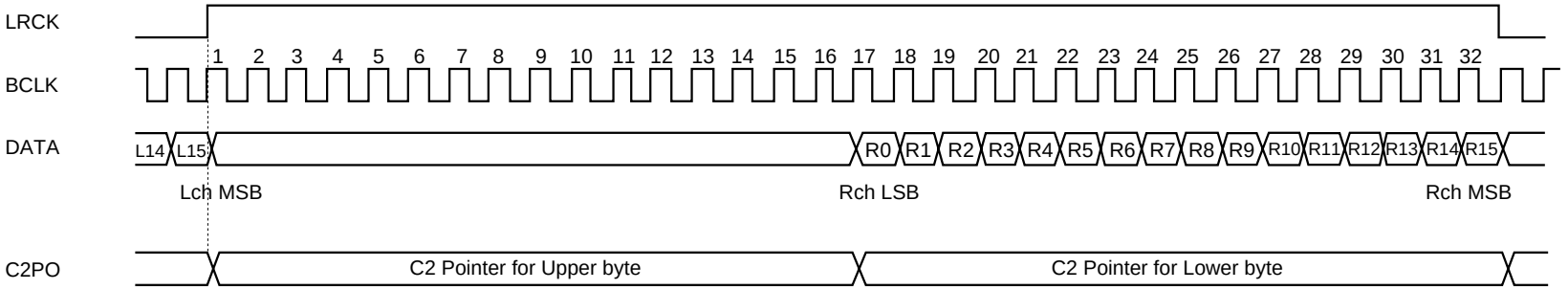


Fig. 2.1.1 (4) CXD2500Q, 64 bit Slot Mode Timing Chart

Table 2.1.1 DRVIF Register setting value

Sony-made CIRC LSI	DRV IF Register								Timing chart
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
CDL30 series CDL35 series	L	*	L	L	L	H	L	L	Fig. 2.1.1 (2)
CDL40 series (48 bit slot mode)	L	*	L	H	L	H	L	L	Fig. 2.1.1 (3)
CDL40 series (64 bit slot mode)	L	*	H	L	H	X	H	L	Fig. 2.1.1 (4)

(Note 1) * at normal speed PB set to "L", at double speed PB set to "H".

(Note 2)

CDL30 series	CXD1125Q/QZ, CXD1130Q/QZ, CXD1135Q/QZ, CXD1241Q/QZ, CXD1245Q, CXD1246Q/QZ, CXD1247Q/QZ/R and others.
CDL35 series	CXD1165Q, CXD1167Q/QZ/R and others.
CDL40 series	CXD2500Q/QZ and others.

2.1.2 Decoder Control (DECCTL) register

bits0 to 2 : DECMDSL2, 1, 0
(Decoder Mode Select 2, 1, 0)

DECMDSL2	1	0	
"L"	"L"	"X"	Decoder disable
"L"	"H"	"X"	Monitor only mode
"H"	"L"	"L"	Write only mode
"H"	"L"	"H"	Real time correction mode
"H"	"H"	"L"	Repeat correction mode
"H"	"H"	"H"	CD-DA mode

bit3 : AUTODIST (Auto Distinction)

"H" ; Error Correction performed according to the Mode byte and FORM bit read from Drive.

"L" ; Error Correction is performed according to the following MODESEL and FORMSEL bits.

bit4 : FORMSEL (Form Select)

bit5 : MODESEL (Mode Select)

When AUTODIST is at "L" the sector is corrected as the following MODE or FORM.

MODESEL	FORMSEL	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit6 : ECCSTR (ECC Strategy)

"H" ; Error Correction is performed with consideration to respective data error flag.

"L" ; Error Correction is performed without consideration to respective data error flag. When an 8 bit/Word RAM is connected, turn this bit to "L".

bit7 : ENDLADR (Enable DLADR)

"H" ; When this bit is set to "H", DLADR is enabled.
When, either write only mode, real time correction, or CD-DA mode is being executed, the decoder stops the buffer write as DADRC and DLADR turn equal.

"L" ; When this bit is set to "L", DLADR is disabled.
During the execution of write only mode or real time correction, even if DADRC and DLADR turn equal, the decoder does not stop buffer write.
(See paragraph 4 for details)

2.1.3 DMA Control (DMACTL) register

bit0 : HSRC (Host Source)
- "H" ; Data is transferred from the host to the buffer memory.
- "L" ; Data is transferred from the buffer memory to the host.

bit1 : HDMAEN (HOST DMA Enable)
- "H" ; DMA of the host port is enabled.
- "L" ; DMA of the host port is prohibited.

bit2 : ENXTC (Enable XTC)
- "H" ; DMA completion of the host port through XTC pin input is enabled.
- "L" ; DMA completion of the host port through XTC pin input is disabled.

bit3 : ENHXFRC (Enable XHFRC)
- "H" ; DMA completion of the host port through HXFRC is enabled.
- "L" ; DMA completion of the host port through HXFRC is disabled.

bit4 : ADMAEN (ADP DMA Enable)
- "H" ; DMA of the audio processor port is enabled.
- "L" ; DMA of the audio processor port is prohibited.

Also, prohibits turning HDMAEN and ADMAEN simultaneously to "H".

bit5 : CSRC (CPU Source)
- "H" ; Data is transferred from the CPU to the buffer memory.
- "L" ; Data is transferred from the buffer memory to the CPU.

bit6 : CDMAEN (CPU DMA Enable)
- "H" ; DMA of the CPU port is enable.
- "L" ; DMA of the CPU port is prohibited.

bit7 : RESERVED
Unused, Keep set to "L".

2.1.4 Configuration (CONFIG) register

bit0 : RESERVED
Unused, Keep set to "L".

bits1 and 2 : SDMACYC1, 0 (SCSI DMA CYCLE)
DMA transfer between this IC, SCSI control IC and ADPCM processor is executed in the following cycle.

SDMACYC1	0	
"L"	"L"	3 cycle.
"L"	"H"	4 cycle.
"H"	"X"	5 cycle.

bit3 : SBSCTL (SCSI Bus Control)
Setting this bit to "H" forces XHWR, XHRD, HDB0 to 7 and HDBP into high impedance condition.

bit4 : CINTPOSI (CPU Interrupt Positive)
- "H" ; INT pin turns to High active.
- "L" ; INT pin turns to Low active.

bit5 : 9 BITRAM
- "H" ; When a 9 bit/word RAM is connected, this bit is turned to "H".
- "L" ; When a 8 bit/word RAM is connected, this bit is turned to "L".

bits6 and 7 : RESERVED
Unused, Keep set to "L".

2.1.5 Interrupt Mask (INTMSK) register

Turning the respective bits of the register to “H” enables interrupt request from this IC to the CPU by means of the corresponding interrupt status. (That is, when interrupt status is turned on, INT pin is activated) The value of the respective bits in this register does not affect the corresponding interrupt status.

bit0 : DECINT (Decoder interrupt)
When the Decoder is executing one of the respective modes, write only, monitor, or real time correction, if Sync mark is detected or introduced, DECINT status is turned on. However, When Sync detection window is open, if sync interval is less than 2352 bytes, Decint status is not turned on.
Also, when Decoder repeat correction mode is being executed, everytime one correction is completed DECINT status is turned on.

bit1 : HDMACMP (Host DMA Complete)
When DMA of the host port is completed through HXFRC or XTC pins, HDMACMP status is turned on.

bit2 : DRVOVRN (Drive Over Run)
When ENDLADR bit (bit7) of DECCTL register is set to “H”, and the DECODER has executed write only, real time correction mode or CD-DA mode, as DADRC and DLADR become equal, DRVOVRN status is turned on.
However, in CD-DA mode, even when ENDLADR bit is turned to “L”, DRVOVRN status is turned on.

bit3 : HSTCMND (Host Command)
As the host writes a command in the Command register, HSTCMND status is turned on.

bit4 : HCRISD (Host Chip Reset Issued)
By having the host write “H” in CHPRST bit (bit7) of the Control register, this IC is reset and HCRISD status is turned on.

bit5 : RSLTEMPT (Result Empty)
When the host reads the Result register, and the Result register becomes empty, RSLTEMPT status turns on.

bit6 : DECTOUT (Decoder Timeout)
After setting the Decoder to either, monitor only, write only or real time correction modes, if, even after the time of three sectors (normal speed PB 40.6 ms) passes, sync is not detected, then DECTOUT status is turned on.

2.1.6 Clear Interrupt Status (INTCLR) register

When any of the respective bits of this register is set to “H”, the corresponding interrupt status is cleared.
After the interrupt status clearance, the bit automatically turns to “L”. Accordingly there is no need for the CPU to set to “L” again.

bit0 : DECINT (Decoder Interrupt)
bit1 : HDMACMP (Host DMA Complete)
bit2 : DRVOVRN (Drive Over Run)
bit3 : HSTCMND (Host Command)
bit4 : HCRISD (Host Chip Reset Issued)
bit5 : RSLTEMPT (Result Empty)
bit6 : DECTOUT (Decoder Timeout)

2.1.7 Drive • Last • Address • Low (DLADR-L) register

2.1.8 Drive • Last • Address • High (DLADR-H) register

When the Decoder is executing either of write only, real time correction mode or CD-DA mode, CPU sets the last address that writes into the buffer, data from the drive. When ENDLADR bit of DECCTL register is set to "H" and the Decoder is executing the above modes, if data from the drive is written into the buffer at the address specified from DLADR, all writing into the buffer is prohibited after that.

2.1.9 Drive • Address • Low (DADRC-L) counter

2.1.10 Drive • Address • Counter High (DADRC-H)

This counter keeps the address that writes data from the drive into the buffer. When drive data is written into the buffer, DADRC contents are output form BA0 to 15. For every byte written in the buffer, DADRC is incremented. Before the Decoder executes either write only, real time correction mode or CD-DA mode, CPU sets the buffer write head address to DADRC.

This counter can also be used as the DMA address of the CPU port. During DMA execution of the CPU port, DADRC contents are output from BA0 to 15, DADRC is incremented at every byte of DMA execution.

CPU can read or set DADRC contents at any time. Do not alter DADRC contents during either write only, real time correction or CD-DA mode and the DMA execution of CPU port.

2.1.11 Host • Address • Low (HADRC-L) counter

2.1.12 Host • Address • High (HADRC-H) counter

This counter keeps the address that writes data from the host into the buffer or reads from the buffer. During execution of the host port DMA, HADRC contents are output from BA0 to 15. The counter is incremented at every DMA of the host port.

Before execution of the host port DMA, CPU sets the DMA head address to HADRC.

CPU can read or set HADRC contents at any time, Do no alter HADRC contents during host port DMA execution.

2.1.13 Host • Transfer • Low (HXFRC-1) counter

2.1.14 Host • Transfer • High (HXFRC-H) counter

This counter indicates the number of host port DMA transfers. It is decremented at every host port DMA.

When ENHXFRC bit (bit3) of DMACTL register is set to "H" and HXFRC value turns to 0, the host port DMA is disabled. At that time it is possible to send an interrupt request from this IC to the CPU.

CPU can read and set HXFRC contents at any time. Do not alter HXFRC contents during Host port DMA execution.

2.1.15 Chip Control (CHPCTL) register

bit0 : CPUBWPO (CPU Buffer Write Pointer)
Sets the pointer value for CPU port DMA (buffer write).

bit1 : CHPRST (Chip Reset)
Setting this bit to "H" initializes the interior of this IC. After the initialization of the interior of this IC is completed, this bit automatically turns to "L". Accordingly it is not necessary to set the CPU to "L".

bit2 : SWOPN (Sync Window Open)

"H" ; Setting this bit to "H" opens the window to allow for SYNC Mark detection. Sync protection circuit inside this IC is disabled.

"L" ; Setting this bit to "L" controls the window through the sync protection circuit inside the IC.

bit3 : RPSTART (Repeat Correction Start)
Setting the Decoder to repeat correction mode and this bit to "H" starts the sector error correction. As correction starts, this bit automatically turns to "L". Accordingly it is not necessary to set the CPU to "L".

bits4 to 7 : Do not fail to set to "L". If set to "H" IC operation is not guaranteed.

2.1.16 CPU Buffer Write Data (CPUBWDT) register

With the CPU port DMA (buffer write), data is written into this register.

When CDMAEN of DMACTL register=CSRC="H", write into this register is subject to the request of CPU port DMA (buffer wire). See paragraph 6 for details.

2.1.17 Host Interface Control (HIFCTL) register

When HMDS is at "L", this register controls the hardware of the host interface.

bit0 : HINT #1 (Host Interrupt #1)
This bit value becomes the value of HINTSTS #1 (bit0) from STATUS register on the host side.

bit1 : HINT #2 (Host Interrupt #2)
This bit value becomes the value of HINTSTS #2 (bit1) from STATUS register on the host side.

bit2 : HINT #3 (Host Interrupt #3)
This bit value becomes the value of HINTSTS #3 (bit2) from STATUS register on the host side.

(Note) Once "H" is written, until bits 0 to 2 are cleared from the host or the chip is reset, keep at "H".
It is not possible to access the register from the CPU and turn bits 0 to 2 from "H" to "L".
Accordingly, to set any of these bits, it is not necessary to take into consideration the value of other bits.
When HINTSTS bit #1 to 3 from HIFSTS register that corresponds to the above bits are at "H", it is prohibited to write "H" in the above bits.
Therefore, before the CPU writes "H" in the above bits HIFSTS register should be read, and confirmation made that corresponding HINTSTS bits #1 to 3 are at "L".

bits3 to 5 : RESERVED
Unused. Keep set to "L". If set to "H" the IC operation is not guaranteed.

bit6 : CLRRSLT (Clear Result)
When this bit is set to "H", the result register is cleared. When these register's clearance is completed, this bit automatically turns to "L". Therefore, there is no need for the CPU to set back to "L".

bit7 : CLRBUSY (Clear, Busy)
When this bit is set to "H", BUSYSTS bit of HINTSTS register is cleared. When these register's clearance is complete, this bit turns automatically turns to "L". Therefore, there is no need for the CPU to reset to L.

2.1.18 Drive Result (DRVRSLT) register

This register is utilized to transfer the command execution result to the host, when HMDS="L". This register is composed of a 10 bytes FIFO. For details see 4.2.1.

2.1.19 Register Address (REGADR) register

bits0 to 6 : Do not fail to set to "L". If set to "H" the IC operation is not guaranteed.

bit7 : REGADR0 (Register Address0)
This bit is used for the register address expansion.

2.2 Read out register

2.2.1 Current Minute Address Low (CMADR-L) register

2.2.2 Current Minute Address High (CMADR-H) register

Indicates the buffer memory address where the current sector (after correction is completed) Minute bytes are written.

2.2.3 Header (HDR) register

A three bytes register that indicates the current sector Header byte.

By reading address 0H successively 4 times the CPU can know the Header byte value of the current sector, starting from the Minute byte.

2.2.4 Sub Header (SHDR) register

A three bytes register that indicates the current sector Sub Header byte.

By reading address 1H successively 4 times, the CPU can know the Sub Header byte value of the current sector, starting from the File byte.

2.2.5 Header Flag (HDRFLG) register

Indicates the Header and Sub Header error pointer value.

2.2.6 Interrupt Status (INTSTS) register

The value of the respective bits in this register indicates the condition of the corresponding interrupt status.

The bit value of INTMSK register does not affect the above mentioned bits.

bit0 : DECINT (DECODER Interrupt)
bit1 : HDMACMP (Host DMA Complete)
bit2 : DRVOVRN (Drive Over Run)
bit3 : HSTCMND (Host Command)
bit4 : HCRISD (Host Chip Reset Issued)
bit5 : RSLTEMPT (Result Empty)
bit6 : DECTOUT (Decoder Timeout)

2.2.7 DECODER Status (DECSTS) register

bit0 : NOSYNC
Indicates that Sync Mark could not be detected and that SYNC was inserted.

bit1 : SHRTSCT (Short Sector)
Indicates the Sync Mark interval was within 2352 bytes. This sector does not execute ECC and EDC.

bit2 : ECCOK (ECC OK)
Indicates there are no more errors from the header of the sector where error correction was completed up to P Parity byte. (In FORM2, this bit turns to don't care.)

bit3 : EDCOK
Indicates EDC check showed there were no errors.

bit4 : CORDONE (Correction Done)
Indicates that sector contains bytes that were error corrected.

bit5 : CORINH (Correction Inhibit)
Indicates there was an error flag at MODE (and FROM) bytes when AUTODIST bit of DECODER register was turned to "H". This sector does not execute ECC and EDC.

bit6 : ERINBLK (Erasure in Block)
Turns to "H" when C2 pointer from CIRC LSI stood in 1 byte or more of all the bytes, with the exception of current sector Sync byte.

bit7 : EDCALL0 (EDC ALL ZERO)
This bit turns to "H" when there are no error flags in any of EDC parity bytes of current sector, and the value is at 00H.

2.2.8 MODE FORM (MDFM) register

This register is effective only during the execution of Real time correction mode or Repeated correction mode.

bit0 : CFORM (Correction FORM)

bit1 : CMODE (Correction MODE)

These bits indicate whether this IC identified MODE and FORM in that sector and executed error correction.

CMODE	CFORM	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bits2 to 4 : RMODE0, 1, 2 (Raw MODE)

RMODE1, 0 : Indicates the lower 2 bits value of raw MODE byte.

RMODE2 : Indicate the logical sum of the upper 6 bits and pointer in raw MODE byte.

2.2.9 DMA Status (DMASTS) register

bit0 : CBFWRDY (CPU Buffer Write Ready)

This bit turns to "H" when data written from CPU into CPUBWDT register is written in the buffer memory. As CPU writes the next data into CPUBWDT register, it turns to "L" until that data is written into the buffer memory. Also, when CSRS is set to "H" and CDMAEN to "H" (DMACTL register), this bit turns to "H".

CPU confirms this bit is at "H" and writes in the data into CPUBWDT register.

bit1 : CBFRRDY (CPU Buffer Read Ready)

When data read from buffer memory is kept ready in CPUBRDT register, this bit turns to "H".

When CPU reads CPUBRDT register out it turns to "L".

CPU confirms this bit is at "H" and reads out data from CPUBRDT register.

bit2 : CBFRDPO (CPU Buffer Read Pointer)

Indicates the value of the pointer bit read from the buffer memory.

bit7 : REGADR (Register Address)

This bit indicates the value of bit7 from Register Address register.

2.2.10 DADRC-L counter

2.2.11 DADRC-H counter

2.2.12 HADRC-L counter

2.2.13 HADRC-H counter

2.2.14 HXFRC-L counter

2.2.15 HXFRC-H counter

2.2.16 CPU Buffer Read Data (CPUBRDT) register

CPU port DMA (buffer read) data is read out from this register.

When CDMAEN of DMACTL register is at "H" and CSRC at "L", the read out of this register is set for the DMA (buffer read) request of the next CPU port.

2.2.17 Host Parameter (HSTPRM) register

When HMDS is at "L", this register is used to know the command parameter from the host. This register is composed of a 10 bytes FIFO.

2.2.18 Host Command (HSTCMD) register

When HMDS is at “L”, this register is used to know the command from the host.

2.2.19 Host Interface Status (HIFSFS) register

When HMDS is at “L”, this register is used to know the host interface condition.

bit0 : HINTSTS #1 (HOST Interrupt Status #1)
This bit turns to “H” as CPU writes “H” into HINT #1 (HIFCTL register bit0). It turns to “L” when the host writes “H” into CLRINT #1 (Control register bit0). This bit is used as interrupt status monitor to the host.

bit1 : HINTSTS #2 (HOST Interrupt Status #2)
This bit turns to “H” as CPU writes “H” into HINT #2 (HIFCTL register bit1). It turns to “L” when the host writes “H” into CLRINT #2 (Control register bit1). This bit is used as interrupt status monitor to the host.

bit2 : HINTSTS #3 (Host Interrupt Status #3)
This bit turns to “H” as CPU writes “H” into HINT #3 (HIFCTL register bit2). It turns to “L” when the host writes “H” into CLRINT #3 (Control register bit2). This bit is used as interrupt status monitor to the host.

bit3 : PRMRRDY (Parameter, Read Ready)
This bit at “H” indicates that HSTPRM register is not empty, so that Parameter data can be read out from the CPU. When this bit is at “L”, HSTPRM register is empty and Parameter data cannot be read out from the CPU.

bit4 : PRMFULL (Parameter Full)
This bit at “H” indicates HSTPRAM register is full.

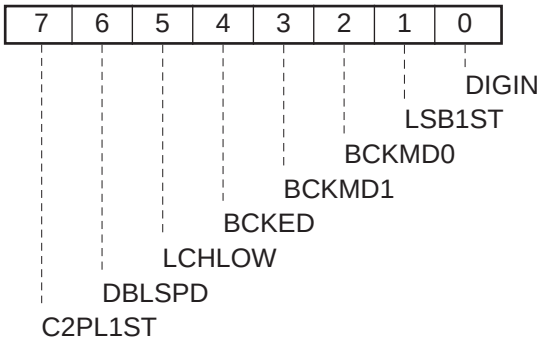
bit5 : RSLWRDY (Result Write Ready)
This bit at “H” indicates that DRVRSLT register is not full, so that the CPU can write Result data. When this bit is at “L” DRVRSLT register is full and the CPU can not write Result data.

bit6 : RSLEMPT (Result Empty)
This bit at “H” indicates DRVRSLT register is empty.

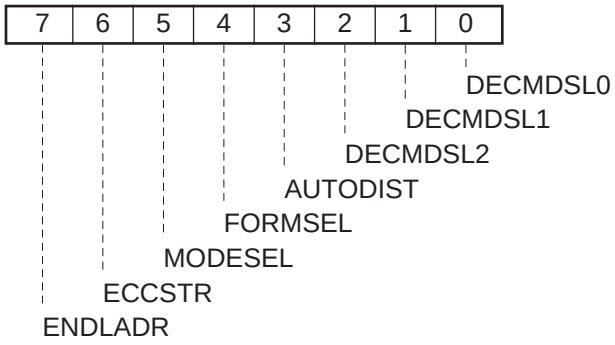
bit7 : BUSYSTS (Busy Status)
This bit has the same value as that of BUSYSTS (bit7) of the status register on the host side.
This bit turns to “H” as the host writes a command in the Command register. It turns to “L”, as the CPU sets CLRBUSY bit of HIFCTL register.

***** **Write register** *****

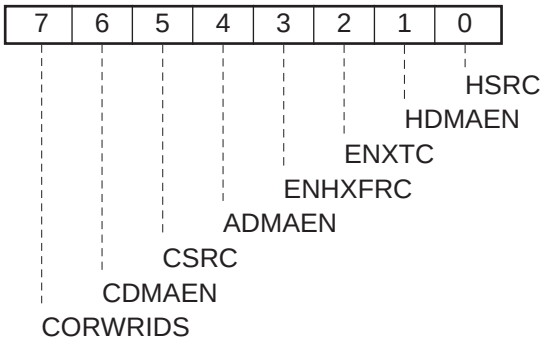
Drive Interface (DRVIF)



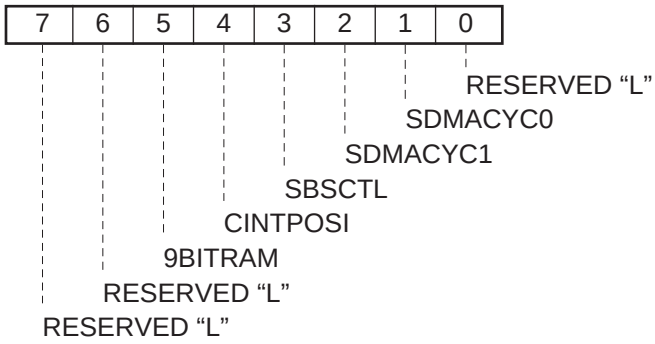
DECODER Control (DECCTL)



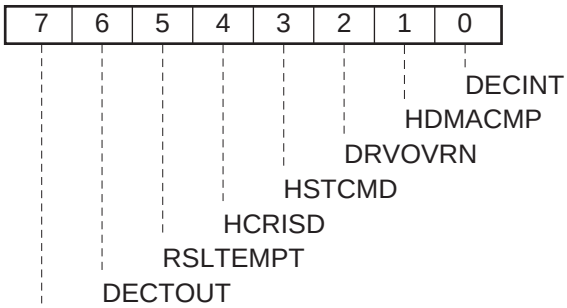
DMA Control (DMACTL)



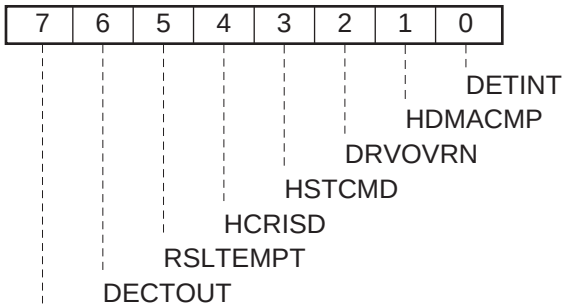
Configuration (CONFIG)



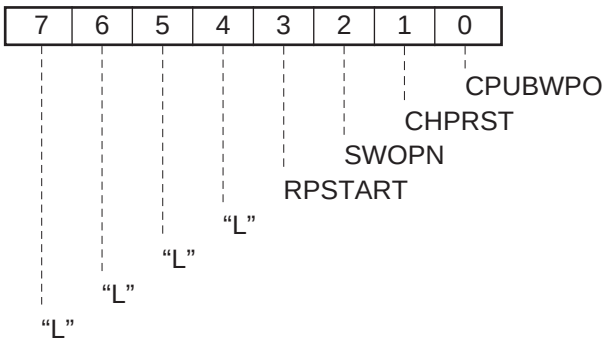
Interrupt Mask (INTMSK)



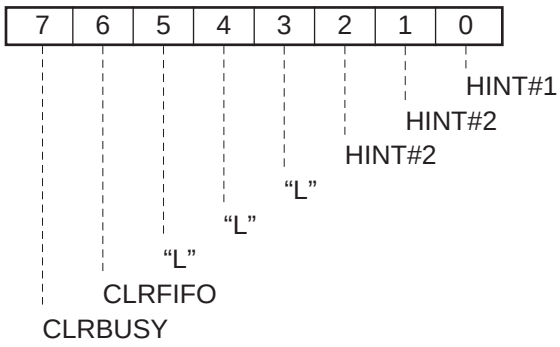
Clear Interrupt Status (INTCLR)



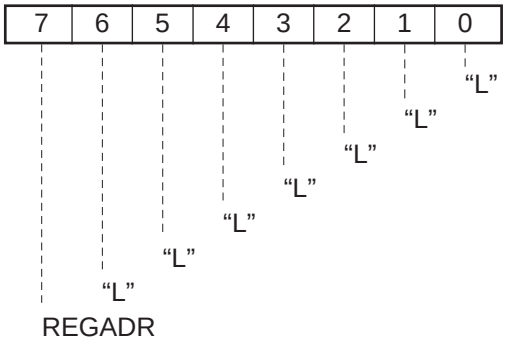
Chip Control (CHPCTL)



Host Interface Control (HIFCTL)



Register Address (REGADR)



Drive • Last • Address • Low
Drive • Last • Address • High

Drive • Address • Counter • Low
Drive • Address • Counter • High

Host • Transfer • Counter • Low
Host • Transfer • Counter • High

Host • Address • Counter • Low
Host • Address • Counter • High

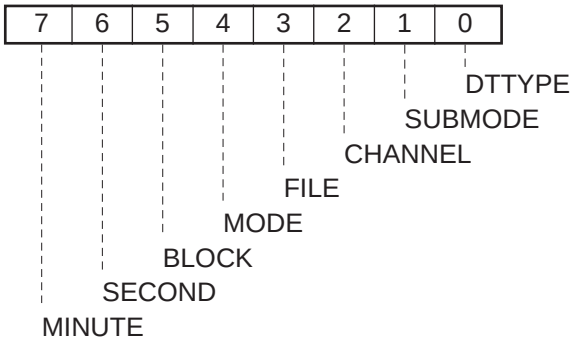
CPU Buffer Write register

Drive Status register

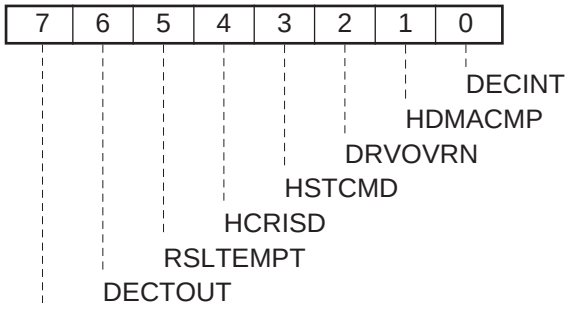
Register Address register

***** **Read register** *****

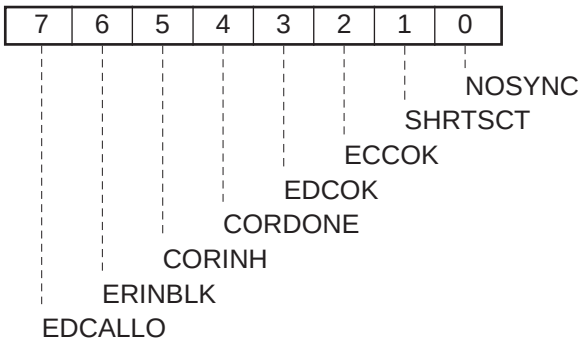
Header Flag



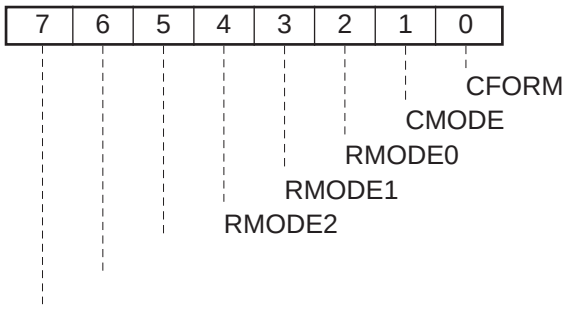
Interrupt Status



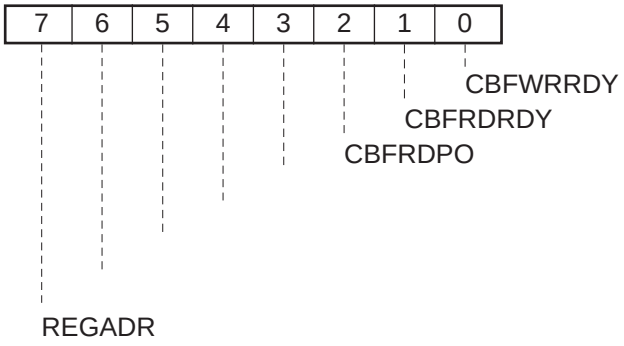
DECODER Status



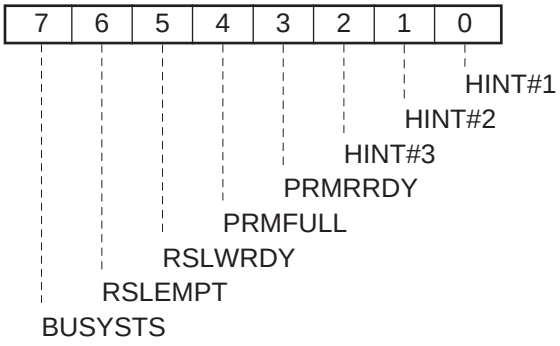
MODEFORM



DMA Status



Host Interface Status



Header register

Sub Header register

Current • Minute • Address • Low
Current • Minute • Address • High

Drive • Last • Address • Low
Drive • Last • Address • High

Drive • Address • Counter • Low
Drive • Address • Counter • High

Host • Transfer • Counter • Low
Host • Transfer • Counter • High

Host • Address • Counter • Low
Host • Address • Counter • High

CPU • Address • Counter • Low
CPU • Address • Counter • High

CPU Buffer Read register

Host Command register
Host Parameter register

CXD1186Q register

ADDRESS	Write		Read	
	REGISTER-ADDRESS		REGISTER-ADDRESS	
	L	H	L	H
0	DRVIF	CONFIG	HDR	
1	DECCTL		SHDR	
2	DMACTL		HDRFLG	
3	INTMSK		MODEFORM	
4	INTCLR		DECSTS	
5	DLADR-L		INTSTS	
6	DLADR-H		DMASTS	
7	DADRC-L			
8	DADRC-H			
9	HXFRC-L			
A	HXFRC-H			TEST2
B	HADRC-L			TEST1
C	HADRC-H			TEST0
D	CPUBWDT	HIFCTL	CPUBRDT	HSTCMD
E	CHPCTL	DRVRSLT	CMADR-L	HSTPRM
F	REGADR		CMADR-H	HIFSTS

3. DECODER Operation

Here after, the block containing functions 1 and 2 is called DECODER.

1 Interface with CIRC LSI
The data stream from CIRC LSI is taken in, while sync detection, descramble and data write to the buffer are executed.

2 Error correction
Executes error correction of the sector written in the buffer.

3.1 DECODER operation mode

The Decoder features 4 operation modes set by means of DECMDSEL0 to 2 bits of DECCTL register.

DECMDSL2	1	0	
"L"	"L"	"X"	Decoder disable
"L"	"H"	"X"	Monitor only mode
"H"	"L"	"L"	Write only mode
"H"	"L"	"H"	Real time correction mode
"H"	"H"	"L"	Repeat correction mode
"H"	"H"	"H"	CD-DA mode

(1) Decoder disable
DECODER operation is disabled.

(2) Monitor only mode
Data from the drive is not written in the buffer. Raw data from the drive is written in the Header, Sub Header and HDRFLG registers.

(3) Write only mode
Set to this mode, first Sync pattern detection is performed. As sync pattern is detected, write from that sector into the buffer starts from Minute byte. The buffer memory address of this Minute byte, is the value set to DADRC though the CPU before setting the DECODER mode. Sectors after that, and the Sync pattern too, are written into the buffer.
This buffer write continues until either Decoder is disabled or when ENDLADR is at "H", DLADR value becomes equal to that of DADRC.

(4) Real time correction mode
Buffer write works the same as write only mode.
At the same time, error correction of the sectors already written in the buffer is executed in real time. (When this mode is set and while the first sector is being written in the buffer, as long as a whole sector is not yet stored in the buffer, correction is not executed.)

(5) Repeat correction mode
Data from the drive is not written in the buffer. Error Correction of sectors already written in the buffer can be executed repeatedly. This way, errors that could not be corrected during real time correction mode, can now be corrected.

(6) CD-DA mode
To write CD-DA (Digital audio) Disc data into the buffer, this mode is set. As this mode is set, write into the buffer is executed from the lower byte of LCH.
This buffer write continues until either Decoder is disabled, or when ENDLADR is at "H", DLADR value becomes equal to that of DADRC.

3.2 DADRC (Drive Address Counter)

DADRC is the counter that holds the address when data from the drive is written into the buffer. When data from the drive is written into the buffer, the contents are output from BA0 to 15 as buffer memory address.
CPU can set or read DADRC contents. CPU sets the buffer write head address in DADRC before the setting of Decoder write only mode, real time correction mode and CD-DA mode.

3.3 DLADR (Drive Last Address)

DLADR is the register that indicates in bytes the value of DADRC that stops the drive data buffer write during the execution of write only mode, real time correction mode and CD-DA mode. When ENDLADR bit of DECCTL register is at "H" and the above modes are being executed, if DADRC value becomes equal to DLADR, it stops the buffer write data from the drive. Then, DRVOVRN status is on. When sync interrupt applies and DRVOVRN bit is at "H", have CPU disable the DECODER. When ENDLADR bit is at "L", even if DADRC value becomes equal to DLADR, buffer write of the data from the drive is not stopped and DRVOVRN status does not turn on.
Through the usage of DLADR, buffer overran of the drive can be prevented.
When a value is set to DLADR, make sure to set the upper byte first and the lower byte next in the order. (Even in case only the value of one of bytes is to be changed, set both bytes in the mentioned order. If this is not performed, IC operation can not be guaranteed.) The DLADR upper byte is first set then the lower byte is set and until data from the drive is written in the buffer, the above function is disabled. DLADR setting should be made carefully.

3.4 Error correction

(1) MODE and FORM discrimination
Mode and Form discrimination in the sector that performs error correction is executed in bits AUTODIST, FORMSEL and MODESEL of DECCTL register, as indicated in Fig. 3.1.

(2) ECC strategy can be chosen through ECCSTR bit of DECCTL register.
At “H”, error correction is performed taking into consideration error flags from respective data.
At “L”, error correction is performed without taking into consideration error flags from respective data.
For systems using 8 bit word RAM, turn ECCSTR to “L”.
When double speed PB is executed (DBLSPD of DRVIF register is at “H”), transfer speed to the host slows down. Data transfer speed to the host when XTL1 frequency is set to 16.9344 MHz is shown below, Moreover, this data transfer speed is the value obtained when data buffer write from the drive, error correction and data transfer to the host are executed at the same time.

	ECCSTR	Data Transfer Speed
Normal PB speed	L	2.1 MB/S
	H	
Double PB speed	L	
	H	0.7 MB/S

From the above table, it appears that during double speed PB, data transfer speed to the host decreases. During double speed PB, Read data speed from the Drive is at 352.8 KB/S. Data transfer speed to the host at 0.7 MB/S is quite faster than this Read speed. Actually, transfer speed to the host does not decrease and as Read data speed from the Drive doubles, transfer speed to the host also approximately doubles.

3.5 CPU control of the IC during Real time correction
CPU control of the IC during the IC execution of Real time correction mode is shown in Fig. 3.2.

3.6 CPU control of the IC during Repeat correction
CPU control of the IC during the IC execution of Repeat correction mode is shown in Fig. 3.3.

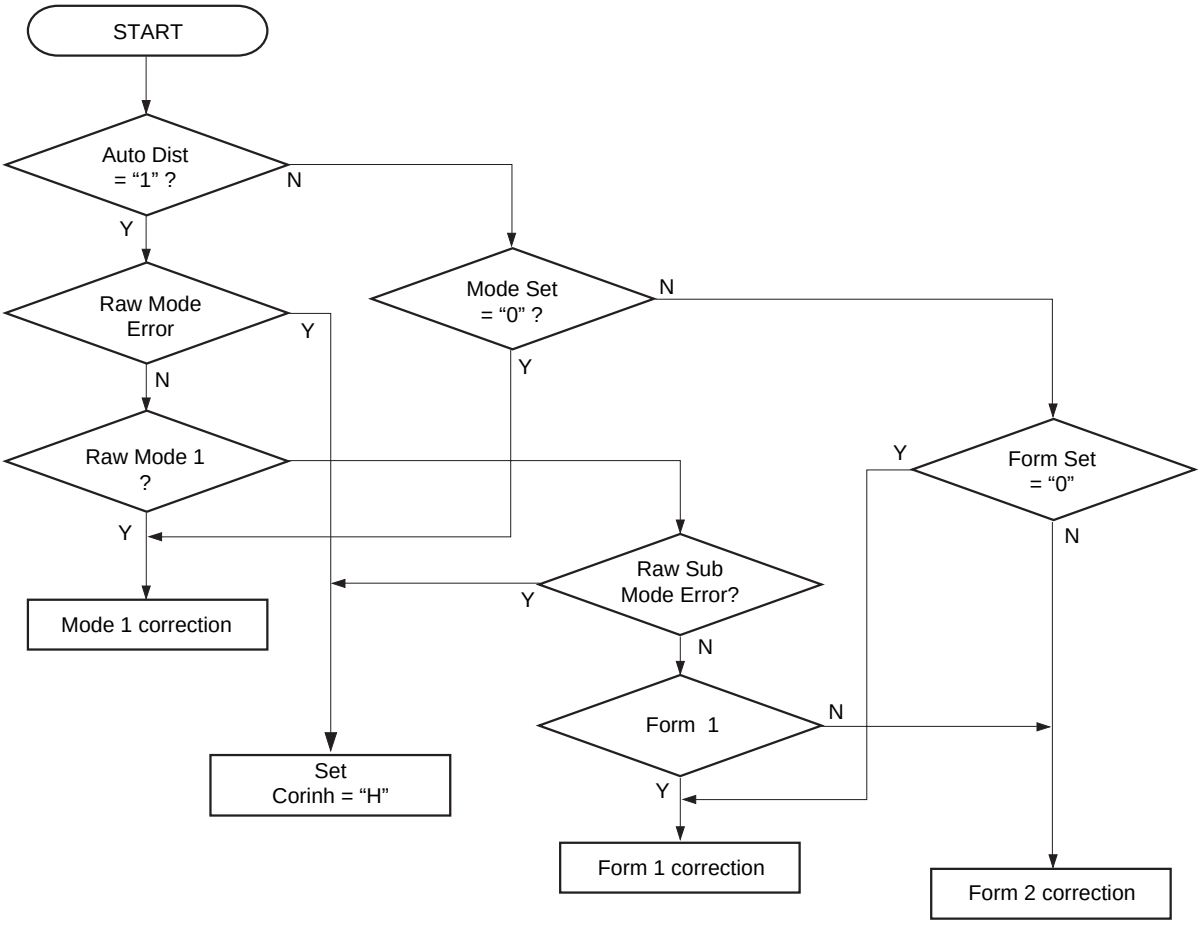


Fig. 3.1 MODE FORM Discrimination method

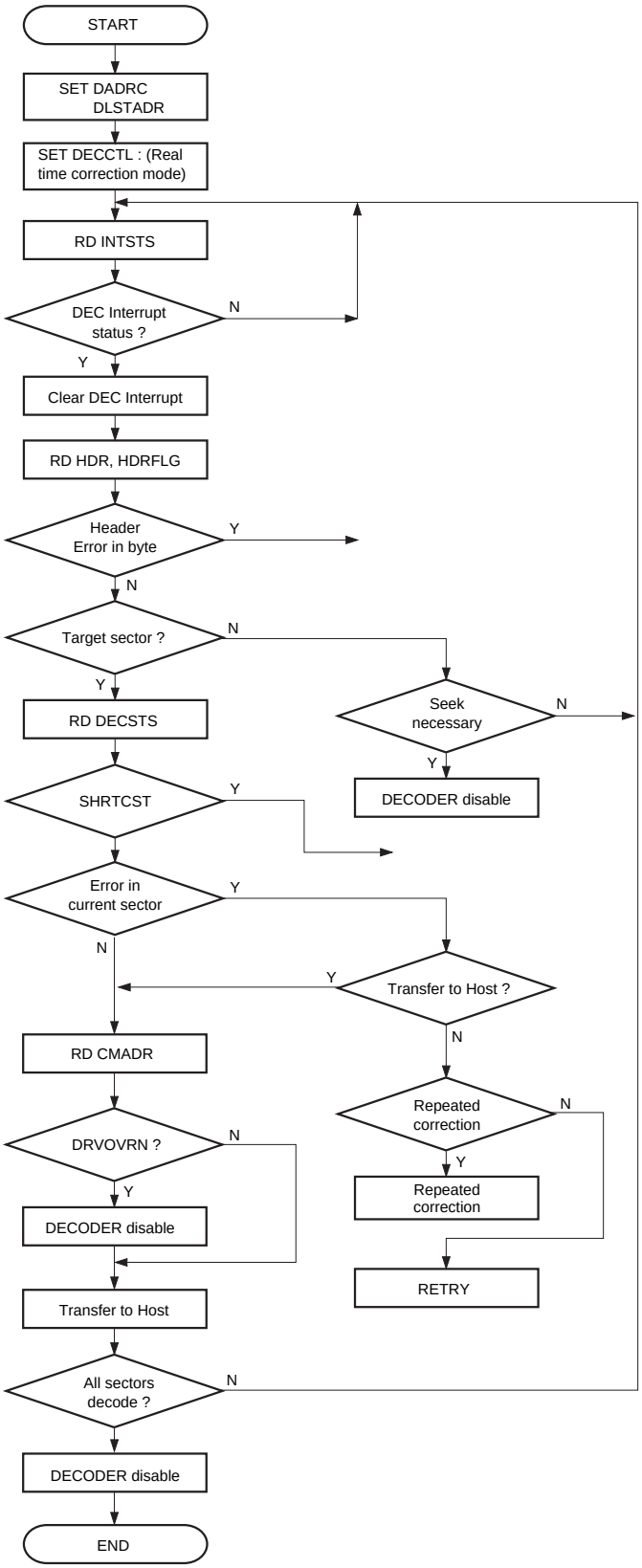


Fig. 3.2 CPU control of the IC during real time correction

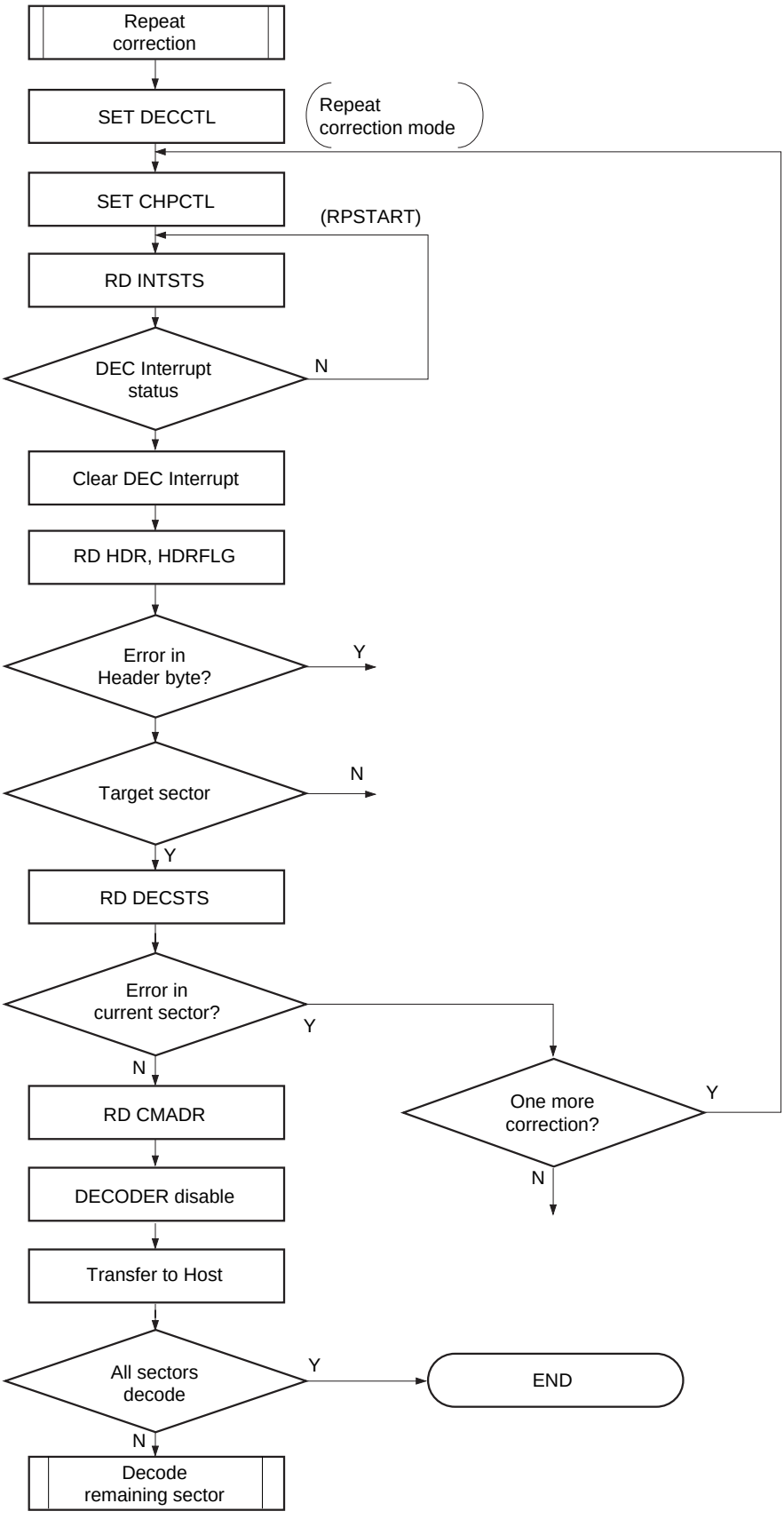


Fig. 3.3 CPU control of the IC during repeated correction

4. Host interface

4.1 Host I/F mode

This IC can be connected to the following, as the host interface.

① SCSI controller IC (CXD1180, CXD1185 and others)
② Intel 80 type host bus

This mode is set by means of HMDS pin, as shown below.

When Intel 80 type host bus is connected, HMDS input is at "L". Otherwise, HMDS pin is set to open.
When SCSI control IC is connected, HMDS input is at "H".

4.2 Connected to Intel 80 type host bus

When this IC is connected to Intel 80 type host bus either "L" is input to pin HMDS or it is left open. This connection is shown an Fig. 4.1.

4.2.1 Command/Status transfer between the Host and the CPU.

(1) Register

The host can access each of the 4 write and read registers. Using pins XHCS, HA0, HA1, XHRD and XHWR, it reads and writes their registers. DMA transfer is also possible with RDDATA and WRDATA registers despite XHCS, HA0 and HA1 values. Their registers are selected by means of XHAC, XHRD, XHWR and DMA transfers performed with the host. Parameter register and Result register are 10 bytes FIFO registers. "L" input to XHAC and XHCS is prohibited at the same time.

∗ Write register

- Command register (address 0)
  The host writes commands in this register. As the host writes in this register, interrupt request is applied from this IC to the CPU. Bit assignment and function attribution is performed by means of a control program.
- Parameter register (address 1)
  To execute commands, the host writes into this register command parameters. This is a 10 bytes FIFO register.
- Write Data (WRDATA) register (address 2)
  This register serves to write data from the host into the buffer memory. Data can be written into either I/O mode or DMA mode. This register is composed of a 2×9 bits FIFO.
- Control register (address 3)
  This register is for the direct control of the hardware in this IC by the host.

bits0 to 2 : INTCLR #1 to 3 (Clear Interrupt #1 to 3)
Setting these bits to "H" will clear the corresponding interrupt status, After the clearance of interrupt status in these bits, they automatically go back to "L".

bits3 to 5 : ENINT #1 to 3 (Enable Interrupt #1 to 3)
Setting these bits to "H" will enable the corresponding interrupt status.
The host can read the respective bits value from the status register.
When the corresponding interrupt status is at "H", it is prohibited to write "H" to these bits, accordingly, before the host sets these bits to "H", the Status register should be read out and interrupt status confirmed.

bit6 : CLRPRM (Clear FIFO)
Setting this bit to "H" clears the Parameter register, After these registers are cleared, this bit automatically goes back to "L".

bit7 : CHPRST (Chip Reset)
Setting this bit to "H" initializes the inside of this IC. As the inside of this IC initialization is completed, this bit automatically return to "L". Setting this bit to "H" enables interrupt request to the CPU.

∗ Read out register

• Status register (Address 0)

The host uses this register to read this IC status.

bits0 to 2 : INTSTS #1 to 3 (Interrupt Status #1 to 3)
The value of the respective bits is the same as that of the bits corresponding to HIFCTL register of the sub CPU. When interrupt corresponding to the respective bits is enabled, they turn to "H" and interrupt request to the host is output.

bits3 to 5 : ENINTST #1 to 3
(Enable Interrupt Status #1 to 3)
The value of the respective bits is the same as that of the bits corresponding to Control register.

bit6 : DREQSTS (Data Request Status)
Indicates this IC is in buffer memory data transfer request condition versus the host. This bit has the same value as that of pin HDRQ. In I/O mode, when buffer memory data transfer is executed, access WRDATA register or RDDATA register after the host confirms this bit is at "H".

bit7 : BUSYSTS (Busy Status)
This bit turns to "H" as the Host writes a command into the Command register. It turns to "L" as the sub CPU sets CLRBUSY bit of HIFCLT register.

• Result register (address 1)

The host reads the results after the command execution from this register.
This is a 10 bytes FIFO.

• Read Data (RDDATA) register (address 2)

This register is for the host to read data from the buffer memory. Data can be read in I/O mode or DMA mode. It is composed of a 2 × 9 bits FIFO.

• FIFO Status register (address 3)

This register is for the host to read the status of Parameter or Result register.

bit0 : PRMWRDY (Parameter Write Ready)
When this bit is at "H" it indicates that Parameter register is not full, and that the host can write parameter data.

bit1 : PRMEEMPT (Parameter Empty)
This bit at "H" indicates Parameter register is empty.

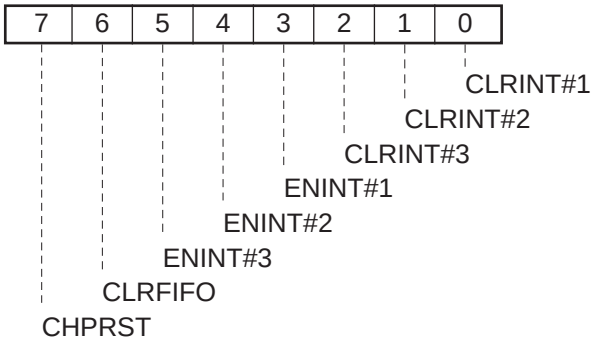
bit2 : RSLRRDY (Result Read Ready)
This bit at "H" indicates that Result register is not empty, and that the host can read Result data.

bit3 : RSLFULL (Result Full)
This bit at "H" indicates Result register is full.

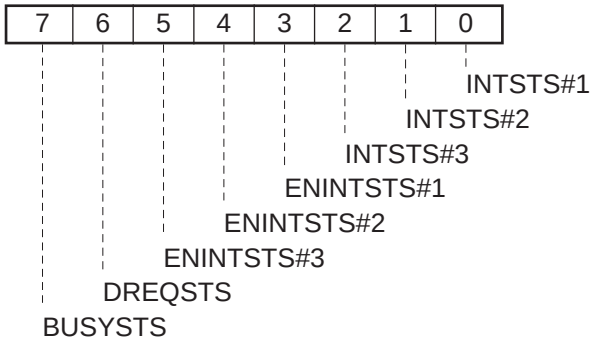
bit4 to 7 : RESERVED
Unused.

Address	Write	Read
0	Command	Status
1	Parameter	Result
2	Write Data	Read Data
3	Control	FIFO Status

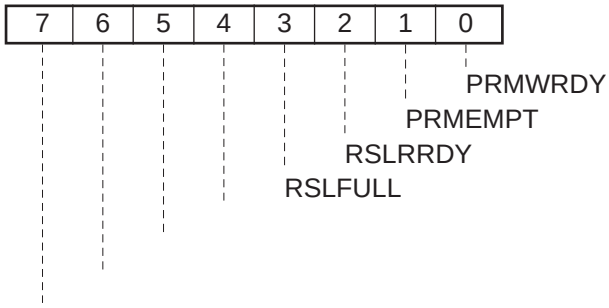
Control



Status



FIFO Status



(2) Host and CPU controlling order
An example of the host and CPU controlling order is shown in Fig. 4.2.1.
In this case the host gets to know interrupt status by polling Status register, Interrupt request can also be enabled.

4.2.2 Data transfer between the host and the buffer memory.
Data transfer between the host and the buffer memory is executed through this IC. This IC incorporates a 2 × 9 bits FIFO (WRDATA, RDDATA registers) to speed up data transfer.

(1) Data transfer in DMA mode
Data transfer between the host and FIFO inside this IC, is performed through handshake utilizing HDRQ/XSAC and XHAC/SDRQ.
HDRQ/XSAC becomes the HDRQ data transfer request signal from this IC to the host while XHAC/SDRQ becomes the corresponding acknowledge signal XHAC.

① Data transfer from the host to the buffer memory (HSRC at "H")
When HDMAEN is at "H" while FIFO in not full and XHAC is at "H", this IC activates HDRQ. As acknowledge signal XHAC comes back from the host, HDRQ is inactivated. With the rising edge of XHAC, data is written into FIFO. Data written into FIFO is written in the buffer memory address in the order prescribed by HADRC.

② Data transfer from the buffer memory to the host (HSRC at "L")
When HDMAEN is at "H", buffer read data from the address prescribed by HADRC is written into the FIFO. As data is written into FIFO, if XHAC is at "H", this IC activates HDRQ. As the acknowledge XHAC comes back from the host, HDRQ is inactivated. During the period when XHAC is at "L", this IC outputs the FIFO data to HDB0 to 7.

(2) Data transfer in I/O mode
The host can transfer data to and from the buffer memory, by writing or reading registers WRDATA and RDDATA. In this case the control of CXD1186Q by the CPU is the same as during DMA transfer mode.
Fig. 4.2.2 indicates the host control flow when data transfer is performed in I/O mode between the host and the buffer memory.

(3) Data transfer completion
The 3 following methods are for data transfer completion.
- HXFRC is used.
- XTC pin is used.
- HDMAEN bit is set to "L".

① When HXFRC is used:
When HXFRC is used for data transfer completion, perform the following before the CPU starts data transfer.
- Set the number of data transfer bytes at HXFRC.
- Set the data transfer direction (HSRC bit) to "H" or "L" and ENHXFRC=HDMAEN to "H". This starts data transfer.

HXFRC is decremented every time data is written into FIFO.
When HXFRC turns to 0, writing of data into FIFO after that is not performed. Then, when all the FIFO data is transferred to the buffer memory or the host, HDMACMP status (DMASTS register) sets on.
When HDMACMP bit of INTMSK register is set to "H", this IC outputs interrupt request (INT output) to the CPU.

② When XTC pin is used
When XTC pin is used for data transfer completion, perform the following before the CPU starts data transfer.
- Set the data transfer direction (HSRC bit) to "H" or "L" and ENXTC=HDMAEN to "H". This starts data transfer.

During the host final DMA byte transfer, turn pin and XHAC, XHWR, XHRD to "L". This way, data transfer to the host is no more performed. (HDRQ is not output to the host.) When HSRC is at "L" and XTC turns to "L", after XHAC becomes inactive, this IC turns to HDMACMP status. In this case, 1 byte of unnecessary data from the buffer memory may already be written in the FIFO.
Then, care should be exercised as the last address of HADRC transfer +2 is indicated. When HSRC is at "H", the IC turns to HDMACMP status, when the writing into the buffer memory of data written into the FIFO as XTC at "L", is completed.
In either case, as HDMACMP status sets on, and HDMACMP bit of INTMSK register is set to "H", this IC output interrupt request (INT output) to the CPU.
Both ENXTC and ENHXFRC bits of DMACTL register, can simultaneously be set to "H".

(Note) In either①or②case, after HDMACMP sets on, before starting up data transfer again, turn bit 1 of INTCLR register to "H" and clear HDMACMP status.

③ When HDMAEN bit is set to "L"
When HDMAEN bit is set to "L" during data transfer with the host, data transfer is stopped. Then, data transfer between this IC and the host or the buffer memory may be stopped half-way. The value of HADRC and HXFRC after that is not guaranteed. Also, in this case, HDMACMP status does not set on.

(4) CPU control of the IC
CPU control of the IC when data transfer is performed between the host and the buffer memory is illustrated as follows. (In this example execute data transfer completion using HXFRC)

① The number of transfer bytes is set to HXFRC.
② HADRC is set at the DMA head address.
③ Set the data transfer direction to "H" or "L" and HDMEAN and ENHXFRC bits of DMACTL register to "H".
④ As the transfer of the specified number of bytes is completed, HDMACMP bit of DMASTS register turns to "H". (Then, this IC can output an interrupt request to the CPU)
⑤ Also, HXFRC is at 0000H, while HADRC value stands as the value next to that of the buffer memory address transferred last.

4.3 When connected to SCSI control IC

When this IC is connected to SCSI control IC, HMDS pin is set to "H".

4.3.1 Connection method to SCSI control IC

- An example for the connection of this IC to an SCSI control IC where CPU bus and DMA bus are not separated (ex. CXD1180AQ) is shown in Fig. 4.3.1.
  To switch CPU and DMA buses, an external circuit is required.
- An example for the connection of this IC to an SCSI control IC where CPU and DMA buses are separated (ex. CXD1185AQ) is shown in Fig. 4.3.2.

4.3.2 Data transfer between SCSI control IC and the buffer memory

Data transfer between SCSI control IC and buffer memory is performed through this IC.

(1) Data transfer handshake
XHAC/SDRQ become the data transfer request signal SDRQ from SCSI control IC to this IC. HDRQ/XSAC become the corresponding acknowledge signal XSAC.

① Data transfer from SCSI control IC to this IC (HSRC at "H")
When HDMAEN is at "H", SDRQ input while FIFO is not full will make this IC activate XSAC. Data is written into FIFO with the rising edge of XHWR.
② Data transfer from this IC to SCSI control IC (HSRC at "L")
When HDMAEN is at "H", SDRQ input while FIFO is not empty will make this IC activate XSAC. It also outputs data from FIFO to HDB0 to 7 during the period XHAC is at "L".

(2) Completion of data transfer

The 2 following methods are for the completion of data transfer.

- HXFRC is used.
- HDMAEN is set to “L”.

For either method refer to paragraph 4.2.2.

(3) Data transfer cycle

The data transfer cycle between this IC and SCSI control IC can be controlled through SDMACYC 0 and 1 bits from CONFIG register. CPU sets these bits in coordination with the speed of SCSI control IC (See A.C characteristics)

SDMACYC1	0	
“L”	“L”	3 cycles.
“L”	“H”	4 cycles.
“H”	“X”	5 cycles.

(4) CPU control of the IC

For CPU control of the IC when data transfer is executed between SCSI control IC and the buffer memory, see paragraph 4.2.2.

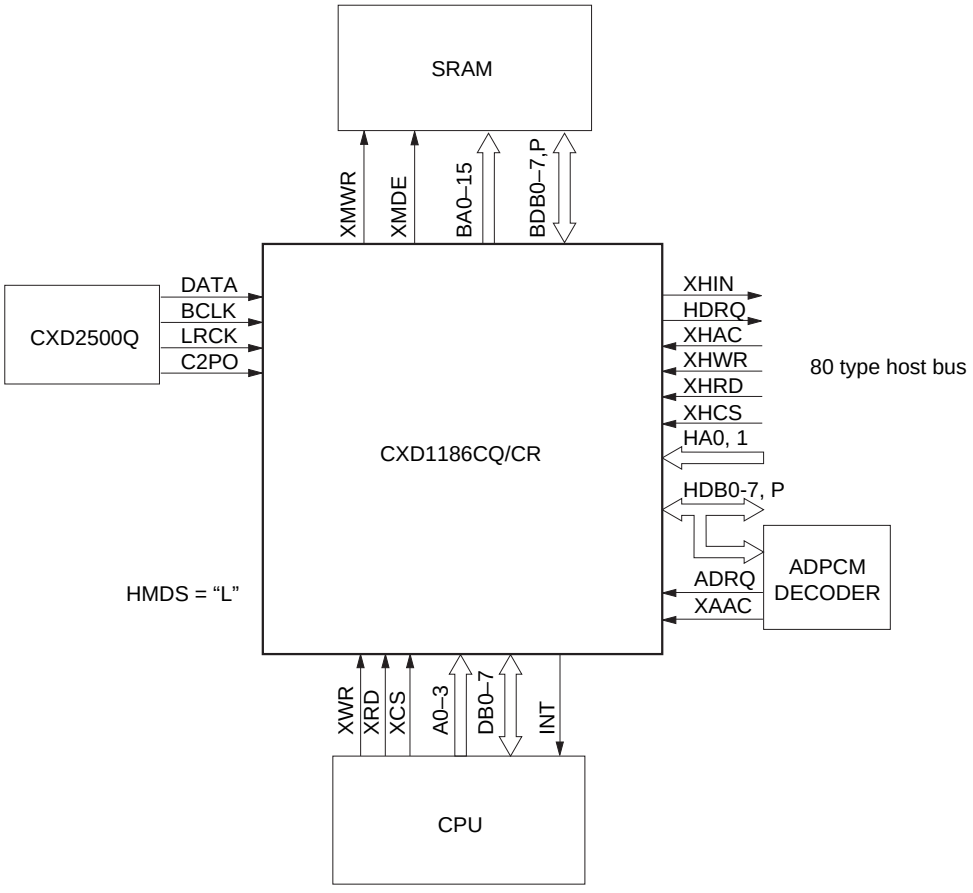


Fig. 4.1 CXD1186CQ/CR connection (80 type host bus)

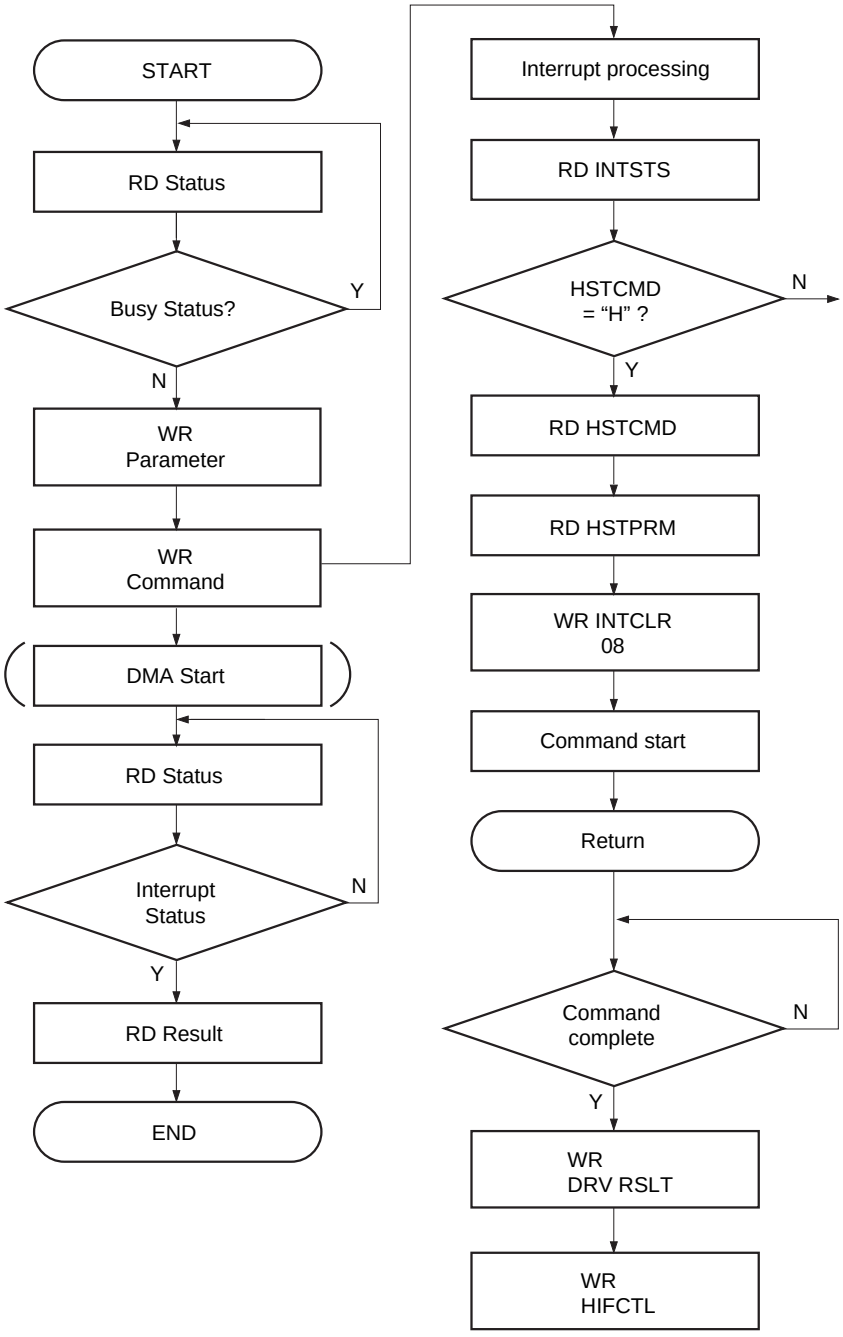


Fig. 4.2.1 Host and CPU control

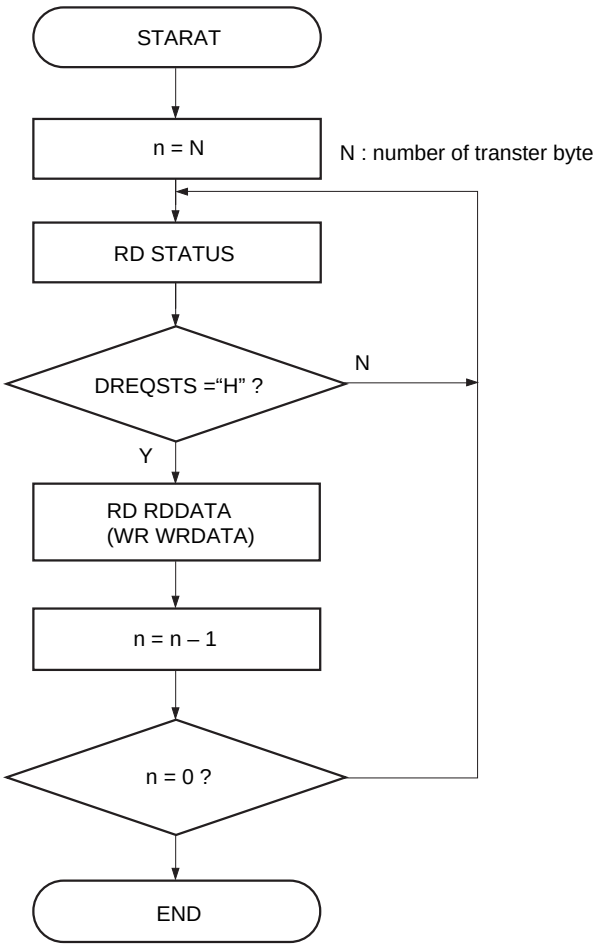


Fig. 4.2.2 I/O mode data transfer

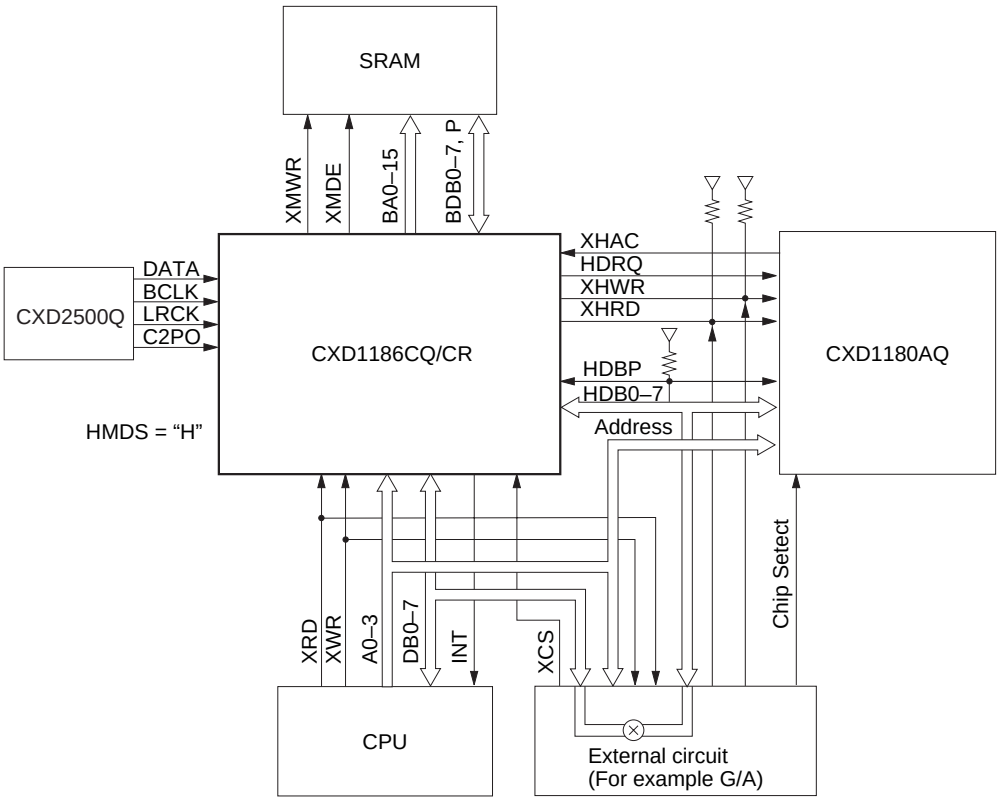


Fig. 4.3.1 CXD1186CQ/CR connection (connecting method 1 with SCSI control IC)

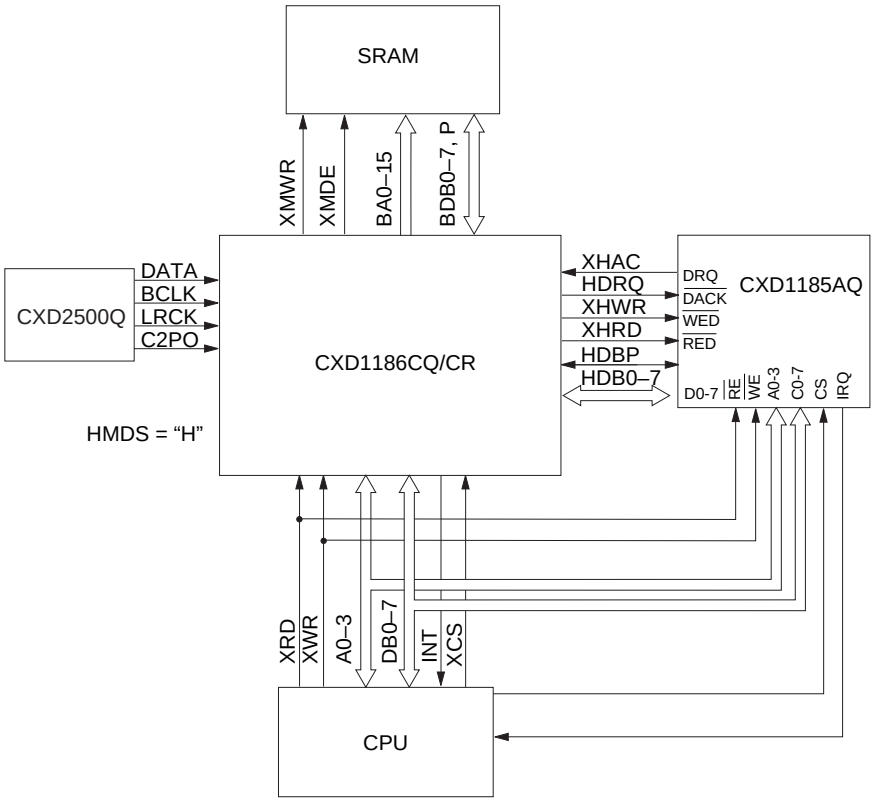


Fig. 4.3.2 CXD1186CQ/CR connection (connecting method 2 with SCSI control IC)

5. Data transfer between audio processor (ADP) and buffer memory

Data transfer between ADP and the buffer memory is performed through this IC.

(1) Data transfer handshake

ADRQ pin is the data transfer request signal from ADP to this IC. XAAC pin becomes the corresponding acknowledge signal. When ADMAEN is at "H" and ADRQ is input while FIFO is not empty, this IC activates XAAC and outputs FIFO data to HDB0 to 7 during the period where XAAC is at "L".

(Note 1) HADRC and HXFRC are used for the transfer of data between both this IC and the host and this IC and ADP. Accordingly, HDMAEN and ADMAEN cannot be set to "H" simultaneously. If both of then are set to "H" simultaneously, HDMAEN will turn to "H" and ADMAEN to "L", inside the IC.

(Note 2) Even when HMDS is at "L" (connected to Intel 80 type host bus), turning ADMAEN to "H" will make XHWR and XHRD pins change from input to output. Therefore access from the host to this IC register is not possible. Watch out for signals collision.

(2) Completion of data transfer

There are 2 ways to complete data transfer.

- Using HXFRC.
- Turning ADMAEN bit to "L".

For details on the 2 ways refer to Paragraph 4.2.2.

(3) Data transfer cycle

The data transfer cycle between this IC and ADP can be controlled using bits SDMACYC 0 and 1 from CONFIG register. CPU sets these bits to match ADP transfer speed.

SDMACYC 1	0	
"L"	"L"	3 cycles.
"L"	"H"	4 cycles.
"H"	"X"	5 cycles.

(4) CPU control of the IC

For CPU control of the IC when data is transferred between ADP and the buffer memory, refer to Paragraph 4.2.2.

6. CPU port DMA

- CPU control of the IC

An example on CPU control of the IC when CPU port performs DMA is indicated in Fig. 6.1 and Fig. 6.2. When CPU port performs DAM, the address uses DADRC. Accordingly, when the Decoder is performing any of the following modes write only, real time correction, CD-DA, CPU cannot access the buffer memory.

When CSRC is at "L", turning CDMAEN to "H" (DMACTL register) will cause data from the buffer memory to be read and written into CPUBRDT register.

When CDMAEN is turned to "H", it is prohibited to change CSRC value. To change CSRC value turn CDMAEN to "L".

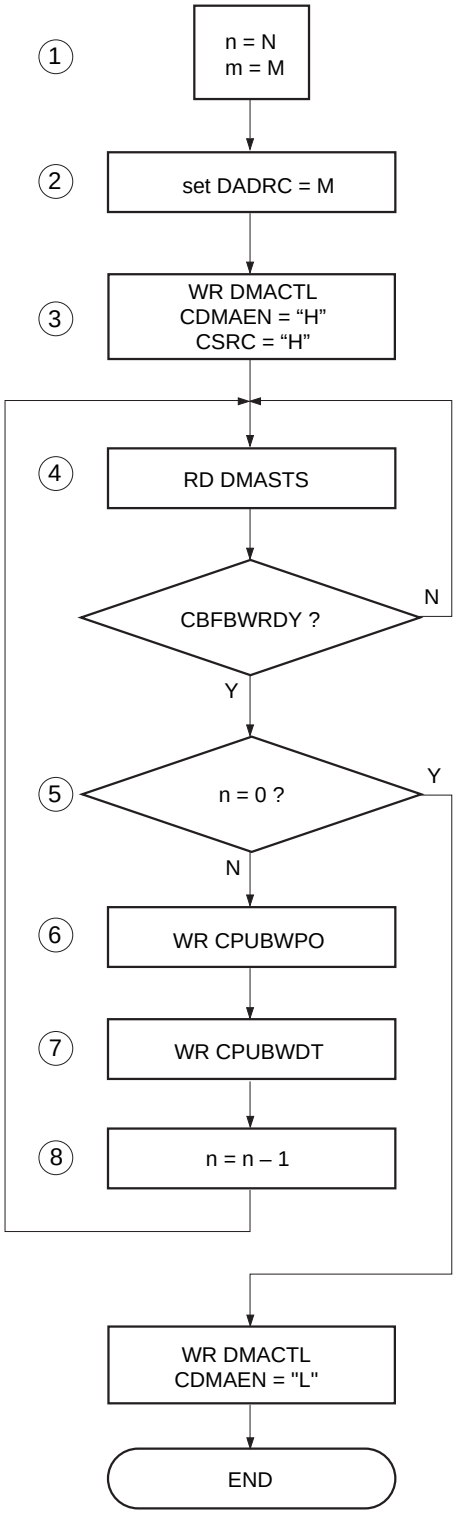


Fig. 6.1 CPU buffer write control

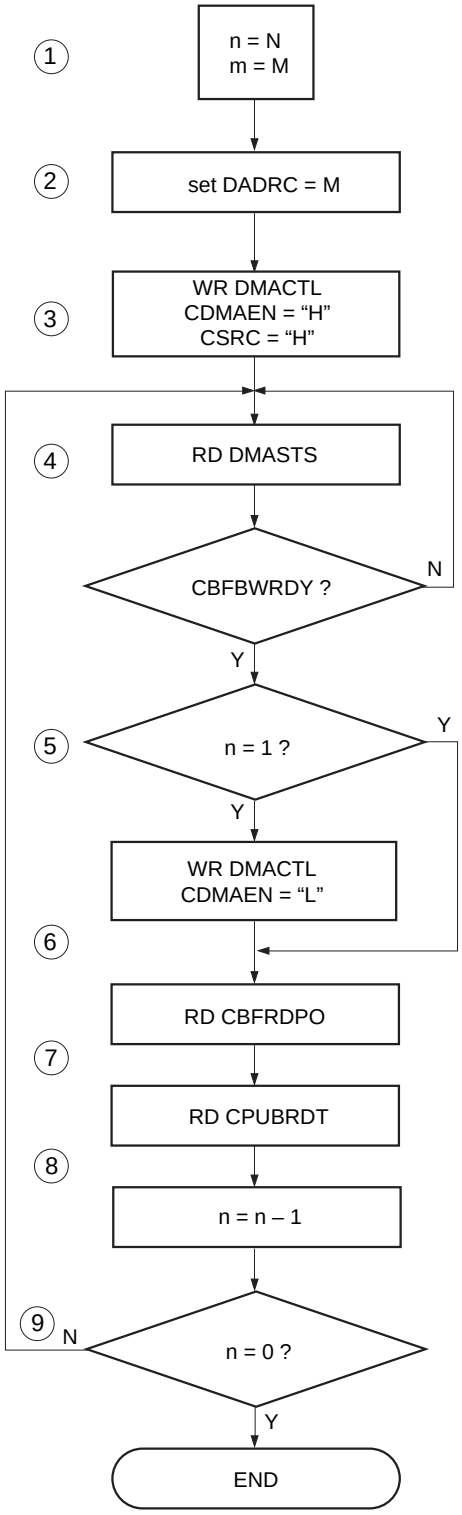
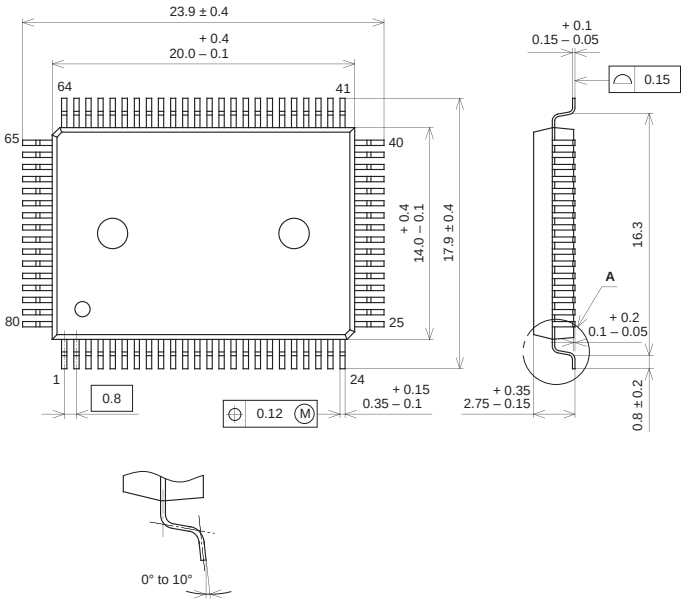


Fig. 6.2 CPU buffer read control

Package Outline Unit : mm

CXD1186CQ

80PIN QFP (PLASTIC)



DETAIL **A**

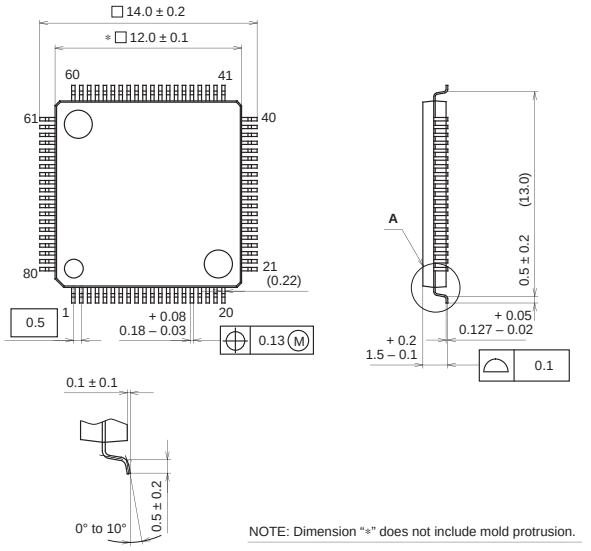
SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

CXD1186CR

80PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-80P-L01
EIAJ CODE	LQFP080-P-1212
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.5g