CIRRUS LOGIC®

CL-GD6412

Data Book

FEATURES

- **Single-chip VGA Controller**
- **Mixed voltage: 3.3 or 5.0 volts on any major interface**
  - Supports JEDEC Number 8 LVCMOS standard 3.3V +/- 0.3V
  - Mix 3.3V or 5.0V system components with no external-level converters
- **Based on proven CL-GD6410 architecture**
  - Same BIOS core, drivers, and utilities
- **IBM® VGA hardware-compatible**
- **Two 256K x 4 DRAM video memory for small form-factor**
- **Simultaneous CRT and LCD (SimulSCAN™) operation**
- **Integrates RAMDAC**
- **Integrates LCD panel interface**
  - Control and data buffering
  - Power sequencing logic
- **Direct connection to ISA (PC AT) Bus**
- **Frame-Accelerator for low-active power**
- **Standby and Suspend Modes to save power**
  - Hardware Suspend Pin
  - Under 100 mW suspend power
- **64-shade grayscale on monochrome STN (Super Twist Nematic) LCD**
  - NTSC sum-to-gray color mapping
  - Multiple sum-to-gray weighting options
- **Enhanced flicker-reduction algorithms for 4 MHz and quick-response LCDs**
- **Direct connection to 512-Color TFT (Thin Film Transistor) LCD**
  - Single-controller design for STN monochrome and TFT color LCDs
- **Graphics expansion and compression maps CRT modes to fixed-resolution LCD**
- **8- or 16-bit CPU Interface**
- **160-pin QFP package**

LCD VGA Controller for Mixed-Voltage Notebook Computers

OVERVIEW

The CL-GD6412 is a single-chip VGA controller optimized for use in systems with a mix of 3.3V and 5.0V components, where quick implementation of a notebook computer with reduced power consumption is the critical design objective. In a design using the CL-GD6412, the internal logic of the IC uses a 3.3V power supply for reduced power consumption. The video memory, host bus interface, panel interface, and clock interface may each be implemented at either 3.3V or 5V. The voltages of these interfaces may be mixed in any combination.

By using the Cirrus Logic Frame-Accelerator, the CL-GD6412 is able to provide a high vertical refresh rate for dual-scan LCD panels while operating at approximately one-half the clock speed of non-accelerated LCD controller solutions. In addition, multiple levels of system power management are supported in the CL-GD6412. Standby Mode can be driven by software, or an internal counter with accuracy to within one second. An output pin is provided to allow the on-chip standby

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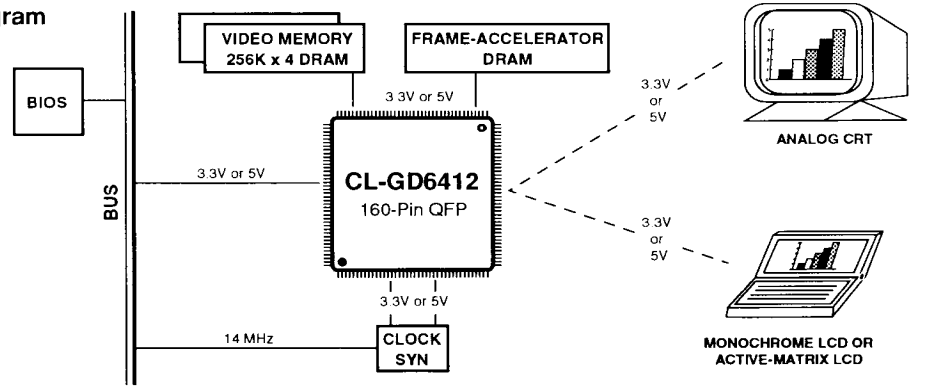
System Block Diagram



OVERVIEW (cont.)

timer to be used for other system purposes. Suspend Mode can be driven by software or by a hardware suspend pin. In Suspend Mode, the status of the CL-GD6412 register and pins is optimized for minimum power consumption. The hardware suspend pin allows a nearly complete shutdown of the device, with no bus decoding for very low power consumption.

The CL-GD6412 is based on the proven and mature CL-GD6410 architecture. Basic design and programming models are unchanged. This allows for the highest confidence in quick development schedules.

With the CL-GD6412, a complete motherboard VGA controller requires only four or five ICs, and three external pull-up/pull-down configuration resistors. It can be designed in less than four square inches (excluding power sources and connectors). A two-DRAM video memory interface (256K x 4), on-chip RAMDAC, direct-connect ISA (PC AT) bus interface, and direct-connect LCD interface, all help to minimize the form-factor.

The CL-GD6412 provides a 16-shade grayscale at 640 x 480 resolution through Frame-Rate Duty Cycle modulation. Stippling techniques provide a 64-shade grayscale in the VGA High-Color Mode, Mode 13H. The CL-GD6412 has enhanced algorithms for dynamic pattern-management within the Frame-Rate Duty Cycle, providing a grayscale with minimum apparent flicker, even on 4-MHz or quick-response ('mouse-quick') panels. In all cases, the Cirrus Logic grayscale provides smooth transitions from black, through the grayscale, to white, for maximum display quality of realistic images.

The CL-GD6412 panel interface includes programmable panel parameters, that allow a controller design to be optimized for excellent display quality on a variety of panels. On-chip power sequencing logic controls both the initial power-up to the panel, as well the resume power-up from Standby or Suspend Modes.

The CL-GD6412 supports SimulSCAN™, a technique introduced by Cirrus Logic for achieving simultaneous CRT and LCD operation. It allows the portable computer to become a key part of presentation environments for sales force automation, field service, and educational organizations. SimulSCAN supports both single- and dual-scan LCDs, and both fixed and multi-frequency analog CRTs. Resolution mapping manages the differences between VGA CRT mode resolutions and the LCD's fixed display resolution, so that a close match is achieved between the aspect ratio of the CRT and the LCD. Reverse video is controlled separately for the LCD display data path, so that page-white LCD operation may occur simultaneously with normal CRT operation.

DESIGN SUPPORT

In addition to offering innovative power-saving features based on a proven LCD VGA architecture, Cirrus Logic provides complete support materials to speed the development of the graphics controller subsystem of a mixed-voltage notebook computer:

Design Documentation:

- Data Book
- Application notes with complete schematics of the graphics subsystem
- Panel Interface Guide
- Register Specification
- BIOS External Function Specification

Software Products:

- Cirrus Logic BIOS
  - Optimized for features and performance of the CL-GD6412
  - Binary license available at no charge
  - Source license available
- Cirrus Logic OEM Utility software
- Cirrus Logic End-User Utility software
- CL-GD6412 BIOS/Utilities available from third-party software vendors

The GDK6412-A-DM1 Demonstration/Evaluation Board:

- Working ISA-bus card based on CL-GD6412
- Options for testing 3.3V or 5V components
- Cirrus Logic BIOS
- OEM Utilities and Demonstration Software

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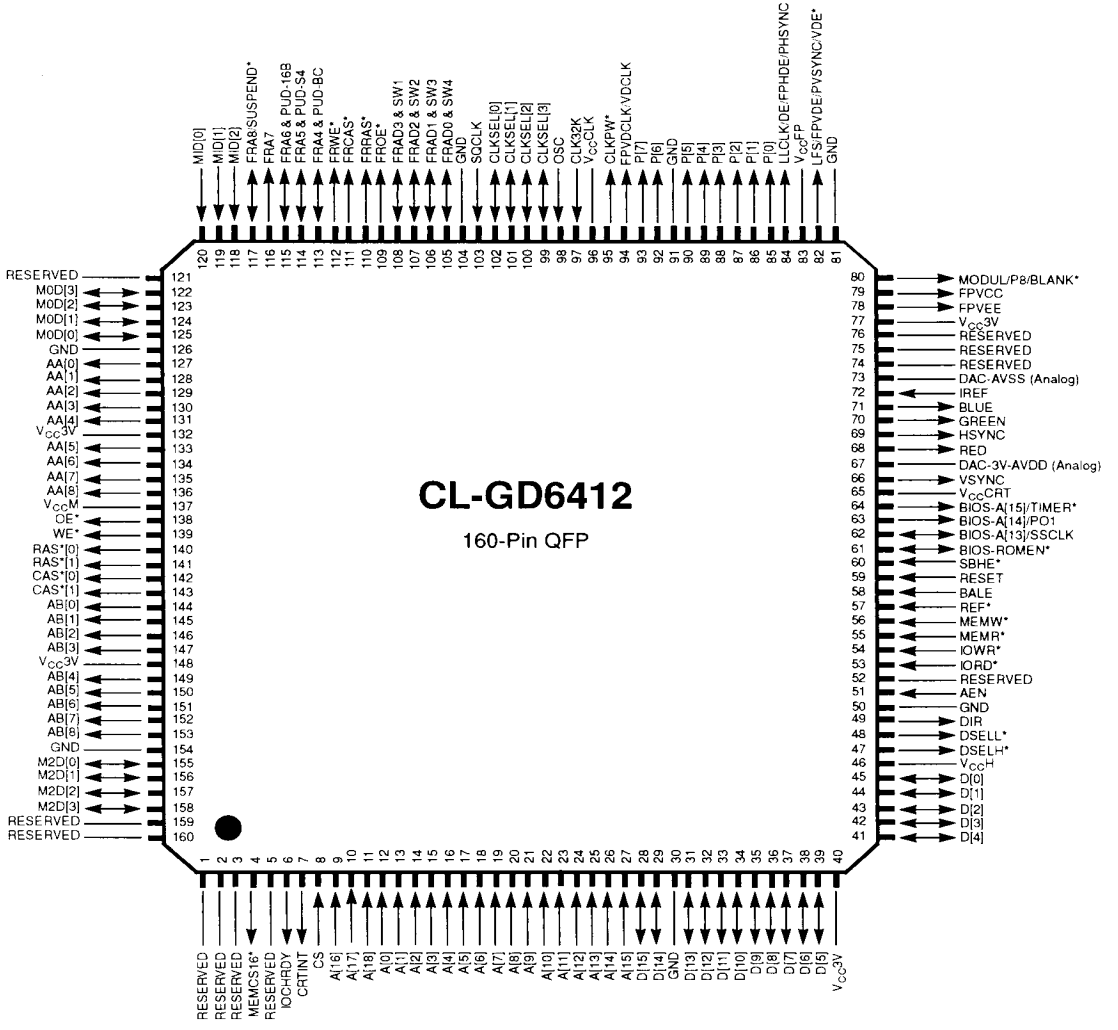
Figures

1. PIN INFORMATION

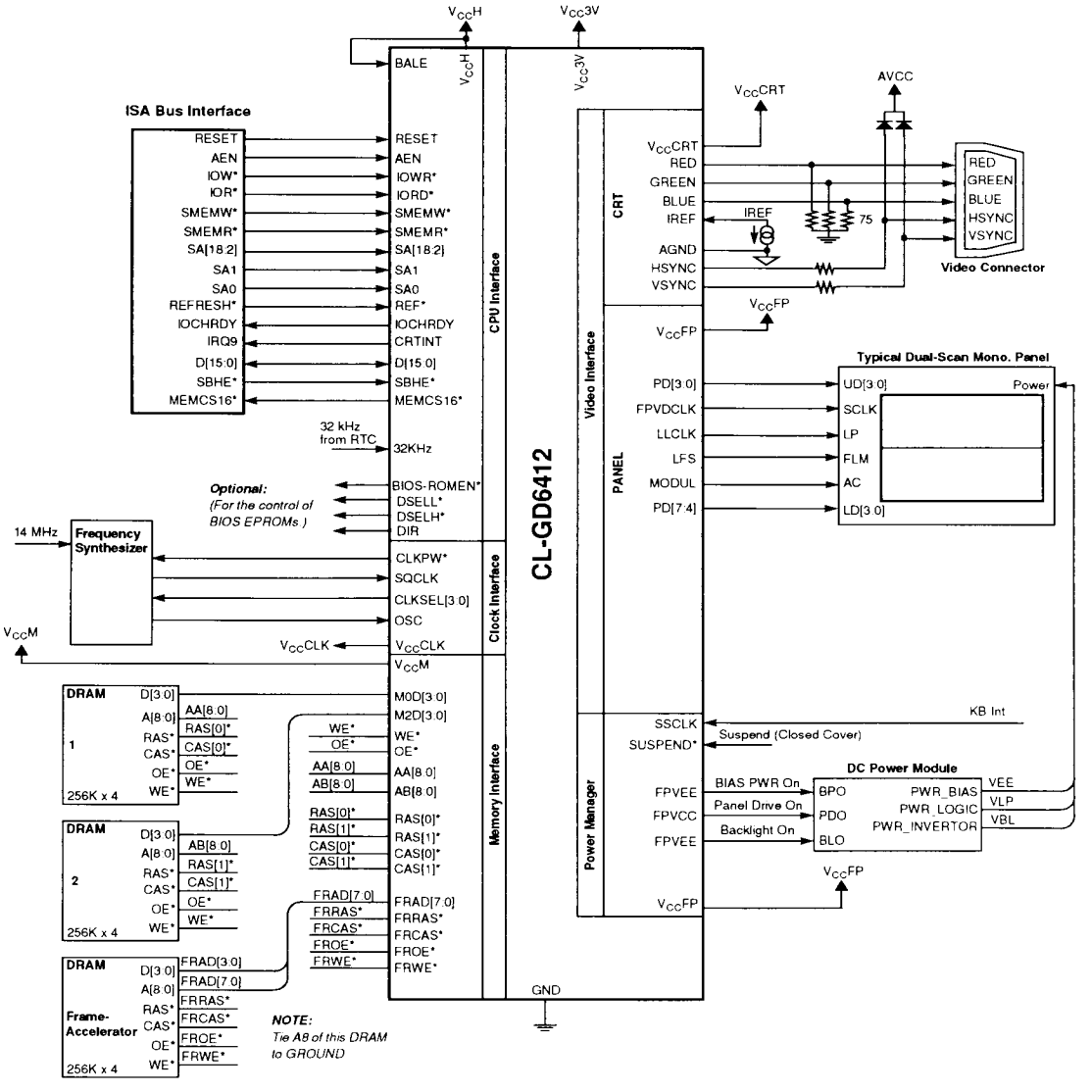
The CL-GD6412 is available in a 160-pin quad flat pack device configuration, shown below.

1.1 Pin Diagram



NOTE: In the figure above, an ampersand (&) in signal names indicates that its associated pin performs two functions simultaneously; a slash (/) indicates either/or operation.

1.2 Typical ISA Bus Dual-Scan Monochrome Panel, 256K x 4 DRAM Connections



2. DETAILED PIN DESCRIPTION

The following conventions are used in the pin assignment: (I) indicates input; (O) indicates output; (OD) indicates open-drain output; (TO) indicates tri-state output; (AO) indicates analog output, (AI) indicates analog input; (PW) indicates power.

2.1 Host Interface Group

Name	Pin No.	Type	Description
CS	8	I	**CHIP SELECT:** This pin defines the VGA memory address space, allowing the CL-GD6412 to respond to the normal VGA address space of 0A0000 to 0BFFFF. If the ISA-bus Signals SMEMR* and SMEMW* are employed, use LA[19] for this pin. If MEMRD* and MEMWR* are employed, use LA[23:19].
A[18:0]	11:9 27:12	I	**CPU ADDRESS INPUTS.** Use LA[18:0] or SA[18:0]. These inputs are used to select the resource to be accessed during any memory or I/O operation.
D[15:0]	28:29 31:39, 41:45	I/O	**CPU DATA I/O.**
DSELH*	47	O	**DATA SELECT HIGH BYTE:** This enables the CPU data bus upper-byte buffer when needed.
DSELL*	48	O	**DATA SELECT LOW BYTE:** This enables the CPU data bus lower-byte buffer when needed.
DIR	49	O	**CPU DATA BUS BUFFER DIRECTION:** When low, this indicates a CPU read. (DIR is used only when CPU data has to be buffered).
SBHE*	60	I	**BYTE HIGH ENABLE**: This input is used in conjunction with A[0] to determine the width and alignment of a data transfer. SBHE# and A[0] are decoded as shown in the following Table 2–1:

Table 2–1. BHE#/SBHE#/A0 Decoding

BHE#/SBHE#	A0	Function
0	0	16-bit Transfer
0	1	Upper-byte Transfer
1	0	Lower-byte Transfer

2.1 Host Interface Group *(cont.)*

Name	Pin No.	Type	Description
IORD*	53	I	**I/O READ:** This active-low input is used to indicate that an I/O read is occurring. If the address on SA[15:0] is within the range of the CL-GD6412, it will respond by placing the contents of the appropriate register on the System Data Bus.
IOWR*	54	I	**I/O WRITE:** This active-low input is used to indicate that an I/O write is occurring. If the address on SA[15:0] is within the range of the CL-GD6412, it will respond by transferring the contents of the System Data Bus into the appropriate register. The transfer will occur on the trailing (rising) edge of this signal.
MEMR*	55	I	**MEMORY READ:** This indicates that a memory read cycle is occurring.
MEMW*	56	I	**MEMORY WRITE:** This indicates that a memory write cycle is occurring.
REF*	57	I	**REFRESH:** This active-low signal indicates that a DRAM refresh is occurring. The CL-GD6412 delays memory read operations when REF* is active, since it explicitly controls the refresh of Display Memory.
BALE	58	I	**ADDRESS LATCH ENABLE:** A high indicates a valid memory address.
RESET	59	I	**SYSTEM RESET:** This input is normally connected to the System Reset Bus Signal and is used as a hardware reset signal for the CL-GD6412.
AEN	51	I	**ADDRESS ENABLE:** This is a host CPU Bus Signal that distinguishes between DMA and non-DMA bus cycles. The signal is high for a DMA cycle, and will cause the CL-GD6412 to ignore IORD* and IOWR*.
MEMCS16*	4	OD	**MEMCS16*:** This output is an acknowledge for 16-bit-wide accesses and is generated by the CL-GD6412 only if the 16-bit peripheral mode is enabled, and a valid memory address range has been decoded.

2.1 Host Interface Group *(cont.)*

Name	Pin No.	Type	Description
IOCHRDY	6	OD	**I/O CHANNEL READY:** This output, when driven low, indicates that additional wait states are to be inserted into the current Display Memory read or write cycle. This output is *never* driven low during I/O cycles or BIOS reads. During a Display Memory read cycle, this signal is always driven low as soon as MEMR* goes active. When the data is ready to be placed on the System Data Bus, this signal is driven high. It remains high until MEMR* goes inactive; it then goes high-impedance. During a Display Memory write cycle, this signal is driven high as soon as MEMW* goes active. If the Write Buffer is full, this signal is driven low as soon as MEMW* goes active and remains low until there is space. Once there is space in the Write Buffer, this signal is driven high. It will remain high until MEMW* goes inactive; it then goes high-impedance.
BIOS-A[13]/SSCLK	62	I/O	**BIOS ADDRESS 13:** This signal is used for pagination if the video BIOS is larger than 32K bytes. **SCREEN SAVE CLOCK:** This input is used to detect keyboard activity for Standby Mode. (Not available if the BIOS is larger than 32K bytes).
BIOS-A[14]/PO1	63	O	**BIOS ADDRESS 14:** This signal is used for pagination if the video BIOS is larger than 32K bytes. **PROGRAMMABLE OUTPUT 1:** (Not available if the BIOS is larger than 32K bytes).
BIOS-A[15]/TIMER*	64	O	**BIOS ADDRESS 15:** This signal is used for pagination if the video BIOS is larger than 32K bytes. **TIMER:** The Timer Output, active in Standby Mode, can be used to power-down system components. (Not available if the BIOS is larger than 32K bytes).
BIOS-ROMEN*	61	O	**BIOS-ROM ENABLE:** This is used to enable C000 BIOS ROM if the CL-GD6412 is used in an adapter card application.

2.1 Host Interface Group *(cont.)*

Name	Pin No.	Type	Description
CRTINT	7	TO	**CRTINT:** Indicates the start of a vertical retrace, normally connected to one of the interrupt inputs on the PC bus.
$V_{CC}H$	46	PW	**HOST BUS V_{CC} PIN:** This pin can be set to 3.3V or 5V. The Host Bus Interface pin group will operate at the voltage applied to this pin independent of the voltage applied to other pin groups.

2.2 Memory Interface Group

Name	Pin No.	Type	Description
AA[8:0]	136:133 131:127	O	**VIDEO MEMORY 'A' ADDRESS BUS:** This bus contains the row/column address information required by the DRAMs in Video Memory Planes 0 and 1. This bus carries different addresses than the AB Bus in text modes.
AB[8:0]	153:149 147:144	O	**VIDEO MEMORY 'B' ADDRESS BUS:** This bus contains the row/column address information required by the DRAMs in Video Memory Planes 2 and 3. This bus carries different addresses than the AA Bus in text modes.
OE*	138	O	**VIDEO MEMORY OUTPUT ENABLE:** This active-low output is used to control the output enables of the DRAMs. This pin must be connected to the OE* Pins of all the DRAMs in the Display Memory array.
WE*	139	O	**VIDEO MEMORY WRITE ENABLE:** This active-low output is used to control the Write Enable Inputs of the DRAMs.
RAS*[1:0]	141:140	O	**VIDEO MEMORY RAS*:** RAS*[0] to AA Bus, RAS*[1] to AB Bus.
CAS*[1:0]	143:142	O	**VIDEO MEMORY CAS*:** CAS*[0] to AA Bus, CAS[*1] to AB Bus.
M0D[3:0]	122:125	I/O	**VIDEO MEMORY DATA PINS:** Planes 0 and 1, Bits 3:0.
MID[2:0]	118:120	I	**MONITOR ID:** Bits 2:0. This pin can be sampled at reset or under software control.
M2D[3:0]	158:155	I/O	**VIDEO MEMORY DATA PINS:** Planes 2 and 3, Bits 3:0.
FRWE*	112	O	**FRAME-ACCELERATOR WRITE ENABLE*.**
FRCAS *	111	O	**FRAME-ACCELERATOR CAS*.**

2.2 Memory Interface Group *(cont.)*

Name	Pin No.	Type	Description
FRRAS*	110	O	**FRAME-ACCELERATOR RAS***.
FROE*	109	O	**FRAME-ACCELERATOR OE***.
FRAD3 & SW1	108	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[3]** multiplexed with Switch 1.
FRAD2 & SW2	107	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[2]** multiplexed with Switch 2.
FRAD1 & SW3	106	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[1]** multiplexed with Switch 3.
FRAD0 & SW4	105	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[0]** multiplexed with Switch 4.
FRA4 & PUD-BC	113	I/O	**FRAME-ACCELERATOR ADDRESS [4]** multiplexed with Pull-Up or Pull-Down BC (BIOS Control).
FRA5 & PUD-S4	114	I/O	**FRAME-ACCELERATOR ADDRESS [5]** multiplexed with Pull-Up or Pull-Down S4 (Sleep Control).
FRA6 & PUD-16B	115	I/O	**FRAME-ACCELERATOR ADDRESS [6]** multiplexed with Pull-Up or Pull-Down 16B (16-Bit BIOS Control).
FRA7	116	O	**FRAME-ACCELERATOR ADDRESS [7]**.
FRA8/SUSPEND*	117	I/O	**FRAME-ACCELERATOR ADDRESS [8]:** Either 64K x 4 or 256K x 4 DRAM may be used for the frame acceleration; 64K x 4 is the minimum requirement for 640 x 480 dual-scan flat panels. **FRA8** is only needed if a 256K x 4 DRAM is used for frame acceleration in a high-resolution LCD environment. If there is no high-resolution LCD environment, and a 256K x 4 DRAM is used, tie **FRA8** low and use **SUSPEND*** as an input. Note that when **SUSPEND*** goes active (low), the CL-GD6412 will enter Suspend Mode.
$V_{CC}M$	137	PW	**MEMORY V_{CC} PIN:** This pin can be set to 3.3V or 5V. The Memory Interface pin group will operate at the voltage applied to this pin independent of the voltage applied to other pin groups.

2.3 Flat Panel Interface Group

Name	Pin No.	Type	Description
LFS/FPVDE/PVSYNC /VDE*	82	O	**LCD FRAME START PULSE:** This indicates the start of a new frame on flat panels, or **FLAT PANEL VERTICAL DISPLAY ENABLE**, or **PANEL VERTICAL SYNC** for special panels, or **VIDEO DISPLAY ENABLE** for connection to the CL-GD6340.
LLCLK/DE/FPHDE/ PHSYNC	84	O	**FLAT PANEL LINE CLOCK**: This is used to increment Row-Shift Registers within LCD panels or **DISPLAY ENABLE** if the CL-GD6412 is used with the CL-GD6340, or **FLAT PANEL HORIZONTAL DISPLAY ENABLE**, or **PANEL HORIZONTAL SYNC** for special panels.
FPVDCLK/VDCLK	94	O	**FLAT PANEL VIDEO CLOCK: MONOCHROME OR COLOR PANEL SHIFT CLOCK,** or **VIDEO CLOCK:** Used with the CL-GD6430.
P[7:0]	93:92 90:85	O	**VIDEO DATA OUT:** Pixel data output for flat panels.
MODUL/P8/BLANK*	80	O	**LCD PANEL MODULATION SIGNAL:** This is required for LCD panels that do not drive the function themselves, or **P8** is needed for 512-color LCD panels. **BLANK*** is needed for interfacing with the CL-GD6340.
FPVCC	79	O	**LCD PANEL VOLTAGE CONTROL:** This signal is used for automatic or software-controlled flat panel power sequencing.
FPVEE	78	O	**LCD PANEL BACKLIGHT POWER CONTROL:** This signal is used for automatic or software-controlled flat panel power sequencing.
V_{CC}FP	83	PW	**FLAT PANEL V_{CC} PIN:** This pin can be set to 3.3V or 5V. The Flat Panel Interface pin group will operate at the voltage applied to this pin independent of the voltage applied to other pin groups.

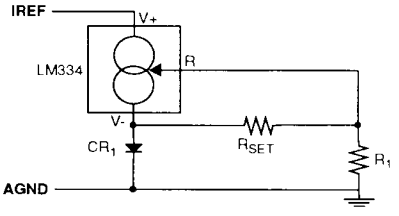
2.4 CRT Interface Group

Name	Pin No.	Type	Description
HSYNC	69	O	**HORIZONTAL SYNC** to CRT Monitor.
VSYNC	66	O	**VERTICAL SYNC** to CRT Monitor.
V_{CC}CRT	65	PW	**CRT V_{CC} PIN:** This pin should be tied to the maximum V_{CC} value applied to any other V_{CC} Pin. If any pin group V_{CC} is set to 5V, then this pin should be tied to 5V. If CRT operation is not required, then this pin should still be tied to the appropriate V_{CC} according to the above rules.

2.5 Clock Interface Group

Name	Pin No.	Type	Description
CLKPW*	95	O	**CLOCK CHIP POWER CONTROL:** Active low, can be used to control external transistor logic connected to clock synthesizer power pins. This signal is high in normal operation and low in Suspend Mode.
CLK32K	97	I	**32 kHz CLOCK:** The input is used both for slow timers and in Suspend Mode. Most system boards have this clock available for the Real Time Clock. **This input is required at all times.**
OSC	98	I	**CLOCK-IN:** This is an input from a multifrequency clock source or an optional 14.318 MHz crystal.
CLKSEL[3:0]	99:102	I/O	**CLOCK SELECT:** These are inputs from optional external oscillators or select outputs to a multifrequency synthesizer.
SQCLK	103	I	**VIDEO MEMORY SEQUENCER CLOCK.**
V_{CC}CLK	96	PW	**CLOCK SELECT V_{CC} PIN:** This pin can be set to 3.3V or 5V. The Clock Select interface pin group will operate at the voltage applied to this pin independent of the voltage applied to other pin groups.

2.6 Miscellaneous Interface Group

Name	Pin No.	Type	Description
RED	68	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. Each of the three DACs consists of 256 summed-current sources. For each pixel, either the 6-bit value from the Lookup Table or a 5- or 6-bit true-color value is applied to each DAC Input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF. To maintain IBM VGA-compatibility, each DAC output is typically terminated to monitor ground with a 75-ohm 1-percent resistor. This resistor, in parallel with the 75-ohm resistor in the monitor, will yield a 37.5-ohm impedance to ground.
GREEN	70	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
BLUE	71	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
IREF	72	I	**DAC CURRENT REFERENCE:** The current drawn from AV_{DD} through this pin determines the full-scale output of each DAC. This pin should be connected to a constant current source. **Example:** R_{SET} = 20 ohms ± 1% R_1 = 200 ohms ± 5% CR_1 = Schottky or equivalent 
DAC-AVSS	73	PW	**RAMDAC ANALOG V_{SS}.**
DAC-3V-AVDD	67	PW	**RAMDAC ANALOG V_{DD}.**

2.7 Miscellaneous Interface Group *(cont.)*

Name	Pin No.	Type	Description
$V_{CC}3V$	40, 77, 132, 148	PW	**3.3 VOLT V_{CC} PINS:** 3.3-volt power supply for internal operation of the CL-GD6412. For reduced power consumption, it is recommended to supply 3.3V on these seven pins even if all V_{CC} Pin groups are set to 5V.
GND	30, 50, 81 91, 104, 126, 154	PW	**GROUND PINS.**

3. FUNCTIONAL DESCRIPTION

3.1 Functional Operation

The CL-GD6412 interfaces with the host processor, video memory, display device, and other external I/O. The host memory interface may be either 8- or 16-bit. Video memory interface is optimized for 256K bytes. The CL-GD6412 is AT-bus-compatible to 10 MHz. Because the CL-GD6412 has a demultiplexed address and data bus, most systems will be able to interface it directly — without the addition of bus-interface buffers.

Flat-panel display devices supported will typically be 640 x 480-resolution monochrome STN or color TFT LCD panels. These panels are supported by a direct interface, precluding the need for buffers. Direct power sequencing is supported for panels that require it.

CRT displays supported are PS/2™ VGA-compatible analog monitors, including the IBM 85XX families, and multifrequency analog monitors, including the NEC® Multisync™ families. The CL-GD6412 also interfaces with the Cirrus Logic CL-GD6340 Color LCD Interface Controller for the best possible color support on a wide variety of color panels.

A PS/2-compatible RAMDAC, necessary to accomplish a VGA design, is built into the CL-GD6412. This provides savings in both power consumption and space requirements. The RAMDAC is fully compatible, and is fully supported by the CL-GD6412 enhanced power management features.

The four major operations supported by the CL-GD6412 are:

- ***Host Access to CL-GD6412 Registers***
- ***Host Access to Video Memory***
- ***Memory Refresh***
- ***Display Refresh***

Host Access to Registers

The host processor is typically a minimum 8088 or 80X86-type microprocessor in a PC/XT/AT bus-compatible environment and can access the CL-GD6412 Registers by setting up a 24-bit address and generating IORD*, IOWR, MEMR*, and MEMW* Signals. Memory reads and writes can be 8- or 16-bit; I/O reads and writes are 8-bit.

DRAM and screen refresh activities occur concurrently and independently. The registers that may be accessed by the host are listed in Section 4. They include all of the standard VGA registers.

All registers have been made host-readable and writable to allow BIOS and driver software to determine the state of the video controller, allowing it to be readily switched and restored in multi-tasking and windowing environments.

Host Access to Video Memory

Host access to video memory is channeled via the CL-GD6412. The host must establish the proper address/data/timing parameters in the CL-GD6412 Registers to transfer to and from video memory.

The CL-GD6412 also contains an intelligent sequencer that allocates video memory cycles not only to the host, but also to the DRAM refresh and the display CRT controllers.

Memory Refresh

Memory bandwidth is allocated to each process according to the actual real-time needs of the process, ensuring efficient use of the available bandwidth. For a CRT display device, the display is blanked during horizontal and vertical retrace intervals, opening memory bandwidth for host access and/or memory refresh.

Unlike early VGA implementations that gave the host only 14% of memory cycles, the CL-GD6412 can give the host from 25-50% access to video memory, or one out of two memory cycles. This is largely due to the sequencing strategy.

Display Refresh

In bit-mapped graphics modes, and text modes, pixel data is latched into the CL-GD6412, transferred to Shift Registers, and shifted out upon translation through the CL-GD6412 self-contained Color Palette Registers and RAMDAC.

The CL-GD6412 tracks the active and unused areas of the screen and cursor positions and consequently supplies screen control signals — VSYNC, HSYNC, and BLANK*.

When the CL-GD6412 is connected to a dual-scan LCD display, an additional 64K x 4 DRAM is needed. This Frame-Accelerator is used for split-panel data formatting. The reconstituted data from the Frame-Accelerator and video memory is then supplied in parallel to the LCD 4-bit upper and lower panel data buses. This technique not only maintains display contrast, but also reduces the power consumption of the video circuitry. The panel frame rate is twice the rate that the data is fetched from video memory.

3.2 CRT Display Modes

The CL-GD6412 includes all registers and data paths required for VGA compatibility. VGA enhancements include 16 simultaneously loadable text fonts (twice the capability of IBM VGA), and Readable Registers.

3.3 Flat Panel Display Modes

The CL-GD6412 will directly drive all of the popular monochrome dual-panel/dual-scan LCD panels. Proprietary techniques minimize flicker, noise, and pattern motion while enhancing contrast within the grayscales being used.

Grayscaling is accomplished by modulating the ON-to-OFF time of individual pixels in the panel and allowing the eye to integrate the superposed pixels to 16 perceptible grayscales. Flicker is reduced by proprietary techniques involving distribution of time between ON and OFF pixels during frame modulation.

The CL-GD6412 allows the full spectrum of PC applications written for analog monitors and various video modes to run on standard 640 x 480 flat panels. This is accomplished through color emulation, attribute remapping, and resolution mapping.

In addition, summing circuitry allows rapid generation of IBM-compatible grayscale equivalents of color images. Up to 64 grayscale levels are available by using proprietary two-dimensional stippling logic. This technique permits all applications that generate monochrome, 4,- 16-, or 256-color images to be run on a monochrome flat-panel display.

Cirrus Logic AutoMap logic can map 256 colors into a monochrome image; the colors then appear in 64 shades. The hardware-based algorithm tracks the particular palette map being used by the internal RAMDAC. RAMDAC data may be stored, as desired by the application, in orderly or random sequences. Realistic renditions of color images are not affected.

In color text modes, foreground and background attributes can be automatically remapped to black and white for maximum contrast. Positive or negative raster may be selected under program control to match the visual qualities of the display and/or needs of the application.

The video resolutions that an application has selected are remapped to a flat panel according to which mode (Compatibility, Compression, or Expanded) is selected.

3.4 Intelligent Power Management and Sequencing

Notebook and laptop PCs have stringent power limitations due to battery operation and heat dissipation. To meet these needs, the CL-GD6412 is manufactured using low-power CMOS technology.

The internal logic of the CL-GD6412 is designed for operation at 3.3V. Major interfaces can operate at 3.3V or 5V in any combination, simply by applying a 3.3V or 5V source to the special V_{CC} Pin in each pin group.

If V_{CC} CRT is 5V, any input or I/O pin can stand an input signal of 5V even if its group V_{CC} is 3.3V.

In addition, the CL-GD6412 has programmable output pins as well as other intelligent power management features that will permit the controller to enter the modes explained below to conserve power.

Several dedicated pins have been assigned to facilitate power management. The FPVCC and FPVEE Signals can be used to control panel logic power and panel back light/contrast, when a panel requires that these functions be sequenced or controlled. The CLKPW* Signal can be used to switch off system components such as the frequency synthesizer in Suspend Mode. The TIMER* Signal can be used to switch off system components in Standby Mode.

Normal Mode

- Power to LCD panel and full screen refresh
- CPU access to Video Memory
- Refresh to Video Memory
- CPU access to RAMDAC
- CPU access to I/O Registers

Since power consumption is directly proportional to the frequency at which the controller is run, the CL-GD6412 uses a proprietary Frame-Accelerator to maintain the maximum screen refresh rate, while the clock to the CL-GD6412 functions at 25 MHz or less. The Frame-Accelerator is used only with dual-scan LCD panels.

Standby Mode

- No power to LCD panel and no screen refresh
- Panel power sequencing is observed
- CPU access to Video Memory
- Refresh to Video Memory
- CPU access to RAMDAC
- CPU access to I/O Registers
- Frequency Synthesizer is not powered-down

The primary power savings in this mode come from cutting power to the LCD panel only. Any RAMDAC I/O can be executed. Since there is no screen refresh, normal clock rates are not required and may be replaced by slower clock rates to further reduce power consumption.

The SSCLK (Screen-Save-Clock) input pin can be used to detect a variety of external system activities; detecting keyboard activity is one recommended implementation. The system will recover from Standby Mode after receiving stimuli in the form of video memory read or write accesses, or the presence of the SSCLK Signal. If power sequencing is in progress, then the CL-GD6412 will allow the sequencing to complete before exiting Standby Mode.

Standby Mode is programmable in increments of one minute up to 63 minutes. If the feature is enabled, this is the time-out time from the last stimuli to automatically switch to Standby Mode. The timer can be activated by either the SSCLK Signal or by CPU memory access (read or write). A TIMER* Signal is provided as an output to provide an external indicator that the CL-GD6412 is in Standby Mode. There is also a register bit flagging the Standby state that can be used for software polling.

Suspend Mode

- No power to LCD panel and no screen refresh
- Panel power sequencing is observed
- No CPU access to Video Memory
- Refresh to Video Memory continues but using a 32-kHz clock
- No CPU access to RAMDAC
- No CPU access to I/O Registers
- Frequency Synthesizer is powered-down

The power savings in this mode occur because host access to video memory is now denied, and a slower clock is used. This slow clock refreshes video memory by performing CAS*-before-RAS* refresh. With slow-refresh DRAM, a clock running as slow as 32 kHz can be used. Other than this refresh logic, the rest of the CL-GD6412 does not have clocks, reducing power consumption even further.

There are two methods of implementing Suspend Mode in the design of a video controller with the CL-GD6412. Suspend Mode can be activated or deactivated under program control by a sequence of three consecutive I/O writes to the 'active' IBM VGA compatible 'Sleep' Port (46E8H or 3C3H), or by externally activating the SUSPEND* Pin.

Shutdown

- No power to LCD panel
- No clocks to the VGA controller subsystem

Prior to initiating a system-wide shutdown, the video-subsystem state can be saved by the system itself for later restoration. The CL-GD6412 allows the system to save or restore the status of all controller registers.

3.5 Internal RAMDAC

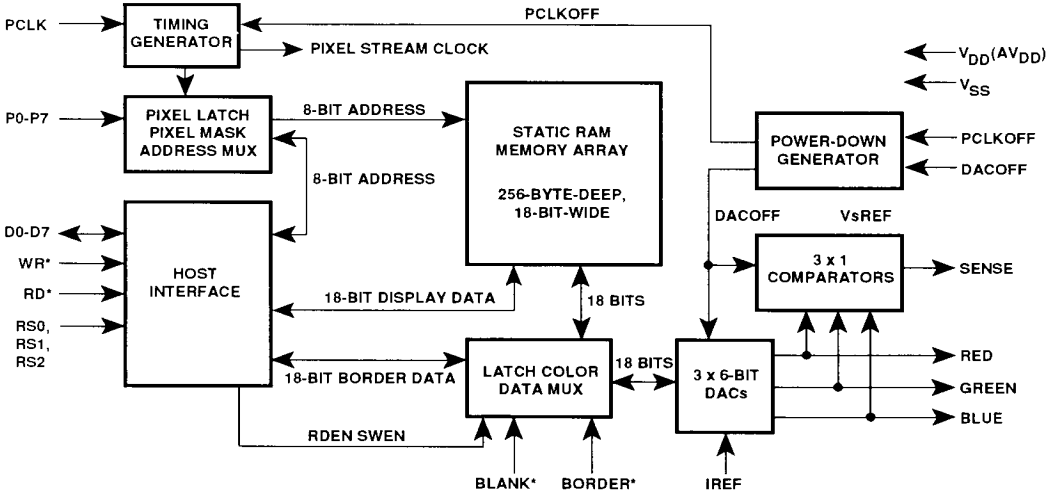
The CL-GD6412 includes an on-chip, high-speed, memory digital-to-analog converter known as a RAMDAC. The RAMDAC circuitry helps the CL-GD6412 process color video signals and timing information to the display.

The RAMDAC includes a 256-entry by 18-bit word color lookup table, three 6-bit digital-to-analog converters (DACs), a Pixel Mask Register and a Border Color Register.

An 8-bit address value applied on the pixel address inputs defines the memory location for reading an 18-bit color data word from the color lookup table. This data is partitioned as three fields of six bits each — one for R, one for G, and one for B — and then applied to the individual DAC inputs.

A pixel word mask is incorporated to allow the incoming pixel address to be altered, permitting changes to the color lookup table contents to be made immediately. This feature allows special display operations such as flashing objects and overlays to be created.

The color lookup table contents are accessed via its 8-bit-wide host interface. An internal synchronizing circuit allows the color value accesses to be completely asynchronous to the pixel video operation.



346412-1

NOTE: This diagram documents the RAMDAC as if it were external. Some signals are not INPUTS or OUTPUTS of the CL-GD6412.

Figure 3–1. RAMDAC Block Diagram

RAMDAC Video Operation

In video operation, pixel addresses P0 through P7, BLANK* is sampled on the rising edge of the pixel clock (PCLK). Its effect appears at the DAC outputs after three further rising edges of PCLK.

BLANK* is an active-low signal. When the BLANK* input is low, a binary 0 is applied to the DAC inputs, producing a zero-volt DAC output.

The DACOFF* Input is both a display disable control and a DAC power-down control. When DACOFF* is low, the DACs in the RAMDAC are totally inoperative, which results in the power dissipation being reduced to standby minimum. During this time, the three DAC outputs are at a zero-volt level. When DACOFF* goes high, several PCLK cycles are required before the DACs in the RAMDAC will function properly.

Analog Outputs

The DAC outputs are designed to produce 0.7-volt peak white amplitude with a reference current (I_{REF}) of 6.7 mA when driving a doubly terminated 75 ohm load, which corresponds to an effective DAC output load of 37.5 ohms ($R_{effective}$).

For all values of I_{REF} and output loading:

$V_{blacklevel}$ = zero volts

Writing to the Color Lookup Table

To write a color definition to the lookup table, a value specifying an address location in the lookup table is first written to the Write Mode Address Register. The color values for the red, green, and blue intensities are then written in succession to the Color Value Register. After the blue data is latched, this new color data is then written into the lookup table at the defined address, and the Address Register is incremented automatically.

Since Address Register increments after each transfer of data to the lookup table, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to the Write Address Mode Register. The color data for each address location is then sequentially written to the Color Value Register. The RAMDAC automatically writes data to the lookup table and increments the Address Register after each host transfer of three bytes of color data.

Reading from the Color Lookup Table

To read color data from the lookup table, a value specifying the address location of the data is written to the Read Mode Address Register. After the address is latched, the data from this location is automatically read out to the Color Value Register, and the Address Register automatically increments.

The color intensity values are then read from the Color Value Register by the sequence of three read (RD*) commands. After the blue value is transferred out, new data is read from the lookup table at the current address to the Color Value Register, and the Address Register to automatically increment again.

If the Address Register is loaded with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This occurs for both read and write operations.

3.6 CL-GD6412 Configuration

The CL-GD6412 provides several configuration options. These options are set by installing 'pull-up' or 'pull-down' resistors on certain CL-GD6412 pins, which are sampled at system reset. The selections made are configurations that need only be made once. All listed connections are required.

Pin Name and No.	Function	Notes
FRA5/PUD-S4 (114)	Sleep Mode I/O Address High = 46E8h; Low = 3C3h	Normally high for adapter controller implementations, low for motherboard implementations.
FRA4/PUD-BC (113)	BIOS Support High = BIOS @ C000; Low = E000	Low for motherboard implementations when the desired BIOS is at E000 or at C000 with no on-chip BIOS support. Pull high for adapter implementations or when the BIOS is at C000.
FRA6/PUD-16B (115)	BIOS Width Select High = 16-bit BIOS; Low = 8-bit	Defines BIOS-to-controller interface.

FRAD0/SW4 (105)
FRAD1/SW3 (106)
FRAD2/SW2 (107)
FRAD3/SW1 (108) Panel Class

SW3	SW2	SW1	Panel Class
0	0	0	0 = 3 MHz
0	0	1	1 = 6/6.3 MHz
0	1	0	2 = 3 MHz with extra line clock
0	1	1	3 = TFT
1	0	0	4 = 3 MHz
1	0	1	5 = 6/6.3 MHz
1	1	0	6 = 3 MHz with extra line clock
1	1	1	7 = Plasma

4. VIDEO MODES

4.1 CRT Video Modes

Table 4–1. IBM Standard VGA Video Modes

Mode No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Dot Clock MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0,1	16/256K	40 x 25	9 x 16	360 x 400	Text	28	31.5	70
2, 3	16/256K	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
4, 5	4/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70
6	2/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70
7	Monochrome	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
D	16/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70
E	16/256K	80 x 25	8 x 14	640 x 200	Graphics	25	31.5	70
F	Monochrome	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
10	16/256K	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
12	16/256K	30 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
13	256/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70

4.2 LCD Video Modes

Table 4–2. IBM Standard VGA Video Modes

Mode No.	Mono. STN Number of Shades	Color STN Number of Colors	Color TFT Number of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Expanded Char. Cell	Expand Size	Display Mode
0,1	16/16	16/256K	16/256K	40 x 25	9 x 16	360 x 400	Text	16 x 19	640 x 475	Text
2, 3	16/16	16/256K	16/256K	80 x 25	9 x 16	720 x 400	Text	8 x 16	640 x 475	Text
4, 5	4/64	4/256K	4/256K	40 x 25	8 x 8	320 x 200	Graphics	NA	640 x 475	Graphics
6	2/16	2/256K	2/256K	80 x 25	8 x 8	640 x 200	Graphics	NA	640 x 475	Graphics
7	2/16	Mono.	Mono.	80 x 25	9 x 16	720 x 400	Text	8 x 19	640 x 475	Text
D	16/64	16/256K	16/256K	40 x 25	8 x 8	320 x 200	Graphics	NA	640 x 475	Graphics
E	16/16	16/256K	16/256K	80 x 25	8 x 14	640 x 200	Graphics	NA	640 x 475	Graphics
F	2/16	Mono.	Mono.	80 x 25	8 x 14	640 x 350	Graphics	NA	640 x 475	Graphics
10	16/16	16/256K	16/256K	80 x 25	8 x 14	640 x 350	Graphics	NA	640 x 475	Graphics
11	2/16	2/256K	2/256K	80 x 30	8 x 16	640 x 480	Graphics	NA	640 x 480	Graphics
12	16/16	16/256K	16/256K	30 x 30	8 x 16	640 x 480	Graphics	NA	640 x 480	Graphics
13	64/256K	256/256K	256/256K	40 x 25	8 x 8	320 x 200	Graphics	NA	640 x 475	Graphics

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0° C to 70° C
Storage temperature ..... -65° C to 150° C
Voltage on any pin with respect to ground ..... -0.5 to V_{CC} + 0.5 Volts
Operating power dissipation ..... 1 Watt
Suspend power dissipation ..... 1 mW
Power supply voltage ..... 7 Volts
Injection current (latch-up) ..... 25 mA

NOTE: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

5.2 CL-GD6412 DC Specifications (Digital)

(V_{CC} = 5V ± 10% or 3.3V ± 0.3V; T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{CC}	Power Supply Voltage	4.5	5.5	Volts		
$V_{CC}3V$	Power Supply Voltage	3.0	3.6	Volts		
V_{IL}	Input Low Voltage	-0.5	0.8	Volts		
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts		3
V_{OL}	Output Low Voltage		0.4	Volts	I_{OL} = 4 mA	1
V_{OH}	Output High Voltage	2.15	V_{CC} - 0.5	Volts	I_{OH} = 400 µA	
I_{OZ}	Input Leakage	-10	10	µA	$0 < V_{IN} < V_{CC}$	
C_{IN}	Input Capacitance		10	pF		2
C_{OUT}	Output Capacitance		10	pF		2

NOTES:

1) I_{OL} MAX for IOCHRDY, MEMCS16* = 24 mA.
   I_{OL} MAX for CRTINT = 12 mA.
   I_{OL} MAX for CPU DATA, WE*, CAS* = 8 mA.
   I_{OL} MAX for LCD Control Signals = 4 mA (FPVDCLK, LLCLK, MODUL, LFS).
2) This is not 100% tested, but is periodically sampled.
3) V_{IH} on any input is controlled by V_{CC} CRT that is higher or equal to any other V_{CC} Pin of the CL-GD6412.

Symbol	Parameter	5V MAX	3.3V MAX	Units	Test Conditions	Note
I_{CC1}	Power Supply Current	150	100	mA	CRT Operation	1
I_{CC2}	Power Supply Current	95	55	mA	LCD Operation	1
I_{CC3}	Power Supply Current	0.1	0.05	mA	Suspend Mode	

NOTE:

1) V_{CC} = 3.3V, FPVDCLK = 28 and 24 MHz, MEMCLK = 43.9 MHz.

5.3 CL-GD6412 DC Specifications (RAMDAC)

(V_{CC} = 5V ± 10% or 3.3V ± 0.3V; T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	DAC Supply Voltage	3.00	3.60	Volts	Normal Operation	
A_{VDD}	DAC Supply Voltage	4.5	5.5	Volts	Normal Operation	
I_{REF}	DAC Reference Current	-3	-10	mA		1

NOTE:
1) See the Detailed Pin Description for information regarding nominal I_{REF}.

5.4 DAC Characteristics

(V_{CC} = 5V ± 10% or 3.3V ± 0.3V; T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
R	Resolution		6	Bits		
IO	Output Current		30	mA	VO < 1V	
TR	Analog Output Rise/Fall Time		8	ns		1, 2, 3
TS	Analog Output Settling Time		30	ns		1, 2, 4

NOTES:
1) Load is 37.5 ohms and 30 pF per analog output.
2) IREF = -6.67 mA.
3) TR is measured from 10% to 90% full-scale.
4) TS is measured from 50% of full-scale transition to output remaining within 2% of final value.

6. AC TIMING CHARACTERISTICS

This section includes system timing requirements for the CL-GD6412. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0 to 70° C, and V_{CC} varying from 3.00 to 3.60V DC and 4.50 to 5.50V DC. The AT Bus speed is 10 MHz unless otherwise noted. Note that (*) denotes an active-low signal.

1. All timings assume a load of 50 pF.
2. TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.
3. On power-up, all DRAM interface signals are inactive. Memory data bus is in Input Mode to sense values on configuration option pins set by pull-up or pull-down resistors.
4. The CL-GD6412 executes eight RAS*-only cycles to initialize DRAMs before executing normal cycles.

6.1 Index of Timing Information

Table 6–1. Bus Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_{MAV}	MEMCS16* active delay from LA[23:17] valid	–	35	ns
t_{IAD}	IOCS16* active delay from address	–	25	ns
t_{ASC}[bc]	Address, SBHE* setup to any command active	15	–	ns
t_{CAI}	Any command active to IOCHRDY inactive low	–	50	ns
t_{MID}	MEMCS16* inactive delay from address invalid	–	25	ns
t_{IPW}	IOW*, IOR* pulse width SMEMW*, SMEMR* pulse width	180 100	– –	ns ns
t_{ICA}	IOW* inactive to any command active SMEMW* inactive to next SMEMW*	100 100	– –	ns ns
t_{ASH}	Address, SBHE* hold from any command inactive	0	–	ns
t_{DVS}	Data valid from SMEMW* active Data valid from IOWR* active	– –	40 130	ns ns
t_{DHS}	Data hold from SMEMW* inactive Data hold from IOW* inactive	10 0	– –	ns ns
t_{DDI}	Data delay from IOR*, SMEMR* active	0	130	ns
t_{DDA}	Data delay from IOCHRDY active	–	15	ns
t_{DHI}	Data hold from IOR*, SMEMR* inactive	0	20	ns
t_{ASI}	AEN setup to IOR* or IOW* active	20	–	ns
t_{AHI}	AEN hold from IOR* or IOW* inactive	5	–	ns
t_{RSS}	REF* active setup to SMEMR* active	20	–	ns
t_{RHS}	REF* active hold from SMEMR* active	0	–	ns

a. The ISA Bus interface specifications are valid from 0° to 70° C at operating voltages of 3.3 volts +/- 0.3 volts and 5 volts +/- 0.5 volts.
b. AEN must be Inactive for t_2, t_3, and t_6.
c. Command is defined as IORD*, IOWR*, SMEMR*, or SMEMW*.

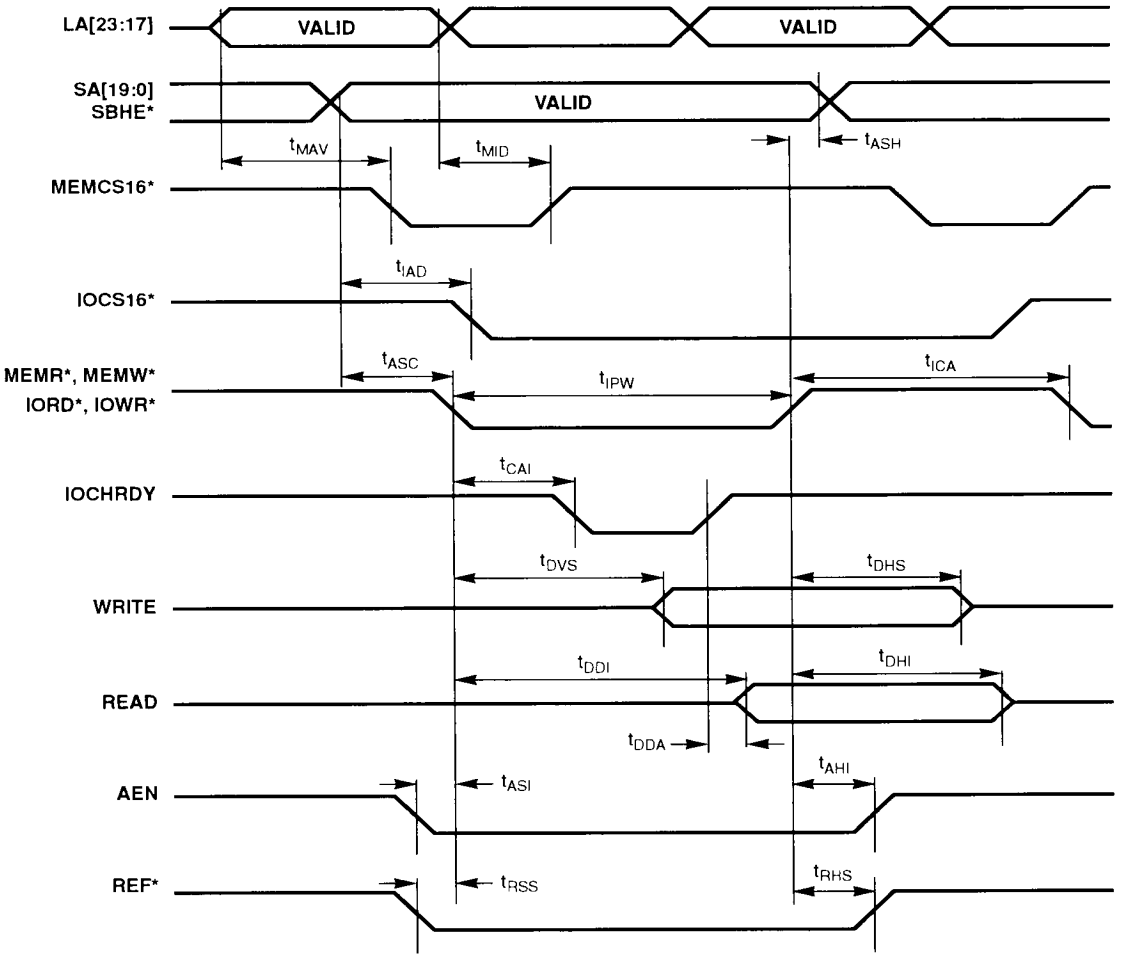


Figure 6–1. Bus Signal Timing (ISA Bus)

Table 6–2. DSELH*/DSELL* and DIR Timing for Read Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_{CD8}	Command active to buffer control active	–	40	ns
t_{ICD8}	Command inactive to buffer control inactive	–	20	ns

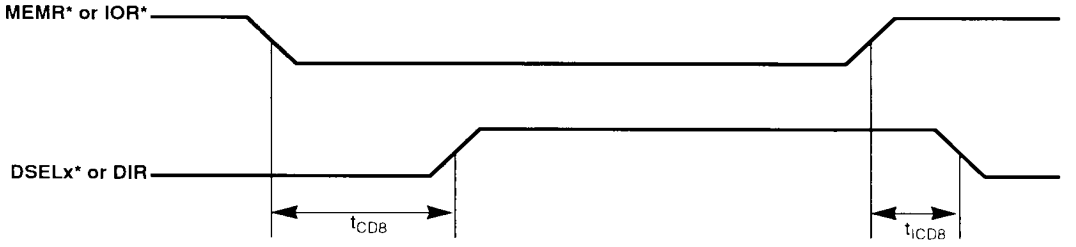


Figure 6–2. DSELH*/DSELL* and DIR Timing for Read Access (ISA Bus)

Table 6–3. DSELH*/DSELL* Timing for Write Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_{CDS}	Command active to DSELx* active	–	40	ns
t_{ICDS}	Command inactive to DSELx* inactive	–	20	ns

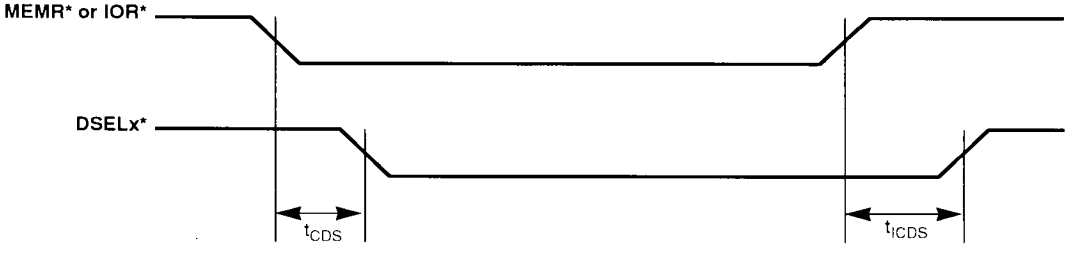


Figure 6–3. DSELH*/DSELL* Timing for Write Access (ISA Bus)

Table 6–4. BIOS-ROMEN* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_{RAM}	BIOS-ROMEN* active delay from MEMR* active	–	30	ns
t_{RIM}	BIOS-ROMEND* inactive delay from MEMR* inactive	–	30	ns

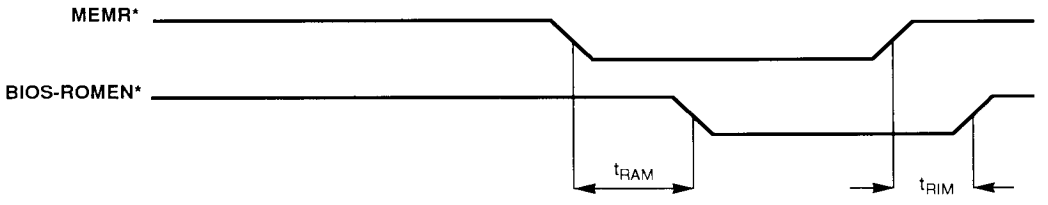


Figure 6–4. BIOS-ROMEN* Timing (ISA Bus)

Table 6–5. Read Timing (Display Memory Bus) (t = SQCLK)[a]

Symbol	Parameter	MIN	MAX
t_{ASR}	Address setup to RAS* active	5 ns	–
t_{ASC}	Address setup to CAS* active	5 ns	–
t_{RCD}	RAS* active to CAS* active delay	2.5t	–
t_{RAH}	Row address hold from RAS* active	1t	–
t_{CAH}	Column address hold from CAS* active	1t	–
t_{RAC}	Data valid from RAS* active	–	4t
t_{CAC}	Data valid from CAS* active	–	1.5t
t_{AA}	Data valid from column address valid	–	2t
t_{RP}	RAS* precharge (RAS* pulse width high)	3t	–
t_{RC}	Read cycle time	7t	–
t_{RCH}	Read command hold from CAS* high	0.5t	–
t_{CP}	CAS* precharge (CAS* pulse width high)	0.5t	–
t_{RAS}	RAS* pulse width low RAS* pulse width low (Page Mode)	4t	 32 µs
t_{CAS}	CAS* pulse width low	1.5t	32 µs
t_{OFF}	Read data hold from CAS* high	10 ns	–
t_{RCS}	Read command setup time	5 ns	–
t_{OE}	Data valid from OE* low	–	1.5t
t_{RRH}	Read command hold from RAS* high	1t	–
t_{RSH}	RAS* hold time from OE* low	1.5t	–
t_{CRP}	CAS* to RAS* precharge	0.5t	–
t_{CSH}	RAS* active to CAS* inactive	4t	–
t_{PC}	CAS* cycle time	2t	–
t_{OD}	Read data hold from OE* high	10 ns	–

a. The memory interface specifications are valid from 0 to 70° C at operating voltages of 3.3 volts +/- 0.3 volts and 5 volts +/- 0.5 volts.

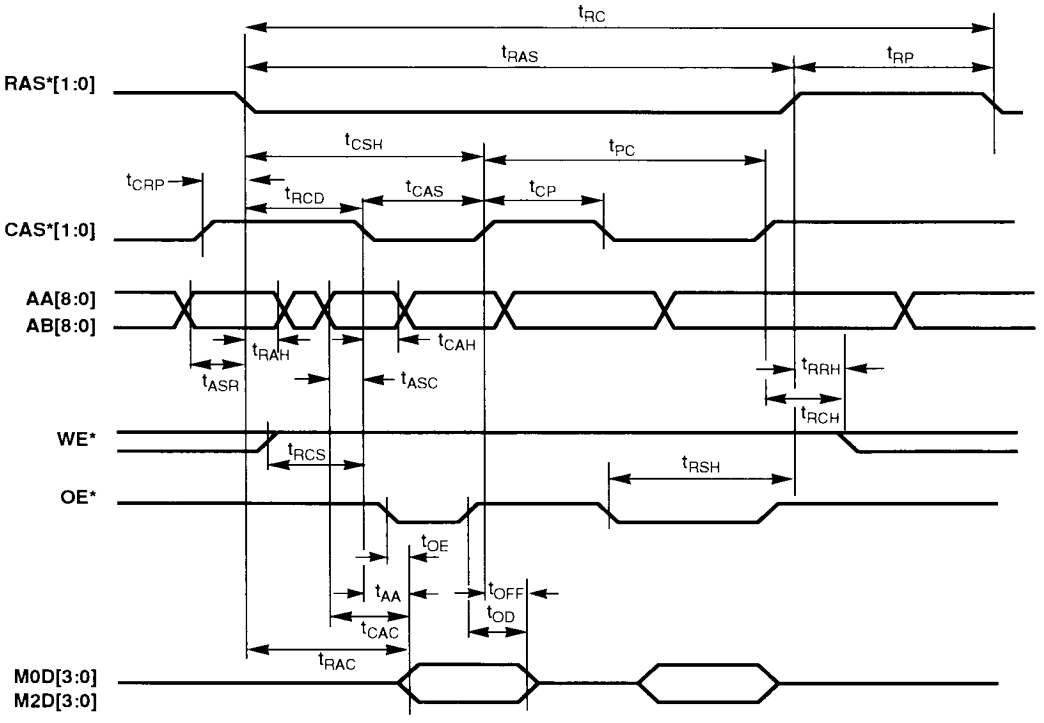


Figure 6–5. Read Timing (Display Memory Bus)

Table 6–6. Write Timing (Display Memory Bus) (t = SQCLK)[a]

Symbol	Parameter	MIN	MAX
t_{ASR}	Address setup to RAS* active	5 ns	–
t_{ASC}	Address setup to CAS* active	5 ns	–
t_{RCD}	RAS* active to CAS* active delay	2.5t	–
t_{RAH}	Row address hold from RAS* active	1t	–
t_{CAH}	Column address hold from CAS* active	1t	–
t_{RP}	RAS* precharge (RAS* pulse width high)	3t	–
t_{RC}	Write cycle time	7t	–
t_{CP}	CAS* precharge (CAS* pulse width high)	0.5t	–
t_{CRP}	CAS* to RAS* precharge	0.5t	–
t_{CSH}	RAS* active to CAS* inactive	4t	–
t_{PC}	CAS* cycle time	2t	–
t_{CAS}	CAS* pulse width low	1.5t	32 µs
t_{RAS}	RAS* pulse width low RAS* pulse width low (Page Mode)	4t	 32 µs
t_{WCS}	WE* active setup to CAS* active	0.5t	–
t_{WCH}	WE* active hold to CAS* active	0.5t	–
t_{WP}	WE* active pulse width	1t	–
t_{DS}	Write data setup to CAS* active	5 ns	–
t_{DH}	Write data hold from CAS* active	1t	–
t_{CWL}	WE* active to CAS* inactive	1t	–

a. The memory interface specifications are valid from 0 to 70° C at operating voltages of 3.3 volts +/- 0.3 volts and 5 volts +/- 0.5 volts.

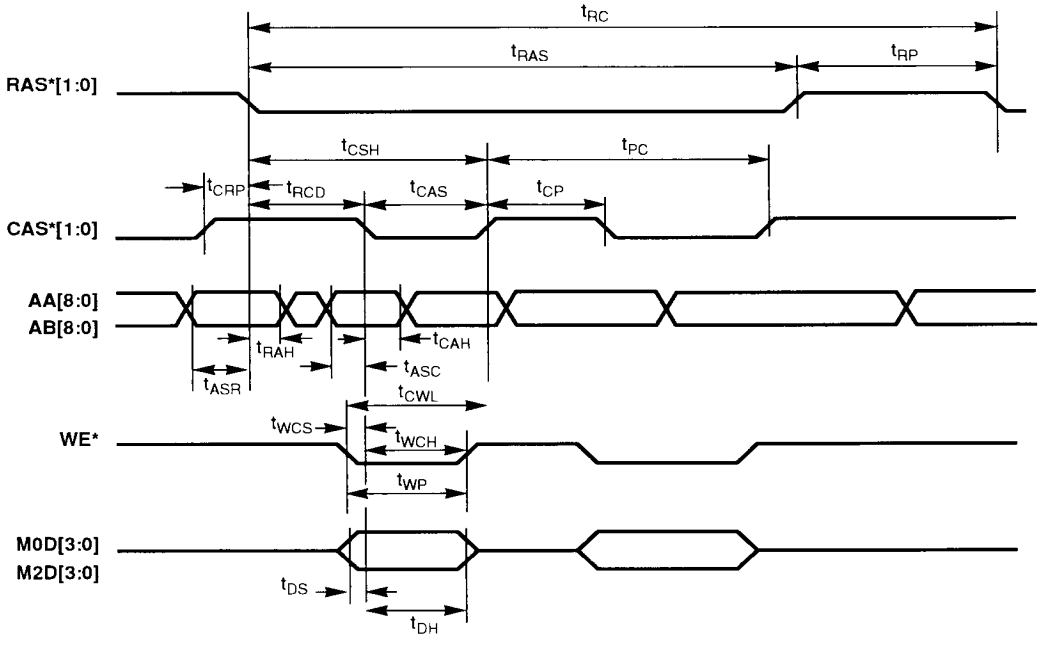


Figure 6–6. Write Timing (Display Memory Bus)

Table 6–7. CAS*-before-RAS* Refresh Timing (Display Memory Bus)[a]

Symbol	Parameter	MIN	MAX
t_{CSA}	CAS* active setup to RAS* active	1t	–
t_{RLP}	RAS* low pulse width	4t	–
t_{RHP}	RAS* high pulse width	3t	–
t_{CHR}	CAS* Hold for refresh	1.5t	–
t_{RCP}	Refresh cycle period	7t	–
t_{CAP}	CAS* precharge	2t	–
t_{RCA}	RAS* to CAS* precharge	1t	–

a. There will be either three or five RAS* pulses while CAS* remains low.

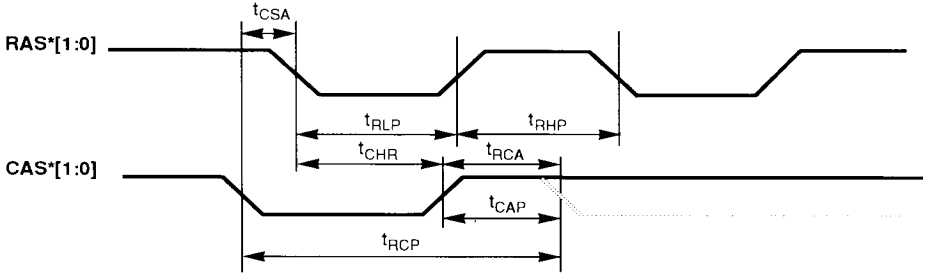


Figure 6–7. CAS*-before-RAS* Refresh Timing (Display Memory Bus)

Table 6–8. Internal RAMDAC Timing

Symbol	Parameter	MIN	MAX	Units
t_{BSV}	P[7:0], BLANK* setup to VDCLK	3	–	ns
t_{BHV}	P[7:0], BLANK* hold from VDCLK	3	–	ns
t_{VCD}	R, G, B delay from VDCLK	20	–	ns

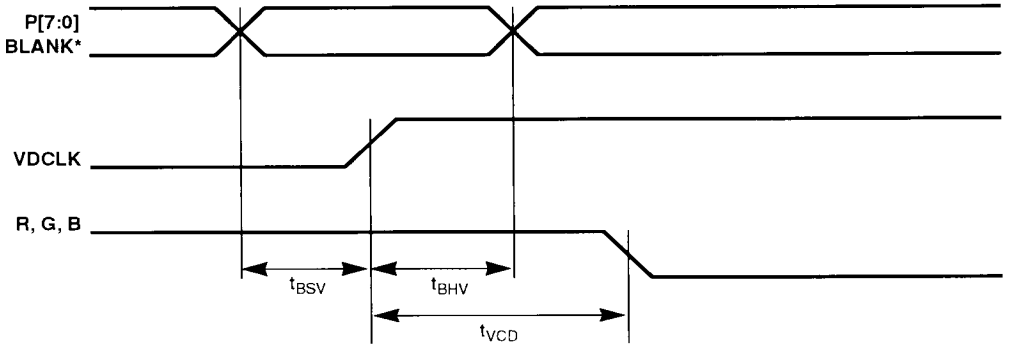


Figure 6–8. Internal RAMDAC Timing

Table 6–9. Clocks

Symbol	Parameter	MIN	MAX	Unit
t_{CP}	Clock period:			
	SQCLK	–	43.9	MHz
	OSC		28	MHz
	OSC (monochrome LCD)		25.175	MHz
	OSC (512-color TFT LCD)		25.175	MHz
t_R	Rise time:			
	SQCLK	–	6	ns
	VDCLK		6	ns
	OSC (below 25 MHz)		10	ns
	OSC (above 25 MHz)		6	ns
	CLKSEL[3:0] (below 25 MHz)		10	ns
	CLKSEL[3:0] (above 25 MHz)		6	ns
t_F	Fall time:			
	SQCLK	–	6	ns
	VDCLK		6	ns
	OSC (below 25 MHz)		10	ns
	OSC (above 25 MHz)		6	ns
	CLKSEL[3:0] (below 25 MHz)		10	ns
	CLKSEL[3:0] (above 25 MHz)		6	ns
t_H	High period (see note below):			
	SQCLK	-5%	+5%	–
	VDCLK	-5%	+5%	
	OSC	-5%	+5%	
	CLKSEL[3:0]	-5%	+5%	
t_L	Low period (see note below):			
	SQCLK	-5%	+5%	–
	VDCLK	-5%	+5%	
	OSC	-5%	+5%	
	CLKSEL[3:0]	-5%	+5%	

NOTE: The percentages for high and low period indicate permissible deviation from $t_{CP}/2$.

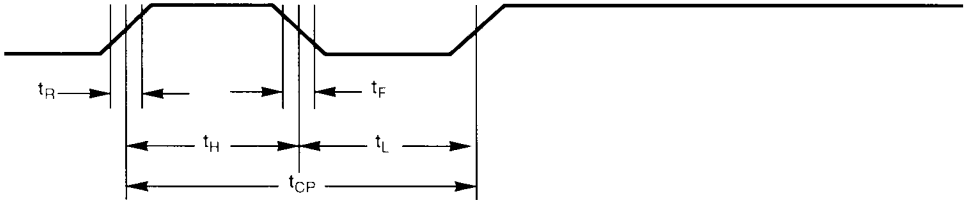


Figure 6–9. Clocks

Table 6–10. Sync, BLANK*, and RGB as Outputs

Symbol	Parameter	MIN	MAX	Units
t_{VBD}	VDCLK to BLANK* delay	3	T_C-5	ns
t_{VPD}	VDCLK to P[7:0] delay	3	T_C-5	ns
t_{VHD}	VDCLK to HSYNC, VSYNC delay	0	T_C-5	ns
t_{AND}	VDCLK to R, G, B, delay	0	T_C-5	ns

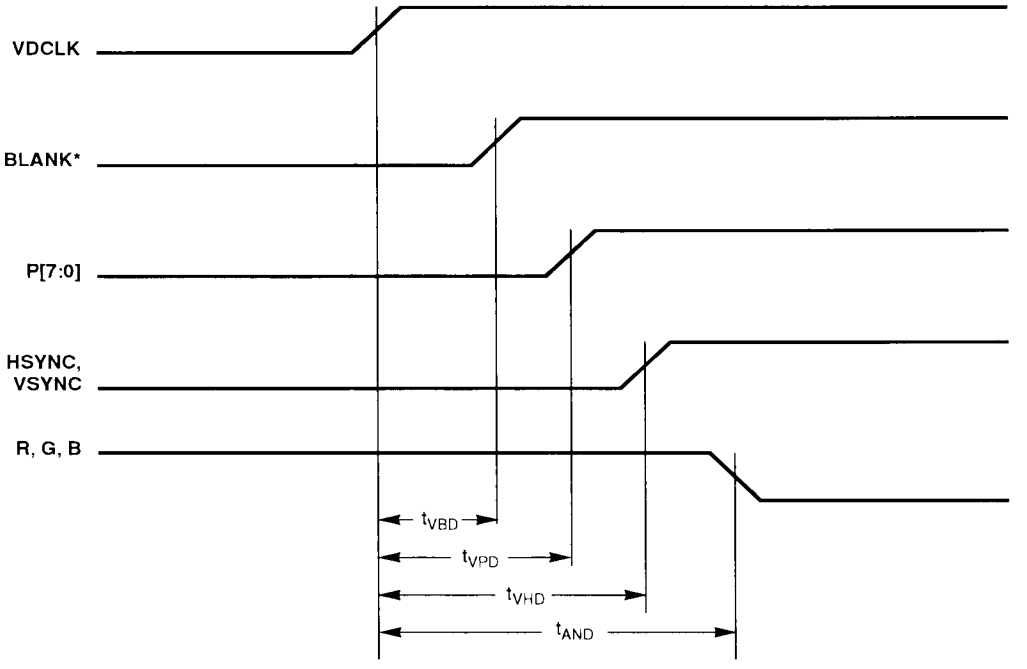


Figure 6–10. Sync, BLANK*, and R, G, B as Outputs (Internal VDCLK)

Table 6–11. Suspend Mode Timing

Symbol	Parameter	MIN	MAX	Units
t_{CSR}	CAS* setup to RAS* low	20	200	ns
t_{CHR}	CAS* hold after RAS* low	100	1000	ns
t_{CL}	CAS* low time	120	1000	ns
t_{RL}	RAS* low time	120	1000	ns
t_{REF}	Refresh period (normal)	$T_{SUSP}/2$	–	ns
t_{REF}	Refresh period (slow)	$T_{SUSP}/4$	–	ns

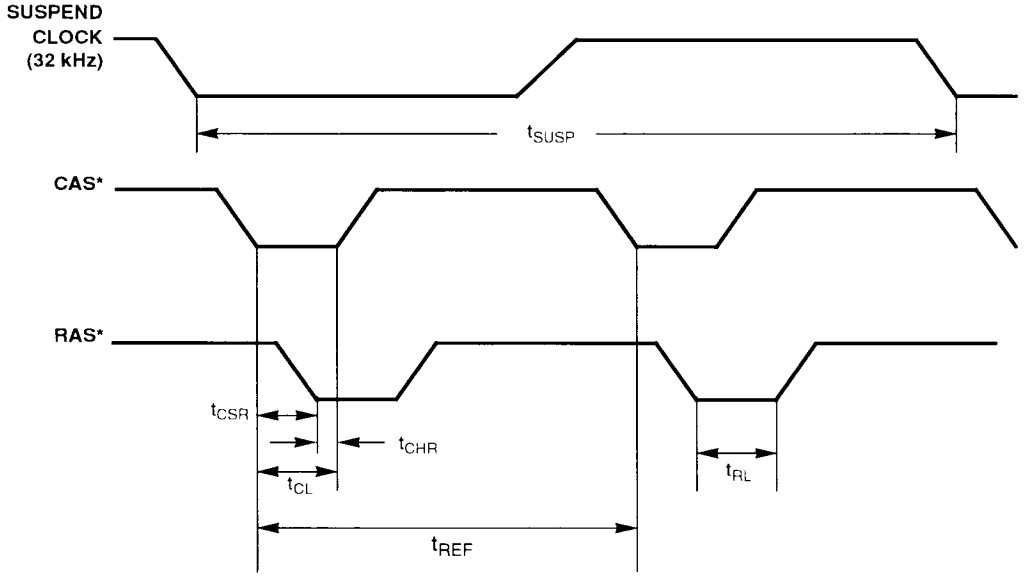


Figure 6–11. Suspend Mode Timing

Table 6–12. Programmable Pins Output Timing

Symbol	Parameter	MIN	MAX	Units
t_{DWO}	Delay from IOW* inactive to output valid	0	100	ns

NOTE: The programmable pins include PO1, FPVCC, FPVEE, and CLKSEL [3:0] in Output Mode. CLKSEL [3:0] is in Output Mode at power-on.

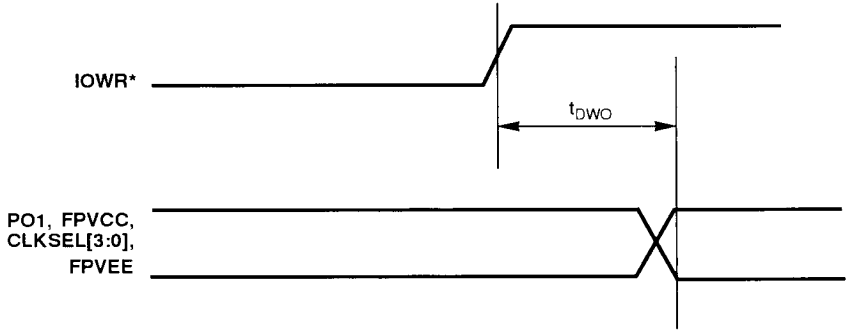


Figure 6–12. Programmable Pins Output Timing

Table 6–13. Frame-Accelerator Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{FRS}	Row address valid setup to FRRAS* active	2 T_C	–	ns
t_{FRH}	Row address hold from FRRAS* active	0.5 T_C	1000	ns
t_{FOD}	Read data delay from FROE* active	5	–	ns
t_{FCS}	Column address valid setup to FRCAS* active	0.5 T_C -5	–	ns
t_{FCH}	Column address valid hold after FRCAS* active	0.5 T_C -5	–	ns
t_{FODH}	Read data hold after FROE* inactive	2	0.5 T_C	ns
t_{FODS}	Read data setup to FROE* inactive	5	–	ns
t_{FCOS}	FRCAS* active delay to FROE* active	0.5 T_C	–	ns
t_{FOE}	FROE* active pulse width	1 T_C	–	ns
t_{FWS}	Write data setup to FRWE* active	0.5 T_C -10	–	ns
t_{FWH}	Write data hold from FRWE* inactive	0.5 T_C -5	0.5 T_C +5	ns
t_{FWA}	FRWE* active time	0.5 T_C -5	0.5 T_C +5	ns
t_{FCC}	FRCAS* cycle time	4 T_C	–	ns
t_{FCI}	FRCAS* inactive time	1 T_C -5	–	ns
t_{FCA}	FRCAS* active time	3 T_C -5	–	ns
t_{FRI}	FRRAS* inactive time	12 T_C -5	–	ns
t_{FRA}	FRRAS* active time	641 T_C -5	–	ns

NOTE: T_C = FPVDCLK period.

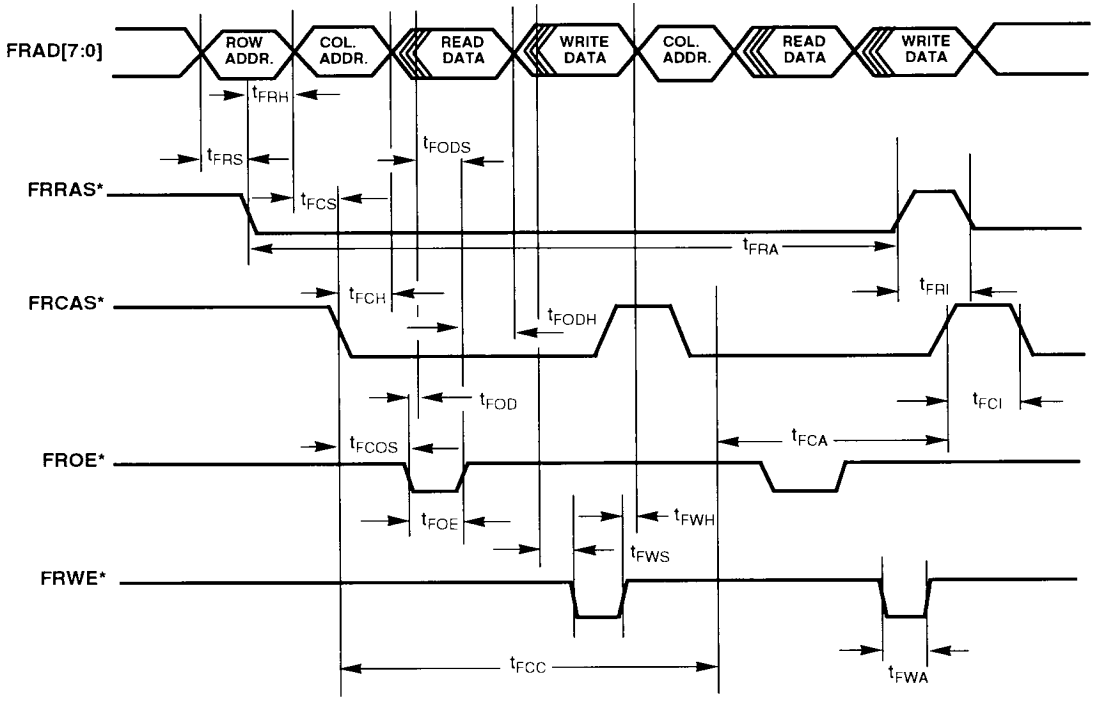


Figure 6–13. Frame-Accelerator Interface Timing

Table 6–14. STN Passive-Matrix Monochrome LCD Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{CLKPW}	FPVDCLK period	2	0.5 T_C	ns
t_{LCLKW}	LLCLK period	T_C	–	ns
t_{CLKH}	FPVDCLK high time	0.5 T_C -10	–	ns
t_{CLKL}	FPVDCLK low time	0.5 T_C -10	–	ns
t_{RF}	FPVDCLK rise and fall time	–	10	ns
t_{CLS}	FPVDCLK low to LLCLK low	T_C +20	–	ns
t_{CLH}	FPVDCLK low from LLCLK low	T_C -20	–	ns
t_{DS}	Data setup time	0.5 T_C -20	–	ns
t_{DH}	Data hold time	0.5 T_C -20	–	ns
t_{LFSH}	LFS high hold time to LLCLK low	T_C	–	ns
t_{LFSS}	LFS high setup to LLCLK low	T_C	–	ns
t_{MTD}	MOD delay from LLCLK high	–	30	ns

NOTE: T_C = 24 MHz/4.

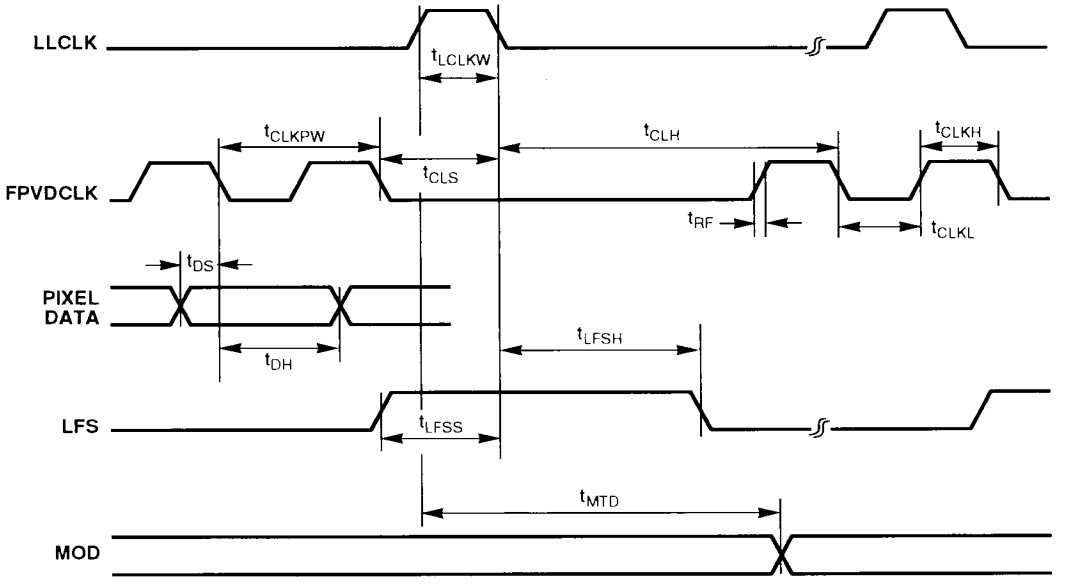


Figure 6–14. STN Passive-Matrix Monochrome LCD Interface Timing

Table 6–15. TFT Active-Matrix Color LCD Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{CLKPW}	FPVDCLK period	0.95 T_C	1.05 T_C	ns
t_{HSW}	HSYNC period	90	–	T_C
t_{CLKH}	FPVDCLK high time	0.5 T_C -5	0.5 T_C +5	ns
t_{CLKL}	FPVDCLK low time	0.5 T_C -5	0.5 T_C +5	ns
t_{RF}	FPVDCLK rise and fall time	–	10	ns
t_{DS}	Data setup time	10	–	ns
t_{DH}	Data hold time	10	–	ns
t_{HSS}	FPHSYNC stup to FPVDCLK	0.5 T_C	–	ns
t_{DES}	FPHDE setup to FPVDCLK	10	–	ns
t_{DEH}	FPHDE hold from FPVDCLK	10	–	ns
t_{VSW}	FPVSYNC period	1600	–	T_C

NOTE: T_C = FPVDCLK period.

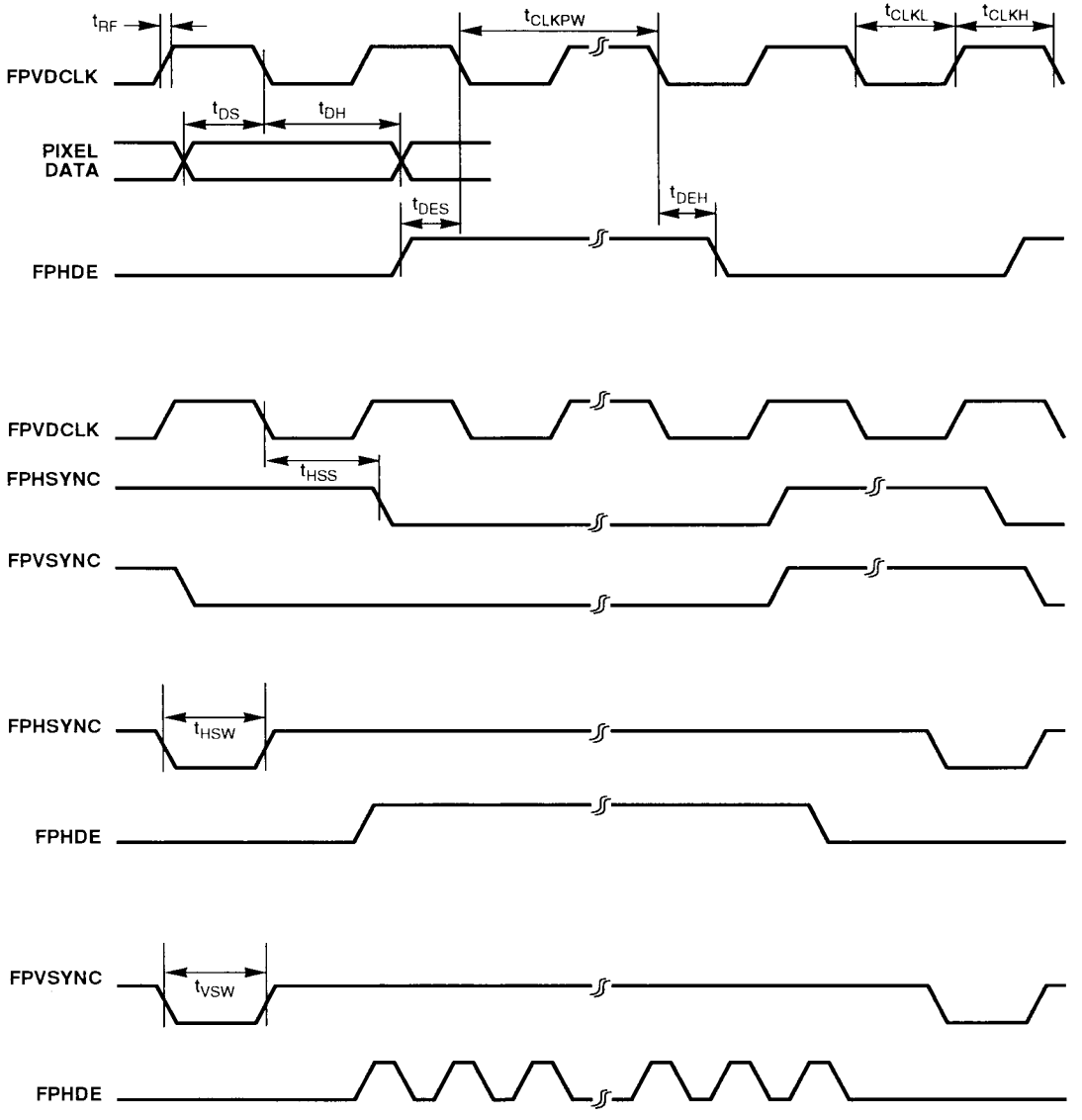


Figure 6–15. TFT Active-Matrix Color LCD Interface Timing

7. CL-GD6412 REGISTERS

The following tables list the CL-GD6412 Extension Registers.

Extension Registers

Abbreviation	Register Name	Index	Port
ER0A	Extension Control	0A	3CF
ER0B	Attribute Controller Index at Extension	0B	3CF
ER0C	CR11 Bit 7 at Extension	0C	3CF
ER0D	CPU Base Address Control	0D	3CF
ER0E	CPU Base Address Mapping Register A	0E	3CF
ER0F	CPU Base Address Mapping Register B	0F	3CF
Reserved	–	30-5F	3CF
ER60	Horizontal Total Extension	60	3CF
ER61	Horizontal Blank Start Extension	61	3CF
ER62	Horizontal Blank End Extension	62	3CF
ER63	Horizontal Retrace Start Extension	63	3CF
ER64	Horizontal Retrace End Extension	64	3CF
Reserved	–	65-6F	3CF
ER70	Vertical Total Extension	70	3CF
ER71	Vertical Display Enable Extension	71	3CF
ER72	Vertical Blank Start Extension	72	3CF
ER73	Vertical Blank End Extension	73	3CF
ER74	Vertical Retrace Start Extension	74	3CF
ER75	Vertical Retrace End Extension	75	3CF
Reserved	–	76-77	3CF
ER78	CR07 Extension	78	3CF
ER79	Vertical Overflow	79	3CF
ER7A	Coarse Vertical Retrace Skew	7A	3CF
Reserved	–	7B	3CF
ER7C	Screen A Start Address Extension	7C	3CF
Reserved	–	7D-7F	3CF
ER80	H/V Retrace Polarity Control	80	3CF
ER81	Display Mode	81	3CF
ER82	Character-Clock Selection	82	3CF
ER83	Write Control	83	3CF
ER84	Clock Select	84	3CF
Reserved	–	85	3CF
ER86	CRTC Test	86	3CF
ER87	CRTC Spare Extension	87	3CF
Unused	–	88-8E	3CF
ER8F	CRTC BIOS Configuration	8F	3CF
ER90	Display Memory Control	90	3CF
ER91	CRT-Circular Buffer Policy Selection	91	3CF
ER92	Font Control	92	3CF
ER95	CRT-Circular Buffer Delta and Burst	95	3CF
ER96	Display Memory Control Test	96	3CF

7. CL-GD6412 REGISTERS *(cont.)*

Abbreviation	Register Name	Index	Port
ER97	Monitor Switches Read-Back	97	3CF
ER98	Scratch	98	3CF
ER99	Configuration	99	3CF
ER9A	Display Memory Configuration	9A	3CF
ER9B	Miscellaneous Configuration 1	9B	3CF
ER9C	PS/2 Monitor ID	9C	3CF
ER9D	Miscellaneous Configuration 2	9D	3CF
Reserved	–	9E-9F	3CF
ERA0	Bus Interface Unit Controls	A0	3CF
ERA1	Three-State and Test Control	A1	3CF
ERA2	BIOS Page Selection	A2	3CF
Reserved	–	A3-A5	3CF
ERA6	Wait State Control	A6	3CF
ERA7	General Programmable I/O Port Controls	A7	3CF
Reserved	–	A8	3CF
ERA9	Bus Interface Unit Cache Controls	A9	3CF
ERAA	Design Revision	AA	3CF
ERAB	Mask Revision	AB	3CF
ERAE	Alternate Extension Decode High	AE	3CF
ERAF	Alternate Extension Decode Low	AF	3CF
Reserved	–	AC-B9	3CF
ERBA-BF	Scratch Register 5-0	BA-BF	3CF
ERC0	Attribute and Graphics Control	C0	3CF
ERC1	Cursor Attributes	C1	3CF
ERC2-C5	Graphics Controller Memory Latches 0-3	C2-C5	3CF
Reserved	–	C6-C7	3CF
ERC8	RAMDAC Controls	C8	3CF
ERC9	Graphics and Attribute Test	C9	3CF
Reserved	–	CA-CF	3CF
ERD0	Flat Panel Column Offset	D0	3CF
ERD1	Flat Panel Horizontal Size	D1	3CF
ERD2	Flat Panel Row Offset	D2	3CF
ERD3	Flat Panel Vertical Size	D3	3CF
ERD4	Flat Panel Overflow	D4	3CF
ERD5	Flat Panel Attribute Control	D5	3CF
ERD6	Flat Panel Grayscale Offset	D6	3CF
ERD7	Flat Panel Retrace Line Clock Control	D7	3CF
ERD8	Flat Panel Frame Color	D8	3CF
ERD9	Flat Panel AC Modulation	D9	3CF
ERDA	Flat Panel Display Control	DA	3CF
ERDB	Standby Timer Control	DB	3CF
ERDC	Flat Panel Color Configuration	DC	3CF
Reserved	–	DD-DF	3CF

7.1 VGA Register Port Map

Table 7–1. VGA Register Port Map

Address	Port
3?4	CRT Controller Index (R/W)
3?5	CRT Controller Data (R/W)
3BA	Feature Control (W), Input Status Register 1 (R) (Monochrome)
3C0	Attribute Controller Index/Data (Write)
3C1	Attribute Controller Index/Data (Read)
3C2	Miscellaneous Output (W), Input Status Register 0 (R)
3C3	VGA Enable (R/W)
3C4	Sequencer Index (R/W)
3C5	Sequencer Data (R/W)
3C6	Video DAC Pixel Mask (R/W), Hidden DAC Register (R/W)
3C7	Pixel Address Read Mode (W), DAC State (R)
3C8	Pixel Mask Write Mode (R/W)
3C9	Pixel Data (R/W)
3CA	Feature Control Readback (R)
3CC	Miscellaneous Output Readback (R)
3CE	Graphics Controller Index (R/W)
3CF	Graphics Controller Data (R/W)
3DA	Feature Control (W), Input Status Register 1 (R) (Color)

NOTE: The '?' in an address would be 'B' for monochrome and 'D' for color.

7.2 CL-GD6412 Extended Register Details

7.2.1 Extension Control Register: ER0A

I/O Port Address: 3CF

Index: 0A

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Extensions Register Access Flag	R/W	0

This register is used to enable or disable access to the Extension Registers.

To enable access to the Extension Registers, write the value EC to this register. A subsequent read from this register will return the value '01', indicating access to the Extension Registers.

To disable access to the Extension Registers, write the value CE to this register. A subsequent read from this register will return the value '00', indicating no access to the Extension Registers.

Bit	Description
Bits 7:1	Reserved
Bit 0	**Extensions Register Access Flag:** A '1' indicates access is allowed to the Extension Registers.

7.2.2 Attribute Controller Index At Extension Register: ER0B

I/O Port Address: 3CF

Index: 0B

Bit	Description	Access	Reset State
7(MSB)	Index/Data State of Attribute Controller	R/W	0
6	Reserved		0
5	Video Enable	R/W	0
4	Attribute Controller Index [4]	R/W	x
3	Attribute Controller Index [3]	R/W	x
2	Attribute Controller Index [2]	R/W	x
1	Attribute Controller Index [1]	R/W	x
0(LSB)	Attribute Controller Index [0]	R/W	x

This register duplicates the Attribute Controller Index Register (3C0) Bits 5-0. In addition, Bit 7 enables the program to unconditionally determine or force the state of the Index/Data Pointer.

Bit	Description
Bit 7	**Index/Data State of Attribute Controller:** This bit reflects and controls the state of the Index/Data Pointer in the Attribute Controller. When the register is read, the state is returned; when the register is written, the state is forced. 0 = Index 1 = Data
Bit 6	Reserved
Bit 5	**Video Enable:** When this bit is reset to a '0', the screen displays the color indicated by Overscan Register AR11 (normally black); when set to a '1', normal video display is enabled. In the standard VGA, this bit also selects the address source for the Palette Registers (0 = CPU and 1 = Video), which requires that CPU writes to the Palette Registers only occur when this bit is a '0' (or else the data will be written to random Palette Register locations as determined by the Video Data Stream at the time of the write). In the CL-GD64XX, the palette is dual-ported and may be accessed at any time, independent of the state of this bit.
Bits 4:0	**Attribute Controller Index Bits:** These five bits form the index to the Data Registers in the Attribute Controller.

7.2.3 CR11 Bit 7 at Extension Register: ER0C

I/O Port Address: 3CF

Index: 0C

Bit	Description	Access	Reset State
7(MSB)	Write Protect CR00-CR07	R/W	0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This register is used to break a deadlock between CR3 and CR11.

Bit	Description
Bit 7	**Write Protect CR00-CR07:** This bit provides write protection for Registers CR00-CR07 (mostly the Horizontal Control Registers). The functionality of this bit is the same as Bit 7 of CR11h. This bit resolves the deadlock issue described in the next paragraph. If CR3[7] is reset to a '0', then CR11 no longer controls write protect for CR0-CR7. If CR11[7] is set to a '1', then CR3[7] is write protected. Since CR3[7] is write-protected, CR10 and CR11 cannot be accessed as Vertical Retrace Control Registers and, in particular, CR11[7] cannot be programmed to change the write-protected state of CR3[7]. ER0C[7] is always accessible and breaks the deadlock.
Bits 6:0	Reserved

7.2.4 CPU Base Address Control Register: ER0D

I/O Port Address: 3CF

Index: 0D

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved	R/W	0
3	Enable Alternate Extension	R/W	0
2	2/1 Page Selection	R/W	0
1	64K/32K Page Size	R/W	0
0(LSB)	Enable Page Remapping	R/W	0

This register is write protected by ERA7[4] = 1.

This register is used to control the mapping of host memory access into the Display Memory. The host has at most a 128K window (A0000h through BFFFFh) to access up to 1024K bytes of the Display Memory. This register, in conjunction with the ER0E and ER0F Registers, provides the necessary remapping.

The remapping is done using an 8-bit adder. It adds the low-order 15 or 16 bits of host address with the 8 bits taken from either ER0E or ER0F. Whether 15 or 16 bits are used depends on the page size. Whether ER0E or ER0F is chosen depends on the page size and number of pages.

Bit 0 of the Remapping Register is aligned with Bit 12 of the CPU Address. This means that the low-order 12 bits of the Display Memory Address are determined strictly by the CPU Address. The high-order eight bits of the Display Memory Address are the arithmetic sum of Bits 15:12 or 14:12 of the CPU Address and Bits 7:0 of the Remapping Register. Bits 23:16 of the CPU Address are ignored by the adder. Overflow is possible and is not detected.

Bit alignment is shown in the following table:

Table 7–2. Adder Alignment

CPU Bit					15	14	13	12
Register Bit	7	6	5	4	3	2	1	0

This scheme provides a 64K block beginning on any 4K boundary accessible through each of the Remapping Registers.

7.2.4 CPU Base Address Control Register: ER0D *(cont.)*

Bit	Description
Bits 7:4	Reserved
Bit 3	**Enable Alternate Extension Decode:** This bit enables an alternate extension address decode option of the CL-GD6412. If this bit is set to a '1', the extension decode is as defined by ERAE and ERAF. If this bit is set to a '0', the default extension decode is 03CE/03CF.
Bit 2	**2/1 Page Selection:** If Bit 2 is reset to a '0', remapping is possible only through ER0E. If Bit 2 is set to a '1', remapping is possible through both ER0E and ER0F.
Bit 1	**64K/32K Page Size:** If Bit 1 is reset to a '0', remapping is done for 32K pages. If Bit 1 is set to a '1', remapping is done for 64K pages. The following table summarizes the remapping according to the CPU Address.
Bit 0	**Enable Page Remapping:** If this bit is reset to a '0', the address is passed through the Remapping Logic with no modification.

Table 7–3. Remapping Register Selection

Bit 2	Bit 1	A000-A7FFF	A8000-AFFFF	B0000-B7FFF	B8000-BFFFF
0	0	ER0E	*[a]	*	*
0	1	ER0E	ER0E	*	*
1	0	ER0E	ER0F	*	*
1	1	ER0E	ER0E	ER0F	ER0F[b]

a. (*) indicates the address is not modified in the Remapping Logic.
b. To use two pages of 64K each, program GR6[3:2] to 0:0; 128K of Display Memory is selected.

7.2.5 CPU Base Address Mapping Register A: ER0E

I/O Port Address: 3CF

Index: 0E

Bit	Description	Access	Reset State
7(MSB)	Address Offset Bit [19]	R/W	0
6	Address Offset Bit [18]	R/W	0
5	Address Offset Bit [17]	R/W	0
4	Address Offset Bit [16]	R/W	0
3	Address Offset Bit [15]	R/W	0
2	Address Offset Bit [14]	R/W	0
1	Address Offset Bit [13]	R/W	0
0(LSB)	Address Offset Bit [12]	R/W	0

If necessary, the contents of this register are added to the upper bits A[19:12] of the CPU Address prior to accessing the Display Memory. The circumstances under which this addition occurs are explained in the description of ER0D above.

Bit	Description
Bits 7:0	**Address Offset Bits:** This is the 8-bit value added to the upper bits of the CPU Address.

7.2.6 CPU Base Address Mapping Register B: ER0F

I/O Port Address: 3CF

Index: 0F

Bit	Description	Access	Reset State
7(MSB)	Address Offset Bit [19]	R/W	0
6	Address Offset Bit [18]	R/W	0
5	Address Offset Bit [17]	R/W	0
4	Address Offset Bit [16]	R/W	0
3	Address Offset Bit [15]	R/W	0
2	Address Offset Bit [14]	R/W	0
1	Address Offset Bit [13]	R/W	0
0(LSB)	Address Offset Bit [12]	R/W	0

If necessary, the contents of this register are added to the upper bits A[19:12] of the CPU Address prior to accessing the Display Memory. The circumstances under which this addition occurs are explained in the description of ER0D above.

Bit	Description
Bits 7:0	**Address Offset Bits:** This is the 8-bit value added to the upper bits of the CPU Address.

7.2.7 Horizontal Total Extension Register: ER60

I/O Port Address: 3CF

Index: 60

Bit	Description	Access	Reset State
7(MSB)	Horizontal Total Extension [7]	R/W	0
6	Horizontal Total Extension [6]	R/W	0
5	Horizontal Total Extension [5]	R/W	0
4	Horizontal Total Extension [4]	R/W	0
3	Horizontal Total Extension [3]	R/W	0
2	Horizontal Total Extension [2]	R/W	0
1	Horizontal Total Extension [1]	R/W	0
0(LSB)	Horizontal Total Extension [0]	R/W	0

The Registers ER60 to ER64 are grouped as the working set of CRTC horizontal display timing; they always control the CRTC to drive horizontal monitor timing. These registers are the counterpart of the CRTC Standard Registers mapped into Extension Address Spaces and are totally transparent to standard VGA applications.

The data sources are controlled by ER83h[1] when the working set is being updated.

ER83h[1] = 0:

The data will be written to both corresponding standard registers in CRTC and the registers in this working set through standard address path, 3X4h (X = D or B).

ER83h[1] = 1:

The working set registers can only be written from the extension address path. The corresponding standard registers in CRTC will not be changed.

Bit	Description
Bits 7:0	**Horizontal Total Extension Bits 7:0:** The value in this register is the least-significant eight bits of a 9-bit field specifying the total number of horizontal character-clocks: the most-significant bit is in ER64[5]. This value includes the number of characters in the active-display area and the number of characters required for the horizontal blanking period. The actual value programmed is the total number of characters in a horizontal display period minus 5. The total number of characters in a horizontal display period is calculated from dotclock, horizontal frequency, and font width. For example: Dotclock = 28.322 MHz, Horizontal Frequency = 32.5 kHz, Font Width = 9 Dots. 28322/31.5 = 900 dots per horizontal cycle (approximately). 900/9 = 100 characters per horizontal cycle. 100 - 5 = 95 (5Fh) to be programmed into this register. In standard VGA, horizontal total has an 8-bit value. In the CL-GD64XX family, the horizontal total is extended to up to 512 character-clocks.

7.2.8 Horizontal Blank Start Extension Register: ER61

I/O Port Address: 3CF

Index: 61

Bit	Description	Access	Reset State
7(MSB)	Horizontal Blank Start Extension Bit [7]	R/W	0
6	Horizontal Blank Start Extension Bit [6]	R/W	0
5	Horizontal Blank Start Extension Bit [5]	R/W	0
4	Horizontal Blank Start Extension Bit [4]	R/W	0
3	Horizontal Blank Start Extension Bit [3]	R/W	0
2	Horizontal Blank Start Extension Bit [2]	R/W	0
1	Horizontal Blank Start Extension Bit [1]	R/W	0
0(LSB)	Horizontal Blank Start Extension Bit [0]	R/W	0

Bit	Description
Bits 7:0	**Horizontal Blank Start Extension Bits 7:0:** The value in this register is the least-significant eight bits of a 9-bit field specifying the start of horizontal blanking. The most-significant bit is ER62[7]. This bit is used to indicate in character-clock units when the Horizontal Blanking Signal becomes active. When the internal character counter reaches the value programmed into this register, blanking starts. If the Blanking Signal is activated too early, some of the display will be lost. If the Blanking Signal is activated after horizontal display enable ends, the timing gap between horizontal display enable end and horizontal blanking start becomes the border. This register is also extended to nine bits instead of the eight bits available to standard VGA.

7.2.9 Horizontal Blank End Extension Register: ER62

I/O Port Address: 3CF

Index: 62

Bit	Description	Access	Reset State
7(MSB)	Horizontal Blank Start Extension [8]	R/W	0
6	Reserved		0
5	Reserved		0
4	Horizontal Blank End [4]	R/W	0
3	Horizontal Blank End [3]	R/W	0
2	Horizontal Blank End [2]	R/W	0
1	Horizontal Blank End [1]	R/W	0
0(LSB)	Horizontal Blank End [0]	R/W	0

Bit	Description
Bit 7	**Horizontal Blank Start Extension Bit 8:** This is Bit 8 of the Horizontal Blank Start Field. It serves to extend ER61, making a 9-bit field.
Bits 6:5	Reserved
Bits 4:0	**Horizontal Blank End Bits:** These bits are used to indicate in character-clocks when the Horizontal Blanking Signal becomes inactive. The value is six bits, with the most-significant bit in ER64[7]. The least-significant bits from the following formula determine the value programmed into this register: Horizontal Blank Start (ER61 and ER62[7]) + Horizontal Blanking Width. The 6-bit value of horizontal blank end limits the length of the horizontal blanking pulse to 63 character-clocks in VGA. The Blanking Signal should go inactive at least one character-clock before the next Horizontal Display Signal enable. The timing gap between Blanking Signal inactive and Horizontal Display Signal active is perceived as the left border. For example, Horizontal Total Number of Characters = 100 (64h). The horizontal blanking end should be at Location 98 (62h).

7.2.10 Horizontal Retrace Start Extension Register: ER63

I/O Port Address: 3CF

Index: 63

Bit	Description	Access	Reset State
7(MSB)	Horizontal Retrace Start [7]	R/W	0
6	Horizontal Retrace Start [6]	R/W	0
5	Horizontal Retrace Start [5]	R/W	0
4	Horizontal Retrace Start [4]	R/W	0
3	Horizontal Retrace Start [3]	R/W	0
2	Horizontal Retrace Start [2]	R/W	0
1	Horizontal Retrace Start [1]	R/W	0
0(LSB)	Horizontal Retrace Start [0]	R/W	0

Bit	Description
Bits 7:0	**Horizontal Retrace Start Bits 7:0:** This entire byte is the lower eight bits of the 9-bit location value of Horizontal Retrace Start. The most-significant bit is at ER64[6]. These eight bits are used to indicate the point that the Horizontal Synchronization Pulse becomes active. The value in the register affects the centering of the screen horizontally.

7.2.11 Horizontal Retrace End Extension Register: ER64

I/O Port Address: 3CF

Index: 64

Bit	Description	Access	Reset State
7(MSB)	Horizontal Blank End [5] R/W	0	
6	Horizontal Retrace Start [8]	R/W	0
5	Horizontal Total Extension [8]	R/W	0
4	Horizontal Retrace End [4]	R/W	0
3	Horizontal Retrace End [3]	R/W	0
2	Horizontal Retrace End [2]	R/W	0
1	Horizontal Retrace End [1]	R/W	0
0(LSB)	Horizontal Retrace End [0]	R/W	0

This register contains extension bits for the horizontal parameters of the CRTC.

Bit	Description
Bit 7	**Horizontal Blank End Bit 5:** This bit is the most-significant bit of the Horizontal Blank End 6-bit Field (refer to ER62).
Bit 6	**Horizontal Retrace Start Extension Bit 8:** This is Bit 9 of the Horizontal Retrace Start Field. It serves to extend CR4, making a 9-bit field (refer to ER63).
Bit 5	**Horizontal Total Extension Bit 8:** This is Bit 8 of the Horizontal Total Extension Field. It serves to extend CR0, making a 9-bit field (refer to ER60).
Bits 4:0	**Horizontal Retrace End Bits:** These are the five bits specifying the value for the character-clock count when the Horizontal Retrace Signal becomes inactive. The least-significant five bits from the following formula determine the value programmed into this register: Horizontal Retrace Start (ER63 + ER64[6]) + Horizontal Synchronization Width. This 5-bit value limits the length of the Retrace Signal to 32 character-clocks. The Horizontal Retrace Signal should always end before the Horizontal Blanking Signal.

7.2.12 Vertical Total Extension Register: ER70

I/O Port Address: 3CF

Index: 70

Bit	Description	Access	Reset State
7(MSB)	Vertical Total Extension [7]	R/W	0
6	Vertical Total Extension [6]	R/W	0
5	Vertical Total Extension [5]	R/W	0
4	Vertical Total Extension [4]	R/W	0
3	Vertical Total Extension [3]	R/W	0
2	Vertical Total Extension [2]	R/W	0
1	Vertical Total Extension [1]	R/W	0
0(LSB)	Vertical Total Extension [0]	R/W	0

The Registers ER70 through ER75, ER78, and ER79 are grouped as a working set for vertical display timing; they are the correspondents of standard registers in the CRTC, mapped into extension address space. This working set always controls the CRTC and is actually driving vertical display timing. The values in the registers of the working set are protected by ER83[0]. When these control registers are set, data is read and written to the standard registers without affecting these working set registers. In this case, the only way to affect the values in the working set registers is through the extension address. When the control registers are cleared, the working set registers will be affected by changes made to the standard registers through the standard address path. The registers in this working set can be read or written to through the extension address path at any time, but the standard registers will not be affected.

Bit	Description
Bits 7:0	**Vertical Total Bits 7:0:** These are the least-significant eight bits of the 11-bit value that specifies the total number of vertical scanlines in one frame. Bits 8 and 9 are at ER78[0,5]; Bit 10 is at ER79[2,3]. The 11-bit value for vertical total scanlines is calculated by subtracting 2 from the actual total number of scanlines in one vertical frame. The functionality of this register is the same as CR06 in the CRTC. The 11-bit value of vertical total scanlines extends the maximum scanline capability to 2048 lines.

7.2.13 Vertical Display Enable Extension Register: ER71

I/O Port Address: 3CF

Index: 71

Bit	Description	Access	Reset State
7(MSB)	Vertical Display Enable End [7]	R/W	0
6	Vertical Display Enable End [6]	R/W	0
5	Vertical Display Enable End [5]	R/W	0
4	Vertical Display Enable End [4]	R/W	0
3	Vertical Display Enable End [3]	R/W	0
2	Vertical Display Enable End [2]	R/W	0
1	Vertical Display Enable End [1]	R/W	0
0(LSB)	Vertical Display Enable End [0]	R/W	0

Bit	Description
Bits 7:0	**Vertical Display Enable End Bits 7:0:** These are the lower eight bits of the 11-bit vertical display value that are used to specify the total number of displayable scan-lines in one vertical frame. Bits 8 and 9 are at ER78[6,1]. The most-significant bit, Bit 10, is at ER79[1].

7.2.14 Vertical Blank Start Extension Register: ER72

I/O Port Address: 3CF

Index: 72

Bit	Description		Access	Reset State
7(MSB)	Vertical Blank Start [7]	R/W	0	
6	Vertical Blank Start [6]		R/W	0
5	Vertical Blank Start [5]		R/W	0
4	Vertical Blank Start [4]		R/W	0
3	Vertical Blank Start [3]		R/W	0
2	Vertical Blank Start [2]		R/W	0
1	Vertical Blank Start [1]		R/W	0
0(LSB)	Vertical Blank Start [0]		R/W	0

Bit	Description
Bits 7:0	**Vertical Blank Start Bits 7:0:** These are the lower eight bits of an 11-bit value that specifies when the Vertical Blanking Signal becomes active. Bit 8 is at ER78[3]; Bits 9 and 10 are at ER79[2,3].

7.2.15 Vertical Blank End Extension Register: ER73

I/O Port Address: 3CF

Index: 73

Bit	Description	Access	Reset State
7(MSB)	Vertical Blank End [7]	R/W	0
6	Vertical Blank End [6]	R/W	0
5	Vertical Blank End [5]	R/W	0
4	Vertical Blank End [4]	R/W	0
3	Vertical Blank End [3]	R/W	0
2	Vertical Blank End [2]	R/W	0
1	Vertical Blank End [1]	R/W	0
0(LSB)	Vertical Blank End [0]	R/W	0

Bit	Description
Bits 7:0	**Vertical Blank End Bits 7:0:** These eight bits specify when the Vertical Blanking Signal becomes inactive. The internal Character-clock Counter is compared with this register. As soon as there is a match, the Blanking Signal is terminated. The value in this register is calculated as follows: Vertical Blanking Start (ER72, ER78[3], and ER79[2,3]) + Vertical Blanking Width.

7.2.16 Vertical Retrace Start Extension Register: ER74

I/O Port Address: 3CF

Index: 74

Bit	Description	Access	Reset State
7(MSB)	Vertical Retrace Start [7]	R/W	0
6	Vertical Retrace Start [6]	R/W	0
5	Vertical Retrace Start [5]	R/W	0
4	Vertical Retrace Start [4]	R/W	0
3	Vertical Retrace Start [3]	R/W	0
2	Vertical Retrace Start [2]	R/W	0
1	Vertical Retrace Start [1]	R/W	0
0(LSB)	Vertical Retrace Start [0]	R/W	0

Bit	Description
Bits 7:0	**Vertical Retrace Start Bits 7:0:** These bits specify when the Vertical Synchronization Signal becomes active. These bits represent the lower eight bits of an 11-bit value. Bits 8 and 9 are in ER78[2,7]; Bit 10 is in ER79[4]. The polarity of the Vertical Synchronization Signal is controlled by Bit 7 of the MISC Output Register.

7.2.17 Vertical Retrace End Extension Register: ER75

I/O Port Address: 3CF

Index: 75

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Vertical Retrace End [3]	R/W	0
2	Vertical Retrace End [2]	R/W	0
1	Vertical Retrace End [1]	R/W	0
0(LSB)	Vertical Retrace End [0]	R/W	0

Bit	Description
Bits 7:4	Reserved
Bits 3:0	**Vertical Retrace End Bits:** These four bits specify when the Vertical Synchronization Signal becomes inactive. The value programmed into this register is calculated by taking the least-significant four bits of the following: Vertical Retrace Start + Vertical Synchronization Width = Vertical Retrace End. The 4-bit value in this register allows the Vertical Synchronization Signal width to be up to 16 scanlines wide. The Vertical Synchronization Signal should be inactive before the Vertical Blanking Signal goes inactive.

7.2.18 CR07 Extension Register: ER78

I/O Port Address: 3CF

Index: 78

Bit	Description	Access	Reset State
7(MSB)	Vertical Retrace Start [9]	R/W	0
6	Vertical Display Enable End [9]	R/W	0
5	Vertical Total [9]	R/W	0
4	Line Compare [8]	R/W	0
3	Vertical Blank Start [8]	R/W	0
2	Vertical Retrace Start [8]	R/W	0
1	Vertical Display Enable End [8]	R/W	0
0(LSB)	Vertical Total [8]	R/W	0

Bit	Description
Bit 7	**Vertical Retrace Start Bit 9:** Refer to the Vertical Retrace Start Field, ER74.
Bit 6	**Vertical Display Enable End Bit 9:** Refer to the Vertical Display Enable End Field, ER71.
Bit 5	**Vertical Total Bit 9:** Refer to the Vertical Total Field, ER70.
Bit 4	**Line Compare Bit 8:** Refer to the Line Compare Field, CR18. This bit is always identical with CR07[4].
Bit 3	**Vertical Blanking Start Bit 8:** Refer to the Vertical Blanking Start Field, ER72.
Bit 2	**Vertical Retrace Start Bit 8:** Refer to the Vertical Retrace Start Field, ER74.
Bit 1	**Vertical Display Enable End Bit 8:** Refer to the Vertical Display Enable End Field, ER71.
Bit 0	**Vertical Total Bit 8:** Refer to the Vertical Total Field, ER70.

7.2.19 Vertical Overflow Register: ER79

I/O Port Address: 3CF

Index: 79

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Vertical Retrace Start [10]	R/W	0
3	Vertical Blank Start [10]	R/W	0
2	Vertical Blanking Start [9]	R/W	0
1	Vertical Display Enable End [10]	R/W	0
0(LSB)	Vertical Total [10]	R/W	0

This register contains five overflow bits for the vertical parameters of the CRTC.

Bit	Description
Bits 7:5	Reserved
Bit 4	**Vertical Retrace Start Bit 10:** Refer to the Vertical Retrace Start Field, ER74.
Bit 3	**Vertical Blank Start Bit 10:** Refer to the Vertical Blank Start Field, ER72.
Bit 2	**Vertical Blanking Start Bit 9:** Refer to the Vertical Blank Start Field, ER72.
Bit 1	**Vertical Display Enable End Bit 10:** Refer to the Vertical Display End Field, ER71.
Bit 0	**Vertical Total Bit 10:** Refer to the Vertical Total Field, ER70.

7.2.20 Coarse Vertical Retrace Skew Register (for Interlaced Modes): ER7A

I/O Port Address: 3CF

Index: 7A

Bit	Description	Access	Reset State
7(MSB)	CLKC Skew [7]	R/W	0
6	CLKC Skew [6]	R/W	0
5	CLKC Skew [5]	R/W	0
4	CLKC Skew [4]	R/W	0
3	CLKC Skew [3]	R/W	0
2	CLKC Skew [2]	R/W	0
1	CLKC Skew [1]	R/W	0
0(LSB)	CLKC Skew [0]	R/W	0

This register specifies the skew for the Odd Fields when interlaced video is being generated. In interlaced video, the scanlines of the Odd Field must be positioned (vertically) halfway between the corresponding scanlines of the Even Field. This register introduces up to 255 character-clock-periods of skew.

Bit	Description
Bits 7:0	**Vertical Retrace Skew Bits 7:0:** These eight bits specify the coarse skew in terms of character-clock periods.

7.2.21 Screen A Start Address Extension Register: ER7C

I/O Port Address: 3CF

Index: 7C

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Screen A Start [19]	R/W	0
2	Screen A Start [18]	R/W	0
1	Screen A Start [17]	R/W	0
0(LSB)	Screen A Start [16]	R/W	0

This register provides the four most-significant bits of the Screen A Start Address. The low-order 16 bits are contained in CRC and CRD in the CRT Controller Group.

Bit	Description
Bits 7:4	Reserved
Bits 3:0	**Screen A Start Bits 19:16:** These four bits are the four high-order bits of the 20-bit Screen A Start Address.

7.2.22 H/V Retrace Polarity Control Register: ER80

I/O Port Address: 3CF

Index: 80

Bit	Description	Access	Reset State
7(MSB)	Vertical Retrace Polarity	R/W	0
6	Horizontal Retrace Polarity	R/W	0
5	Source of Polarity Control	R/W	0
4	Enable Expanded Graphics	R/W	0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This register contains polarity control bits for the CRTC.

Bit	Description
Bit 7	**Vertical Retrace Polarity:** This is a control bit for Vertical Retrace Polarity in the extension address space. If this bit is set to a '1', then polarity is negative (active-low). If this bit is set to a '0', the polarity is positive (active-high).
Bit 6	**Horizontal Retrace Polarity:** This is a control bit for Horizontal Retrace Polarity in the extension address space. If this bit is set to a '1', then polarity is negative (active-low). If this bit is set to a '0', the polarity is positive (active-high).
Bit 5	**Source of Polarity Control:** This bit sets the source of polarity control for both Vertical and Horizontal Synchronization. If this bit is set to a '1', then the source of control is from ER80[7,6]. If this bit is a '0', the source of control is from MISC[7,6].
Bit 4	**Enable Expanded Graphics:** This bit enables display expansion in Graphics Modes. When this bit is set to a '1', a predetermined ratio (16 to 19) of scanlines will be replicated in Graphics Mode. This bit can be programmed at any time.
Bits 3:0	Reserved

7.2.23 Display Mode Register: ER81

I/O Port Address: 3CF

Index: 81

Bit	Description	Access	Reset State
7(MSB)	SimulSCAN	R/W	0
6	Reserved		
5	AutoMap Enable	R/W	0
4	LCD Flat Panel Scan Control	R/W	0
3	CL-GD6340 Mode Enable	R/W	0
2	Reserved		
1	Reserved		
0(LSB)	Display Type	R/W	0

This register is used for specific display mode control.

Bit	Description
Bits 7	**SimulSCAN:** This bit determines if display information is being generated for the LCD only or for the LCD and CRT at the same time (SimulSCAN). A '1' indicates that the display mode is SimulSCAN; a '0' indicates LCD only.
Bit 6	Reserved
Bit 5	**AutoMap Enable:** This bit enables automatic mapping of color information to shades of gray. If it is set to a '1', AutoMap is enabled. If it is set to a '0', then automatic gray scaling does not occur.
Bit 4	**LCD Flat Panel Scan Control:** This bit determines support for single-scan or dual-scan LCD flat panels. If it is set to a '1', then single-scan flat panels are supported and internal half-frame buffer logic is disabled. If it is set to a '0', then support is set for dual-scan LCD flat panels.
Bit 3	**CL-GD6340 Mode Enable:** This bit affects the definition of Pin 98. If it is set to a '1', then the function of Pin 98 becomes DE (Display Enable for the CL-GD6340). If it is a '0', then Pin 98 becomes LLCLK.
Bits 2:1	Reserved
Bit 0	**Display Type:** This bit sets the active display type. If it is set to a '1', then the LCD flat panel is the active display. If it is set to a '0', then the CRT is active.

7.2.24 Character-Clock Selection Register: ER82

I/O Port Address: 3CF

Index: 82

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Disable SR1 Bit 0	R/W	0	
2	Character Clock Width Select [2]	R/W	0	
1	Character Clock Width Select [1]	R/W	0	
0(LSB)	Character Clock Width Select [0]	R/W	0	

This register is used to select the number of dotclocks in each character-clock.

Bit	Description
Bits 7:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Disable SR1 Bit 0 Functionality:** If this bit is set to a '1', the character-clock width is determined by Bits 2:0 of this register. If this bit is reset to a '0', the character-clock width, Bit 0, is determined by SR1 Bit 0.
Bits 2:0	**Character-Clock Width Select Bits 2:0:** These three bits choose the number of dotclocks per character as indicated in the following table. The three bits are shown as a decimal number where Bit 2 is the MSB.

Table 7–4. Dotclock/Character-Clock

Value	Dotclocks per Character-Clock
0	9 Dots
1	8 Dots
2	4 Dots
3	Reserved
4	11 Dots
5	Reserved
6	Reserved
7	Reserved

7.2.25 Write Control Register: ER83

I/O Port Address: 3CF

Index: 83

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Attribute Registers Write Protect	R/W	0
5	Reserved		0
4	CRTC Total/Retrace Effect Protect	R/W	0
3	CRTC Blank Effect Protect	R/W	0
2	CRTC Vertical Display End Effect Protect	R/W	0
1	CRTC Display Timing Effect Protect	R/W	0
0(LSB)	CRTC Vertical Parameters Write Protect	R/W	0

This register is used to provide write protection for the Horizontal and Vertical Working Sets.

Bit	Description
Bit 7	Reserved
Bit 6	**Attribute Registers Write Protect:** This bit provides hardware-level write protection of the internal attribute controller palette-registers, AR00-AR0F, preventing them from being changed by application programs. If this bit is set to a '1', protection is in effect. If the bit is set to a '0', protection is disabled.
Bit 5	Reserved
Bit 4	**CRTC Total/Retrace Effect Protect:** When this bit is set to a '1', the CRTC is controlled by the CRTC Extension Registers, which now become the Working Set. In effect, this protects the standard VGA CRTC Registers CR00, CR04, CR05[4:0], CR06, CR07[7,5,2,0], CR10, and CR11. These registers become read-only. Writing to them does not affect the CRTC. When this bit is a '0', the standard CRTC Registers have control. Data written to the standard address path, 3x4h, will also be written to the Working Set.
Bit 3	**CRTC Blank Effect Protect:** This bit operates the same as Bit 4 except the registers affected are CR02, CR03[4:0], CR05[7], CR07[3], CR9[5], CR15, and CR16.
Bit 2	**CRTC Vertical Display End Effect Protect:** This bit operates the same as Bits 4 and 3 except the registers affected are CR12 and CR07[6,1].
Bit 1	**CRTC Display Timing Effect Protect:** This bit operates the same as Bits 4, 3, and 2 except the registers affected are CR07[6,1], CR09, CR0A, CR0B, CR12, and CR14.
Bit 0	**CRTC Vertical Parameters Write Protect:** This bit operates the same as Bits 4, 3, 2, and 1 except the registers affected are CR06, CR07[7,5,3,2,0], CR09[5], CR10, CR11[3:0], CR15, and CR16.

7.2.26 Clock Select Register: ER84

I/O Port Address: 3CF

Index: 84

Bit	Description	Access	Reset State
7(MSB)	Source of Clock Selection	R/W	0
6	Reserved		
5	Clock Selection [3]	R/W	1
4	Clock Selection [2]	R/W	0
3	Clock Selection [1]	R/W	0
2	Clock Selection [0]	R/W	0
1	ClkIn/2	R/W	0
0(LSB)	Reserved		

This register is used to program the video clock section of the Dual-frequency Synthesizer. Bits 3:2 of the MISC Register (External Group) can be selected to replace Bits 3:2 of this register. See the description for ER9E for information on programming the SQCLK Section of the Dual-frequency Synthesizer.

Bit **Description**

Bit 7 **Source of Clock Selection:** If this bit is set to a '1', then Bits 5:2 of this register are used to program the synthesizer. If this bit is reset to a '0', then Bits 5:4 of this register and Bits 3:2 of the MISC Register (External/General Registers) are used to program the synthesizer. This is shown in the table below:

Table 7–5. VDCLK Select Code Source

ER84[7]	CLKSEL3	CLKSEL2	CLKSEL1	CLKSEL0
1	ER84[5]	ER84[4]	ER84[3]	ER84[2]
0	ER84[5]	ER84[4]	MISC[3]	MISC[2]

Bit 6 Reserved

7.2.26 Clock Select Register: ER84 *(cont.)*

Bit	Description
Bits 5:2	**Clock Selection Bits:** These four bits are used to program the Video Clock Section of the Dual-frequency Synthesizer. If Bit 7 is a reset to a '0', then Bits 3:2 of the MISC Register replace Bits 3:2 of this register as shown in Table 7–5 above. The following table enumerates the available frequencies:

Table 7–6. VDCLK Select Code vs. Frequencies

VDCLK Select Code	Frequency (MHz)	Mode(s)	(ER84)
0000	Reserved		80
0001	65.028	1024 x 768 at 60 Hz	84
0010	85 (Future)	1024 x 768 at 76 Hz	88
0011	36	800 x 600 at 56 Hz	8C
0100	25.175	VGA Graphics Modes	90
0101	28.318	VGA Text Modes	94
0110	24.017		98
0111	39.999	800 x 600 at 60 Hz 132-Column Text Modes	9C
1000	44.907	1024 x 768 at 87 Hz Interlaced	A0
1001	50.344	640 x 480 Direct Color	A4
1010	31.5	VESA 72 Hz (Mode 12)	A8
1011	32.514	100-Column Text Modes	AC
1100	63.0	Direct-Color VESA 72 Hz	B0
1101	72 (Future)	800 x 600 Direct-Color 56 Hz	B4
1110	75 (Future)	1024 x 768 at 70 Hz	B8
1111	80 (Future)	800 x 600 Direct-Color 60 Hz	BC

Bit 1	**ClkIn/2:** This bit, when set to a '1', implements an additional divide by 2 for the frequency selected by Bits 5:2. This feature is primarily used for 3-MHz LCD panels where SimulSCAN support is not required. When this bit is set to a '0' there is no effect.
Bit 0	Reserved

7.2.27 CRTC Test Register: ER86

I/O Port Address: 3CF

Index: 86

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	HSYNC, VSYNC Disable	R/W	0
4	CRTC Outputs Three-State Control	R/W	0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This register is used to configure the CL-GD6412 during factory testing. This register should never be modified by an application program; it is described here for information only.

Bit	Description
Bits 7:6	Reserved
Bit 5	**HSYNC, VSYNC Disable:** This bit is used to disable HSYNC and VSYNC when in Panel-only Mode. If this bit is programmed to a '1', HSYNC and VSYNC are disabled and driven to a '0'.
Bit 4	**CRTC Outputs Three-State Control:** If this bit is set to a '1', the HSYNC and VSYNC Outputs will be placed in the high-impedance (three-state) condition.
Bits 3:0	Reserved

7.2.28 CRTC Spare Extension Register: ER87

I/O Port Address: 3CF

Index: 87

Bit	Description	Access	Reset State
7(MSB)	Enable Short Vertical Total	R/W	0
6	Enable Short Horizontal Total	R/W	0
5	Reserved		
4	LFS/VDE* Pin Configuration	R/W	0
3	Enable Short VSYNC Total	R/W	0
2	Reserved		
1	PVSYNC Configuration	R/W	0
0(LSB)	Reserved		

This register is used for display modification and pin definition.

Bit	Description
Bit 7	**Enable Short Vertical Total:** This bit is used to modify the amount of vertical scanlines generated. Its purpose is to help maintain a more constant refresh rate across video modes. If this bit is set to a '1', the vertical total for any given video mode is set based on the Vertical Display End value in CR12 plus 4 lines. If this bit is set to a '0', then the vertical total is calculated based on the video mode set.
Bit 6	**Enable Short Horizontal Total:** This bit is used to modify the amount of horizontal characters generated. Its purpose is to help maintain a more constant refresh rate across video modes. If this bit is set to a '1', the horizontal total for any given video mode is set based on the Horizontal Display End value in CR01 plus seven character-clocks. If this bit is set to a '0', then the horizontal total is calculated based on the video mode set.
Bit 5	Reserved

7.2.28 CRTC Spare Extension Register: ER87 *(cont.)*

Bit	Description
Bit 4	**LFS/VDE* Pin Configuration:** This bit controls the function definition of Pin 82. It has a higher priority than other bits that affect Pin 82 function definition. If this bit is set to a '1', the Pin 82 function is VDE* (Video Display Enable) for the CL-GD6340. If this bit is set to a '0', then ER8F[4] and ER9B[6:5] have the following definitive effect on Pin 82:
Bit 3	**Enable Short VSYNC Total:** This bit is used in conjunction with Bits 7 and 6 of this register. Software programs that interrogate the display for the occurrence of VSYNC could receive erroneous information if Short-vertical and Short-horizontal Total Bits are set and this bit is not set. If this bit is set to a '1', the VSYNC will track the Display End settings affected by Bits 7 and 6. If this bit is set to a '0', then VSYNC timing will be set to VGA-compatible CRT VSYNC.
Bit 2	Reserved
Bit 1	**PVSYNC Configuration:** This bit defines the function of Pin 82 as PVSYNC. When this bit is set to a '1', and ER87[4] is a '0', then the function of Pin 82 is PVSYNC. Refer to Table 7–7 for further configuration information.
Bit 0	Reserved

Table 7–7. Pin 82 Configuration Matrix

Pin 82 Function	ER87[4]	ER87[1]	ER8F[4]
LFS	0	0	0
FPVDE	0	0	1
VDE*	1	0	x
PVSYNC	0	1	x

7.2.29 CRTC BIOS Configuration Register: ER8F

I/O Port Address: 3CF

Index: 8F

Bit	Description	Access	Reset State
7(MSB)	LLCLK Generation	R/W	0
6	Frame-Accelerator Control Signals	R/W	0
5	Reserved		
4	LFS/FPVDE Pin Configuration	R/W	0
3	FPVDCLK/VDCLK Pin Configuration	R/W	0
2	Suspend* Pin Configuration	R/W	0
1	Clock-Select Pinout Configuration [1]	R/W	0
0(LSB)	Clock-Select Pinout Configuration [0]	R/W	0

This register is used to select between an external synthesizer and a specific group of external oscillators. It must be reset to a '0' when the Dual-frequency Synthesizer is used.

Bit	Description
Bits 7	**LLCLK Generation:** This bit will enable the generation of LLCLK (Line Clock) even during non-display time and will continue to do so until the LFS (Line Frame Start) pulse begins. This is used for flat panels that use LLCLK for the generation of their own Modulation Signal and are sensitive to the lack of modulation during vertical non-display time. If this bit is set to a '1', LLCLK generation will continue until LFS. If it is set to a '0', LLCLKs will terminate normally.
Bit 6	**Frame-Accelerator Control Signals:** This bit controls the high/low logic state of the Frame-Accelerator DRAM control signals FROE*, FRRAS*, FRCAS* and FRWE* while in Suspend Mode. If this bit is set to a '1', these control signals are low at Suspend (to be used in systems that power-down the Frame-Accelerator DRAM). If this bit is set to a '0', these control signals are high at Suspend (to be used in systems that do not power-down the Frame-Accelerator DRAM).
Bit 5	Reserved
Bit 4	**LFS/FPVDE Pin Configuration:** This bit participates in the function definition of Pin 82. Refer to Table 7–7 in this chapter for the configuration matrix.
Bit 3	**FPVDCLK/VDCLK Pin Configuration:** This bit controls the functional configuration of Pin 94. If this bit is set to a '1', Pin 94 is configured as VDCLK. If this bit is a '0', Pin 94 is the flat-panel Shift-clock Signal FPVDCLK.
Bit 2	**Suspend* Pin Configuration:** This bit controls the functional configuration of Pin 117. If this bit is set to a '1', Pin 117 is configured as Suspend* Input. If this bit is set to a '0', Pin 117 is FRA8.

7.2.29 CRTC BIOS Configuration Register: ER8F *(cont.)*

Bit **Description**

Bits 1:0 **Clock-Select Pinout Configuration Bits:** These two bits are used to choose the Clock-Select Configuration as shown in the following table:

Table 7–8. Clock Select Configurations

Value	Configuration
0	Clock Synthesizer or Multiplexer
1	External Oscillators Configuration 1
2	External Oscillators Configuration 2
3	External Oscillators Configuration 3

These bits are reset to a '0' in cases when both the Dual-frequency Synthesizer and External-Frequency Synthesizer are used.

The following table indicates the nominal frequencies that are expected on each pin for Configurations 1, 2, and 3.

Table 7–9. External Oscillator Expectations

Input Pin	Config. 1	Config. 2	Config. 3
OSC	14 MHz	36 MHz	36 MHz
CLKSEL0	32 MHz	45 MHz	65 MHz
CLKSEL1	25 MHz	50 MHz	50 MHz
CLKSEL2	28 MHz	56 MHz	56 MHz
CLKSEL3	24 MHz	40 MHz	40 MHz

7.2.30 Display Memory Control Register: ER90

I/O Port Address: 3CF

Index: 90

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Display Memory Refresh Ext.	R/W	0	
2	Reserved		0	0
1	RAS Precharge	R/W	0	
0(LSB)	Scanline Double Control	R/W	0	

This register is used in the configuration of Display Memory. Each bit used controls an individual element of the configuration.

Bit	Description
Bits 7:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Display Memory Refresh Extension:** This bit is used in conjunction with Bit 6 of CR11 (in the CRTC Group) to specify the number of refresh cycles per scanline. The number is chosen to guarantee an average of one refresh cycle every 16 microseconds (typically). The horizontal period is divided by 16 microseconds, and the result increased to the next integer. The table below indicates the number of refresh cycles executed per horizontal period:

Table 7–10. Refresh Cycle Select

ER90[3]	CR11[6]	Refresh Cycles
0	0	3
0	1	5
1	0	1
1	1	1

7.2.30 Display Memory Control Register: ER90 *(cont.)*

Bit	Description
Bit 2	Reserved: This bit should be programmed as shown above.
Bit 1	**RAS Precharge:** If this bit is set to a '1', the CL-GD6412 will be configured for normal RAS Precharge (three SQCLK cycles). If this bit is set to a '0', the CL-GD6412 will be programmed for Extended-RAS Precharge (four SQCLK cycles).
Bit 0	**Scanline Double Control:** If this bit is set to a '1', each scanline will be sent to the display twice. This is appropriate when displaying Low-resolution Modes (e.g., 640 x 200) on higher-resolution monitors (e.g., 640 x 400). If this bit is reset to a '0', each scanline will be displayed just once per frame.

7.2.31 CRT-Circular Buffer Policy Selection Register: ER91

I/O Port Address: 3CF

Index: 91

Bit	Description	Access	Reset State	Programmed
7(MSB)	CBP7	R	0	
6	CBP6	R	0	
5	CBP5		0	0
4	CBP4		0	0
3	CBP3		0	BIOS
2	CBP2		0	0
1	CBP1		0	0
0(LSB)	CBP0		0	0

This register should never be modified by an application program; it is described here for information only.

Bit	Description
Bits 7:0	**CBP7-CBP0:** These bits should be programmed as shown above, or as determined by the Video BIOS.

7.2.32 Font Control Register: ER92

I/O Port Address: 3CF

Index: 92

Bit	Description	Access	Reset State	Programmed
7(MSB)	Enable Expanded Text	R/W	0	
6	Text Expansion Method Select	R/W	0	
5	Enable Full-Height Cursor	R/W	0	
4	Reserved		0	0
3	Reserved		0	0
2	Reserved		0	0
1	Font Address 17	R/W	0	
0(LSB)	Font Address 16	R/W	0	

Bit	Description
Bit 7	**Enable Expanded Text:** When this bit is set to a '1', the hardware will expand 16-scanline text to 19-scanline text. The three extra scanlines are controlled by Bit 6 of this register. This bit is only used in Text Modes. Setting this bit to a '0' disables text expansion.
Bit 6	**Text Expansion Method Select:** When this bit is set to a '1', Scanlines 0, 8, and 15 are duplicated in expanded text. When this bit is set to a '0', Scanline 0 is repeated twice, and Scanline 15 is repeated once. This bit is effective only when Bit 7 is set to a '1'.
Bit 5	**Enable Full-Height Cursor:** When this bit is set to a '1', a full-height cursor will be generated independently of Cursor-start and Cursor-end Registers. The purpose is to make the cursor more easily visible on the LCD panel.
Bits 4:2	Reserved: These bits should be programmed as shown above.
Bits 1:0	**Font Address:** These bits are used for font control address extension. These bits are also used for bold-font selection, as an alternate font in 16- and 32-bit-wide Video-memory configurations.

7.2.33 CRT-Circular Buffer Delta and Burst Register: ER95

I/O Port Address: 3CF

Index: 95

Bit	Description	Access	Reset State	Programmed
7(MSB)	BURST [3]	R/W	0	0
6	BURST [2]	R/W	0	0
5	BURST [1]	R/W	0	0
4	BURST [0]	R/W	0	0
3	DELTA [3]	R/W	0	0
2	DELTA [2]	R/W	0	0
1	DELTA [1]	R/W	0	0
0(LSB)	DELTA [0]	R/W	0	0

This register should never be modified by an application program; it is described here for information only.

Bit	Description
Bits 7:0	**BURST[3:0] and DELTA[3:0]:** These bits should be programmed as shown above.

7.2.34 Display Memory Control Test Register: ER96

I/O Port Address: 3CF

Index: 96

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Display Memory Bus Three-State	R/W	0	
2	Memory Data 0, 2 Three-State	R/W	0	
1	Reserved		0	
0(LSB)	Latch Monitor ID	R/W	0	

Bit	Description
Bits 7:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Display Memory Bus Three-State:** If this bit is set to a '1', the address and control pins of the Memory Sequencer will be put into high-impedance. These are AA[8:0], AB[8:0] OE*, WE*, RAS*, and CAS*. If this bit is reset to a '0', the address and control pins will be active-high or active-low for normal operation.
Bit 2	**Memory Data 0, 2 Three-State:** If this bit is set to a '1', the M0D and M2D Buses will be put into high-impedance. If this bit is reset to a '0', these buses will behave normally.
Bit 1	Reserved
Bit 0	**Latch Monitor ID:** If this bit is set to a '1', the Monitor ID Bits will be latched just as if reset was being asserted at power-on time. See the description for ER9C. Before setting this bit to a '1', the program must force the screen to blank. Before reading the MONID Register, the program should wait one full-frame time with no screen-refresh cycles. To initiate the latching mechanism, this bit must be programmed to a '1', then to a '0'. The read function occurs when this bit is a '1'; the latch occurs when this bit returns to a '0'.

7.2.35 Monitor Switches Read-Back Register: ER97

I/O Port Address: 3CF

Index: 97

Bit	Description	Access	Default State
7(MSB)	SW7	R	0
6	SW6	R	0
5	SW5	R	0
4	SW4	R	0
3	Reserved	R	0
2	Reserved	R	0
1	Reserved	R	0
0(LSB)	Reserved	R	0

This is a read-only configuration register. It reflects the presence or absence of pull-up or pull-down resistors on several of the MD (Memory Data) Bits. The meanings described below are assigned by the Cirrus Logic BIOS.

Bit	Description		
Bits 7:4	**Default**	**Pin**	**Default Meaning**
	0	FRAD0	Reserved for BIOS
	0	FRAD1	Reserved for BIOS
	0	FRAD2	Panel Class
	0	FRAD3	Panel Class
Bits 3:0	Reserved		

7.2.36 Scratch Register: ER98

I/O Port Address: 3CF

Index: 98

Bit	Description	Access	Reset State
7(MSB)	Scratch [7]	R/W	x
6	Scratch [6]	R/W	x
5	Scratch [5]	R/W	x
4	Scratch [4]	R/W	x
3	Scratch [3]	R/W	x
2	Scratch [2]	R/W	x
1	Scratch [1]	R/W	x
0(LSB)	Scratch [0]	R/W	x

Bit	Description
Bits 7:0	**Scratch Bits 7:0:** This register has no effect on the operation of the CL-GD6412. It is reserved for the use of the BIOS.

7.2.37 Configuration Register: ER99

I/O Port Address: 3CF

Index: 99

Bit	Description	Access	Default State
7(MSB)	Reserved	R	0
6	Reserved	R	0
5	Reserved	R	0
4	BIOS Width	R	0
3	Sleep Location	R	1
2	Reduced Decode	R	0
1	Reserved		0
0(LSB)	Enable ROM Decode (C000:0)	R	1

This is a read-only configuration register. It reflects the presence or absence of pull-up or pull-down resistors on several pins. It is updated at reset time or whenever ER96[0] is toggled. The configuration resistors described in this register have a direct effect on the hardware.

Bit	Description		
Bits 7:0	**Default**	**Pin**	**Default State**
	0	PD7	Reserved
	0		Reserved
	0		Reserved
	0	FRA8	BIOS Width (8- or 16-bit)
	1	FRA7	Sleep Location (3C3h or 46E8h)
	0	FRA6	Reserved
	0	FRA5	Reserved
	1	FRA4	Enable ROM Decode (C000:0)

7.2.38 Display Memory Configuration Register: ER9A

I/O Port Address: 3CF

Index: 9A

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Reserved		0	0
2	Reserved		0	0
1	Reserved		0	0
0(LSB)	Reserved		0	0

This register is used to choose memory-width configuration.

Bit	Description
Bits 7:0	Reserved: These bits should be programmed as shown above.

7.2.39 Miscellaneous Configuration 1 Register: ER9B

I/O Port Address: 3CF

Index: 9B

Bit	Description	Access	Reset State	Programmed
7(MSB)	Paged BIOS Disable	R/W	0	
6	LLCLK/DE/FPHDE/PHSYNC Pin Config. [1]	R/W	0	
5	LLCLK/DE/FPHDE/PHSYNC Pin Config. [0]	R/W	0	
4	MOD/P8/BLANK* Pin Config.[1]	R/W	0	
3	MOD/P8/BLANK* Pin Config. [0]	R/W	0	
2	Reserved		0	0
1	On-Chip Monitor Sense Enable	R/W	0	
0(LSB)	SQCLK Phase Inversion	R/W	0	

Bit	Description
Bit 7	**Paged BIOS Disable:** This bit controls the function of Pins 64:62. If it is set to a '1', then Pins 64:62 become TIMER*, PO1, and SSCLK, respectively. If this bit is set to a '0', Pins 64:62 become the BIOS paging bits BIOS-A[15], BIOS-A[14], and BIOS-A[13], respectively. If a paged BIOS greater than 32K is desired, this bit must be set to a '0' to allow for pagination.
Bits 6:5	**LLCLK/DE/FPHDE/PHSYNC Pin Configuration Bits:** These two bits configure the function of Pin 98 as shown in the following table. These bits have no effect if ER81[3] is set to a '1' (CL-GD6340 Mode Enable).

Table 7–11. LLCLK/DE/FPHDE/PHSYNC Pin Configuration

Bit 6	Bit 5	Pin Function
0	0	LLCLK (Default at Power-On)
0	1	DE (for the CL-GD6340)
1	0	FPHDE
1	1	PHSYNC

7.2.39 Miscellaneous Configuration 1 Register: ER9B *(cont.)*

Bit — **Description**

Bits 4:3 — **MODULATION/P8/BLANK* Pin Configuration Bits:** These two bits configure the function of Pin 80 as shown in the following table.

Table 7–12. MODULATION/P8/BLANK* Pin Configuration

Bit 4	Bit 3	Pin Function
0	0	MODULATION (for the LCD panel)
0	1	MODULATION (for the LCD panel)
1	0	P[8] for 512-color TFT panel video Red[2] Bit. This function can also be forced by ERDC[0] = 0.
1	1	BLANK* for CL-GD6340 support

Bit 2 — Reserved: This bit should be programmed as shown above.

Bit 1 — **On-Chip Monitor Sense Enable:** If this bit is reset to a '0', the On-chip Monitor Sense is enabled.

Bit 0 — **SQCLK Phase Inversion:** When this bit is set to a '1', the phase of the SQCLK (Memory Clock) is inverted. When this bit is set to a '0', SQCLK phase is normal.

7.2.40 PS/2 Monitor ID Register: ER9C

I/O Port Address: 3CF

Index: 9C

Bit	Description	Access	Reset State
7(MSB)	PS/2 Monitor ID [2]	R	
6	PS/2 Monitor ID [1]	R	
5	PS/2 Monitor ID [0]	R	
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This read-only configuration register returns a value corresponding to the PS/2 Monitor connected to Pins M0D[7:5]. The levels on these pins are sensed when RESET goes active or whenever ER96[0] is toggled.

Bit	Description		
Bits 7:5	**Description** PS/2 Monitor ID 010: 8514 Monitor 101: 8503 Monitor 110: 8512/8513 Monitor 111: No Monitor **NOTE**: A '1' denotes a 'no-connect'.	**Default** (none)	**MD Pin** M0D[7:5]
Bits 4:0	Reserved. These bits are reserved, and the value returned is a '0'.		

7.2.41 Miscellaneous Configuration 2 Register: ER9D

I/O Port Address: 3CF

Index: 9D

Bit	Description	Access	Reset State	Programmed
7(MSB)	Select OSC as SQCLK	R/W	0	
6	5/3.3V Monitor Sense Select	R/W	0	
5	Reserved		0	
4	Reserved		0	
3	Reserved		0	0
2	Reserved		0	
1	Select OE* Delay	R/W	0	
0(LSB)	FPVDCLK Delay	R/W	0	

Bit	Description
Bit 7	**Select OSC as SQCLK:** When this bit is set to a '1', then SQCLK is derived from the clock connected to OSC. When this bit is set to a '0', then both SQCLK and OSC clock inputs are required.
Bit 6	**5/3.3V Monitor Sense Select:** If this is set to a '1', the Monitor Sense threshold is adjusted for 5.0-volt operation. If this bit is set to a '0', the Monitor Sense threshold is set for 3.3-volt operation.
Bits 5:4	Reserved
Bit 3	Reserved: This bit must be programmed as shown above.
Bit 2	Reserved
Bit 1	**Select OE* Delay:** If this bit is set to a '1', then the Output Enable (OE*) Signal for the DRAMs is delayed by one full SQCLK. If this bit is set to a '0', then no delays occur.
Bit 0	**FPVDCLK Delay:** If this bit is set to a '1', the Flat Panel Video Clock (FPVDCLK) Signal is delayed one-half a VDCLK period (dotclock). If this bit is reset to a '0', then no delays occur.

7.2.42 Bus Interface Unit Control Register: ERA0

I/O Port Address: 3CF

Index: A0

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	CPU Address Scramble Disable	R/W	0
5	Enable 16-Bit I/O	R/W	0
4	Enable 16-Bit Memory	R/W	0
3	MEMCS16* Mode Select	R/W	0
2	RAMDAC RAM Write Protect	R/W	0
1	Disable Sleep Mechanism	R/W	0
0(LSB)	Disable ROM BIOS	R/W	0

This register is used in conjunction with other Extension Registers in the ERAX range, to configure the Bus Interface Unit (host interface).

Bit	Description
Bit 7	Reserved
Bit 6	**CPU Address Scramble Disable:** If this is set to a '1', SR3[3,1] Address Scrambling is disabled.
Bit 5	**Enable 16-Bit I/O:** If this is set to a '1', 16-bit I/O Response is enabled. If this bit is reset to a '0', all I/O operations will be executed in 8-bit Mode (ISA Bus).
Bit 4	**Enable 16-Bit Memory:** This bit is a simple memory-enable bit. If it set to a '0', 8-bit memory interface applies; if it is set to a '1', 16-bit memory interface is enabled.

7.2.42 Bus Interface Unit Control Register: ERA0 *(cont.)*

Bit	Description
Bit 3	**MEMCS16* Mode Select:** If this bit is set to a '1', the entire Memory Address Range A000:0 to BFFF:F and C000:0 to C7FF:F will be decoded as valid for 16-bit memory operations. If this bit is reset to a '0', only the sub-range required for the current Video Mode will be decoded as valid for 16-bit memory operations.
Bit 2	**RAMDAC RAM Write Protect:** If this bit is set to a '1', then the internal RAMDAC RAM is write-protected. This bit should be set only in LCD Mode when it is desired that the application program does not change the grayscale values.
Bit 1	**Disable Sleep Mechanism:** If this bit is set to a '1', the Sleep Mechanism is disabled (3C3 or 46E8). Accesses to the Sleep Mechanism Address will be ignored. If this bit is reset to a '0', the Sleep Mechanism is enabled and operates normally.
Bit 0	**Disable ROM BIOS:** If this bit is set to a '1', the ROM BIOS is disabled and accesses in the range C000:0 will be ignored. If this bit is reset to a '0', the ROM BIOS is enabled and operates normally. This bit must be reset to a '0' and BIOS Enable configuration (described in ER99) must be a '1' (default) for the ROM to operate.

7.2.43 Three-State and Test Control Register: ERA1

I/O Port Address: 3CF

Index: A1

Bit	Description	Access	Reset State	Programmed
7(MSB)	Disable IOR*	R/W	0	
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Three-State Control on I/O Pins	R/W	0	
2	Reserved		0	0
1	Reserved		0	0
0(LSB)	Reserved		0	0

This register contains bits that are used for testing the Bus Interface Unit (host interface). This register should never be modified by an application program.

Bit	Description
Bit 7	**Disable IOR*:** When this bit is set to a '1', I/O reads are disabled to the CL-GD6412. This feature is used primarily for testing and should not be programmed by any application.
Bits 6:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Three-State Control on I/O Pins:** If this bit is set to a '1', all Output and I/O Pins are forced into the high-impedance state.
Bits 2:0	Reserved: These bits should be programmed as shown above.

7.2.44 BIOS Page Selection Register: ERA2

I/O Port Address: 3CF

Index: A2

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	BIOS Page [2]	R/W	0
1	BIOS Page [1]	R/W	0
0(LSB)	BIOS Page [0]	R/W	0

This register contains bits that are used for BIOS pagination in the event that EPROMs are being used for the Video BIOS.

Bit	Description
Bits 7:3	Reserved
Bits 2:0	**BIOS Pagination Bits**: These three bits are used as a method of extending the normal VGA address space occupied by the Video BIOS. The pagination method is indicated in the following table:

Table 7–13. BIOS Pagination

Bit 2	Bit 1	Bit 0	Description
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Page 0 (Address Range 25K bytes to 32K bytes)
1	0	0	Page 1 (Address Range 33K bytes to 40K bytes)
1	0	1	Page 2 (Address Range 41K bytes to 48K bytes)
1	1	0	Page 3 (Address Range 49K bytes to 56K bytes)
1	1	1	Page 4 (Address Range 57K bytes to 64K bytes)

7.2.45 Wait State Controls Register: ERA6

I/O Port Address: 3CF

Index: A6

Bit	Description	Access	Reset State	Programmed
7(MSB)	Bus Width Status	R	0	
6	BIOS Wait-State Control	R/W	0	
5	Reserved		0	0
4	I/O Write Wait Control	R/W	0	
3	RAMDAC Wait Control	R/W	0	
2	0WS* for Memory Write	R/W	0	
1	I/O Read Wait Control	R/W	0	
0(LSB)	Display Memory Write Wait Control	R/W	0	

This register is used to control the insertion of wait states in various host accesses. This register should never be modified by an application program.

Bit	Description
Bit 7	**Bus Width Status:** This is a read-only bit. If a '1' is returned, the CL-GD6412 has detected at least one transition on SBHE*, indicating that it is connected to a 16-bit interface.
Bit 6	**BIOS Wait-State Control:** Setting this bit to a '1' allows for the BIOS to operate with zero wait states. In most cases this bit will be a '0'.
Bit 5	Reserved: This bit should be programmed as shown above.
Bit 4	**I/O Write Wait Control:** If this bit is set to a '1', no wait states will be inserted for I/O writes. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for I/O writes.
Bit 3	**RAMDAC Wait Control:** If this bit is set to a '1', no wait states will be inserted for I/O read or write accesses to the external RAMDAC. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for I/O read or write accesses to the external RAMDAC.
Bit 2	**0WS* for Memory Write:** If this bit is set to a '1', 0WS* will be asserted for Display Memory writes (that can be executed immediately). If this bit is reset to a '0', 0WS* will not be asserted for any Display Memory writes.
Bit 1	**I/O Read Wait Control:** If this bit is set to a '1', no wait states will be inserted for I/O reads. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for I/O reads.
Bit 0	**Display Memory Write Wait Control:** If this bit is set to a '1', no wait states will be inserted for Display Memory writes. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for Display Memory writes.

7.2.46 General Programmable I/O Port Control: ERA7

I/O Port Address: 3CF

Index: A7

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	PO1 Control	R/W	0
0(LSB)	Reserved		0

Bit	Description
Bits 7:2	Reserved
Bit 1	**Programmable Output Pin Configuration:** This bit is used to program Pin 63 (PO1) if ER9B is a '1'. Set this bit to a '1' to establish a high condition on Pin 63. Set it to a '0' for a low condition.
Bit 0	Reserved

7.2.47 Bus Interface Unit Cache Controls Register: ERA9

I/O Port Address: 3CF

Index: A9

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Internal BIUC Timing [1]	R/W	0	
5	Internal BIUC Timing [0]	R/W	0	
4	Reserved		0	0
3	Enable Compaction in Modes 2 and 3	R/W	0	
2	Reserved		0	0
1	Enable Read Cache	R/W	0	
0(LSB)	Reserved		0	0

This register controls options regarding the Bus Interface Unit (host interface). This register should never be modified by an application program.

Bit	Description
Bit 7	Reserved: This bit should be programmed as shown above.
Bits 6:5	**Internal BIUC Timing Bits:** These two bits control the Internal BIUC (Bus Interface Unit Cache) Timing delay, and they must be programmed according to the period of the Sequencer Clock (SQCLK). The following table indicates the limits:

Table 7–14. Internal BIUC Timing

Value	SQCLK Period	SQCLK Frequency
00	20-23 ns	49.09 MHz
01	23-25 ns	43.90 MHz
10	25-29 ns	35.90 MHz
11	–	–

Bit 4	Reserved: This bit should be programmed as shown above.
Bit 3	**Enable Compaction in Modes 2 and 3:** If this bit is set to a '1', write-overwrite compaction is enabled for Write Modes 2 and 3. If this bit is reset to a '0', write-overwrite compaction is not enabled for Write Modes 2 and 3.

7.2.47 Bus Interface Cache Controls Register: ERA9 *(cont.)*

Bit	Description
Bit 2	Reserved: This bit should be programmed as shown above.
Bit 1	**Enable Read Cache:** If this bit is set to a '1', the CPU Data Latches can be used as a source of data for CPU reads. If this bit is reset to a '0', the function is disabled and all CPU reads must be satisfied from the Display Memory.
Bit 0	Reserved: This bit should be programmed as shown above.

7.2.48 Design Revision Register: ERAA

I/O Port Address: 3CF

Index: AA

Bit	Description	Access	Reset State
7(MSB)	CL-GD6412 Revision [7]	R	0
6	CL-GD6412 Revision [6]	R	1
5	CL-GD6412 Revision [5]	R	1
4	CL-GD6412 Revision [4]	R	0
3	CL-GD6412 Revision [3]	R	1
2	CL-GD6412 Revision [2]	R	1
1	CL-GD6412 Revision [1]	R	1
0(LSB)	CL-GD6412 Revision [0]	R	1

This read-only register returns a unique value that is factory-programmed into the CL-GD6412.

Bit	Description
Bit 7:0	**Design Revision Bits 7:0:** These eight bits identify the chip revision level.

7.2.49 Mask Revision Register: ERAB

I/O Port Address: 3CF

Index: AB

Bit	Description	Access	Reset State
7(MSB)	CL-GD6412 Mask Revision [7]	R	0
6	CL-GD6412 Mask Revision [6]	R	1
5	CL-GD6412 Mask Revision [5]	R	1
4	CL-GD6412 Mask Revision [4]	R	0
3	CL-GD6412 Mask Revision [3]	R	1
2	CL-GD6412 Mask Revision [2]	R	1
1	CL-GD6412 Mask Revision [1]	R	1
0(LSB)	CL-GD6412 Mask Revision [0]	R	1

This read-only register returns a unique value that is factory-programmed into the CL-GD6412.

Bit	Description
Bit 0	**Mask Revision Bits 7:0:** These eight bits identify the chip mask revision level.

7.2.50 Alternate Extension Decode High Register: ERAE

I/O Port Address: 3CF

Index: AE

Bit	Description	Access	Reset State
7(MSB)	Extension Decode High [7]	R/W	0
6	Extension Decode High [6]	R/W	0
5	Extension Decode High [5]	R/W	0
4	Extension Decode High [4]	R/W	0
3	Extension Decode High [3]	R/W	0
2	Extension Decode High [2]	R/W	0
1	Extension Decode High [1]	R/W	1
0(LSB)	Extension Decode High [0]	R/W	1

This register is defined to allow for the CL-GD6412 I/O address space to be remapped to an address other than standard VGA.

Bit	Description
Bits 7:0	**Extension Decode High Bits 7:0:** This register works in conjunction with ERAF, and defines an alternate I/O address space for the CL-GD6412. ERAE and ERAF are enabled by ER0D[3]. The reset value is 03 to conform to standard VGA.

7.2.51 Alternate Extension Decode Low Register: ERAF

I/O Port Address: 3CF

Index: AF

Bit	Description	Access	Reset State
7(MSB)	Extension Decode Low [7]	R/W	1
6	Extension Decode Low [6]	R/W	1
5	Extension Decode Low [5]	R/W	0
4	Extension Decode Low [4]	R/W	0
3	Extension Decode Low [3]	R/W	1
2	Extension Decode Low [2]	R/W	1
1	Extension Decode Low [1]	R/W	1
0(LSB)	Extension Decode Low [0]	R/W	0

This register is defined to allow for the CL-GD6412 I/O address space to be remapped to an address other than standard VGA.

Bit	Description
Bits 7:0	**Extension Decode Low Bits 7:0:** This register works in conjunction with ERAE, and defines an alternate I/O address space for the CL-GD6412. ERAE and ERAF are enabled by ER0D[3]. The reset value is CE to conform to standard VGA.

7.2.52 Scratch Registers 5-0: ERBA-BF

I/O Port Address: 3CF

Index: BA-BF

Bit	Description	Access	Reset State
7(MSB)	Scratch Register [7]	R/W	0
6	Scratch Register [6]	R/W	0
5	Scratch Register [5]	R/W	0
4	Scratch Register [4]	R/W	0
3	Scratch Register [3]	R/W	0
2	Scratch Register [2]	R/W	0
1	Scratch Register [1]	R/W	0
0(LSB)	Scratch Register [0]	R/W	0

Bit	Description
Bits 7:0	**Scratch Register Bits 7:0:** The six registers, ERAB-BF, have no effect on the operation of the CL-GD6412. These registers are reserved for the exclusive use of the Cirrus Logic BIOS.

7.2.53 Attribute and Graphics Control Register: ERC0

I/O Port Address: 3CF

Index: C0

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Background Color Enhancement	R/W	0	
2	Enable 4-Bit Monochrome Flat Panels	R/W	0	
1	Bypass Internal Palettes	R/W	0	
0(LSB)	Foreground Color Enhancement	R/W	0	

Bit	Description
Bits 7:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Background Color Enhancement:** If this bit is set to a '1', then the contrast ratio for background and foreground colors is enhanced by the following formula: *If* Foreground Color = 0 Background Color = 7 *else* Background Color = 0 If this bit is set to a '0', then normal background color applies.
Bit 2	**Enable 4-Bit (Single-Scan) Monochrome Flat Panel:** If this bit is set to a '1', support for single-scan monochrome flat panels is provided.
Bit 1	**Bypass Internal Palettes:** If this bit is set to a '1', the internal palette (AR0-F) is bypassed. If this bit is reset to a '0', the internal palette is used.
Bit 0	**Foreground Color Enhancement:** If this bit is set to a '1', the intensity bit of the foreground color will be XOR, except when the foreground color = 0 or 8. If this bit is set to a '0', normal foreground color applies.

7.2.54 Cursor Attributes Register: ERC1

I/O Port Address: 3CF

Index: C1

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Force Cursor Color	R/W	0	
4	Invert Border Color	R/W	0	
3	Cursor Mode	R/W	0	
2	Cursor Blink Rate [1]	R/W	0	
1	Cursor Blink Rate [0]	R/W	0	
0(LSB)	Cursor Blink Disable	R/W	0	

This register controls the cursor in the CL-GD6412.

Bit	Description
Bits 7:6	Reserved: These bits should be programmed as shown above.
Bit 5	**Force Cursor Color:** If this bit is set to a '1', cursor color is forced to black and white in LCD Mode. If it is set to a '0', the cursor color is normal.
Bit 4	**Invert Border Color:** If this bit is set to a '1', the bits of the border color (see AR11) are inverted. If this bit is reset to a '0', the bits of the border color are not inverted.
Bit 3	**Cursor Mode:** If this bit is set to a '1', the cursor is displayed by inverting the screen 'behind' the cursor. If this bit is reset to a '0', the cursor is displayed by replacing the screen 'behind' the cursor.
Bits 2:1	**Cursor Blink Rate Bits:** This 2-bit field controls the cursor blinking rate if enabled by Bit 0. The following table shows the blink rates:
Bit 0	**Cursor Blink Disable:** If this bit is set to a '0', cursor blinking is enabled at the rate specified in Bits 2:1. If this bit is reset to a '1', cursor blinking is disabled and Bits 2:1 are ignored.

Table 7–15. Blink Rates

Value	Blink Rate	Note
00	Vertical Scan Rate/16	Normal
01	Vertical Scan Rate/32	Slow
10	Vertical Scan Rate/8	Fast
11	Vertical Scan Rate/4	Very fast

7.2.55 Graphics Controller Memory Latches 0-3 Register: ERC2-C5

I/O Port Address: 3CF

Index: C2-C5

Bit	Description	Access	Reset State
7(MSB)	Reserved	R/W	0
6	Reserved	R/W	0
5	Reserved	R/W	0
4	Reserved	R/W	0
3	Reserved	R/W	0
2	Reserved	R/W	0
1	Reserved	R/W	0
0(LSB)	Reserved	R/W	0

Bit	Description
Bits 7:0	Reserved

7.2.56 RAMDAC Controls Register: ERC8

I/O Port Address: 3CF

Index: C8

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Blank to RAMDAC	R/W	0	
4	Reserved	R/W	0	0
3	Reserved	R/W	0	0
2	Reserved	R/W	0	0
1	Extended 16-Color Modes	R/W	0	
0(LSB)	Reserved		0	0

This register is used to control the integrated RAMDAC. This register should never be modified by an application program.

Bit	Description
Bits 7:6	Reserved: These bits should be programmed as shown above.
Bit 5	**Blank to RAMDAC:** If this bit is set to a '1', the internal RAMDAC is forced to the current levels corresponding to BLANK.
Bits 4:2	Reserved: These bits should be programmed as shown above.
Bit 1	**Extended 16-Color (Packed-Pixel) Mode:** This bit should be set to a '1' for any 16-color Packed-pixel Mode.
Bit 0	Reserved: This bit should be programmed as shown above.

7.2.57 Graphics and Attribute Test Register: ERC9

I/O Port Address: 3CF

Index: C9

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved	R/W	0	0
6	Reserved	R/W	0	0
5	Reserved	R/W	0	0
4	Three-State P, VDCLK	R/W	0	
3	9-Dot Font Enable	R/W	0	
2	Reserved	R/W	0	0
1	Reserved	R/W	0	0
0(LSB)	Reserved	R/W	0	0

Bit	Description
Bits 7:5	Reserved: These bits should be programmed as shown above.
Bit 4	**Three-State P, VDCLK:** If this bit is set to a '1', then P[7:0], FPVDCLK, and VDCLK are forced into high impedance. If this bit is reset to a '0', then P[7:0], FPVDCLK, and VDCLK operate normally.
Bit 3	**9-Dot Font Enable:** If this bit is set to a '1', the ninth bit of the font is fetched from Bit Plane 3, Bit 7 — MD[31] — rather than being a replication of the eighth bit.
Bits 2:0	Reserved: These bits should be programmed as shown above.

7.2.58 Flat Panel Column Offset Register: ERD0

I/O Port Address: 3CF

Index: D0

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Column Offset [7]	R/W	0
6	Flat Panel Column Offset [6]	R/W	0
5	Flat Panel Column Offset [5]	R/W	0
4	Flat Panel Column Offset [4]	R/W	0
3	Flat Panel Column Offset [3]	R/W	0
2	Flat Panel Column Offset [2]	R/W	0
1	Flat Panel Column Offset [1]	R/W	0
0(LSB)	Flat Panel Column Offset [0]	R/W	0

This register performs a panning offset function on the flat panel display. The normal displayed image will be affected according to the values programmed into this register. These are the eight least-significant bits of a 9-bit value. The most significant bit is in Bit 0 of ERD4. The value is used to indicate when the data begins to be displayed on the flat panel and is represented in nibbles.

Bit	Description
Bits 7:0	**Flat Panel Column Offset Bits 7:0:** These are the eight least-significant bits of a 9-bit value. The most-significant bit is in Bit 0 of ERD4. The value is used to indicate when the data begins to be displayed on the flat panel. If the value = 0Ah: The normal display image will be displayed at the left-most column of flat panel. If the value > 0Ah: The normal display image will be displaced to the left by the difference between the values and 0Ah. If the value < 0Ah: The normal display image will be displaced to the right by the difference between the values and 0Ah.

7.2.59 Flat Panel Horizontal Size Register: ERD1

I/O Port Address: 3CF

Index: D1

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Horizontal Size [7]	R/W	0
6	Flat Panel Horizontal Size [6]	R/W	0
5	Flat Panel Horizontal Size [5]	R/W	0
4	Flat Panel Horizontal Size [4]	R/W	0
3	Flat Panel Horizontal Size [3]	R/W	0
2	Flat Panel Horizontal Size [2]	R/W	0
1	Flat Panel Horizontal Size [1]	R/W	0
0(LSB)	Flat Panel Horizontal Size [0]	R/W	0

This register contains the eight least-significant bits of a 9-bit value for the number of horizontal displayable nibbles on the panel. The most-significant bit (Bit 8), is located in Bit 1 of the Flat Panel Overflow Register (ERD4).

Bit	Description
Bits 7:0	**Flat Panel Horizontal Size Bits 7:0:** The value determines the horizontal width of the panel in nibble units. For 640-column panels, this register should be programmed to (640 ÷ 4) - 1 = 159 decimal (9Fh).

7.2.60 Flat Panel Row Offset Register: ERD2

I/O Port Address: 3CF

Index: D2

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Row Offset [7]	R/W	0
6	Flat Panel Row Offset [6]	R/W	0
5	Flat Panel Row Offset [5]	R/W	0
4	Flat Panel Row Offset [4]	R/W	0
3	Flat Panel Row Offset [3]	R/W	0
2	Flat Panel Row Offset [2]	R/W	0
1	Flat Panel Row Offset [1]	R/W	0
0(LSB)	Flat Panel Row Offset [0]	R/W	0

This register provides vertical centering for the display image. This register is active only if auto-center is disabled.

Bit	Description
Bits 7:0	**Flat Panel Row Offset Bits 7:0:** These bits are eight least-significant bits of a 10-bit value. The most-significant bits are located at ERD4[3:2]. The 10-bit value determines the row location of the display image, calculated from the top of the flat panel.

7.2.61 Flat Panel Vertical Size Register: ERD3

I/O Port Address: 3CF

Index: D3

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Vertical Size [7]	R/W	0
6	Flat Panel Vertical Size [6]	R/W	0
5	Flat Panel Vertical Size [5]	R/W	0
4	Flat Panel Vertical Size [4]	R/W	0
3	Flat Panel Vertical Size [3]	R/W	0
2	Flat Panel Vertical Size [2]	R/W	0
1	Flat Panel Vertical Size [1]	R/W	0
0(LSB)	Flat Panel Vertical Size [0]	R/W	0

This register provides the number of vertical lines for the display image.

Bit	Description
Bits 7:0	**Flat Panel Vertical Size Bits 7:0:** These bits are the eight least-significant bits of a 10-bit value. The most-significant bits are located at ERD4[6:4]. If using a single-scan panel, the 10-bit value determines the number of rows minus 1; if using a dual-scan panel, the 10-bit value determines the number of half-panel rows divided by 2, minus 1.

7.2.62 Flat Panel Overflow Register: ERD4

I/O Port Address: 3CF

Index: D4

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Flat Panel Vertical Size Overflow [10]	R/W	0
5	Flat Panel Vertical Size Overflow [9]	R/W	0
4	Flat Panel Vertical Size Overflow [8]	R/W	0
3	Flat Panel Row Offset Overflow [9]	R/W	0
2	Flat Panel Row Offset Overflow [8]	R/W	0
1	Flat Panel Horizontal Size Overflow [8]	R/W	0
0(LSB)	Flat Panel Column Offset Overflow [8]	R/W	0

This register provides overflow bits for other registers.

Bit	Description
Bit 7	Reserved
Bits 6:4	**Flat Panel Vertical Size Overflow Bits 10:8:** Refer to ERD3.
Bits 3:2	**Flat Panel Row Offset Overflow Bits 9:8:** Refer to ERD2.
Bit 1	**Flat Panel Horizontal Size Overflow Bit 8:** Refer to ERD1.
Bit 0	**Flat Panel Column Offset Overflow Bit 8:** Refer to ERD0.

7.2.63 Flat Panel Attribute Control Register: ERD5

I/O Port Address: 3CF

Index: D5

Bit	Description	Access	Reset State
7(MSB)	Enable AutoMap	R/W	0
6	Enable Reverse Video in Text Mode	R/W	0
5	Enable Reverse Video in Graphics Mode	R/W	0
4	Extra Line Clock Enable	R/W	0
3	Attribute Emulation Enable	R/W	0
2	Standby Mode Status	R	0
1	9-Dot Text Compression Control [1]	R/W	0
0(LSB)	9-Dot Text Compression Control [0]	R/W	0

Bit	Description
Bit 7	**Enable AutoMap:** When this bit is set to a '1', the internal grayscale palette is enabled. This palette stores sum-to-gray data mapped from the RAMDAC, allowing 256-color graphics to be automatically mapped to 64 grayscales. When this bit is set to '0', the internal LCD palette is bypassed.
Bit 6	**Enable Reverse Video in Text Mode:** Setting this bit to a '1' enables reverse video in Text Mode for flat panels only.
Bit 5	**Enable Reverse Video in Graphics Mode:** Setting this bit to a '1' enables reverse video in Graphics Mode for flat panels only.
Bit 4	**Extra Line Clock Enable (FPLCLK):** If this bit is set to a '1', an extra line-clock pulse is generated on the lower half of dual-scan flat panels. This feature is provided for those flat panels that have the first row-driver of the lower panel disconnected. If this bit is set to a '0', no extra line-clock pulse is generated.
Bit 3	**Attribute Emulation Enable:** If this bit is set to a '1', attribute emulation is enabled. It is a function used only in text modes that optimizes the contrast of the displayed text by taking background and foreground colors into consideration. If this bit is set to a '0', then colors are freely mapped into shades of gray under control of the attribute controller palette registers and the LCD palette RAM.
Bit 2	**Standby Mode Status:** This is a read-only bit indicating that the CL-GD6412 is in Standby Mode.

7.2.63 Flat Panel Attribute Control Register: ERD5 *(cont.)*

Bit	Description
Bits 1:0	**9-Dot Text Compression Control Bits:** These two bits control the compression methods used to allow a 720-pixel display image to be fitted into a 640-pixel display. During SimulSCAN, these bits allow for the simultaneous display of 9-dot text on the CRT and 8-dot text on an LCD. These bits are defined as follows:

Table 7–16. 9-Dot Text Compression Control

ERD5[1]	ERD5[0]	Meaning
0	x	Display 640 pixels out of 720-pixel image. To be panned with the Column Offset Register (ERD0h). Only a partial image will be displayed.
1	0	Skip every ninth pixel. The whole 720-pixel image will be compressed into a 640-pixel display.
1	1	Logical OR the eighth pixel and the ninth pixel and place the result back into the eighth pixel.

7.2.64 Flat Panel Grayscale Offset Register: ERD6

I/O Port Address: 3CF

Index: D6

Bit	Description	Access	Reset State
7(MSB)	Enable Vertical Stippling	R/W	0
6	Enable Horizontal Stippling	R/W	0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Power Sequencing Time Control	R/W	0
1	Power Sequencing Control	R/W	0
0(LSB)	Grayscale Offset value	R/W	0

Bit	Description
Bit 7	**Enable Vertical Stippling:** When this bit is set to a '1', vertical stippling is enabled, increasing the effective number of gray shades applied to the flat panel.
Bit 6	**Enable Horizontal Stippling:** When this bit is set to a '1', horizontal stippling is enabled, increasing the effective number of gray shades applied to the flat panel.
Bits 5:3	Reserved
Bit 2	**Power Sequencing Time Control:** This bit, which is a flat-panel-dependent parameter, controls the length of the time interval between two power sequencing steps. If this bit is set to a '1', 128-136 milliseconds is selected. If this bit is set to a '0', 32-40 milliseconds is selected.
Bit 1	**Power Sequencing Control:** This bit can be used by the BIOS or a utility program to control when the flat-panel power-sequencing on- or off-sequence starts. It is typically set by the BIOS after POST or at any time there is a power-up or power-down sequence. Setting this bit allows the power-sequencing state machine to proceed; otherwise, the flat panel will not be powered-on.
Bit 0	**Grayscale Offset Value:** This bit is normally set to a '0' (selecting a value of 13). Optionally, this bit could be programmed to a '1' (selecting a value of 4) to reduce flicker on some flat panels.

7.2.65 Flat Panel Retrace Line Clock Control Register: ERD7

I/O Port Address: 3CF

Index: D7

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Retrace Line Clocks [4]	R/W	0
3	Retrace Line Clocks [3]	R/W	0
2	Retrace Line Clocks [2]	R/W	0
1	Retrace Line Clocks [1]	R/W	0
0(LSB)	Retrace Line Clocks [0]	R/W	0

Bit	Description
Bits 7:5	Reserved
Bits 4:0	**Retrace Line Clocks Bits 4:0:** These five bits define a number (from 1 to 32) of extra Line Clocks (LLCLKs) that are required during vertical retrace (actually between flat-panel frames). These extra Line Clocks are generated at an accelerated rate compared to normal Line Clocks and use a different pulse width.

7.2.66 Flat Panel Frame Color Register: ERD8

I/O Port Address: 3CF

Index: D8

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Enable Extra LLCLK	R/W	0
5	Reserved		0
4	Enable Frame Color	R/W	0
3	Frame Color [3]	R/W	0
2	Frame Color [2]	R/W	0
1	Frame Color [1]	R/W	0
0(LSB)	Frame Color [0]	R/W	0

Bit	Description
Bit 7	Reserved
Bit 6	**Enable Extra LLCLK:** This bit allows for the insertion of one extra LLCLK (Line Clock) after Line 240 on dual-scan monochrome flat panels as required by some panel manufacturers.
Bit 5	Reserved
Bit 4	**Enable Frame Color:** Setting this bit to a '1' enables setting the frame color.
Bits 3:0	**Frame Color Bits [3:0]:** This register provides color control for the non-displayed portion of the flat panel. This register will track the reverse video in text and graphics modes.

7.2.67 Flat Panel AC Modulation Register: ERD9

I/O Port Address: 3CF

Index: D9

Bit	Description	Access	Reset State
7(MSB)	Flat Panel AC Modulation [7]	R/W	0
6	Flat Panel AC Modulation [6]	R/W	0
5	Flat Panel AC Modulation [5]	R/W	0
4	Flat Panel AC Modulation [4]	R/W	0
3	Flat Panel AC Modulation [3]	R/W	0
2	Flat Panel AC Modulation [2]	R/W	0
1	Flat Panel AC Modulation [1]	R/W	0
0(LSB)	Flat Panel AC Modulation [0]	R/W	0

This register specifies the value applied for AC Modulation.

Bit	Description
Bits 7:0	**Flat Panel AC Modulation Bits 7:0:** These eight bits determine the half-period of the square wave applied to the MOD Output Pin, measured in line clocks. Normally this value is one that does not divide evenly into the panel size.

7.2.68 Flat Panel Display Control Register: ERDA

I/O Port Address: 3CF

Index: DA

Bit	Description	Access	Reset State
7(MSB)	RGB Weight Control [2]	R/W	0
6	RGB Weight Control [1]	R/W	0
5	RGB Weight Control [0]	R/W	0
4	Flat Panel Size Select [1]	R/W	0
3	Flat Panel Size Select [0]	R/W	0
2	Vertical Alignment Control [1]	R/W	0
1	Vertical Alignment Control [0]	R/W	0
0(LSB)	Reserved		0

This register provides miscellaneous control functions.

Bit **Description**

Bits 7:5 **RGB Weight Control Bits 2:0:** Programming these three bits provides for the following control over the RGB color weighting (the shaded area is the default):

Table 7–17. RGB Weight Control

Bit 7	Bit 6	Bit 5		R	G	B
0	0	0		11%	30%	59%
0	0	1		30%	11%	59%
0	1	0		11%	59%	30%
0	1	1		30%	59%	11%
1	0	0		59%	11%	30%
1	0	1		59%	30%	11%
110 through 111				Reserved		

7.2.68 Display Control Register: ERDA *(cont.)*

Bit	Description
Bits 4:3	**Flat Panel Size Select Bits:** These two bits select the default panel size according to the following table:

Table 7–18. Flat Panel Size Select

Bit 4	Bit 3	Meaning
0	0	640 x 480
0	1	640 x 400
10 through 11		Reserved

Bits 2:1	**Vertical Alignment Control Bits:** These two bits control vertical alignment according to the following table:

Table 7–19. Vertical Alignment Control

Bit 2	Bit 1	Meaning
0	0	Top Alignment
0	1	Bottom Alignment
1	x	Center Alignment

Bit 0	Reserved

7.2.69 Standby Timer Control Register: ERDB

I/O Port Address: 3CF

Index: DB

Bit	Description	Access	Reset State
7(MSB)	Standby Timer Mode Selection [1]	R/W	0
6	Standby Timer Mode Selection [0]	R/W	0
5	Standby Timer Interval [5]	R/W	0
4	Standby Timer Interval [4]	R/W	0
3	Standby Timer Interval [3]	R/W	0
2	Standby Timer Interval [2]	R/W	0
1	Standby Timer Interval [1]	R/W	0
0(LSB)	Standby Timer Interval [0]	R/W	0

Bit **Description**

Bits 7:6 **Standby Timer Mode Selection Bits:** When activated, these two bits control the CL-GD6412 internal Standby Timer as follows:

Table 7–20. Standby Timer Mode Selection

Bit 7	Bit 6	Meaning
0	0	Disable Standby Timer
0	1	The timer will run and time-outs will be reset by the Screen Save Clock Pin (SSCLK) (Pin 80).
1	0	Reset timer on Video Memory CPU requests (read or write)
1	1	Reserved

Bits 5:0 **Standby Timer Interval Bits 5:0:** This register specifies the time interval for the Standby Timer in units of one minute. The range is from 0 to 63 minutes.

7.2.70 Flat Panel Color Configuration Register: ERDC

I/O Port Address: 3CF

Index: DC

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	MOD/FPHDE/P8 Pin Function Control	R/W	0
0(LSB)	9-Bit Color Panel Select	R/W	0

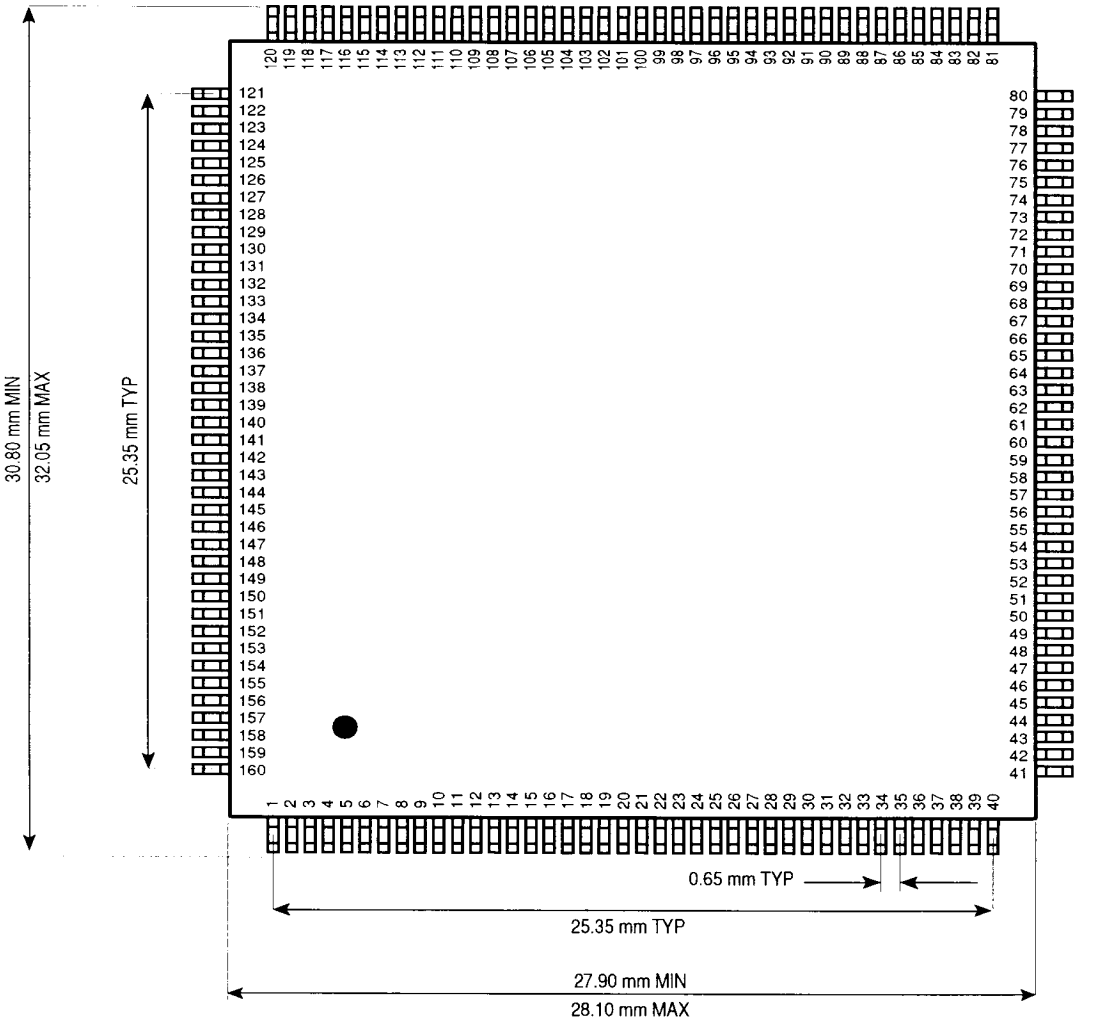
Bit	Description
Bits 7:2	Reserved
Bit 1	**MOD/FPHDE/P8 Pin Function Control:** This bit, along with Bit 0, selects the function of the MOD/FPHDE/P8 Pin (Pin 100).
Bit 0	**9-Bit Color Panel Select:** When a color TFT 9-bit flat panel is used, this bit must be set to a '1'. This bit overrides Bit 1.

Table 7–21. MOD/FPHDE/P8 Select

Bit 1	Bit 0	Meaning
0	0	MOD
0	1	FPHDE
1	x	9-Bit Color Flat Panel

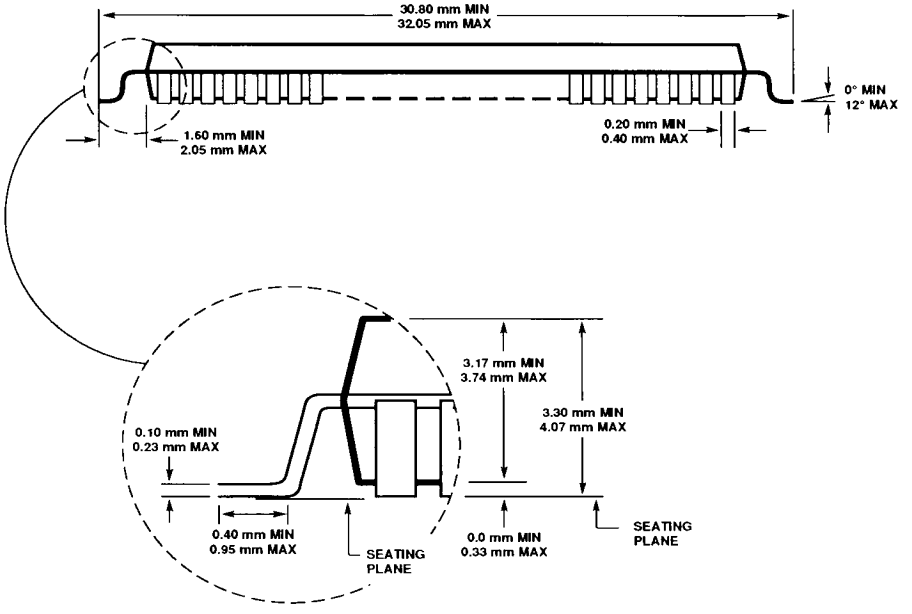
8. SAMPLE PACKAGE

8.1 160-Pin Quad Flat Pack (QFP, EIAJ)



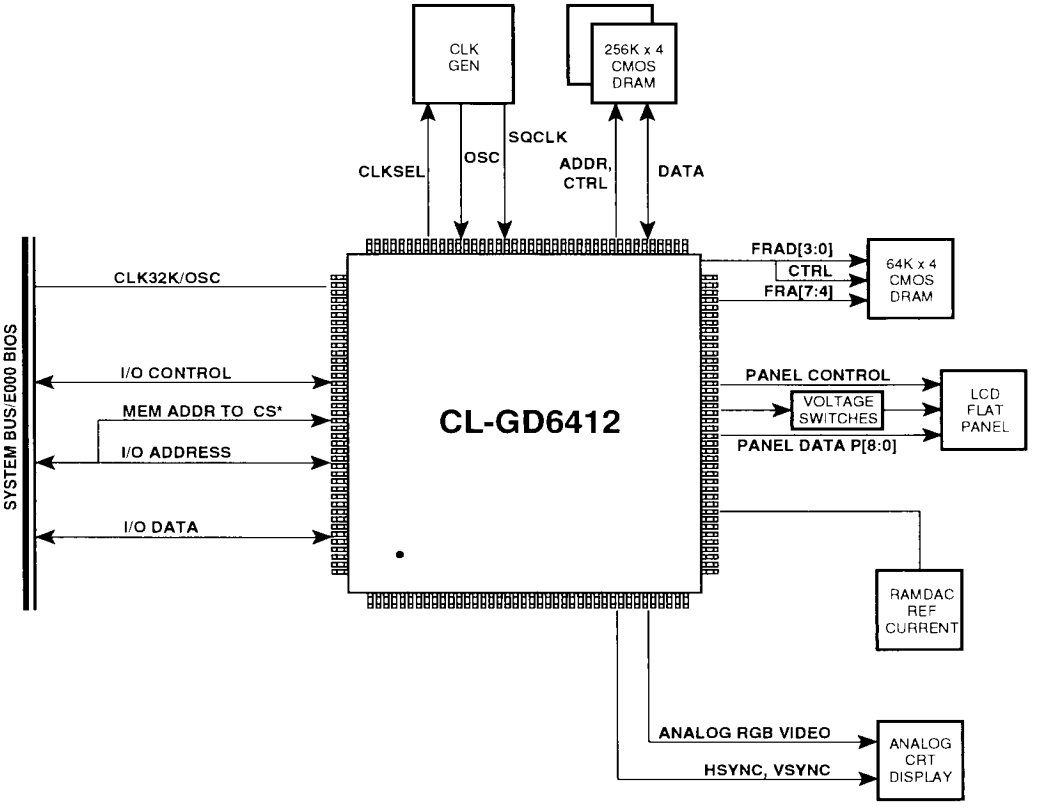
346412-2

8.2 160-Pin Quad Flat Pack Expanded View (QFP, EIAJ)



346412-3

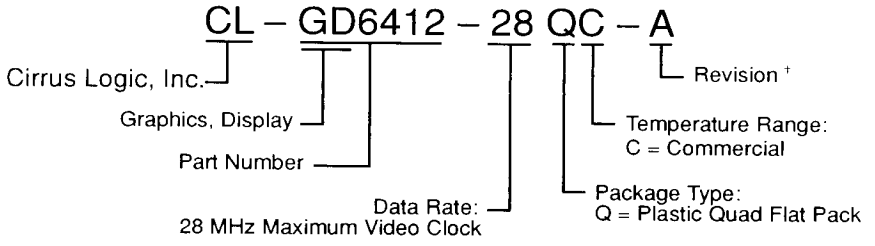
9. TYPICAL APPLICATION



346412-4

10. ORDERING INFORMATION

10.1 Cirrus Logic Numbering Guide



† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

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